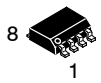
# Half Bridge Gate Driver(Isolated High & Non-Isolated Low) NCV57200




**SOIC-8 NB**
**CASE 751-07**

The NCV57200 is a high voltage gate driver with one non-isolated low side gate driver and one galvanic isolated high or low side gate driver. It can directly drive two IGBTs in a half bridge configuration. Isolated high side driver can be powered with an isolated power supply or with Bootstrap technique from the low side power supply.

The galvanic isolation for the high side gate driver guarantees reliable switching in high power applications for IGBTs that operate up to 800 V, at high dv/dt. The optimized output stages provide a mean of reducing IGBT losses. Its features include two independent inputs with deadtime and interlock, accurate asymmetric UVLOs, and short and matched propagation delays. The NCV57200 operates with its $V_{CC}/V_B$ up to 20 V.

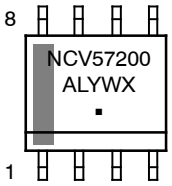
### Features

- High Peak Current Output (+1.9 A / -2.3 A)
- Low Output Voltage Drop for Enhanced IGBT Conduction
- Secured Output Low State without $V_{DD}/V_B$
- Floating Channel for Bootstrap Operation up to +800 V
- CMTI up to 50 kV / μs
- Reliable Operation for $V_S$ Negative Swing to -800 V
- $V_{DD}$ & $V_{BS}$ Supply Range up to 20 V
- 3.3 V, 5 V, and 15 V Logic Input
- Asymmetric Under Voltage Lockout Thresholds for High Side and Low Side
- Matched Propagation Delay 90 ns
- Built-in 20 ns Minimum Pulse Width Filter (or Input Noise Filter)
- Built-in 340 ns Dead-Time and High and Low Inputs Interlock
- Output in Phase with Input Signal
- AEC-Q100 Qualified and PPAP Capable
- This Device is Pb-Free, Halogen Free/BFR Free and is RoHS Compliant

### Typical Applications

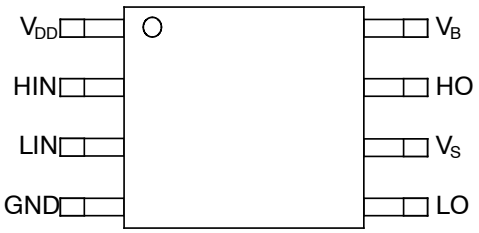
- OBC
- PTC Heater
- e-Compressors
- Automotive Power Supplies

### MARKING DIAGRAM




| | |
|---|---|
| NCV57200 | = Specific Device Code |
| A | = Assembly Location |
| L | = Wafer Lot |
| Y | = Year |
| W | = Work Week |
| ▪ | = Pb-Free Package |

### PIN CONNECTIONS




### ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

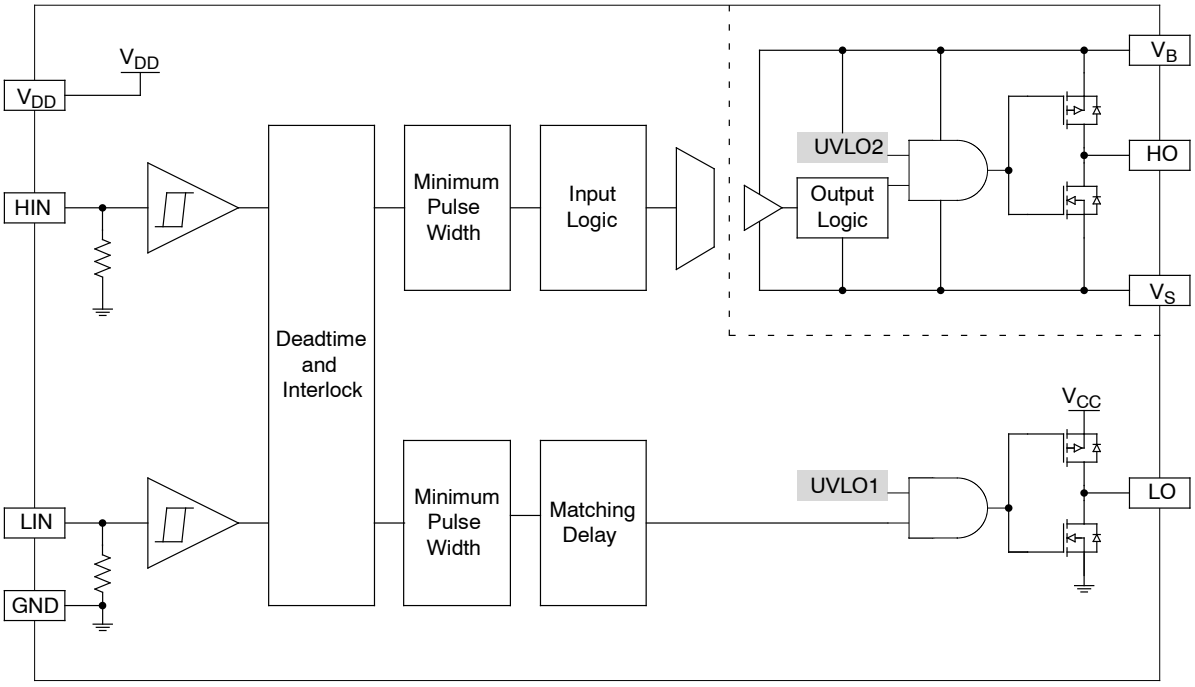



**Figure 1. Simplified Block Diagram**

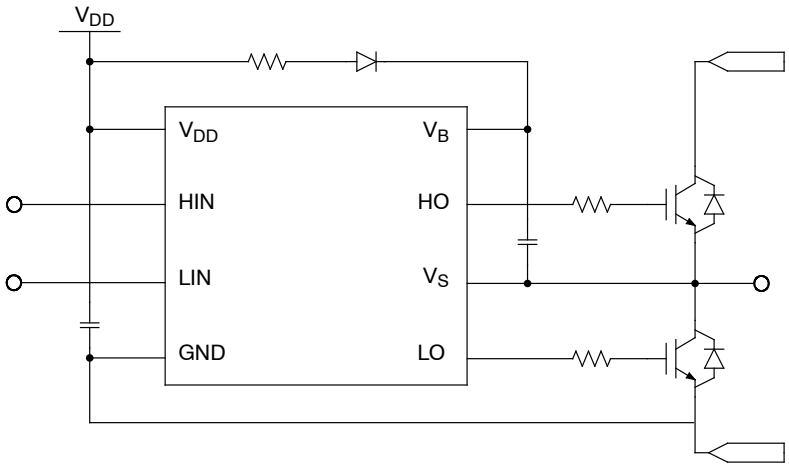



**Figure 2. Simplified Application Schematics**

**Table 1. FUNCTION DESCRIPTION**

| Pin Name | No. | I/O | Description |
|---|---|---|---|
| $V_{DD}$ | 1 | Power | Low side and main power supply. A good quality bypassing capacitor is required from this pin to GND and should be placed close to the pins for best results.<br>The under voltage lockout (UVLO) circuit enables the device to operate at power on when a typical supply voltage higher than $V_{UVLO1-OUT-ON}$ is present. Please see Figure 5 for more details. A filter time of typical 1.5 μs helps to suppress noise on $V_{DD}$ pin. |
| HIN | 2 | I | High side non-inverting gate driver input. It has an equivalent pull-down resistor of 125 kΩ to ensure that output is low in the absence of an input signal.<br>A minimum positive or negative going pulse width is required at HIN before HO reacts.<br>It adopts 3.3 V logic signal thresholds for input voltage up to $V_{DD}$.<br>There is deadtime and interlocking logic between HIN and LIN. |
| LIN | 3 | I | Low side non-inverting gate driver input. It has an equivalent pull-down resistor of 125 kΩ to ensure that output is low in the absence of an input signal.<br>A minimum positive or negative going pulse width is required at LIN before LO reacts.<br>It adopts 3.3 V logic signal thresholds for input voltage up to $V_{DD}$.<br>There is deadtime and interlocking logic between HIN and LIN. |
| GND | 4 | Power | Logic ground and low side driver return. |
| LO | 5 | O | Low side driver output that provides the appropriate drive voltage and source/sink current to the IGBT gate. LO is actively pulled low during startup and under UVLO1 condition. There is deadtime and interlocking logic to prevent unintended HO and LO cross conduction. |
| $V_S$ | 6 | Power | Bootstrap return or high side floating supply offset. |
| HO | 7 | O | Galvanic isolated high side driver output that provides the appropriate drive voltage and source/sink current to the IGBT gate. HO is actively pulled low during startup and under UVLO2 condition. There is deadtime and interlocking logic to prevent unintended HO and LO cross conduction. |
| $V_B$ | 8 | Power | Bootstrap or high side floating power supply. A good quality bypassing capacitor is required from this pin to $V_S$ and should be placed close to the pins for best results.<br>The under voltage lockout (UVLO) circuit enables the device to operate at power on when a typical supply voltage higher than $V_{UVLO2-OUT-ON}$ is present. Please see Figure 5 for more details. A filter time of typical 1.5 μs helps to suppress noise on $V_B$ pin. |

**Table 2. SAFETY AND INSULATION RATINGS**

| Symbol | Parameter | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | Installation Classifications per DIN VDE 0110/1.89 Table 1 Rated Mains Voltage | < 150 $V_{RMS}$ | - | - | - | |
| | | < 300 $V_{RMS}$ | - | - | - | |
| | | < 450 $V_{RMS}$ | - | - | - | |
| | | < 600 $V_{RMS}$ | - | - | - | |
| | | < 1000 $V_{RMS}$ | - | - | - | |
| CTI | Comparative Tracking Index (DIN IEC 112/VDE 0303 Part 1) | | 600 | - | - | |
| $V_{IORM}$ | Maximum Working Insulation Voltage | | 800 | - | - | $V_{PK}$ |
| $E_{CR}$ | External Creepage | | 4.0 | - | - | mm |
| $E_{CL}$ | External Clearance | | 4.0 | - | - | mm |
| DTI | Insulation Thickness | | 8.65 | - | - | μm |
| $T_{Case}$ | Safety Limit Values – Maximum Values in Failure; Case Temperature | | 150 | - | - | °C |
| $P_{S,INPUT}$ | Safety Limit Values – Maximum Values in Failure; Input Power | | 75 | - | - | mW |
| $P_{S,OUTPUT}$ | Safety Limit Values – Maximum Values in Failure; Output Power | | 1335 | - | - | mW |
| $R_{IO}$ | Insulation Resistance at TS, $V_{IO}$ = 500 V | | $10^9$ | - | - | Ω |

**Table 3. ABSOLUTE MAXIMUM RATINGS** (Note 1) Over operating free- air temperature range unless otherwise noted

| Parameter | Symbol | Minimum | Maximum | Unit |
|---|---|---|---|---|
| High- Side Offset Voltage | $V_S$ | - 900 | 900 | V |
| High- Side Offset Voltage ($t_p$ < 500 ns) | | - 900 | 900 | |
| High- Side Supply Voltage | $V_B$ | - 900 | 900 | V |
| High- Side Supply Voltage ($t_p$ < 500 ns) | | - 900 | 900 | |
| Low- Side and Logic- Fixed Supply Voltage | $V_{DD}$ | - 0.3 | 25 | V |
| High- Side Floating Supply Voltage | $V_{BS}$ | - 0.3 | 25 | V |
| High- Side Floating Output Voltage $V_{HO}$ | $V_{HO}$ | $V_S$ - 0.3 | $V_B$+0.3 | V |
| Low- Side Floating Output Voltage $V_{LO}$ | $V_{LO}$ | - 0.3 | $V_{DD}$+0.3 | V |
| Logic Input Voltage (HIN, LIN) | $V_{IN}$ | - 0.3 | $V_{DD}$+0.3 | V |
| Allowable Offset Voltage Slew Rate | $dV_S/dt$ | | ±50 | V/ns |
| Maximum Junction Temperature | TJ(max) | - 40 | 150 | °C |
| Storage Temperature Range | TSTG | - 65 | 150 | °C |
| ESD Capability, Human Body Model (Note 2) | ESDHBM | | ±4 | kV |
| ESD Capability, Charged Device Model (Note 2) | ESDCDM | | ±2 | kV |
| Moisture Sensitivity Level | MSL | | 1 | - |
| Lead Temperature Soldering Reflow | TSLD | | 260 | °C |
| (SMD Styles Only), Pb- Free Versions (Note 3) | | | | |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC- Q100- 002 (EIA/JESD22- A114).
   ESD Charged Device Model tested per AEC- Q100- 011 (EIA/JESD22- C101).
   Latchup Current Maximum Rating: ≤ 100 mA per JEDEC standard: JESD78, 125°C.
3. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**Table 4. THERMAL CHARACTERISTICS**

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Thermal Characteristics, SOIC- 8 (Note 4)<br>Thermal Resistance, Junction- to- Air (Note 5) | $R_{\theta JA}$ | 167 | °C/W |

4. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
5. Values based on copper area of 100 $mm^2$ (or 0.16 $in^2$) of 1 oz copper thickness and FR4 PCB substrate.

**Table 5. RECOMMENDED OPERATING RANGES** (Note 6)

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| High- Side Supply Voltage | $V_B$ | $V_S$+UVLO2 | $V_S$+20 | V |
| High- Side Supply Offset Voltage | $V_S$ | - 800 | 800 | V |
| High- Side (HO) Output Voltage | $V_{HO}$ | $V_S$ | $V_B$ | V |
| Low- Side (LO) Output Voltage | $V_{LO}$ | GND | $V_{DD}$ | V |
| Logic Input Voltage (HIN, LIN) | $V_{IN}$ | GND | $V_{DD}$ | V |
| Low- Side Supply Voltage | $V_{DD}$ | UVLO1 | 20 | V |
| Ambient Temperature | $T_A$ | - 40 | +125 | °C |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

6. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.

**Table 6. ELECTRICAL CHARACTERISTICS** $V_{DD}$ = $V_{BS}$ = 15 V.
For typical values $T_A$ = 25°C, for min/max values, $T_A$ is the operating ambient temperature range that applies, unless otherwise noted.

| Parameter | Test Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **VOLTAGE SUPPLY** | | | | | | |
| $V_{BS}$ Supply Under Voltage Output Enabled | | $V_{UVLO2-OUT-ON}$ | 11 | 11.5 | 12 | V |
| $V_{BS}$ Supply Under Voltage Output Disabled | | $V_{UVLO2-OUT-OFF}$ | 10 | 10.5 | 11 | V |
| $V_{BS}$ Supply Voltage Output Enabled/Disabled Hysteresis | | $V_{UVLO2-HYST}$ | | 1.0 | | V |
| $V_{DD}$ Supply Under Voltage Output Enabled | | $V_{UVLO1-OUT-ON}$ | 12 | 12.5 | 13 | V |
| $V_{DD}$ Supply Under Voltage Output Disabled | | $V_{UVLO1-OUT-OFF}$ | 11 | 11.5 | 12 | V |
| $V_{DD}$ Supply Voltage Output Enabled/Disabled Hysteresis | | $V_{UVLO1-HYST}$ | | 1.0 | | V |
| Leakage Current Between $V_S$ and GND | $V_S$ = ± 800 V, $T_A$ = 25°C<br>$V_S$ = ± 800 V, $T_A$ = −40°C to 125°C | $I_{HV\_LEAK1}$<br>$I_{HV\_LEAK2}$ | | 20 | 200<br>600 | nA |
| Quiescent Current $V_{BS}$ Supply ($V_B$ Only) | HO = Low | $I_{QBS1}$ | | 260 | 325 | μA |
| Quiescent Current $V_{BS}$ Supply ($V_B$ Only) | HO = High | $I_{QBS2}$ | | 330 | 440 | μA |
| Quiescent Current $V_{DD}$ Supply ($V_{DD}$ Only) | $V_{LIN}$ = Float, $V_{HIN}$ = 0 V, | $I_{QDD1}$ | | 380 | 440 | μA |
| Quiescent Current $V_{DD}$ Supply ($V_{DD}$ Only) | $V_{LIN}$ = 3.3 V, $V_{HIN}$ = 0 V, | $I_{QDD2}$ | | 440 | 500 | μA |
| Quiescent Current $V_{DD}$ Supply ($V_{DD}$ Only) | $V_{LIN}$ = 0 V, $V_{HIN}$ = 3.3 V, | $I_{QDD3}$ | | 2.4 | 3 | mA |
| **LOGIC INPUT** | | | | | | |
| Low Level Input Voltage | | $V_{IL}$ | | | 0.9 | V |
| High Level Input Voltage | | $V_{IH}$ | 2.4 | | | V |
| Logic “1” Input Bias Current | $V_{LIN}$ = 3.3 V, $V_{HIN}$ = 3.3 V | $I_{LIN1+}$, $I_{HIN1+}$ | | 25 | 50 | μA |
| Logic “1” Input Bias Current | $V_{LIN}$ = 20 V, $V_{HIN}$ = 20 V,<br>$V_{DD}$ = $V_{BS}$ = 20 V | $I_{LIN2+}$, $I_{HIN2+}$ | | 100 | 150 | μA |
| Logic “0” Input Bias Current | $V_{LIN}$ = 0 V, $V_{HIN}$ = 0 V | $I_{LIN-}$, $I_{HIN-}$ | | 40 | 100 | nA |
| **DRIVER OUTPUT** | | | | | | |
| Output Low State | $I_{SINK}$ = 200 mA, $T_A$ = 25°C | $V_{OL1}$ | | 0.2 | 0.3 | V |
| | $I_{SINK}$ = 200 mA,<br>$T_A$ = −40°C to 125°C | $V_{OL2}$ | | | 0.5 | |
| Output High State | $I_{SRC}$ = 200 mA, $T_A$ = 25°C | $V_{OH1}$ | 14.4 | 14.5 | | V |
| | $I_{SRC}$ = 200 mA,<br>$T_A$ = −40°C to 125°C | $V_{OH2}$ | 14 | | | |
| Peak Driver Current, Sink (Note 7) | $V_{HO}$ = $V_{LO}$ = 15 V | $I_{PK-SNK1}$ | | 2.3 | | A |
| | $V_{HO}$ = $V_{LO}$ = 9 V<br>(near Miller Plateau) | $I_{PK-SNK2}$ | | 2.1 | | |
| Peak Driver Current, Source (Note 7) | $V_{HO}$ = $V_{LO}$ = 0 V | $I_{PK-SRC1}$ | | 1.9 | | A |
| | $V_{HO}$ = $V_{LO}$ = 9 V<br>(near Miller Plateau) | $I_{PK-SRC2}$ | | 1.5 | | |

**Table 6. ELECTRICAL CHARACTERISTICS** $V_{DD} = V_{BS} = 15$ V.
For typical values $T_A = 25°C$, for min/max values, $T_A$ is the operating ambient temperature range that applies, unless otherwise noted.

| Parameter | Test Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **IGBT SHORT CIRCUIT CLAMPING** | | | | | | |
| Clamping Voltage $(V_{HO} - V_B) / (V_{LO} - V_{DD})$ | $I_{HO}$ = 100 mA, $I_{LO}$ = 100 mA (pulse test, $t_{CLPmax}$ = 10 μs) | $V_{CLAMP-OUT}$ | | 0.8 | 1.3 | V |
| **DYNAMIC CHARACTERISTIC** | | | | | | |
| HO High Propagation Delay | $C_{LOAD}$ = 1 nF, $V_{IH}$ to 10% of Output Change for PW > 150 ns | $t_{PD-ON-H}$ | 60 | 90 | 110 | ns |
| HO Low Propagation Delay | $C_{LOAD}$ = 1 nF, $V_{IL}$ to 90% of Output Change for PW > 150 ns | $t_{PD-OFF-H}$ | 60 | 90 | 110 | ns |
| Propagation Delay Distortion(HS) (= $t_{PD-ON} - t_{PD-OFF}$) | PW >150 ns | $t_{DISTORT-H}$ | -25 | 0 | 25 | ns |
| LO High Propagation Delay | $C_{LOAD}$ = 1 nF, $V_{IH}$ to 10% of Output Change for PW > 150 ns | $t_{PD-ON-L}$ | 60 | 90 | 110 | ns |
| LO Low Propagation Delay | $C_{LOAD}$ = 1 nF, $V_{IL}$ to 90% of Output Change for PW > 150 ns | $t_{PD-OFF-L}$ | 60 | 90 | 110 | ns |
| Propagation Delay Distortion(LS) (= $t_{PD-ON} - t_{PD-OFF}$) | PW >150 ns | $t_{DISTORT-L}$ | -25 | 0 | 25 | ns |
| High Prop Delay Distortion between High and Low Sides | PW > 150 ns | $t_{DISTORT-HLH}$ | -25 | 0 | 25 | ns |
| Low Prop Delay Distortion between High and Low Sides | PW > 150 ns | $t_{DISTORT-HLL}$ | -25 | 0 | 25 | ns |
| Rise Time(HS) (see timing diagram) | $C_{LOAD}$ = 1 nF, 10% to 90% of Output Change | $t_{RISE-H}$ | | 13 | | ns |
| Fall Time(HS) (see timing diagram) | $C_{LOAD}$ = 1 nF, 90% to 10% of Output Change | $t_{FALL-H}$ | | 8 | | ns |
| Rise Time(LS) (see timing diagram) | $C_{LOAD}$ = 1 nF, 10% to 90% of Output Change | $t_{RISE-L}$ | | 13 | | ns |
| Fall Time(LS) (see timing diagram) | $C_{LOAD}$ = 1 nF, 90% to 10% of Output Change | $t_{FALL-L}$ | | 8 | | ns |
| Deadtime, HO Delays | $V_{LIN/HIN}$ = 0 V and 3.3 V | $t_{DT1}$ | | 340 | | ns |
| Deadtime, LO Delays | $V_{LIN/HIN}$ = 0 V and 3.3 V | $t_{DT2}$ | | 350 | | ns |
| Deadtime Matching | | $t_{MDT}$ | | 10 | | ns |
| Minimum Pulse Width Filtering Time | $T_A = 25°C$ | $t_{MIN1}$, $t_{MIN2}$ | 10 | | 40 | ns |
| UVLO Fall Delay (HO and LO) | | $t_{UV1}$ | | 1300 | | ns |
| UVLO Rise Delay (HO and LO) | | $t_{UV2}$ | | 1100 | | ns |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
7. Values based on design and/or characterization.

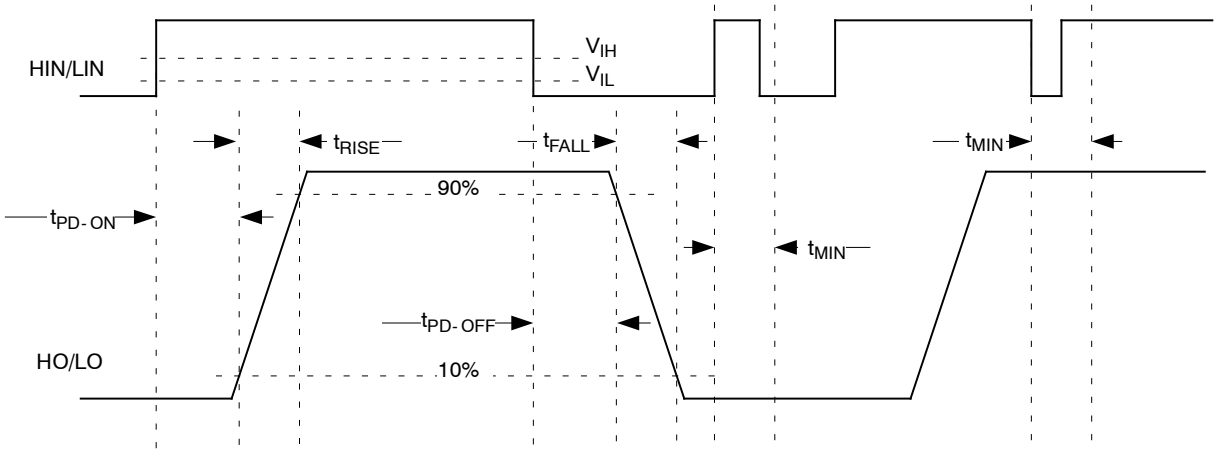



**Figure 3. Propagation Delay, Rise and Fall Time**

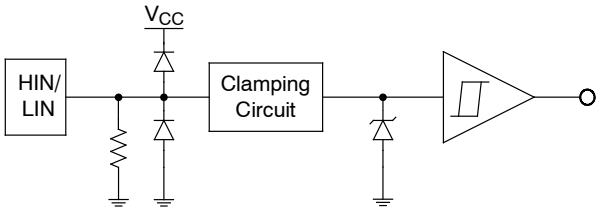



**Figure 4. Input Pin Structure**

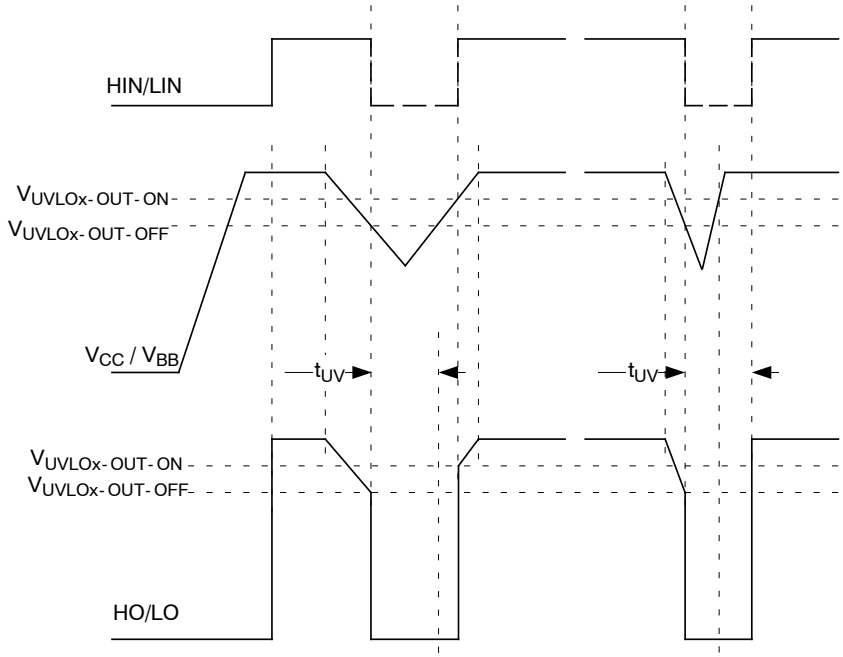



**Figure 5. UVLO**

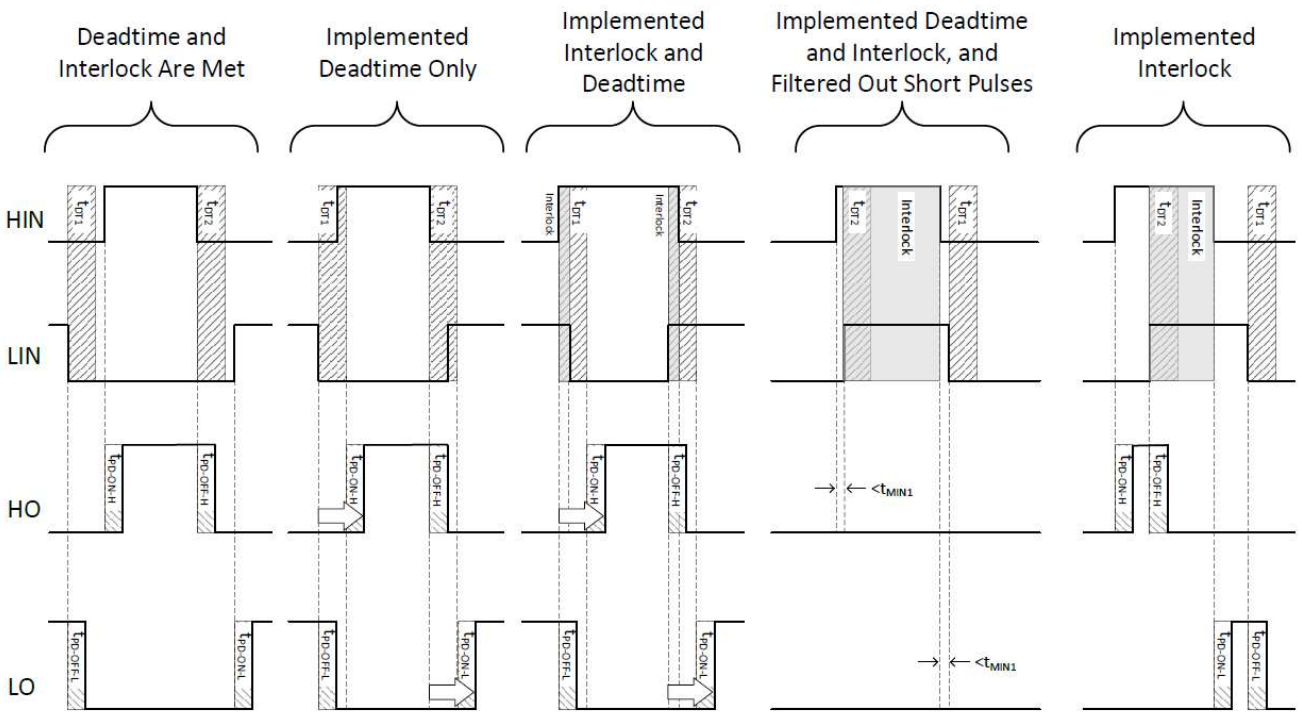



**Figure 6. Deadtime, Interlock and Output Minimum Pulse Width**

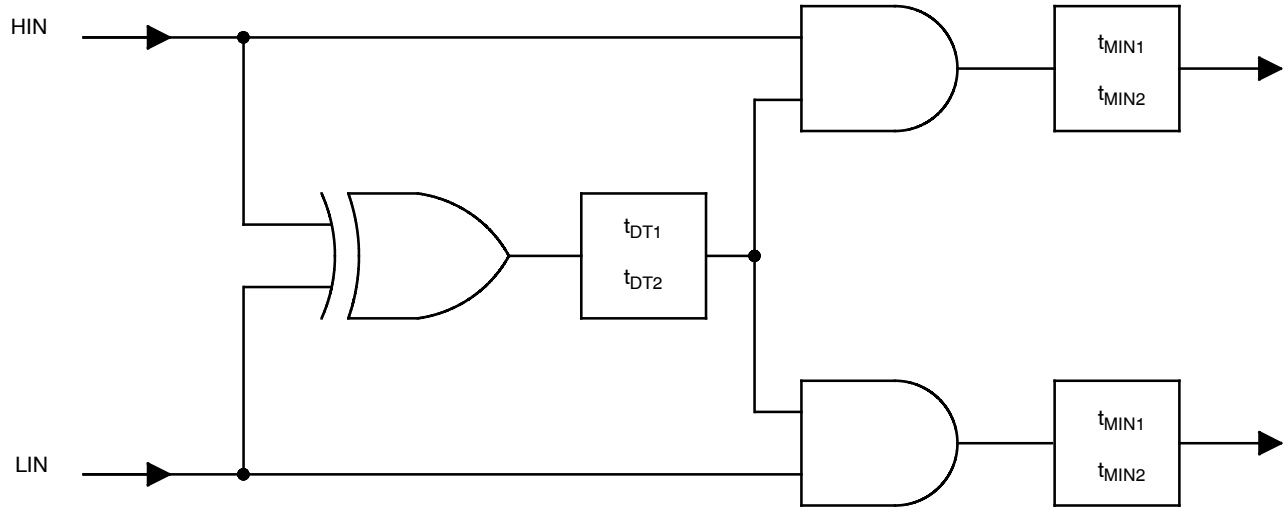



**Figure 7. Input Circuit**

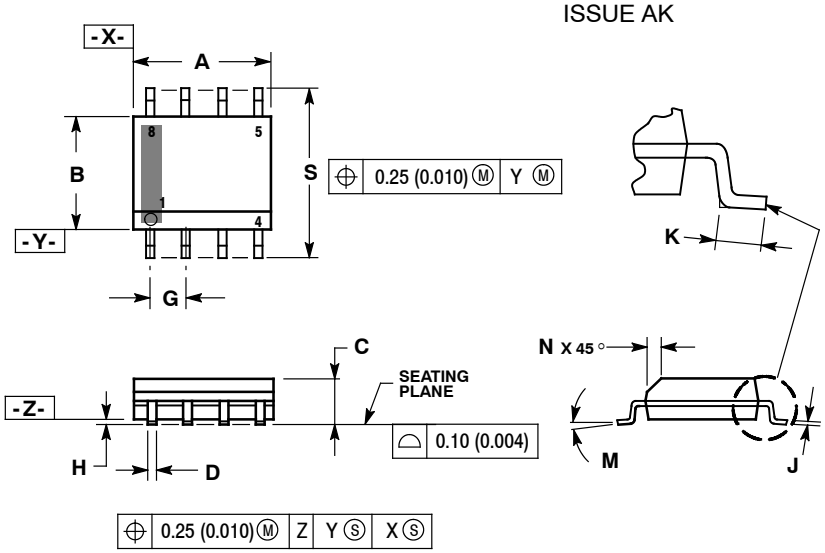
## ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| NCV57200DR2G | SOIC−8 (Pb−Free) | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## PACKAGE DIMENSIONS

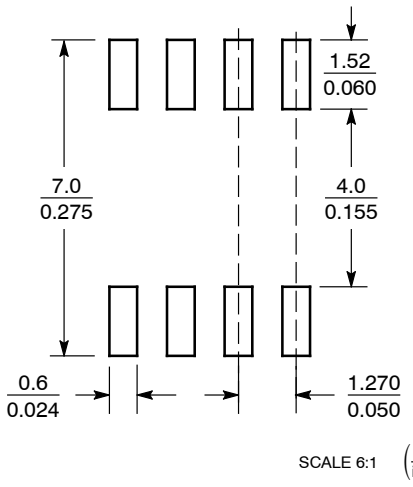
**SOIC-8 NB**
CASE 751-07
ISSUE AK




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 4.80 | 5.00 | 0.189 | 0.197 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.053 | 0.069 |
| D | 0.33 | 0.51 | 0.013 | 0.020 |
| G | 1.27 BSC | | 0.050 BSC | |
| H | 0.10 | 0.25 | 0.004 | 0.010 |
| J | 0.19 | 0.25 | 0.007 | 0.010 |
| K | 0.40 | 1.27 | 0.016 | 0.050 |
| M | 0° | 8° | 0° | 8° |
| N | 0.25 | 0.50 | 0.010 | 0.020 |
| S | 5.80 | 6.20 | 0.228 | 0.244 |

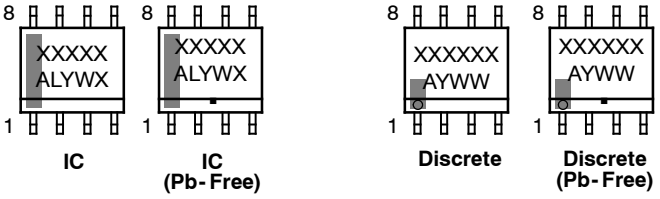
### SOLDERING FOOTPRINT*




SCALE 6:1 (mm / inches)

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAM*




XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

**SOIC-8 NB**
CASE 751-07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N-SOURCE
2. N-GATE
3. P-SOURCE
4. P-GATE
5. P-DRAIN
6. P-DRAIN
7. N-DRAIN
8. N-DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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