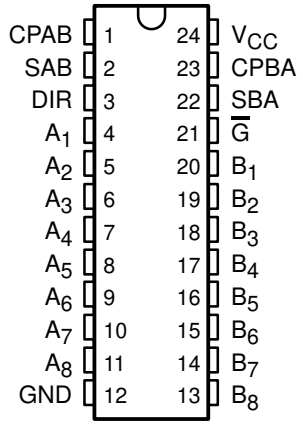
- **Function and Pinout Compatible With FCT and F Logic**
- **Reduced $V_{OH}$ (Typically = 3.3 V) Versions of Equivalent FCT Functions**
- **25-Ω Output Series Resistors to Reduce Transmission-Line Reflection Noise**
- **Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics**
- **$I_{off}$ Supports Partial-Power-Down Mode Operation**
- **Matched Rise and Fall Times**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**
- **Fully Compatible With TTL Input and Output Logic Levels**
- **12-mA Output Sink Current 15-mA Output Source Current**
- **Independent Register for A and B Buses**
- **3-State Outputs**

**Q PACKAGE**
**(TOP VIEW)**




## description

The CY74FCT2646T consists of a bus transceiver circuit with 3-state, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus is clocked into the registers as the appropriate clock pin goes to a high logic level. Output-enable ($\overline{G}$) and direction-control (DIR) inputs determine the transceiver function. On-chip termination resistors at the outputs reduce system noise caused by reflections, so that the CY74FCT2646T can replace the CY74FCT646T in an existing design.

In the transceiver mode, data present at the high-impedance port can be stored in either the A or B register, or in both. Select controls (SAB, SBA) can multiplex stored and real-time (transparent mode) data. DIR determines which bus receives data when $\overline{G}$ is active low. In the isolation mode ($\overline{G}$ is high), A data can be stored in the B register and/or B data can be stored in the A register.

This device is fully specified for partial-power-down applications using $I_{off}$. The $I_{off}$ circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

**PIN DESCRIPTION**

| NAME | DESCRIPTION |
|---|---|
| A | Data register A inputs, data register B outputs |
| B | Data register B inputs, data register A outputs |
| CPAB, CPBA | Clock pulse inputs |
| SAB, SBA | Output data source select inputs |
| DIR, $\overline{G}$ | Output-enable inputs |

## ORDERING INFORMATION

| $T_A$ | PACKAGE† | | SPEED (ns) | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|---|
| –40°C to 85°C | QSOP – Q | Tape and reel | 5.4 | CY74FCT2646CTQCT | FCT2646C |
| | QSOP – Q | Tape and reel | 6.3 | CY74FCT2646ATQCT | FCT2646A |

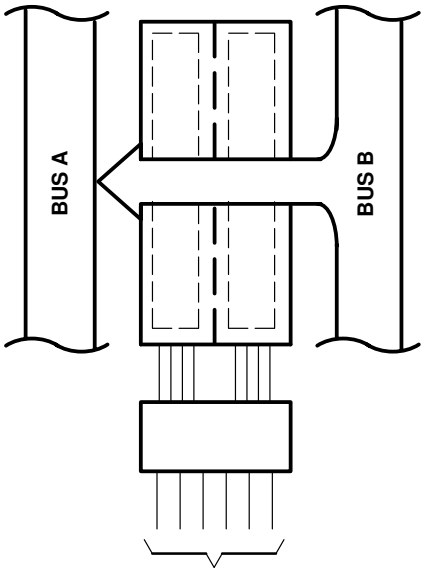
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

### FUNCTION TABLE

| INPUTS | | | | | | DATA I/O‡ | | OPERATION OR FUNCTION |
|---|---|---|---|---|---|---|---|---|
| $\overline{G}$ | DIR | CPAB | CPBA | SAB | SBA | $A_1$–$A_8$ | $B_1$–$B_8$ | |
| H | X | H or L | H or L | X | X | Input | Input | Isolation |
| H | X | ↑ | ↑ | X | X | Input | Input | Store A and B data |
| L | L | X | X | X | L | Output | Input | Real-time B data to A bus |
| L | L | X | H or L | X | H | Output | Input | Stored B data to A bus |
| L | H | X | X | L | X | Input | Output | Real-time A data to B bus |
| L | H | H or L | X | H | X | Input | Output | Stored A data to B bus |

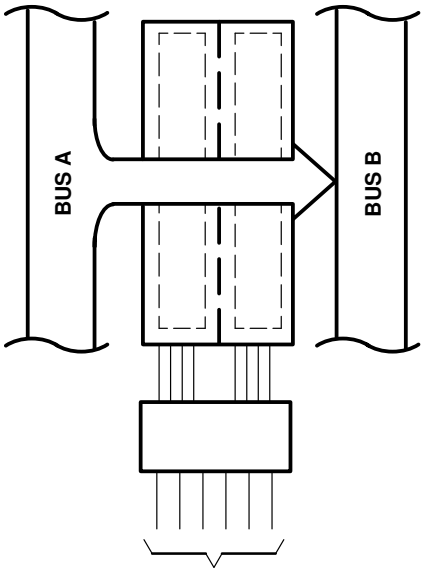
H = High logic level, L = Low logic level, X = Don't care, ↑ = Low-to-high clock transition

‡ The data output functions can be enabled or disabled by various signals at the $\overline{G}$ or DIR inputs. Data input functions always are enabled, i.e., data at the bus pins is stored on every low-to-high transition of the clock inputs.



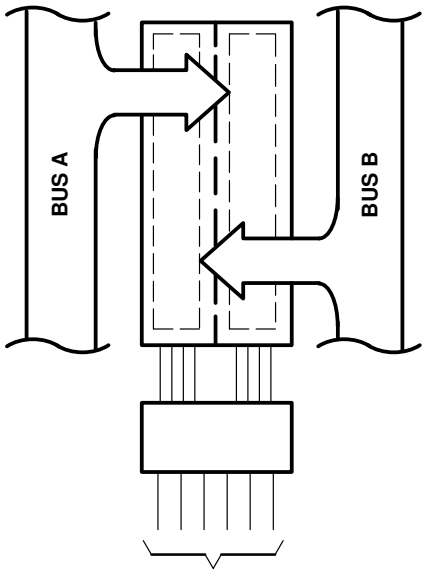

| 3 | 21 | 1 | 23 | 2 | 22 |
|---|---|---|---|---|---|
| DIR | $\overline{G}$ | CPAB | CPBA | SAB | SBA |
| L | L | X | X | X | X |

**REAL-TIME TRANSFER**
**BUS B TO BUS A**



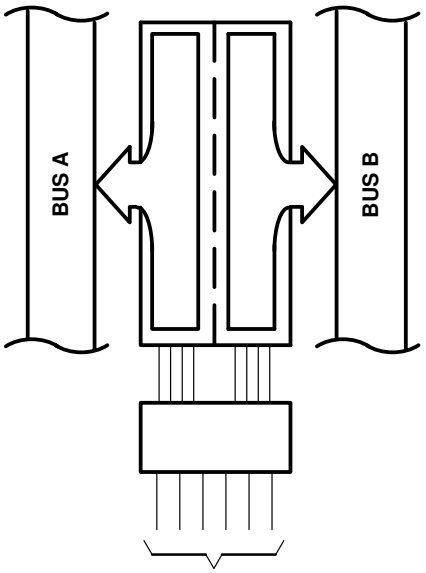

| 3 | 21 | 1 | 23 | 2 | 22 |
|---|---|---|---|---|---|
| DIR | $\overline{G}$ | CPAB | CPBA | SAB | SBA |
| H | L | X | X | L | X |

**REAL-TIME TRANSFER**
**BUS A TO BUS B**




| 3 | 21 | 1 | 23 | 2 | 22 |
|---|---|---|---|---|---|
| DIR | $\overline{G}$ | CPAB | CPBA | SAB | SBA |
| H | L | ↑ | X | X | X |
| L | L | X | ↑ | X | X |
| X | H | ↑ | ↑ | X | X |

**STORAGE FROM**
**A AND/OR B**



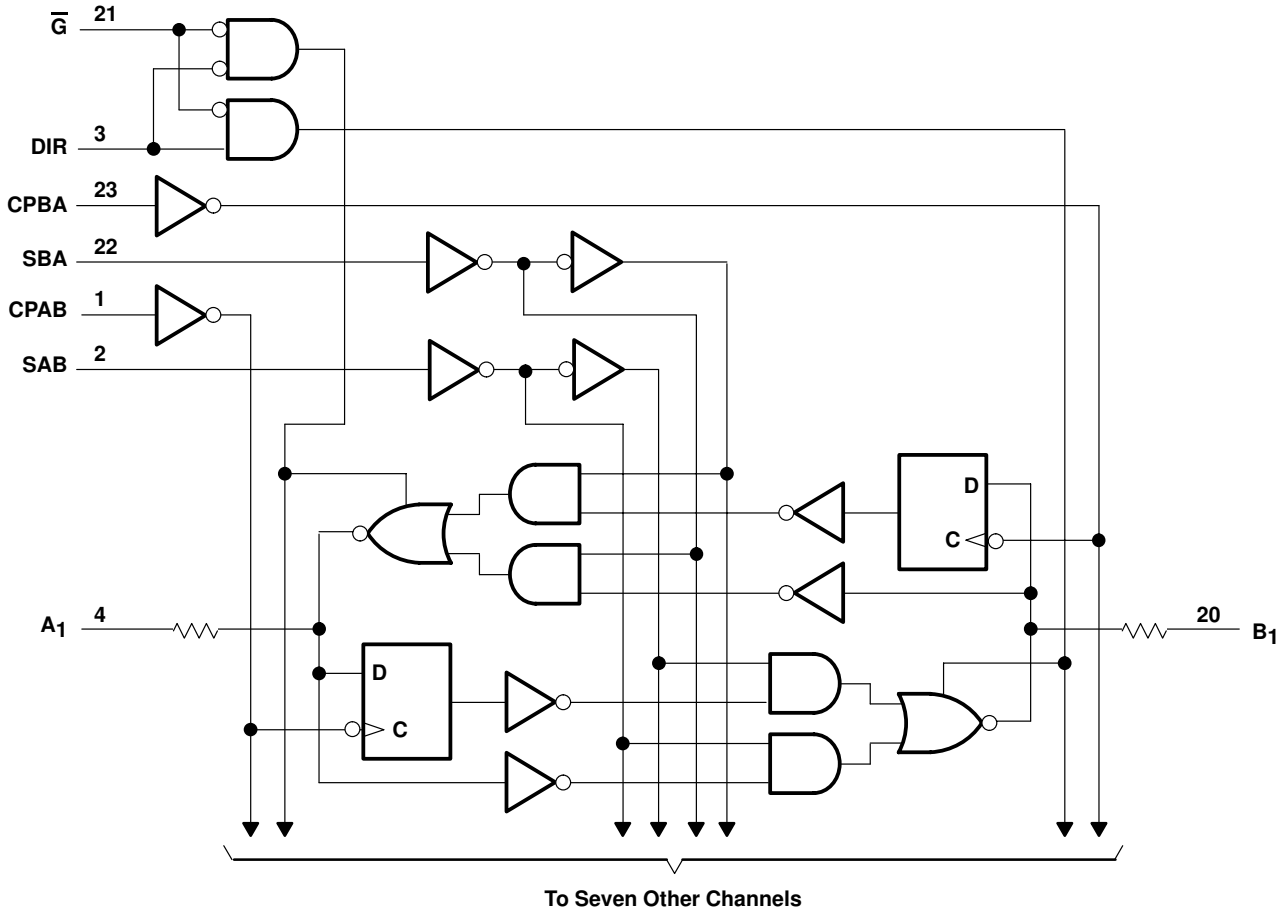

| 3 | 21 | 1 | 23 | 2 | 22 |
|---|---|---|---|---|---|
| DIR† | $\overline{G}$ | CPAB | CPBA | SAB | SBA |
| L | L | X | H or L | X | H |
| H | L | H or L | X | H | H |

**TRANSFER STORED DATA**
**TO A AND/OR B**

† Cannot transfer data to A bus and B bus simultaneously.

**Figure 1. Bus-Management Functions**

## logic diagram




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|---|
| Supply voltage range to ground potential | –0.5 V to 7 V |
| DC input voltage range | –0.5 V to 7 V |
| DC output voltage range | –0.5 V to 7 V |
| DC output current (maximum sink current/pin) | 120 mA |
| Package thermal impedance, $\theta_{JA}$ (see Note 1) | 61°C/W |
| Ambient temperature range with power applied, $T_A$ | –65°C to 135°C |
| Storage temperature range, $T_{stg}$ | –65°C to 150°C |

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 2)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4.75 | 5 | 5.25 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | | | –15 | mA |
| $I_{OL}$ | Low-level output current | | | 12 | mA |
| $T_A$ | Operating free-air temperature | –40 | | 85 | °C |

NOTE 2: All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | $V_{CC}$ = 4.75, | $I_{IN}$ = –18 mA | | | –0.7 | –1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.75, | $I_{OH}$ = –15 mA | | 2.4 | 3.3 | | V |
| $V_{OL}$ | $V_{CC}$ = 4.75, | $I_{OL}$ = 12 mA | | | 0.3 | 0.55 | V |
| $R_{out}$ | $V_{CC}$ = 4.75, | $I_{OL}$ = 12 mA | | 20 | 25 | 40 | Ω |
| $V_{hys}$ | All inputs | | | | 0.2 | | V |
| $I_{IH}$ | $V_{CC}$ = 5.25 V | $V_{IN} = V_{CC}$ | | | | 5 | µA |
| | | $V_{IN}$ = 2.7 V | | | | ±1 | |
| $I_{IL}$ | $V_{CC}$ = 5.25 V, | $V_{IN}$ = 0.5 V | | | | ±1 | µA |
| $I_{OZH}$ | $V_{CC}$ = 5.25 V, | $V_{OUT}$ = 2.7 V | | | | 10 | µA |
| $I_{OZL}$ | $V_{CC}$ = 5.25 V, | $V_{OUT}$ = 0.5 V | | | | –10 | µA |
| $I_{OS}$‡ | $V_{CC}$ = 5.25 V, | $V_{OUT}$ = 0 V | | –60 | –120 | –225 | mA |
| $I_{off}$ | $V_{CC}$ = 0 V, | $V_{OUT}$ = 4.5 V | | | | ±1 | µA |
| $I_{CC}$ | $V_{CC}$ = 5.25 V, | $V_{IN} \le$ 0.2 V, | $V_{IN} \ge V_{CC}$ – 0.2 V | | 0.1 | 0.2 | mA |
| $\Delta I_{CC}$ | $V_{CC}$ = 5.25 V, $V_{IN}$ = 3.4 V§, $f_1$ = 0, Outputs open | | | | 0.5 | 2 | mA |
| $I_{CCD}$¶ | $V_{CC}$ = 5.25 V, One input switching at 50% duty cycle, Outputs open, $\overline{G}$ = DIR = GND, GAB = $\overline{GBA}$ = GND, $V_{IN} \le$ 0.2 V or $V_{IN} \ge V_{CC}$ – 0.2 V | | | | 0.06 | 0.12 | mA/ MHz |
| $I_C$# | $V_{CC}$ = 5.25 V, Outputs open, $\overline{G}$ = DIR = GND, GAB = $\overline{GBA}$ = GND | One input switching at $f_1$ = 5 MHz at 50% duty cycle | $V_{IN} \le$ 0.2 V or $V_{IN} \ge V_{CC}$ – 0.2 V | | 0.7 | 1.4 | mA |
| | | | $V_{IN}$ = 3.4 V or GND | | 1.2 | 3.4 | |
| | | Eight bits switching at $f_1$ = 5 MHz at 50% duty cycle | $V_{IN} \le$ 0.2 V or $V_{IN} \ge V_{CC}$ – 0.2 V | | 2.8 | 5.6‖ | |
| | | | $V_{IN}$ = 3.4 V or GND | | 5.1 | 14.6‖ | |
| $C_i$ | | | | | 6 | 10 | pF |
| $C_o$ | | | | | 8 | 12 | pF |

† Typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, $I_{OS}$ tests should be performed last.

§ Per TTL-driven input ($V_{IN}$ = 3.4 V); all other inputs at $V_{CC}$ or GND

¶ This parameter is derived for use in total power-supply calculations.

# $I_C = I_{CC} + \Delta I_{CC} \times D_H \times N_T + I_{CCD} (f_0/2 + f_1 \times N_1)$

Where:

$I_C$ = Total supply current
$I_{CC}$ = Power-supply current with CMOS input levels
$\Delta I_{CC}$ = Power-supply current for a TTL high input ($V_{IN}$ = 3.4 V)
$D_H$ = Duty cycle for TTL inputs high
$N_T$ = Number of TTL inputs at $D_H$
$I_{CCD}$ = Dynamic current caused by an input transition pair (HLH or LHL)
$f_0$ = Clock frequency for registered devices, otherwise zero
$f_1$ = Input signal frequency
$N_1$ = Number of inputs changing at $f_1$

All currents are in milliamperes and all frequencies are in megahertz.

‖ Values for these conditions are examples of the $I_{CC}$ formula.

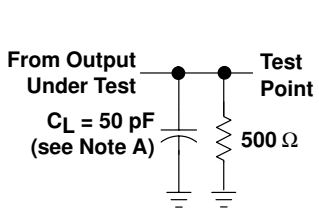
**timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)**

| | | | CY74FCT2646AT | | CY74FCT2646CT | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration, high or low | | 5 | | 5 | | ns |
| $t_{su}$ | Setup time, high or low | Data before CPBA↑ or CPAB↑ | 2 | | 2 | | ns |
| $t_h$ | Hold time, high or low | Data after CPBA↑ or CPAB↑ | 1.5 | | 1.5 | | ns |

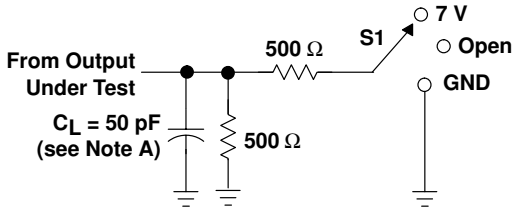
**switching characteristics over operating free-air temperature range (see Figure 2)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | CY74FCT2646AT | | CY74FCT2646CT | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A or B | B or A | 1.5 | 6.3 | 1.5 | 5.4 | ns |
| $t_{PHL}$ | | | 1.5 | 6.3 | 1.5 | 5.4 | |
| $t_{PZH}$ | $\overline{G}$ | A or B | 1.5 | 9.8 | 1.5 | 7.8 | ns |
| $t_{PZL}$ | | | 1.5 | 9.8 | 1.5 | 7.8 | |
| $t_{PZH}$ | DIR | A or B | 1.5 | 9.8 | 1.5 | 7.8 | ns |
| $t_{PZL}$ | | | 1.5 | 9.8 | 1.5 | 7.8 | |
| $t_{PHZ}$ | $\overline{G}$ | A or B | 1.5 | 6.3 | 1.5 | 6.3 | ns |
| $t_{PLZ}$ | | | 1.5 | 6.3 | 1.5 | 6.3 | |
| $t_{PHZ}$ | DIR | A or B | 1.5 | 6.3 | 1.5 | 6.3 | ns |
| $t_{PLZ}$ | | | 1.5 | 6.3 | 1.5 | 6.3 | |
| $t_{PLH}$ | CPAB or CPBA | B or A | 1.5 | 6.3 | 1.5 | 5.7 | ns |
| $t_{PHL}$ | | | 1.5 | 6.3 | 1.5 | 5.7 | |
| $t_{PLH}$ | SAB or SBA | B or A | 1.5 | 7.7 | 1.5 | 6.2 | ns |
| $t_{PHL}$ | | | 1.5 | 7.7 | 1.5 | 6.2 | |

## PARAMETER MEASUREMENT INFORMATION

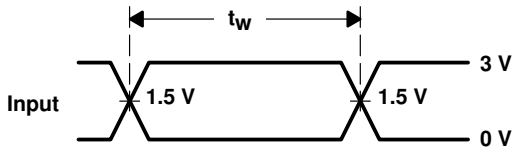



LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

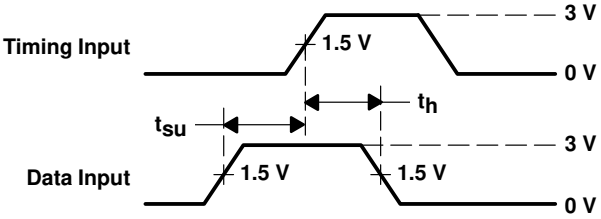



LOAD CIRCUIT FOR
3-STATE OUTPUTS

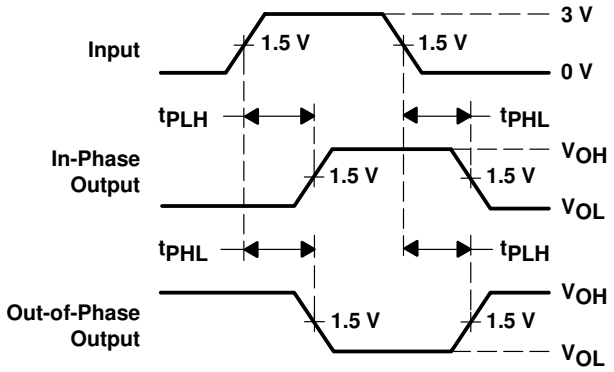
| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V |
| $t_{PHZ}/t_{PZH}$ | Open |



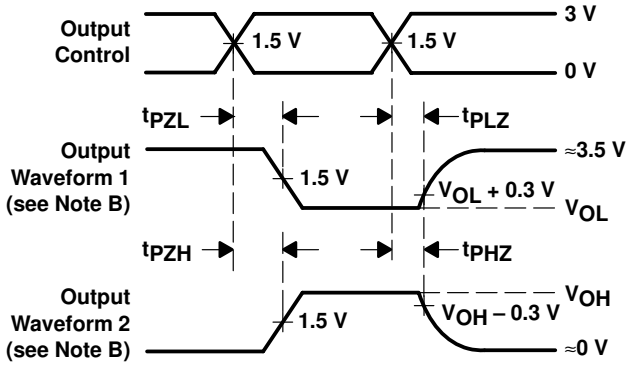

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. The outputs are measured one at a time with one input transition per measurement.

**Figure 2. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

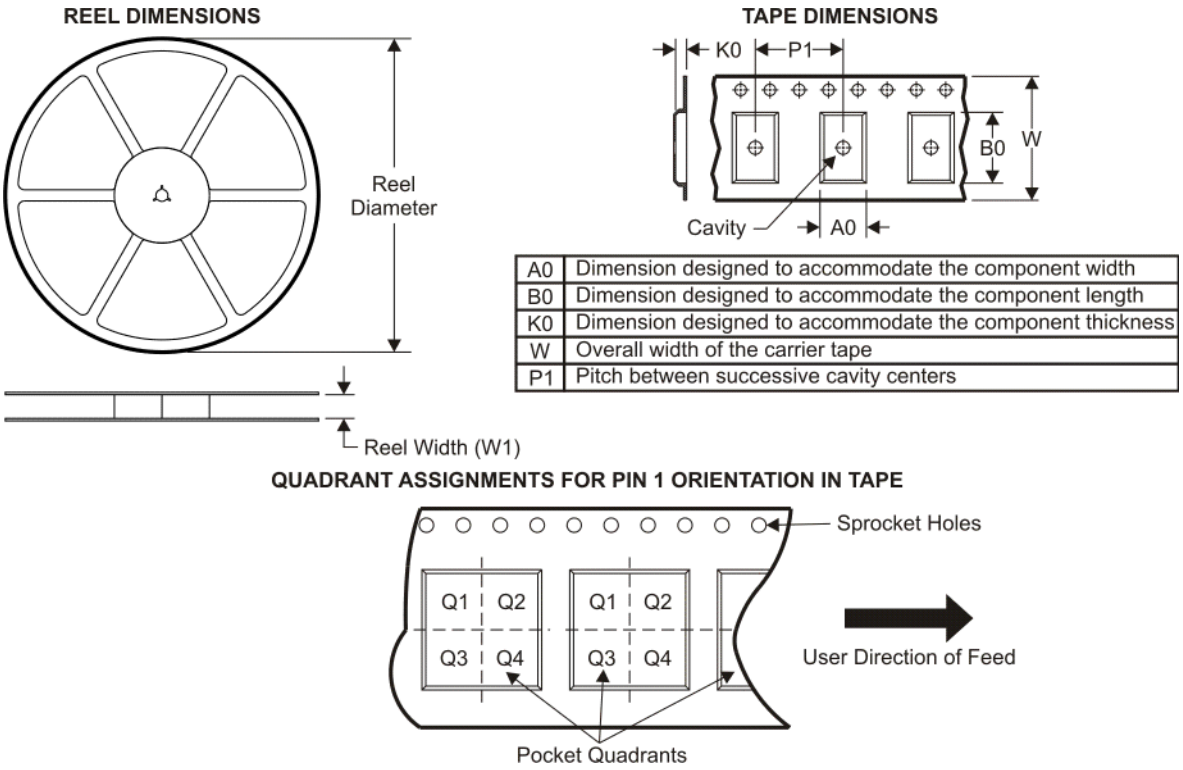
| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| 74FCT2646ATQCTE4 | ACTIVE | SSOP/ QSOP | DBQ | 24 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| CY74FCT2646ATQCT | ACTIVE | SSOP/ QSOP | DBQ | 24 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| SN74FCT2646ATQCTG4 | ACTIVE | SSOP/ QSOP | DBQ | 24 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

## TAPE AND REEL INFORMATION

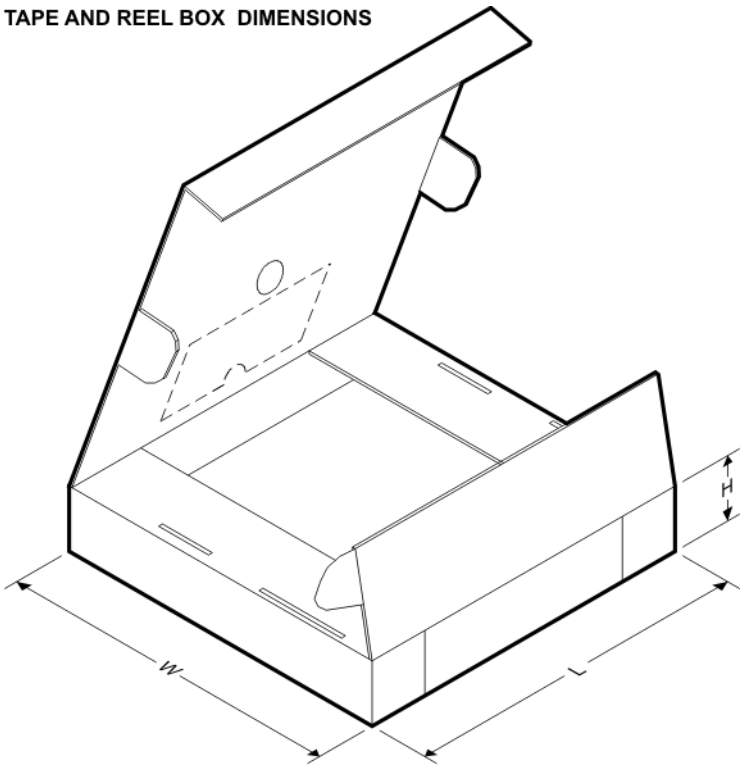



| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CY74FCT2646ATQCT | SSOP/ QSOP | DBQ | 24 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |

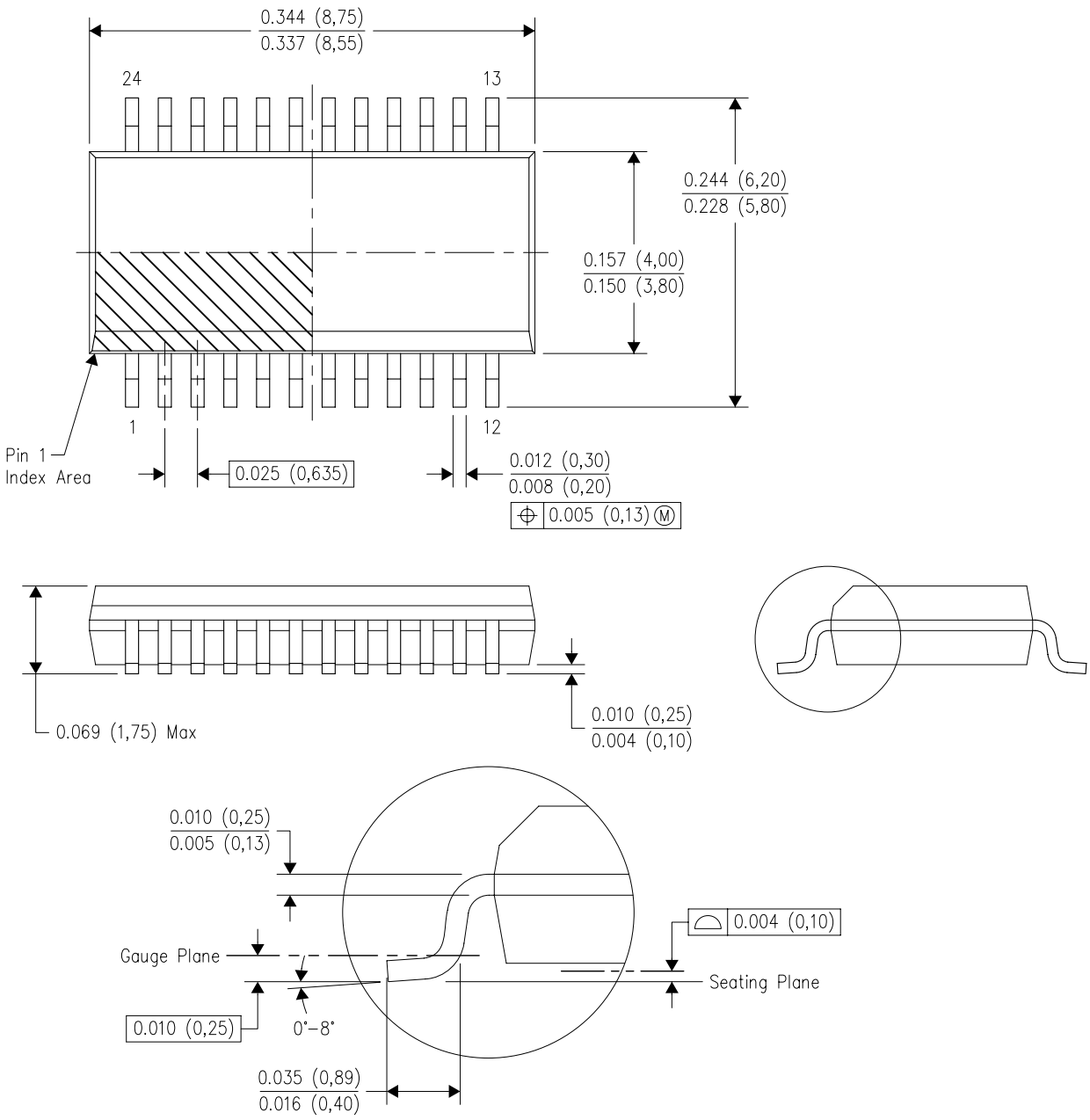
**TAPE AND REEL BOX DIMENSIONS**




*All dimensions are nominal

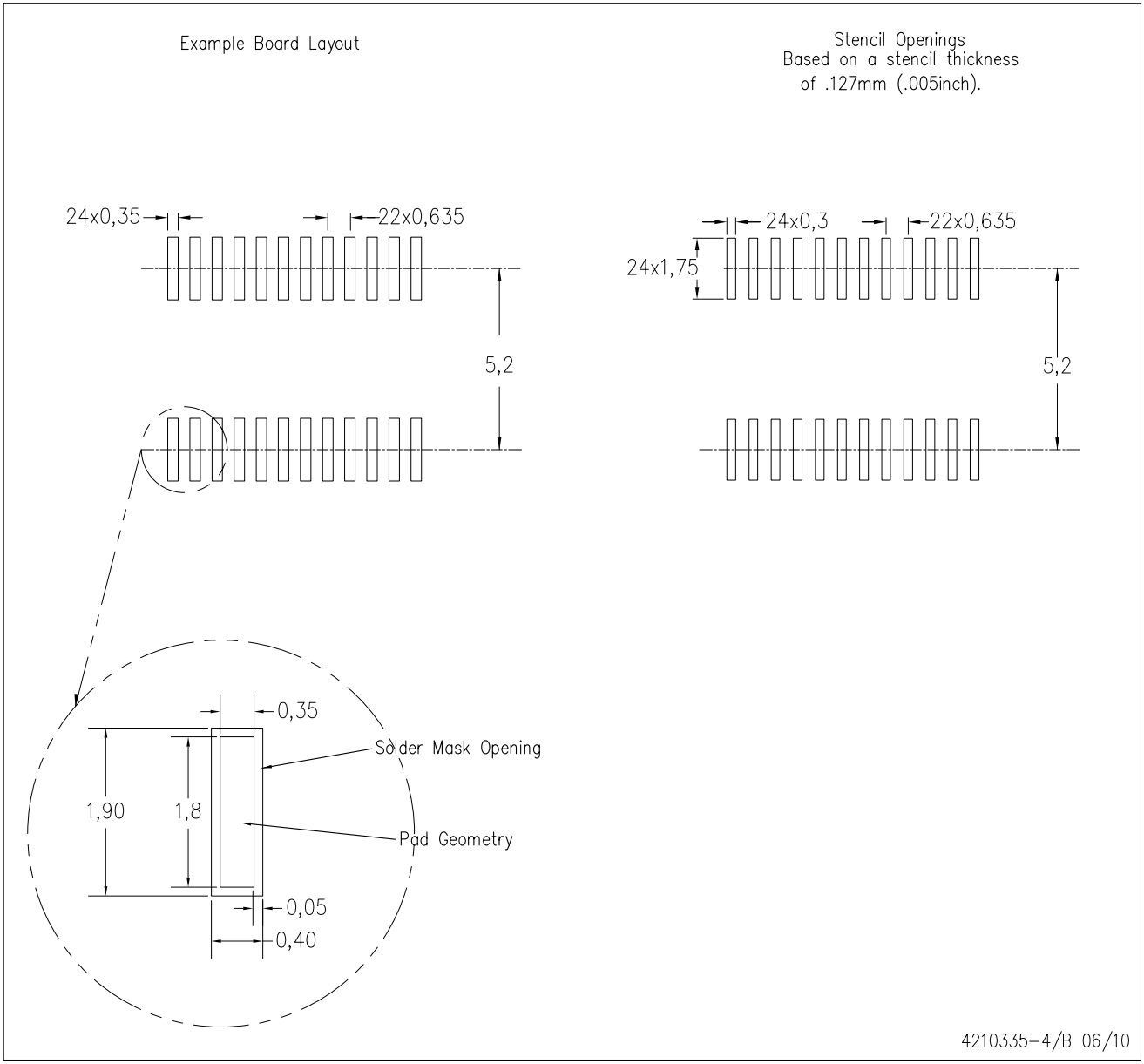
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CY74FCT2646ATQCT | SSOP/QSOP | DBQ | 24 | 2500 | 346.0 | 346.0 | 33.0 |

DBQ (R–PDSO–G24) PLASTIC SMALL–OUTLINE PACKAGE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO–137 variation AE.

DBQ (R–PDSO–G24) PLASTIC SMALL OUTLINE PACKAGE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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