ADSANTEC
Ultra High-Speed Mixed Signal ASICs

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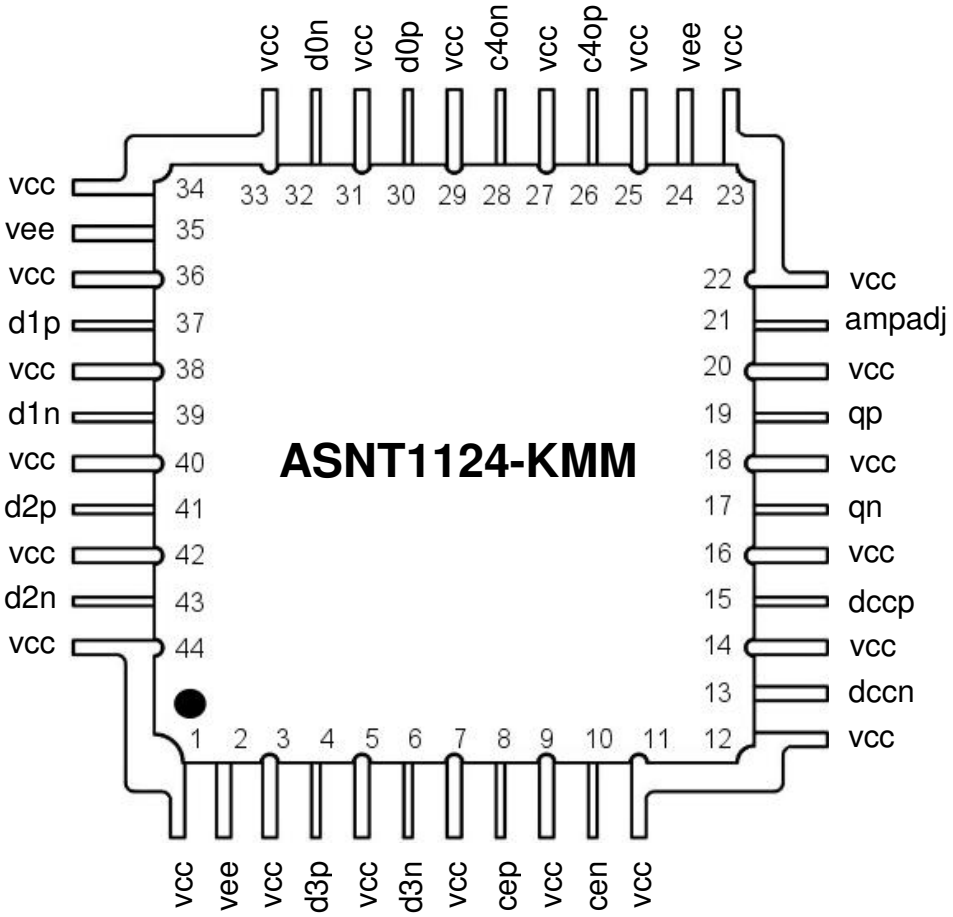
# ASNT1124-KMM
# DC-64*Gbps* Broadband Digital DDR 4:1 Multiplexer

- High speed broadband 4:1 Multiplexer (MUX)
- Exhibits low jitter and limited temperature variation over industrial temperature range
- Ideal for high speed proof-of-concept prototyping
- Differential CML I/O data and clock buffers
- Differential duty cycle adjustment control for input clock
- SE amplitude adjustment control for output data
- Half-rate clock input (DDR mode)
- Quarter-rate clock output
- Single +3.3*V* or -3.3*V* power supply
- Power consumption: 1.18*W*
- Fabricated in SiGe for high performance, yield, and reliability
- Custom CQFP 44-pin package



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# DESCRIPTION

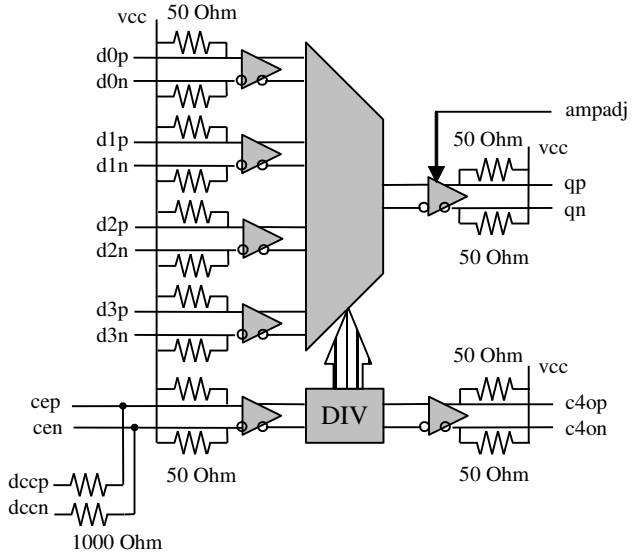


*Fig. 1. Functional Block Diagram*

The ASNT1124-KMM SiGe IC is a low power and high-speed digital 4 to 1 serializer-multiplexer (MUX) that functions seamlessly over data rates ($f_{bit}$) ranging from DC to its maximum frequency.

The main function of the part shown in Fig. 1 is to multiplex 4 parallel differential CML data signals d0p/d0n, d1p/d1n, d2p/d2n, d3p/d3n running at a bit rate of $f_{bit}/4$ into a high speed serial bit stream qp/qn running at a bit rate of $f_{bit}$. Differential or single-ended half-rate clock cep/cen (DDR mode) must be provided by an external source for the part to function properly.

The serialized data words qp/qn and the clock divided-by-4 signal c4op/c4on are transmitted through CML output interfaces. The clock and data outputs are phase-matched to each other resulting in very little relative skew over the operating temperature range of the device.

The part's I/O's support the CML logic interface with on chip 50*Ohm* termination to vcc and may be used differentially, AC/DC coupled, single-ended, or in any combination (see also POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the AC-coupling mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance.

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# Output Amplitude Adjustment Port

The output amplitude is controlled through a SE tuning port ampadj. The simulated dependence of the output amplitude vs. the control voltage is shown in Fig. 2. The ampadj control signal should **not** be set higher than the default value of vcc – 0.66V (see Electrical Characteristics table for allowable range.)

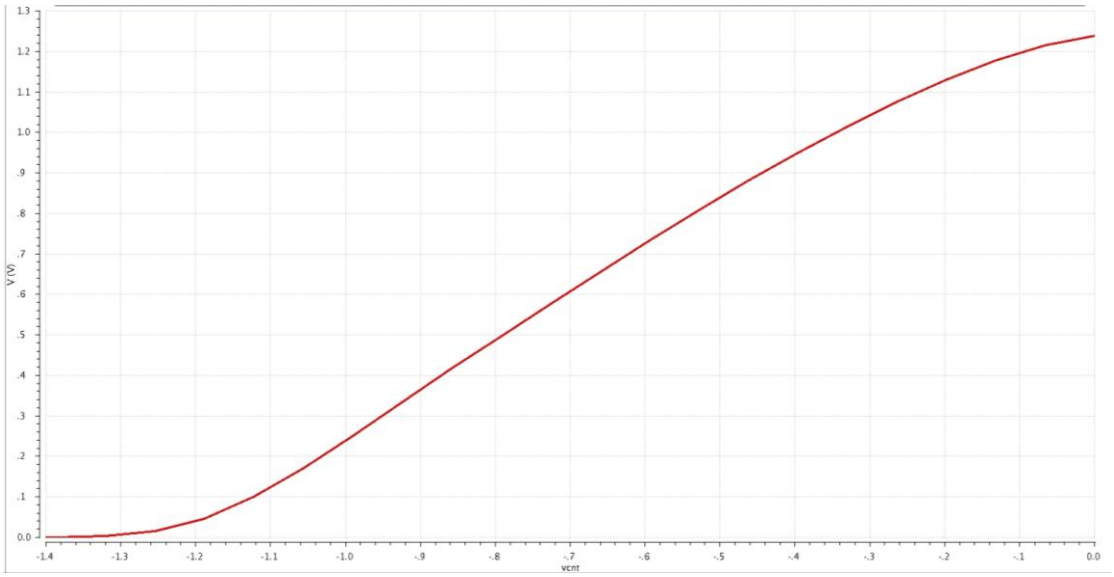


*Fig. 2. Simulated Output Amplitude vs. Control Voltage Diagram*

## *Input Clock Duty Cycle Adjustment Port*

In AC coupled mode of operation duty cycle of the input clock signal can be adjusted via a pair of DC analog tuning ports dccp and dccn. By lowering the voltage of one of the ports below vcc while keeping the other one at vcc or not connected the common mode voltage of the corresponding clock input can be lowered below vcc. If both control inputs are left not connected the common mode voltages of both clock inputs are at vcc. The dependence of either input clock common mode voltage on the control voltage is shown in Fig. 3.

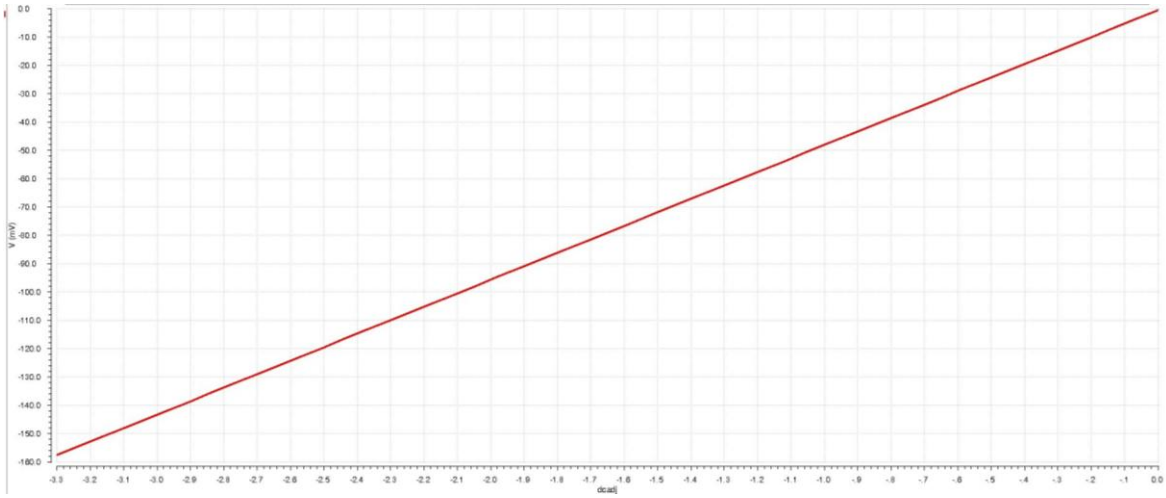


*Fig. 3. Dependence of cep (or cen) Common Mode Voltage on dccp (or dccn) Voltage*

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# POWER SUPPLY CONFIGURATION

The part can operate with either negative supply (vcc = 0.0*V* = ground and vee = −3.3*V*), or positive supply (vcc = +3.3*V* and vee = 0.0*V* = ground). In case of the positive supply, all I/Os need AC termination when connected to any devices with 50*Ohm* termination to ground. Different PCB layouts will be needed for each different power supply combination.

**All the characteristics detailed below assume vcc = 0.0*V* and vee = -3.3*V*.**

# ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 1 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground.

*Table 1. Absolute Maximum Ratings*

| Parameter | Min | Max | Units |
|---|---|---|---|
| Supply Voltage (vee) | | -3.6 | *V* |
| Power Consumption | | 1.3 | *W* |
| RF Input Voltage Swing (SE) | | 1.4 | *V* |
| Case Temperature | | +90 | *ºC* |
| Storage Temperature | -40 | +100 | *ºC* |
| Operational Humidity | 10 | 98 | % |
| Storage Humidity | 10 | 98 | % |

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# TERMINAL FUNCTIONS

| TERMINAL | | | DESCRIPTION |
|---|---|---|---|
| **Name** | **No.** | **Type** | |
| **Low-Speed I/Os** | | | |
| d0p | 30 | CML input | Differential quarter-rate data inputs with internal SE 50*Ohm* termination to vcc |
| d0n | 32 | | |
| d1p | 37 | CML input | Differential quarter-rate data inputs with internal SE 50*Ohm* termination to vcc |
| d1n | 39 | | |
| d2p | 41 | CML input | Differential quarter-rate data inputs with internal SE 50*Ohm* termination to vcc |
| d2n | 43 | | |
| d3p | 4 | CML input | Differential quarter-rate data inputs with internal SE 50*Ohm* termination to vcc |
| d3n | 6 | | |
| c4op | 26 | CML output | Differential quater-rate clock outputs with internal SE 50*Ohm* termination to vcc. Require external SE 50*Ohm* termination to vcc |
| c4on | 28 | | |
| **Analog DC Control Inputs** | | | |
| ampadj | 21 | Analog input | SE tuning port terminated to internal resistive divider between vee and vcc. |
| dccp | 15 | Analog inputs | Differential or SE tuning ports with internal SE connections to dp/dn through 1000*Ohm* resistors. |
| dccn | 13 | | |
| **High-Speed I/Os** | | | |
| cep | 8 | CML input | Differential half-rate clock input signals with internal 50*Ohm* termination to vcc |
| cen | 10 | | |
| qp | 19 | CML output | Differential full-rate data outputs with internal SE 50*Ohm* termination to vcc. Require external SE 50*Ohm* termination to vcc |
| qn | 17 | | |

| **Supply and Termination Voltages** | | |
|---|---|---|
| **Name** | **Description** | **Pin Number** |
| vcc | Positive power supply (+3.3*V* or 0) | 1, 3, 5, 7, 9, 11, 12, 14, 16, 18, 20, 22, 23, 25, 27, 29, 31, 33, 34, 36, 38, 40, 42, 44 |
| vee | Negative power supply (0*V* or -3.3*V*) | 2, 24, 35 |

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# ELECTRICAL CHARACTERISTICS

| PARAMETER | MIN | TYP | MAX | UNIT | COMMENTS |
|---|---|---|---|---|---|
| **General Parameters** | | | | | |
| vee | -3.1 | -3.3 | -3.5 | *V* | ±6% |
| vcc | | 0.0 | | *V* | External ground |
| *I*vee | | 358 | | *mA* | |
| Power consumption | | 1180 | | *mW* | |
| Junction temperature | -40 | 25 | 125 | *°C* | |
| **LS Input Data (d0p/d0n, d1p/d1n, d2p/d2n, d3p/d3n)** | | | | | |
| Data Rate | DC | 10 | 16 | *Gb/s* | |
| Swing | 0.2 | | 0.8 | *V* | Differential or SE, p-p |
| CM Voltage Level | vcc-0.8 | | vcc | *V* | Must match for both inputs |
| **HS Input Clock (cep/cen)** | | | | | |
| Frequency | DC | 20 | 32 | *GHz* | |
| Swing | 0.2 | | 0.8 | *V* | Differential or SE, p-p |
| CM Voltage Level | vcc-0.8 | | vcc | *V* | Must match for both inputs |
| Duty Cycle | 40 | 50 | 60 | *%* | |
| **DC Tuning port (dccp/dccn)** | | | | | |
| Control voltage range | vee | | vcc | | |
| **DC Tuning port (ampadj)** | | | | | |
| Control voltage range | vcc-1.4 | | vcc-0.66 | *V* | Default voltage is vcc-0.66*V* |
| **HS Output Data (qp/qn)** | | | | | |
| Data Rate | DC | 40 | 64 | *Gb/s* | |
| Logic “1” level | | vcc | | *V* | |
| Logic “0” level | | vcc-0.4 | | *V* | With external 50*Ohm* DC termination |
| Output Jitter | | 2 | | *ps* | Peak-to-peak at 40*Gb/s* |
| **LS Output Clock (c4op/c4on)** | | | | | |
| Frequency | DC | 10 | 16 | *GHz* | |
| Logic “1” level | | vcc | | *V* | |
| Logic “0” level | | vcc-0.4 | | *V* | With external 50*Ohm* DC termination |
| Duty Cycle | | 50 | | *%* | |
| Output Jitter | | | 1 | *ps* | Peak-to-peak at 10*GHz* |

# PACKAGE INFORMATION

The chip die is housed in a custom 44-pin CQFP package shown in Fig. 4. The package provides a center heat slug located on its back side to be used for heat dissipation. ADSANTEC recommends for this section to be soldered to the vcc plain, which is ground for a negative supply, or power for a positive supply.

The part’s identification label is ASNT1124-KMM. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part

version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

The IC complies with the Restriction of Hazardous Substances (RoHS) per 2011/65/EU for all ten substances.

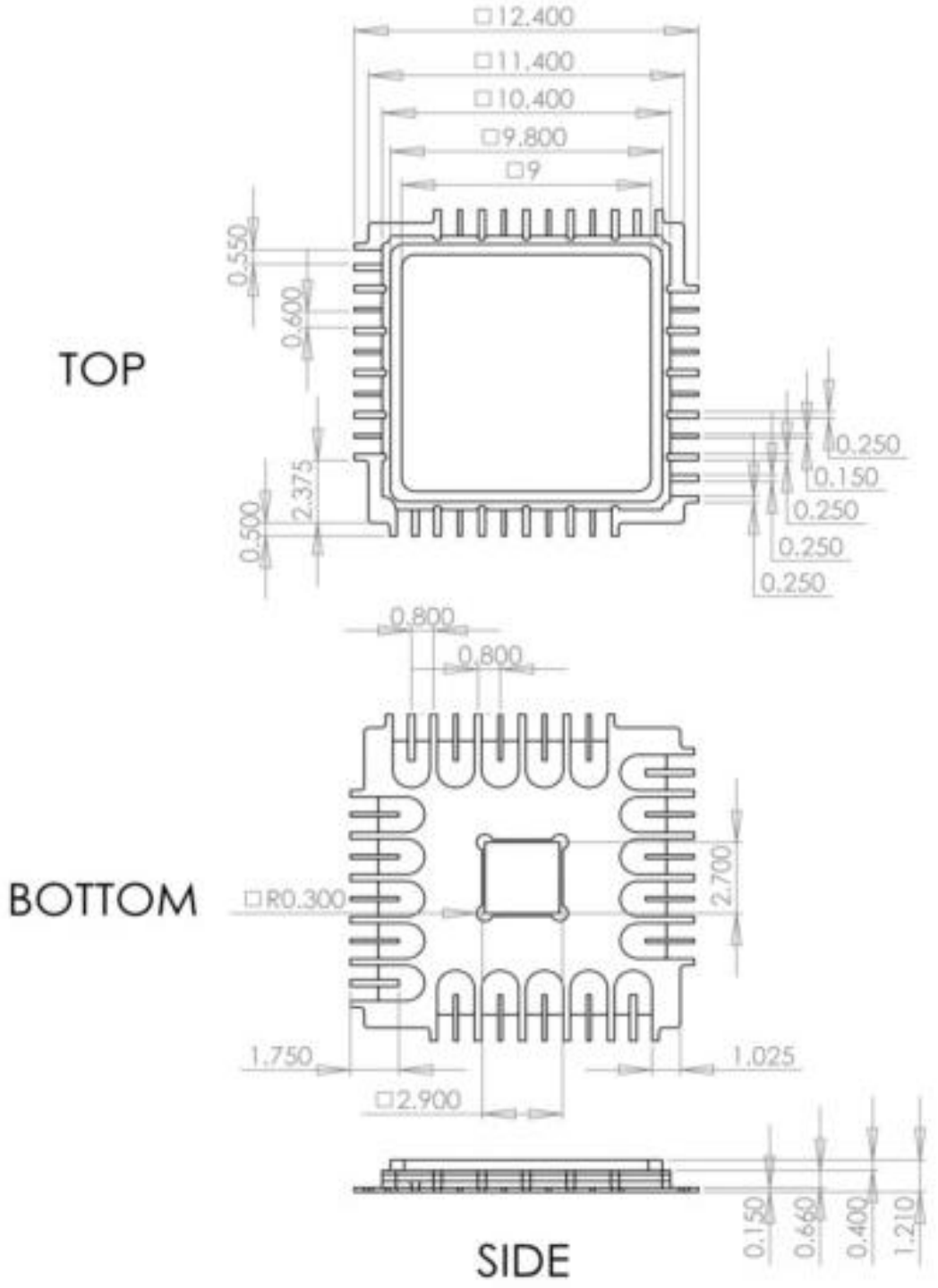


*Fig. 4. CQFP 44-Pin Package Drawing (All Dimensions in mm)*

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# REVISION HISTORY

| Revision | Date | Changes |
|---|---|---|
| 1.2.2 | 05-2020 | Updated Package Information |
| 1.1.2 | 07-2019 | Updated Letterhead |
| 1.1.1 | 07-2015 | Correction of the duty cycle control function description including:<br>- block diagram<br>- pinout diagram<br>- part description<br>- terminal functions<br>Corrected power consumption and current consumption<br>Modified maximum voltage value on DC tuning port ampadj |
| 1.0.1 | 05-2015 | First release |
| 1.0.0 | 09-2014 | Preliminary release |