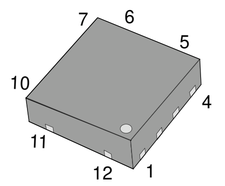
STL7N60M2

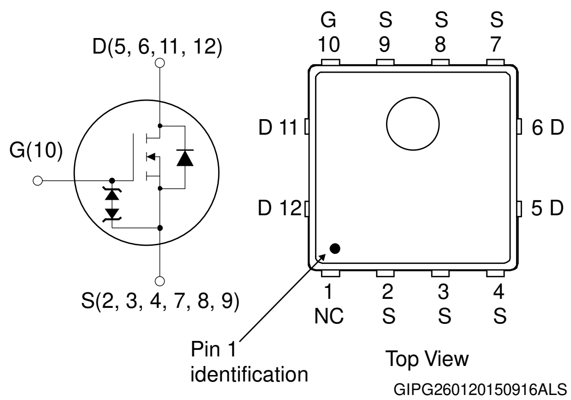
N-channel 600 V, 0.92 Ω typ., 5 A MDmesh™ M2 Power MOSFET in a PowerFLAT™ 5x5 package

Datasheet - production data



PowerFLAT™ 5x5

Figure 1: Internal schematic diagram



Features

Order code	V_{DS} @ Tjmax	$R_{DS(on)}$ max	I_D
STL7N60M2	650 V	1.05 Ω	5 A

- Extremely low gate charge
- Excellent output capacitance (C_{OSS}) profile
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using MDmesh™ M2 technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance and optimized switching characteristics, rendering it suitable for the most demanding high efficiency converters.

Table 1: Device summary

Order code	Marking	Package	Packaging
STL7N60M2	7N60M2	PowerFLAT 5x5	Tape and reel

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at T_C = 25 °C	5	A
I_D	Drain current (continuous) at T_C = 100 °C	3.2	A
I_{DM}(1)	Drain current (pulsed)	20	A
I_D(2)	Drain current (continuous) at T_{pcb} = 25 °C	1.2	A
I_D(2)	Drain current (continuous) at T_{pcb} = 100 °C	0.8	A
I_{DM}(1)(2)	Drain current (pulsed)	4.8	A
P_{TOT}	Total dissipation at T_C = 25 °C	67	W
P_{TOT}(2)	Total dissipation at T_{pcb} = 25 °C	4	W
dv/dt(3)	Peak diode recovery voltage slope	15	V/ns
dv/dt(4)	MOSFET dv/dt ruggedness	50	V/ns
T_{stg}	Storage temperature	- 55 to 150	°C
T_j	Max. operating junction temperature	150	°C

Notes:

(1)Pulse width limited by safe operating area.

(2)When mounted on FR-4 Board of 1 inch², 2 oz Cu (t < 10 s)

(3)I_{SD} ≤ 5 A, di/dt ≤ 400 A/μs; $V_{DS\ peak}$ < $V_{(BR)DSS}$, V_{DD} = 400 V.

(4)V_{DS} ≤ 480 V

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.83	°C/W
$R_{thj-pcb}$	Thermal resistance junction-pcb max	31.3	°C/W

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	1	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}; V_{DD} = 50 V)	80	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified

Table 5: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	600			V
I_{DSS}	Zero gate voltage Drain current	V_{GS} = 0 V, V_{DS} = 600 V			1	µA
		V_{GS} = 0 V, V_{DS} = 600 V, T_C = 125 °C			100	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 2 A		0.92	1.05	Ω

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS}= 100 V, f = 1 MHz, V_{GS} = 0 V	-	271	-	pF
C_{oss}	Output capacitance		-	15.7	-	pF
C_{rss}	Reverse transfer capacitance		-	0.68	-	pF
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{DS} = 0 to 480 V, V_{GS} = 0 V	-	75.5	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	7.2	-	Ω
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 5 A, V_{GS} = 10 V (see *Figure 15: "Gate charge test circuit"*)	-	8.8	-	nC
Q_{gs}	Gate-source charge		-	1.8	-	nC
Q_{gd}	Gate-drain charge		-	4.3	-	nC

Notes:

(1) $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 2.5 A R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 14: "Switching times test circuit for resistive load"* and *Figure 19: "Switching time waveform"*)	-	7.6	-	ns
t_r	Rise time		-	7.2	-	ns
$t_{d(off)}$	Turn-off-delay time		-	19.3	-	ns
t_f	Fall time		-	15.9	-	ns

Table 8: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		5	A
I_{SDM} (1)	Source-drain current (pulsed)		-		20	A
V_{SD} (2)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 5 A	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 5 A, di/dt = 100 A/µs, V_{DD} = 60 V (see *Figure 19: "Switching time waveform"*)	-	275		ns
Q_{rr}	Reverse recovery charge		-	1.55		µC
I_{RRM}	Reverse recovery current		-	11		A
t_{rr}	Reverse recovery time	I_{SD} = 5 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_j = 150 °C (see *Figure 19: "Switching time waveform"*)	-	376		ns
Q_{rr}	Reverse recovery charge		-	2.1		µC
I_{RRM}	Reverse recovery current		-	11		A

Notes:

(1)Pulse width is limited by safe operating area

(2)Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.2 Electrical characteristics (curves)

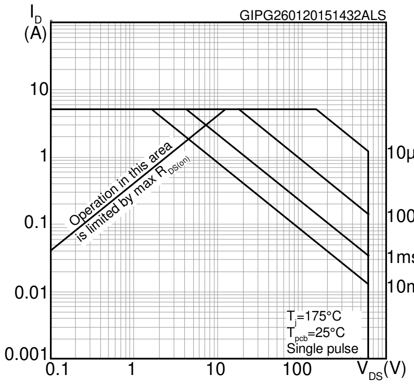


Figure 2: Safe operating area

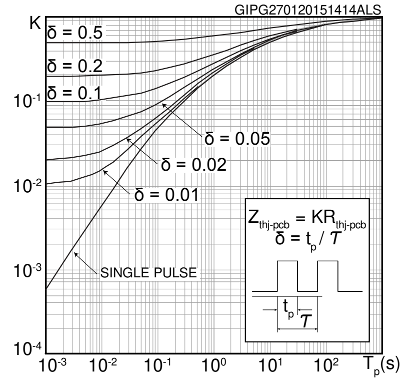


Figure 3: Thermal impedance

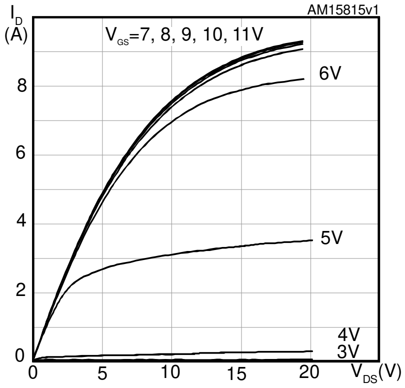


Figure 4: Output characteristics

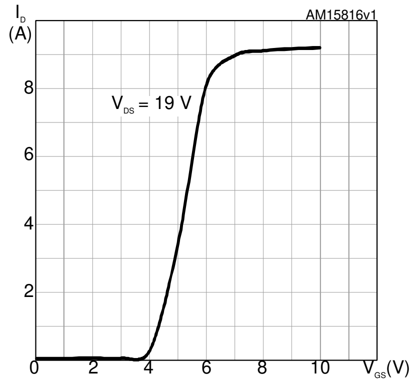


Figure 5: Transfer characteristics

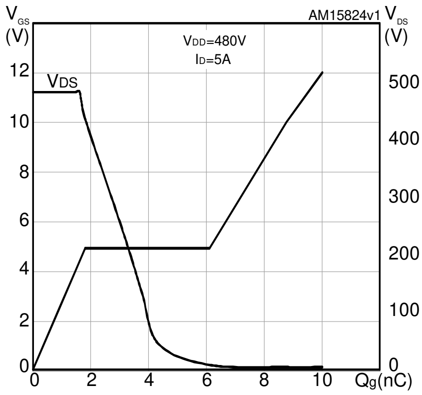


Figure 6: Gate charge vs gate-source voltage

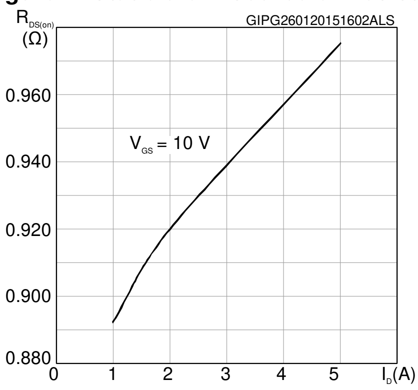


Figure 7: Static drain-source on-resistance

Figure 8: Capacitance variations

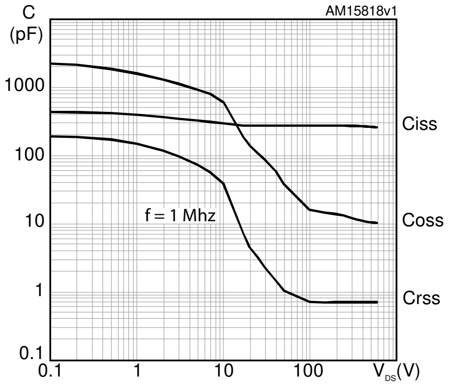


Figure 9: Output capacitance stored energy

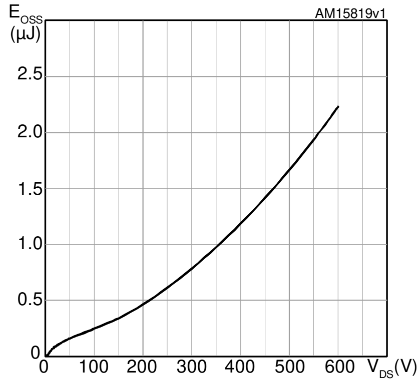


Figure 10: Normalized gate threshold voltage vs temperature

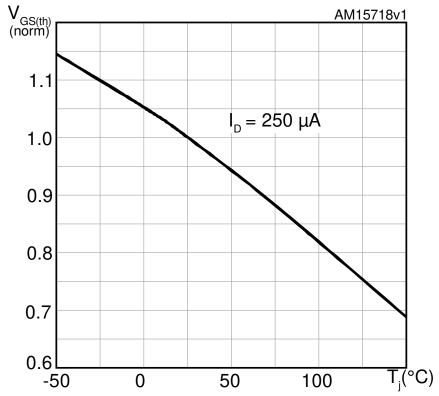


Figure 11: Normalized on-resistance vs temperature

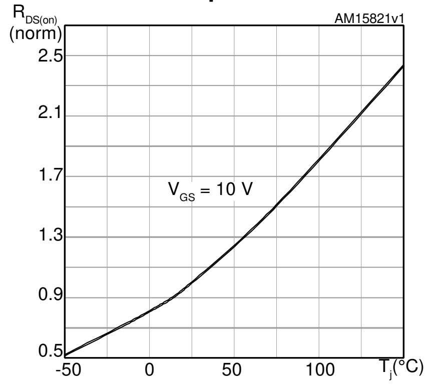


Figure 12: Source-drain diode forward characteristics

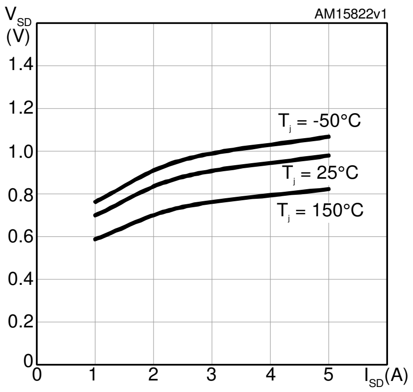
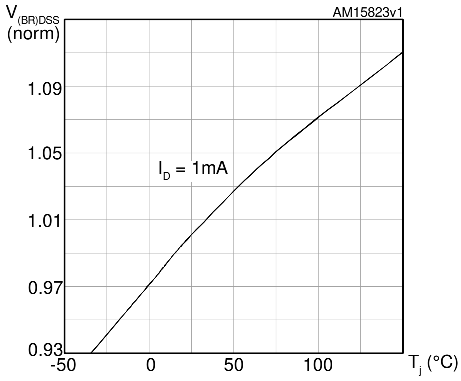


Figure 13: Normalized V(BR)DSS vs temperature



3 Test circuits

Figure 14: Switching times test circuit for resistive load

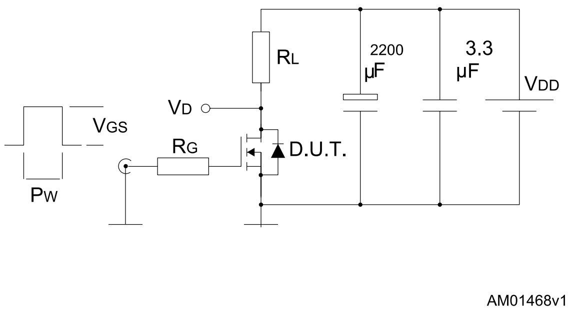


Figure 15: Gate charge test circuit

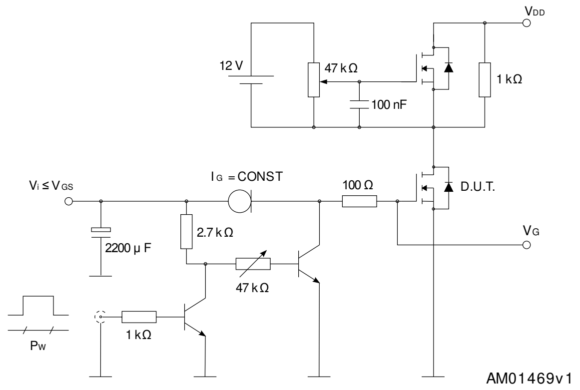


Figure 16: Test circuit for inductive load switching and diode recovery times

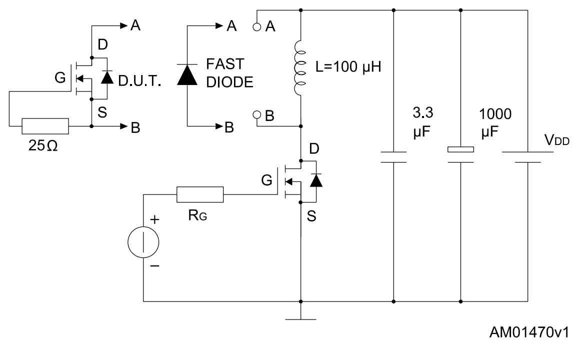


Figure 17: Unclamped inductive load test circuit

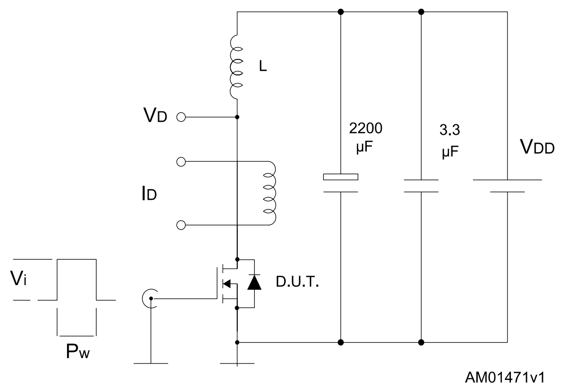


Figure 18: Unclamped inductive waveform

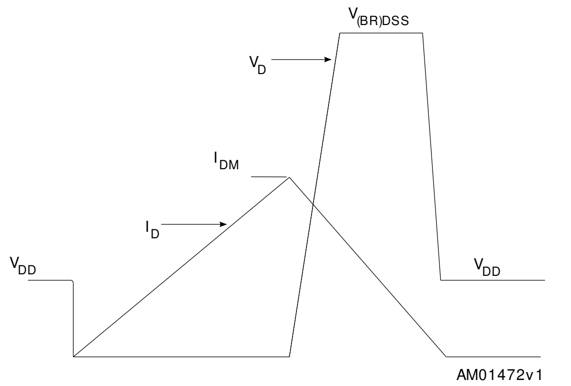
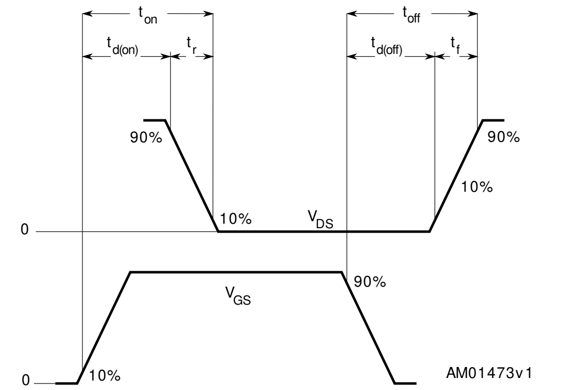


Figure 19: Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 Package mechanical data

Figure 20: PowerFLAT™ 5x5 drawings

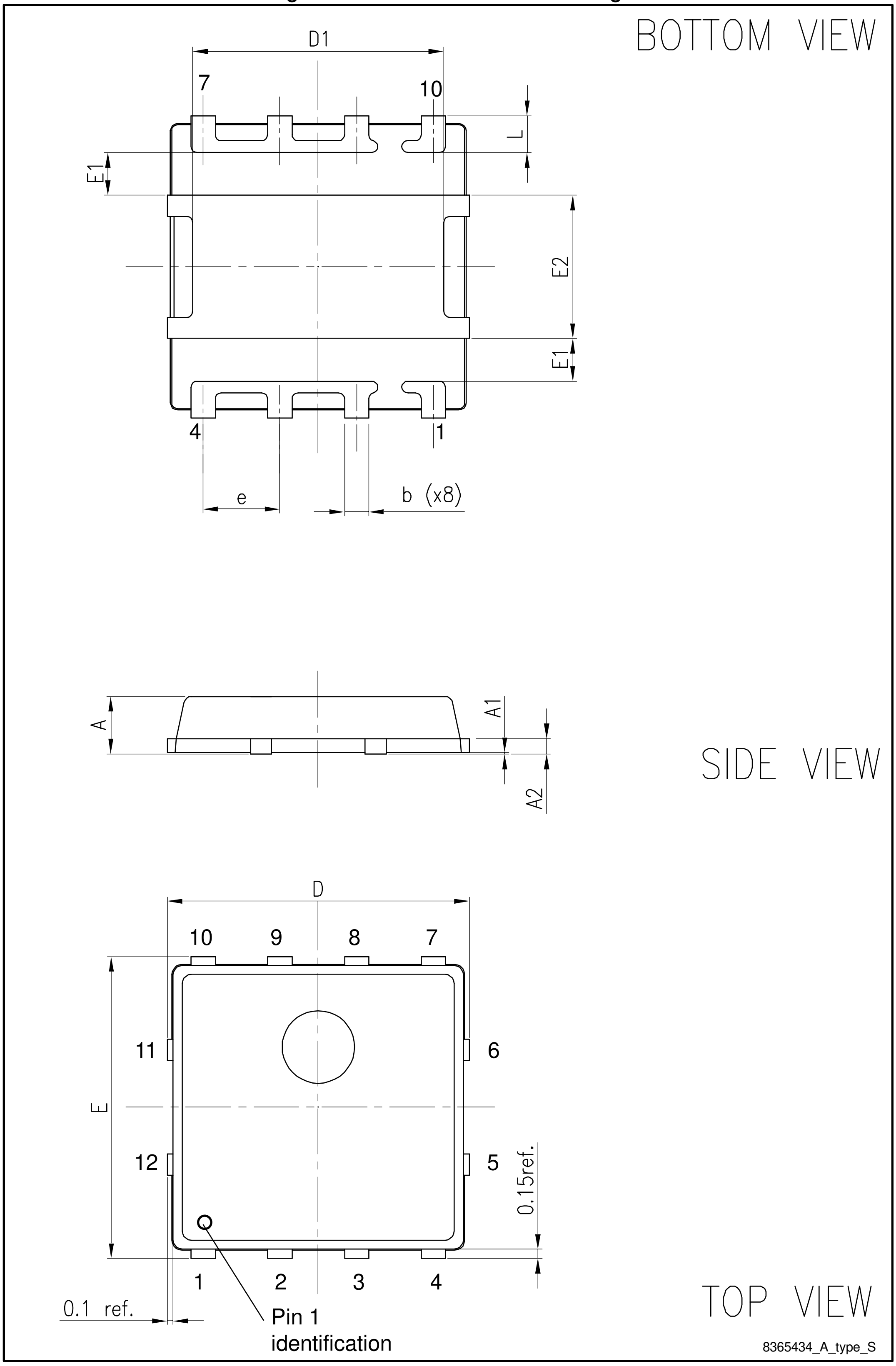
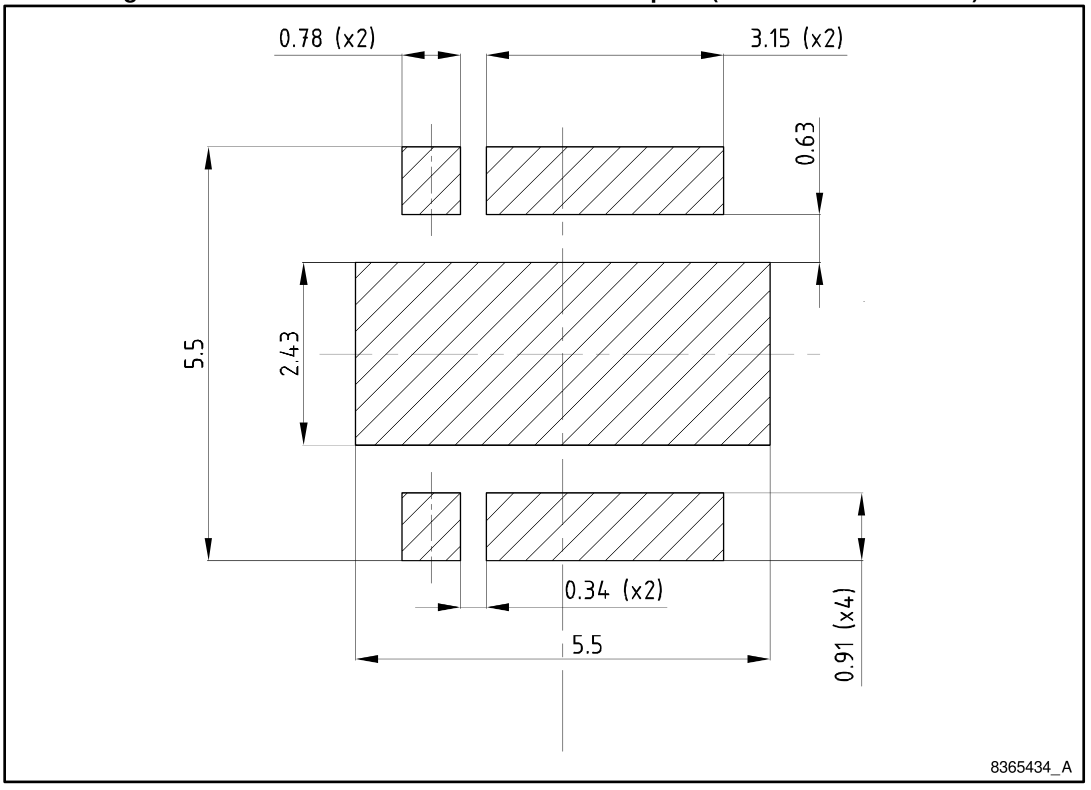


Table 9: PowerFLAT 5x5 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.0
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D		5.00	
D1	4.05		4.25
E		5.00	
E1	0.64		0.79
E2	2.25		2.45
e		1.27	
L	0.45		0.75

Figure 21: PowerFLAT™ 5x5 recommended footprint (dimensions are in mm)



5 Revision history

Table 10: Document revision history

Date	Revision	Changes
26-Jan-2015	1	First release.