ISO742x Low-Power Dual Channel Digital Isolators

1 Features

- Signaling Rate > 50 Mbps
- Default Output 'High' and 'Low' Options
- Low Power Consumption: Typical I_{CC} per Channel (3.3-V Supplies):
  - ISO7420: 1.4 mA at 1 Mbps, 2.5 mA at 25 Mbps
  - ISO7421: 1.8 mA at 1 Mbps, 2.8 mA at 25 Mbps
- Low Propagation Delay: 7 ns Typical
- Low Pulse Skew: 200 ps Typical
- Wide T_A Range Specified: –40°C to 125°C
- 50-KV/µs Transient Immunity, Typical
- Isolation Barrier Life: > 25 Years
- Operates from 3-V to 5.5-V Supply Levels
- 3.3-V and 5-V Level Translation
- Narrow Body SOIC-8 Package
- Safety and Regulatory Approvals:
  - 4242 V_{PK} Isolation per DIN V VDE V 0884-10 and DIN EN 61010-1
  - 2500 V_{RMS} Isolation for 1 minute per UL 1577
  - CSA Component Acceptance Notice 5A, IEC 60950-1 and IEC 61010-1 Standards
  - CQC Certification per GB4943.1-2011
  -

2 Applications

- Opto-Coupler Replacement in:
  - Industrial FieldBus
    - ProfiBus
    - ModBus
    - DeviceNet™ Data Buses
  - Servo Control Interface
  - Motor Control
  - Power Supplies
  - Battery Packs

3 Description

ISO742x provide galvanic isolation up to 2500 V_{RMS} for 1 minute per UL and 4242 V_{PK} per VDE. These devices have two isolated channels. Each channel has a logic input and output buffer separated by a silicon dioxide (SiO_2) insulation barrier. Used in conjunction with isolated power supplies, these devices prevent noise currents on a data bus or other circuit from entering the local ground and interfering with or damaging sensitive circuitry. ISO7420 has both channels in the same direction while ISO7421 has the two channels in opposite direction. In case of input power or signal loss, default output is 'low' for devices with suffix 'F' and 'high' for devices without suffix 'F'. ISO742x have no integrated noise filter and thus have fast propagation delays.

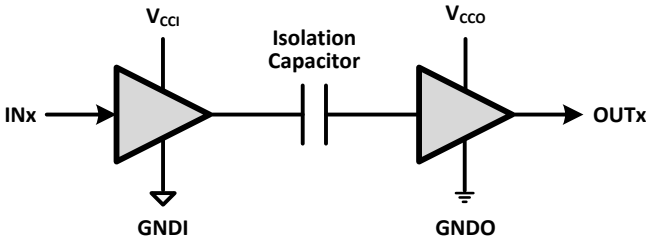
These devices have TTL input thresholds and operate from 3-V to 5.5-V supplies. All inputs are 5-V tolerant when supplied from a 3.3-V supply.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ISO7420E	SOIC (8)	4.90 mm x 3.91 mm
ISO7420FE		
ISO7421E		
ISO7421FE		

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



V_{CCI} and GNDI are supply and ground connections respectively for the input channels.

V_{CCO} and GNDO are supply and ground connections respectively for the output channels.

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (January 2013) to Revision F — **Page**

- Changed the datasheet format to the new TI standard ... 1
- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted text from the Description: "CC-grade devices have integrated 10ns-filters for harsh environments where short noise pulses may be present at the device input pins." ... 1
- VDE standard changed to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 ... 1
- Deleted CC-grade from t_{PLH}, t_{PHL} in the Switching Characteristics table ... 10
- Deleted CC-grade from t_{PLH}, t_{PHL} in the Switching Characteristics table ... 10
- Deleted CC-grade from t_{PLH}, t_{PHL} in the Switching Characteristics table ... 11
- Deleted CC-grade from t_{PLH}, t_{PHL} in the Switching Characteristics table ... 11
- Changed the Available Options Table To the Feature Description table ... 17

Changes from Revision D (December 2011) to Revision E — **Page**

- Deleted devices ISO7420FCC and ISO7421FCC ... 1
- Changed the NOTE: text ... 17
- Added table Note to V_{IORM} ... 18
- Changed Z to Undetermined for the OUTPUT OUTA, OUTB column of the FUNCTION TABLE ... 20

Changes from Revision C (March 2011) to Revision D **Page**

- Changed SAFETY feature Bullet From: UL 1577 Approved; Other Approvals Pending To: All Agencies Approvals Completed 1
- Changed the REGULATORY INFORMATION table 18

Changes from Revision B (January 2011) to Revision C **Page**

- Added devices ISO7420FCC and ISO7421FCC 1
- Changed Feature bullet To: Low Propagation Delay: 7 ns Typical (E-Grade) 1
- Changed Feature bullet To: Low Pulse Skew: 200 Typical (E-Grade) 1
- Changed the SAFETY and REGULATORY APPROVALS list 1
- Changed the data sheet DESCRIPTION 1
- Changed the Supply Current values for ISO7421x at 10, 25, and 50 Mbps 6
- Changed the Supply Current values for ISO7421x at 10, 25, and 50 Mbps 7
- Changed the Supply Current values for ISO7421x at 10, 25, and 50 Mbps 8
- Changed the Supply Current values for ISO7421x 25 and 50 Mbps 9
- Added CC-grade and valued to t_{PLH}, t_{PHL} in the Switching Characteristics table 10
- Added ISO7421x values for Pulse width distortion, Channel-to-channel output skew time, and Part-to-part skew time 10
- Added CC-grade and valued to t_{PLH}, t_{PHL} in the Switching Characteristics table 10
- Added ISO7421x values for Pulse width distortion and Channel-to-channel output skew time 10
- Added CC-grade and valued to t_{PLH}, t_{PHL} in the Switching Characteristics table 11
- Added CC-grade and valued to t_{PLH}, t_{PHL} in the Switching Characteristics table 11
- Added graphs Figure 5, Figure 6, Figure 7, and Figure 8 12
- Added graphs Figure 14 and Figure 15 13
- Changed Note 1 Figure 16 15
- Changed Figure 17 15
- Changed the Available Options Table 17
- Changed Isolation resistance test conditions 17
- Changed the values of V_{IORM} and V_{PR} in the INSULATION CHARACTERISTICS table 18
- Changed the value of V_{IOTM} in the INSULATION CHARACTERISTICS table From: 4000 To: 4242 18
- Changed Figure 21 19
- Changed PU to X in the last row of the FUNCTION TABLE 20
- Added section: SUPPLY CURRENT EQUATIONS 22

Changes from Revision A (December 2010) to Revision B **Page**

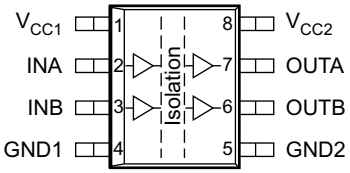
- Changed Feature bullet From: ISO7421: TBDmA at 1Mbps, TBDmA at 25Mbps To: ISO7421: 1.8mA at 1Mbps, 2.8mA at 25Mbps 1
- Updated the ISO7421x Supply Current values for V_{CC1} and V_{CC2} = 5V 6
- Updated the ISO7421x Supply Current values for V_{CC1} = 5V and V_{CC2} = 3.3V 7
- Updated the ISO7421x Supply Current values for V_{CC1} = 3.3V and V_{CC2} = 5V 8
- Updated the ISO7421x Supply Current values for V_{CC1} and V_{CC2} = 3.3V 9

Changes from Original (December 2010) to Revision A **Page**

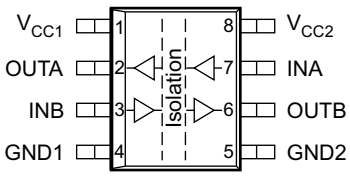
- Changed the Max values for Supply current for V_{CC1} and V_{CC2}, C_L = 15pF 9

5 Pin Configuration and Functions

ISO7420 D Package
8-Pin SOIC
Top View



ISO7421 D Package
8-Pin SOIC
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	ISO7420x	ISO7421x		
INA	2	7	I	Input, channel A
INB	3	3	I	Input, channel B
GND1	4	4	–	Ground connection for V_{CC1}
GND2	5	5	–	Ground connection for V_{CC2}
OUTA	7	2	O	Output, channel A
OUTB	6	6	O	Output, channel B
V_{CC1}	1	1	–	Power supply, V_{CC1}
V_{CC2}	8	8	–	Power supply, V_{CC2}

6 Specifications

6.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage(2), V_{CC1}, V_{CC2}	–0.5	6	V
V_I	Voltage at IN, OUT	–0.5	V_{CC} + 0.5(3)	V
I_O	Output current		±15	mA
V_{SRG}	Maximum surge immunity - Supports IEC 61000-4-5		4000	V_{PK}
$T_{J(Max)}$	Maximum junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal and are peak voltage values.
(3) Maximum voltage must not exceed 6 V.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	
		Machine model (MM) ANSI/ESDS5.2-1996	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage	3.0		5.5	V
I_{OH}	High-level output current	–4			mA
I_{OL}	Low-level output current			4	mA
V_{IH}	High-level input voltage	2		5.5	V
V_{IL}	Low-level input voltage	0		0.8	V
t_{ui}	Input pulse duration	20			ns
1 / t_{ui}	Signaling rate	0		50(1)	Mbps
T_J(2)	Junction temperature	–40		136	°C
T_A	Ambient Temperature	-40	25	125	°C

(1) Under typical conditions, these devices are capable of signaling rate > 150 Mbps.
(2) To maintain the recommended operating conditions for T_J, see the *Thermal Information* table.

6.4 Thermal Information

THERMAL METRIC(1)			ISO742x D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	Low-K board	212	°C/W
		High-K board	116.6	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		71.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		57.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter		28.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter		56.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics: V_{CC1} and V_{CC2} = 5 V ± 10%

T_A = –40°C to 125°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 16.		V_{CCO} (1) – 0.8	4.6		V
		I_{OH} = –20 µA; see Figure 16.		V_{CCO} – 0.1	5		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 16.			0.2	0.4	V
		I_{OL} = 20 µA; see Figure 16.			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				400		mV
I_{IH}	High-level input current	INx at 0 V or V_{CCI} (1)				10	µA
I_{IL}	Low-level input current			–10			µA
CMTI	Common-mode transient immunity	V_I = V_{CCI} or 0 V; see Figure 18.		25	50		kV/µs
SUPPLY CURRENT (ALL INPUTS SWITCHING WITH SQUARE WAVE CLOCK SIGNAL FOR DYNAMIC I_{CC} MEASUREMENT)							
	ISO7420x						
I_{CC1}	Supply current for V_{CC1} and V_{CC2}	DC to 1 Mbps	DC Input: V_I = V_{CCI} or 0 V, AC Input: C_L = 15 pF		0.4	0.8	mA
I_{CC2}					3.4	5	
I_{CC1}		10 Mbps	C_L = 15 pF		0.6	1	
I_{CC2}					4.5	6	
I_{CC1}		25 Mbps			1	1.5	
I_{CC2}					6.2	8	
I_{CC1}		50 Mbps			1.7	2.5	
I_{CC2}					9	12	
	ISO7421x						
I_{CC1}	Supply current for V_{CC1} and V_{CC2}	DC to 1 Mbps	DC Input: V_I = V_{CCI} or 0 V, AC Input: C_L = 15 pF		2.3	3.6	mA
I_{CC2}					2.3	3.6	
I_{CC1}		10 Mbps	C_L = 15 pF		2.9	4.5	
I_{CC2}					2.9	4.5	
I_{CC1}		25 Mbps			4.3	6	
I_{CC2}					4.3	6	
I_{CC1}		50 Mbps			6	8.5	
I_{CC2}					6	8.5	

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}

6.6 Electrical Characteristics: V_{CC1} = 5 V ± 10%, V_{CC2} = 3.3 V ± 10%

T_A = –40°C to 125°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 16.	ISO7421x (5-V side)	V_{CC1} – 0.8	4.6		V
			ISO7420x/7421x (3.3-V side)	V_{CC2} - 0.4	3		
		I_{OH} = –20 µA; see Figure 16,	ISO7421x (5-V side)	V_{CC1} – 0.1	5		
			ISO7420x/7421x (3.3-V side)	V_{CC2} – 0.1	3.3		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 16.			0.2	0.4	V
		I_{OL} = 20 µA; see Figure 16.			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				400		mV
I_{IH}	High-level input current	INx at 0 V or V_{CCI}				10	µA
I_{IL}	Low-level input current			–10			µA
CMTI	Common-mode transient immunity	V_I = V_{CCI} or 0 V; see Figure 18.		25	50		kV/µs
SUPPLY CURRENT (ALL INPUTS SWITCHING WITH SQUARE WAVE CLOCK SIGNAL FOR DYNAMIC I_{CC} MEASUREMENT)							
	ISO7420x						
I_{CC1}	Supply current for V_{CC1} and V_{CC2}	DC to 1 Mbps	DC Input: V_I = V_{CCI} or 0 V, AC Input: C_L = 15 pF		0.4	0.8	mA
I_{CC2}					2.6	3.7	
I_{CC1}		10 Mbps	C_L = 15 pF		0.6	1	
I_{CC2}					3.3	4.3	
I_{CC1}		25 Mbps			1	1.5	
I_{CC2}					4.4	5.6	
I_{CC1}		50 Mbps			1.7	2.5	
I_{CC2}					6.2	7.5	
	ISO7421x						
I_{CC1}	Supply current for V_{CC1} and V_{CC2}	DC to 1 Mbps	DC Input: V_I = V_{CCI} or 0 V, AC Input: C_L = 15 pF		2.3	3.6	mA
I_{CC2}					1.8	2.8	
I_{CC1}		10 Mbps	C_L = 15 pF		2.9	4.5	
I_{CC2}					2.2	3.2	
I_{CC1}		25 Mbps			4.3	6	
I_{CC2}					2.8	4.1	
I_{CC1}		50 Mbps			6	8.5	
I_{CC2}					3.8	5.5	

6.7 Electrical Characteristics: V_{CC1} = 3.3 V ± 10%, V_{CC2} = 5 V ± 10%

T_A = –40°C to 125°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 16.	ISO7421x (3.3-V side)	V_{CC1} – 0.4	3		V
			ISO7420x/7421x (5-V side)	V_{CC2} – 0.8	4.6		
		I_{OH} = –20 µA; see Figure 16	ISO7421x (3.3-V side)	V_{CC1} – 0.1	3.3		
			ISO7420x/7421x (5-V side)	V_{CC2} – 0.1	5		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 16.			0.2	0.4	V
		I_{OL} = 20 µA; see Figure 16.			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				400		mV
I_{IH}	High-level input current	INx at 0 V or V_{CCI}				10	µA
I_{IL}	Low-level input current			–10			µA
CMTI	Common-mode transient immunity	V_I = V_{CCI} or 0 V; see Figure 18.		25	50		kV/µs
SUPPLY CURRENT (ALL INPUTS SWITCHING WITH SQUARE WAVE CLOCK SIGNAL FOR DYNAMIC I_{CC} MEASUREMENT)							
	ISO7420x						
I_{CC1}	Supply current for V_{CC1} and V_{CC2}	DC to 1 Mbps	DC Input: V_I = V_{CCI} or 0 V, AC Input: C_L = 15 pF		0.2	0.4	mA
I_{CC2}					3.4	5	
I_{CC1}		10 Mbps	C_L = 15 pF		0.4	0.6	
I_{CC2}					4.5	6	
I_{CC1}		25 Mbps			0.6	0.9	
I_{CC2}					6.2	8	
I_{CC1}		50 Mbps			1	1.3	
I_{CC2}					9	12	
	ISO7421x						
I_{CC1}	Supply current for V_{CC2} and V_{CC2}	DC to 1 Mbps	DC Input: V_I = V_{CCI} or 0 V, AC Input: C_L = 15 pF		1.8	2.8	mA
I_{CC2}					2.3	3.6	
I_{CC1}		10 Mbps	C_L = 15 pF		2.2	3.2	
I_{CC2}					2.9	4.5	
I_{CC1}		25 Mbps			2.8	4.1	
I_{CC2}					4.3	6	
I_{CC1}		50 Mbps			3.8	5.5	
I_{CC2}					6	8.5	

6.8 Electrical Characteristics: V_{CC1} and V_{CC2} = 3.3 V ± 10%

T_A = –40°C to 125°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 16.		V_{CCO} (1) – 0.4	3		V
		I_{OH} = –20 µA; see Figure 16.		V_{CCO} – 0.1	3.3		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 16.			0.2	0.4	V
		I_{OL} = 20 µA; see Figure 16.			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				400		mV
I_{IH}	High-level input current	INx at 0 V or V_{CCI} (1)				10	µA
I_{IL}	Low-level input current			–10			µA
CMTI	Common-mode transient immunity	V_I = V_{CCI} or 0 V; see Figure 18.		25	50		kV/µs
SUPPLY CURRENT (ALL INPUTS SWITCHING WITH SQUARE WAVE CLOCK SIGNAL FOR DYNAMIC I_{CC} MEASUREMENT)							
	ISO7420x						
I_{CC1}	Supply current for V_{CC1} and V_{CC2}	DC to 1 Mbps	DC Input: V_I = V_{CCI} or 0 V, AC Input: C_L = 15 pF		0.2	0.4	mA
I_{CC2}					2.6	3.7	
I_{CC1}		10 Mbps	C_L = 15 pF		0.4	0.6	
I_{CC2}					3.3	4.3	
I_{CC1}		25 Mbps			0.6	0.9	
I_{CC2}					4.4	5.6	
I_{CC1}		50 Mbps			1	1.3	
I_{CC2}					6.2	7.5	
	ISO7421x						
I_{CC1}	Supply current for V_{CC2} and V_{CC2}	DC to 1 Mbps	DC Input: V_I = V_{CCI} or 0 V, AC Input: C_L = 15 pF		1.8	2.8	mA
I_{CC2}					1.8	2.8	
I_{CC1}		10 Mbps	C_L = 15 pF		2.2	3.2	
I_{CC2}					2.2	3.2	
I_{CC1}		25 Mbps			2.8	4.1	
I_{CC2}					2.8	4.1	
I_{CC1}		50 Mbps			3.8	5.5	
I_{CC2}					3.8	5.5	

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}

6.9 Power Dissipation Characteristics

THERMAL METRIC			ISO742x D (SOIC) 8 PINS	UNIT
P_D	Device power dissipation	V_{CC1} = V_{CC2} = 5.5 V, T_J = 150°C, C_L = 15 pF, Input a 100-Mbps 50% duty-cycle square wave	138	mW

6.10 Switching Characteristics: V_{CC1} and V_{CC2} = 5 V ± 10%

T_A = –40°C to 125°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time		See Figure 16.		7	11	ns
PWD(1)	Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$	ISO7420x			0.2	3	ns
		ISO7421x			0.3	3.7	
$t_{sk(o)}$(2)	Channel-to-channel output skew time	ISO7420x			0.3	1	ns
		ISO7421x			0.3	2	
$t_{sk(pp)}$(3)	Part-to-part skew time	ISO7420x				3.7	ns
		ISO7421x				4.9	
t_r	Output signal rise time		See Figure 16.		1.8		ns
t_f	Output signal fall time				1.7		ns
t_{fs}	Fail-safe output delay time from input power loss		See Figure 17.		6		µs

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.11 Switching Characteristics: V_{CC1} = 5 V ± 10%, V_{CC2} = 3.3 V ± 10%

T_A = –40°C to 125°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time		See Figure 16.		8	13.5	ns
PWD(1)	Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$	ISO7420x			0.3	3	ns
		ISO7421x			0.5	5.6	
$t_{sk(o)}$(2)	Channel-to-channel output skew time	ISO7420x				1.5	ns
		ISO7421x			0.5	3	
$t_{sk(pp)}$(3)	Part-to-part skew time	ISO7420x				5.4	ns
		ISO7421x				6.3	
t_r	Output signal rise time		See Figure 16.		2		ns
t_f	Output signal fall time				2		ns
t_{fs}	Fail-safe output delay time from input power loss		See Figure 17.		6		µs

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.12 Switching Characteristics: V_{CC1} = 3.3 V ± 10%, V_{CC2} = 5 V ± 10%

T_A = –40°C to 125°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	ISO7420x	See Figure 16.		7.5	12	ns
		ISO7421x			7.5	14	
PWD(1)	Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$	ISO7420x			0.7	3	ns
		ISO7421x			0.7	3.6	
$t_{sk(o)}$(2)	Channel-to-channel output skew time	ISO7420x			0.5	1.5	ns
		ISO7421x			0.5	3	
$t_{sk(pp)}$(3)	Part-to-part skew time	ISO7420x				4.6	ns
		ISO7421x				8.5	
t_r	Output signal rise time		See Figure 16.		1.7		ns
t_f	Output signal fall time				1.6		ns
t_{fs}	Fail-safe output delay time from input power loss		See Figure 17.		6		µs

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.13 Switching Characteristics: V_{CC1} and V_{CC2} = 3.3 V ± 10%

T_A = –40°C to 125°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time		See Figure 16		8.5	14	ns
PWD(1)	Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$	ISO7420x and ISO7421x			0.5	2	ns
$t_{sk(o)}$(2)	Channel-to-channel output skew time	ISO7420x			0.4	2	ns
		ISO7421x			0.4	3	
$t_{sk(pp)}$(3)	Part-to-part skew time	ISO7420x				6.2	ns
		ISO7421x				6.8	
t_r	Output signal rise time		See Figure 16		2		ns
t_f	Output signal fall time				1.8		ns
t_{fs}	Fail-safe output delay time from input power loss		See Figure 17		6		µs

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.14 Typical Characteristics

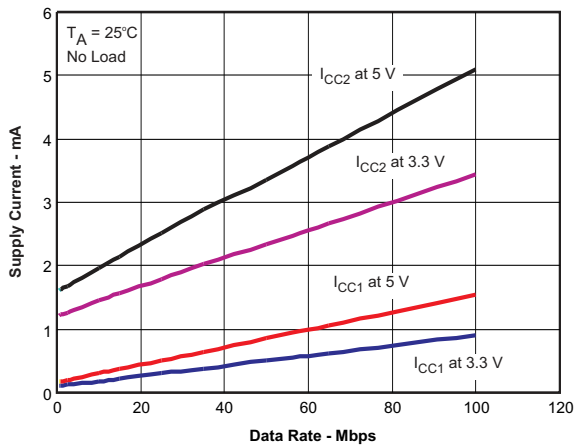


Figure 1. ISO7420 Supply Current Per Channel vs Data Rate (No Load)

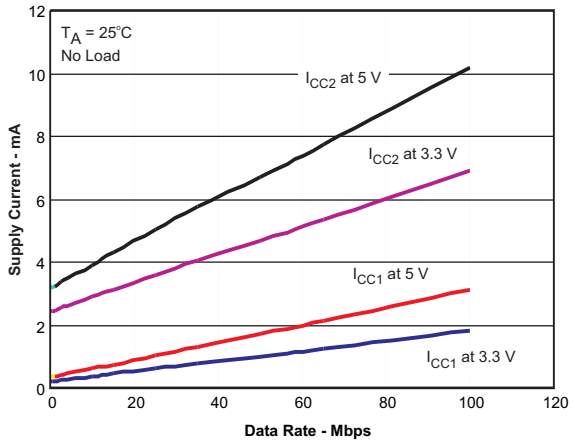


Figure 2. ISO7420 Supply Current Both Channels vs Data Rate (No Load)

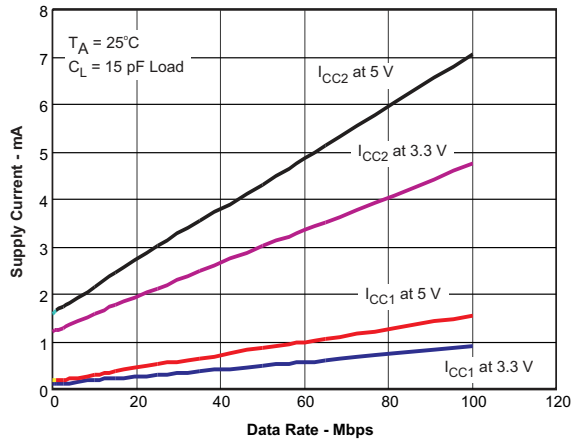


Figure 3. ISO7420 Supply Current Per Channel vs Data Rate (15 pF Load)

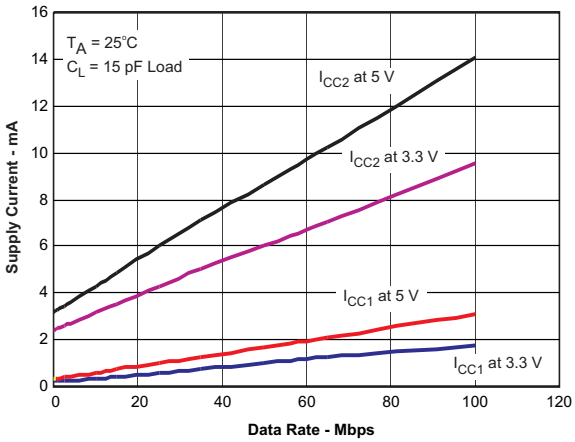


Figure 4. ISO7420 Supply Current Both Channels vs Data Rate (15 pF Load)

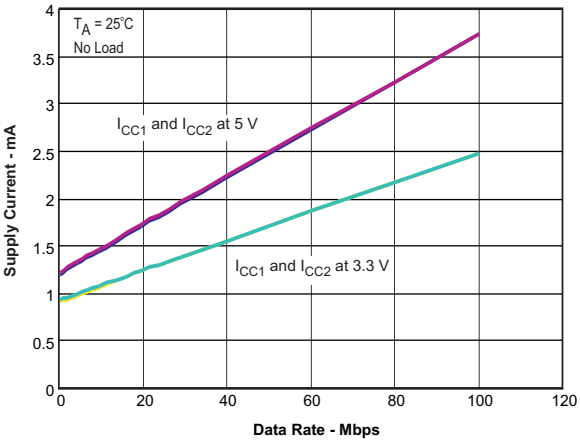


Figure 5. ISO7421 Supply Current Per Channel vs Data Rate (No Load)

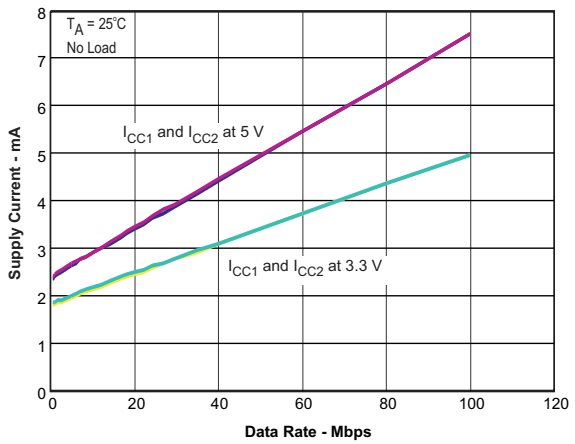


Figure 6. ISO7421 Supply Current Both Channels vs Data Rate (No Load)

Typical Characteristics (continued)

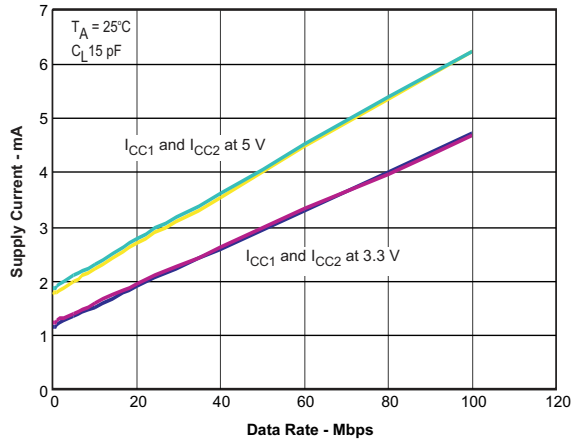


Figure 7. ISO7421 Supply Current Per Channel vs Data Rate (15 pF Load)

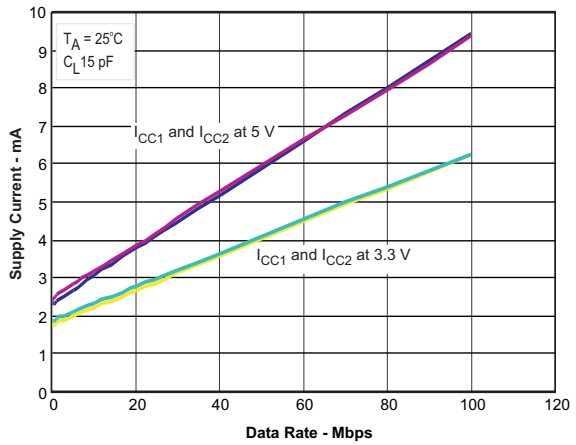


Figure 8. ISO7421 Supply Current Both Channels vs Data Rate (15 pF Load)

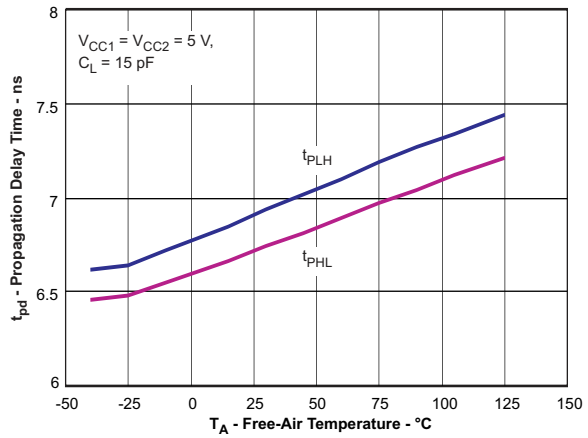


Figure 9. Propagation Delay Time vs Free-Air Temperature

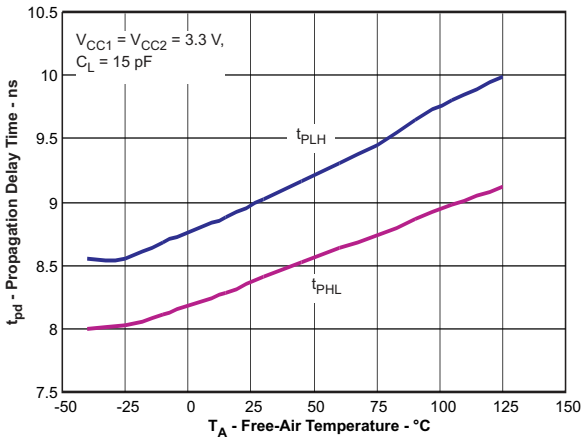


Figure 10. Propagation Delay Time vs Free-Air Temperature

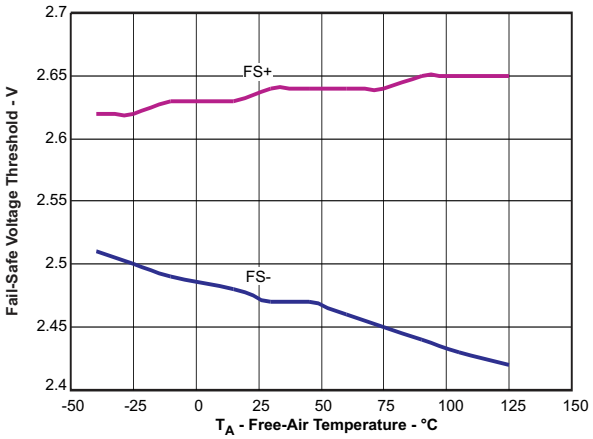


Figure 11. Input V_{CC} Fail-Safe Voltage Threshold vs Free-Air Temperature

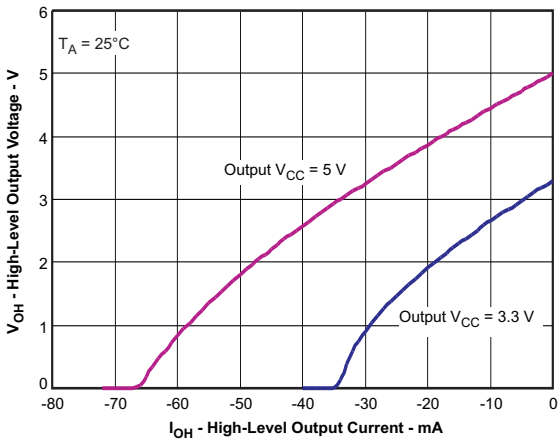


Figure 12. High-Level Output Voltage vs High-Level Output Current

Typical Characteristics (continued)

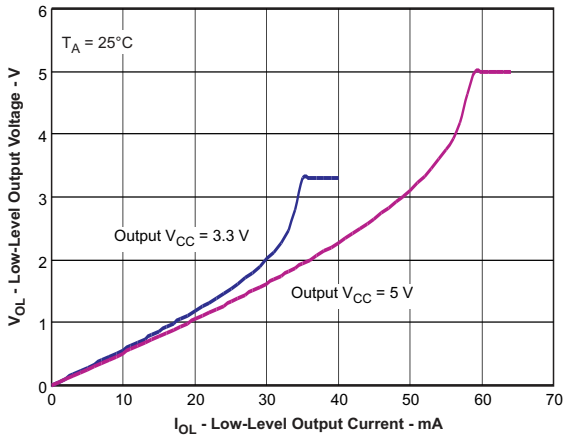


Figure 13. Low-Level Output Voltage vs Low-Level Output Current

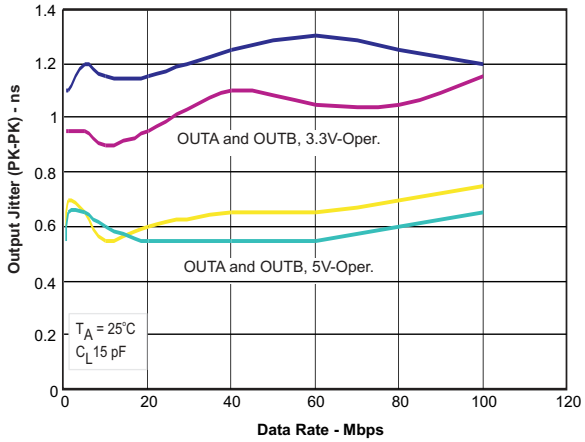


Figure 14. ISO7420FE Output Jitter vs Data Rate

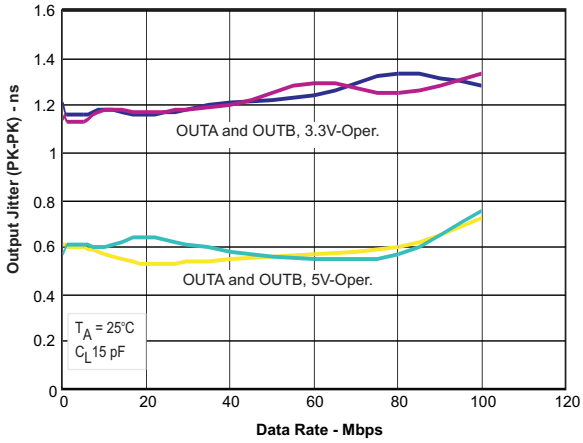
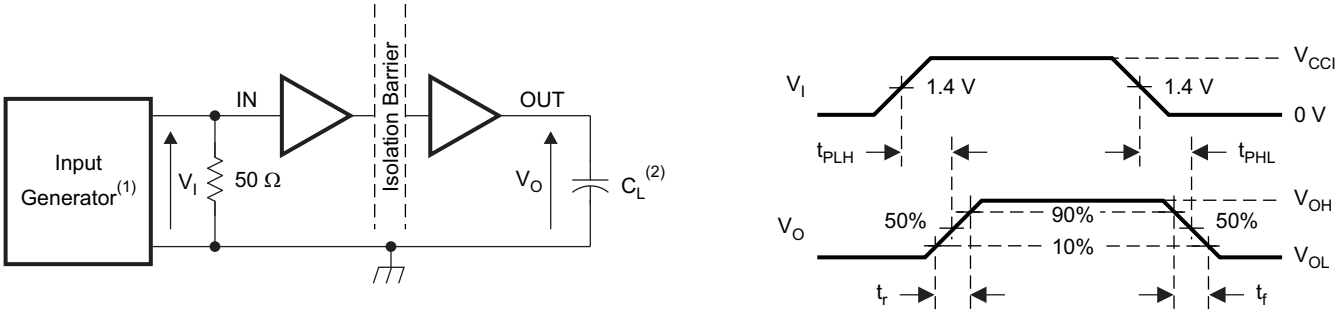


Figure 15. ISO7421FE Output Jitter vs Data Rate

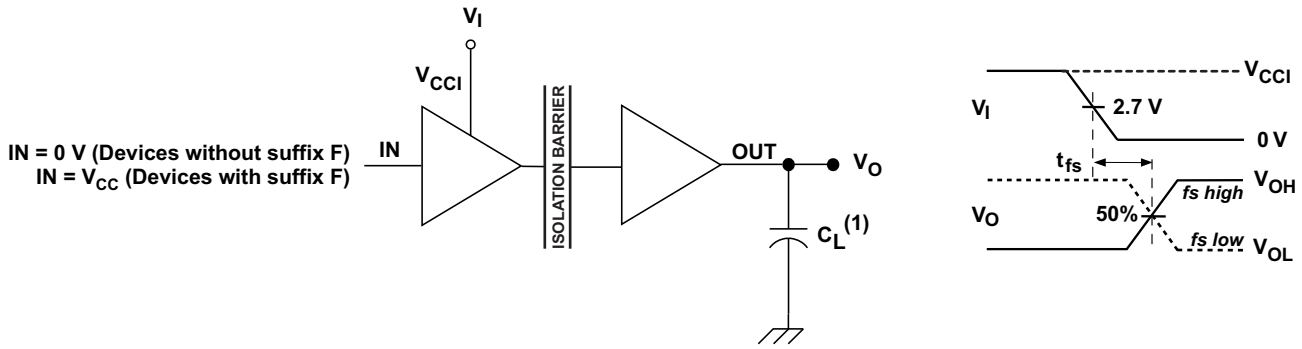
7 Parameter Measurement Information



(1) The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω. At the input, a 50-Ω resistor is required to terminate the Input Generator signal. It is not needed in an actual application.

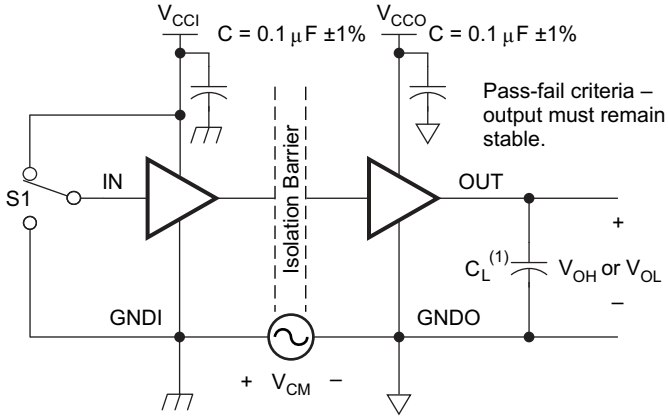
(2) C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 16. Switching Characteristic Test Circuit and Voltage Waveforms



(1) C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 17. Fail-Safe Output Delay-Time Test Circuit and Voltage Waveforms



(1) C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 18. Common-Mode Transient Immunity Test Circuit

8 Detailed Description

8.1 Overview

The isolator in Figure 19 is based on a capacitive isolation barrier technique. The I/O channel of the device consists of two internal data channels, a high-frequency channel (HF) with a bandwidth from 100 kbps up to 150 Mbps, and a low-frequency channel (LF) covering the range from 100 kbps down to DC. In principle, a single- ended input signal entering the HF-channel is split into a differential signal via the inverter gate at the input. The following capacitor-resistor networks differentiate the signal into transients, which then are converted into differential pulses by two comparators. The comparator outputs drive a NOR-gate flip-flop whose output feeds an output multiplexer. A decision logic (DCL) at the driving output of the flip-flop measures the durations between signal transients. If the duration between two consecutive transients exceeds a certain time limit, (as in the case of a low-frequency signal), the DCL forces the output-multiplexer to switch from the high- to the low-frequency channel.

Because low-frequency input signals require the internal capacitors to assume prohibitively large values, these signals are pulse-width modulated (PWM) with the carrier frequency of an internal oscillator, thus creating a sufficiently high frequency signal, capable of passing the capacitive barrier. As the input is modulated, a low-pass filter (LPF) is needed to remove the high-frequency carrier from the actual data before passing it on to the output multiplexer.

8.2 Functional Block Diagram

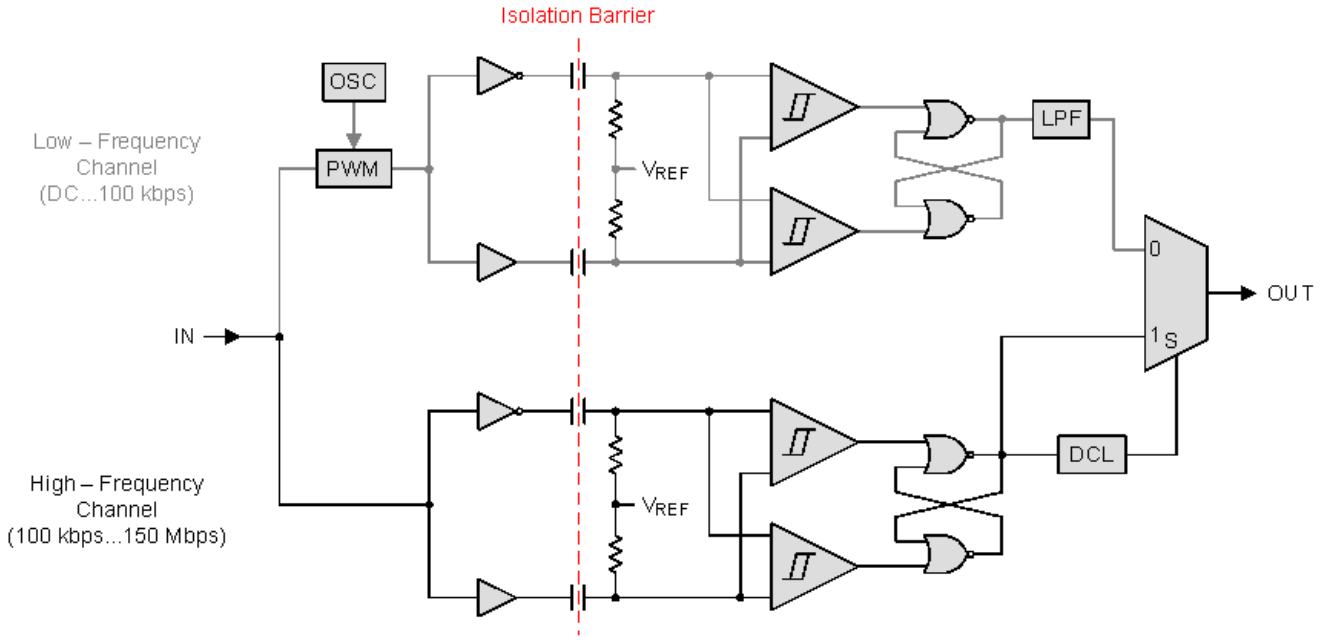


Figure 19. Conceptual Block Diagram of a Digital Capacitive Isolator

8.3 Feature Description

ISO742x are available in multiple channel configurations and default output state options to enable wide variety of application uses.

PRODUCT	DATA RATE	DEFAULT OUTPUT	RATED T_A	CHANNEL DIRECTION
ISO7420E	50 Mbps	High	–40°C to 125°C	Same
ISO7420FE		Low		
ISO7421E		High		Opposite
ISO7421FE		Low		

8.3.1 Insulation and Safety-Related Specifications for D-8 Package

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (clearance)	Shortest terminal-to-terminal distance through air	4			mm
L(I02)	Minimum external tracking (creepage)	Shortest terminal-to-terminal distance across the package surface	4			mm
CTI	Tracking resistance (comparative tracking index)	DIN EN 60112 (VDE 0303-11); IEC 60112	>400			V
	Minimum internal gap (internal clearance)	Distance through the insulation	0.014			mm
R_{IO}	Isolation resistance, input to output(1)	V_{IO} = 500 V, T_A = 25°C		$>10^{12}$		Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ max		$>10^{11}$		Ω
C_{IO}	Barrier capacitance, input to output(1)	V_{IO} = 0.4 sin (2πft), f = 1 MHz		1		pF
C_I	Input capacitance(2)	$V_I = V_{CC}/2$ + 0.4 sin (2πft), f = 1 MHz, V_{CC} = 5 V		1		pF

(1) All pins on each side of the barrier tied together creating a two-terminal device.
(2) Measured from input pin to ground.

NOTE

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

8.3.2 Insulation Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER(1)		TEST CONDITIONS	SPECIFICATION	UNIT
DIN V VDE V 0884-10 (VDE V 0884-10):2006-12				
V_{IORM}	Maximum workingisolation voltage		566	V_{PEAK}
V_{PR}	Input-to-output test voltage	Method a, After environmental tests subgroup 1, V_{PR} = V_{IORM} x 1.6, t = 10 s, Partial Discharge < 5 pC	906	V_{PEAK}
		Method b1, V_{PR} = V_{IORM} x 1.875, t = 1 s (100% Production test) Partial discharge < 5 pC	1062	
		After Input/Output safety test subgroup 2/3, V_{PR} = V_{IORM} x 1.2, t = 10 s, Partial discharge < 5 pC	680	
V_{IOTM}	Maximum transient isolation voltage	V_{TEST} = V_{IOTM} = 4242 V_{PK} t = 60 sec (qualification) t= 1 sec (100% production)	4242	V_{PEAK}
R_S	Isolation resistance	V_{IO} = 500 V at T_S = 150°C	>10^9	Ω
	Pollution degree		2	
UL 1577				
V_{ISO}	Maximum withstand isolation voltage	V_{TEST} = V_{ISO} = 2500 V_{RMS}, t = 60 sec (qualification); V_{TEST} = 1.2 x V_{ISO} = 3000 V_{RMS}, t = 1 sec (100% production)	2500	V_{RMS}

(1) Climatic Classification 40/125/21

Table 1. IEC 60664-1 Ratings Table

PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic isolation group	Material group	II
Installation classification	Rated mains voltage ≤ 150 V_{RMS}	I–IV
	Rated mains voltage ≤ 300 V_{RMS}	I–III

8.3.3 Regulatory Information

VDE	CSA	UL	CQC
Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 and DIN EN 61010-1 (VDE 0411-1):2011-07	Approved under CSA Component Acceptance Notice 5A, IEC 60950-1, and IEC 61010-1	Recognized under UL 1577 Component Recognition Program	Certified according to GB 4943.1-2011
Basic Insulation; Maximum Transient Isolation Voltage, 4242 V_{PK}; Maximum Working Isolation Voltage, 566 V_{PK}	2500 V_{RMS} Isolation Rating; Basic insulation per CSA 60950-1-07+A1 and IEC 60950-1 2nd Ed+A1, 384 V_{RMS} maximum working voltage; CSA 61010-1-04 and IEC 61010-1 2nd Ed, 300 V_{RMS} maximum working voltage for basic insulation and 150 V_{RMS} for reinforced insulation	Single Protection Isolation Voltage, 2500 V_{RMS} (1)	Basic Insulation, Altitude ≤ 5000 m, Tropical Climate, 250 V_{RMS} maximum working voltage
Certificate number: 40016131	Master contract number: 220991	File number: E181974	Certificate number: CQC14001109540

(1) Production tested ≥ 3000 V_{RMS} for 1 second in accordance with UL 1577.

8.3.4 Life Expectancy vs Working Voltage

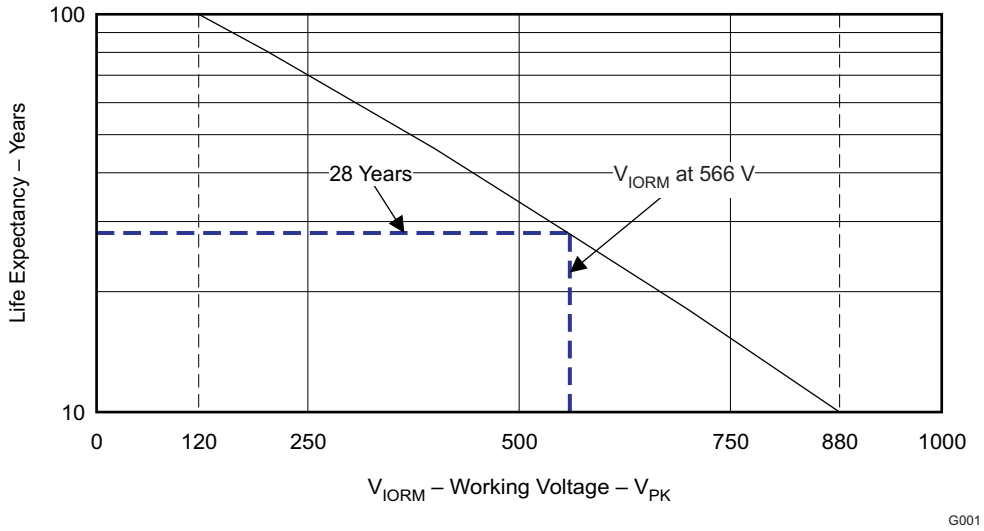


Figure 20. Life Expectancy vs Working Voltage

8.3.5 Safety Limiting Values

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	θ_{JA} = 212°C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C			107	mA
		θ_{JA} = 212°C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C			164	
T_S	Maximum safety temperature				150	°C

The safety-limiting constraint is the absolute-maximum junction temperature specified in the *Absolute Maximum Ratings*(1) table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Information* table is that of a device installed in the JESD51-3, Low-Effective-Thermal-Conductivity Test Board for Leaded Surface-Mount Packages and is conservative. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

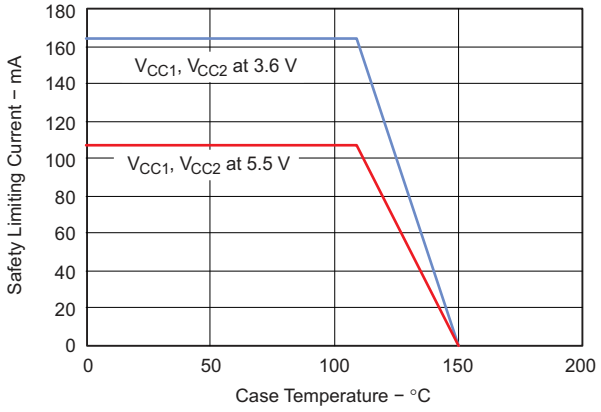


Figure 21. θ_{JC} Thermal Derating Curve per VDE

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

8.4 Device Functional Modes

Table 2. Functional Table(1)

V_{CCI}	V_{CCO}	INPUT INA, INB	OUTPUT OUTA, OUTB	
			ISO7420E / ISO7421E	ISO7420FE / ISO7421FE
PU	PU	H	H	H
		L	L	L
		Open	H(2)	L(3)
PD	PU	X	H(2)	L(3)
X	PD	X	Undetermined	Undetermined

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}; PU = Powered up (V_{CC} ≥ 3 V); PD = Powered down (V_{CC} ≤ 2.1 V); X = Irrelevant; H = High level; L = Low level;
(2) In fail-safe condition, output defaults to high level
(3) In fail-safe condition, output defaults to low level

8.4.1 Device I/O Schematic

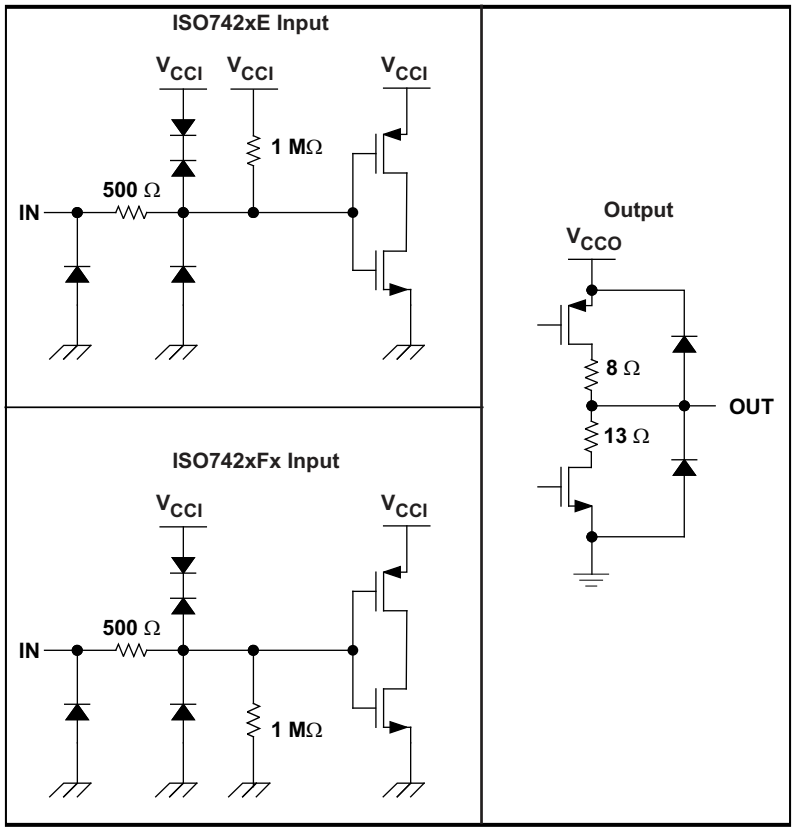


Figure 22. Device I/O Schematics

9 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

ISO742x utilize single-ended TTL-logic switching technology. Its supply voltage range is from 3 V to 5.5 V for both supplies, V_{CC1} and V_{CC2}. When designing with digital isolators, it is important to keep in mind that due to the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (i.e. µC or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

9.2 Typical Application

ISO7421 can be used with Texas Instruments' mixed signal micro-controller, digital-to-analog converter, transformer driver, and voltage regulator to create an isolated 4-20 mA current loop.

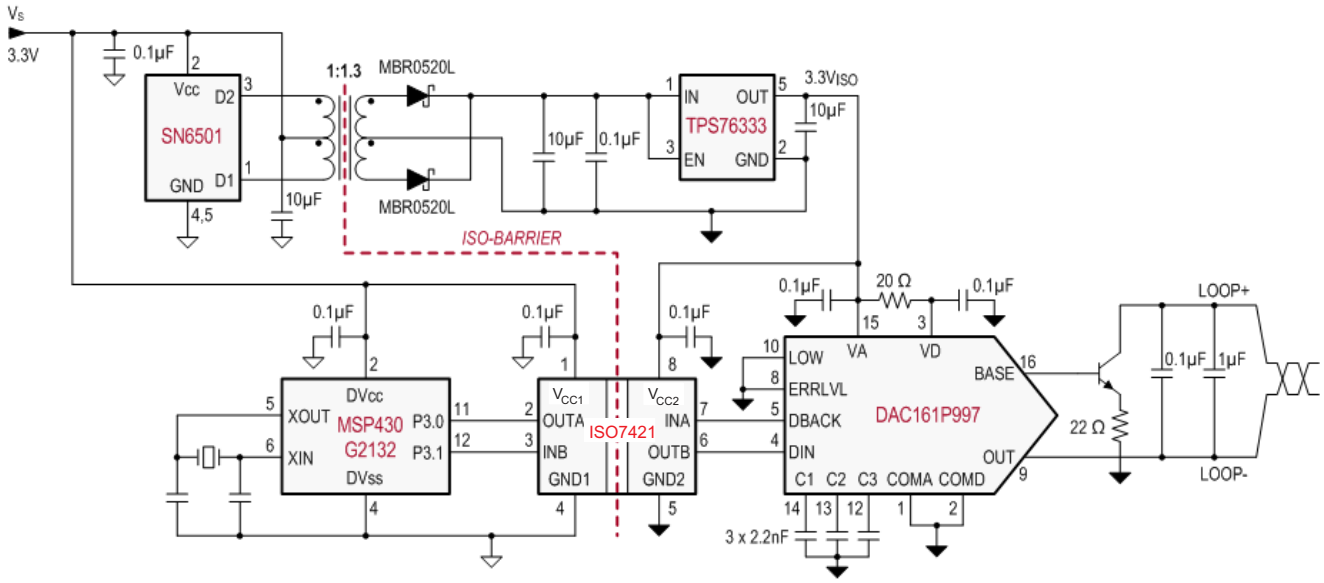


Figure 23. Isolated 4-20 mA Current Loop

Typical Application (continued)

9.2.1 Design Requirements

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the ISO742x only require two external bypass capacitors to operate.

9.2.2 Detailed Design Procedure

9.2.2.1 Maximum Supply Current Equations

(Calculated over recommended operating temperature range and Silicon process variation)

9.2.2.1.1 ISO7420

At $V_{CC1} = V_{CC2} = 3.3V \pm 10\%$

$$I_{CC1}(max) = I_{CC1\_Q}(max) + 1.791 \times 10^{-2} \times f \quad (1)$$

$$I_{CC2}(max) = I_{CC2\_Q}(max) + 1.687 \times 10^{-2} \times f + 3.570 \times 10^{-3} \times f \times C_L \quad (2)$$

At $V_{CC1} = V_{CC2} = 5V \pm 10\%$

$$I_{CC1}(max) = I_{CC1\_Q}(max) + 3.152 \times 10^{-2} \times f \quad (3)$$

$$I_{CC2}(max) = I_{CC2\_Q}(max) + 2.709 \times 10^{-2} \times f + 5.365 \times 10^{-3} \times f \times C_L \quad (4)$$

9.2.2.1.2 ISO7421

At $V_{CC1} = V_{CC2} = 3.3V \pm 10\%$

$$I_{CC1}(max) = I_{CC1\_Q}(max) + 1.726 \times 10^{-2} \times f + 1.785 \times 10^{-3} \times f \times C_L \quad (5)$$

$$I_{CC2}(max) = I_{CC2\_Q}(max) + 1.726 \times 10^{-2} \times f + 1.785 \times 10^{-3} \times f \times C_L \quad (6)$$

At $V_{CC1} = V_{CC2} = 5V \pm 10\%$

$$I_{CC1}(max) = I_{CC1\_Q}(max) + 2.920 \times 10^{-2} \times f + 2.682 \times 10^{-3} \times f \times C_L \quad (7)$$

$$I_{CC2}(max) = I_{CC2\_Q}(max) + 2.920 \times 10^{-2} \times f + 2.682 \times 10^{-3} \times f \times C_L \quad (8)$$

I_{CC1_Q} (max) and I_{CC2_Q} (max) are equivalent to the maximum supply currents measured in mA under DC input conditions (provided in the specification tables of this data sheet); f is data rate in Mbps of both channels; C_L is the capacitive load in pF of both channels. I_{CC1}(max) and I_{CC2}(max) are measured in mA.

9.2.2.2 Typical Supply Current Equations:

(Calculated over recommended operating temperature range and Silicon process variation)

9.2.2.2.1 ISO7420

At $V_{CC1} = V_{CC2} = 3.3V$

$$I_{CC1}(typ) = I_{CC1\_Q}(typ) + 1.528 \times 10^{-2} \times f \quad (9)$$

$$I_{CC2}(typ) = I_{CC2\_Q}(typ) + 1.637 \times 10^{-2} \times f + 3.275 \times 10^{-3} \times f \times C_L \quad (10)$$

At $V_{CC1} = V_{CC2} = 5V$

$$I_{CC1}(typ) = I_{CC1\_Q}(typ) + 2.640 \times 10^{-2} \times f \quad (11)$$

$$I_{CC2}(typ) = I_{CC2\_Q}(typ) + 2.502 \times 10^{-2} \times f + 4.919 \times 10^{-3} \times f \times C_L \quad (12)$$

9.2.2.2.2 ISO7421

At $V_{CC1} = V_{CC2} = 3.3V$

$$I_{CC1}(typ) = I_{CC1\_Q}(typ) + 1.567 \times 10^{-2} \times f + 1.640 \times 10^{-3} \times f \times C_L \quad (13)$$

$$I_{CC2}(typ) = I_{CC2\_Q}(typ) + 1.567 \times 10^{-2} \times f + 1.640 \times 10^{-3} \times f \times C_L \quad (14)$$

At $V_{CC1} = V_{CC2} = 5V$

$$I_{CC1}(typ) = I_{CC1\_Q}(typ) + 2.550 \times 10^{-2} \times f + 2.416 \times 10^{-3} \times f \times C_L \quad (15)$$

$$I_{CC2}(typ) = I_{CC2\_Q}(typ) + 2.550 \times 10^{-2} \times f + 2.461 \times 10^{-3} \times f \times C_L \quad (16)$$

Typical Application (continued)

I_{CC1_Q} (typ) and I_{CC2_Q} (typ) are equivalent to the typical supply currents measured in mA under DC input conditions (provided in the specification tables of this data sheet); f is data rate in Mbps of each channel; C_L is the capacitive load in pF of each channel. I_{CC1}(typ) and I_{CC2}(typ) are measured in mA.

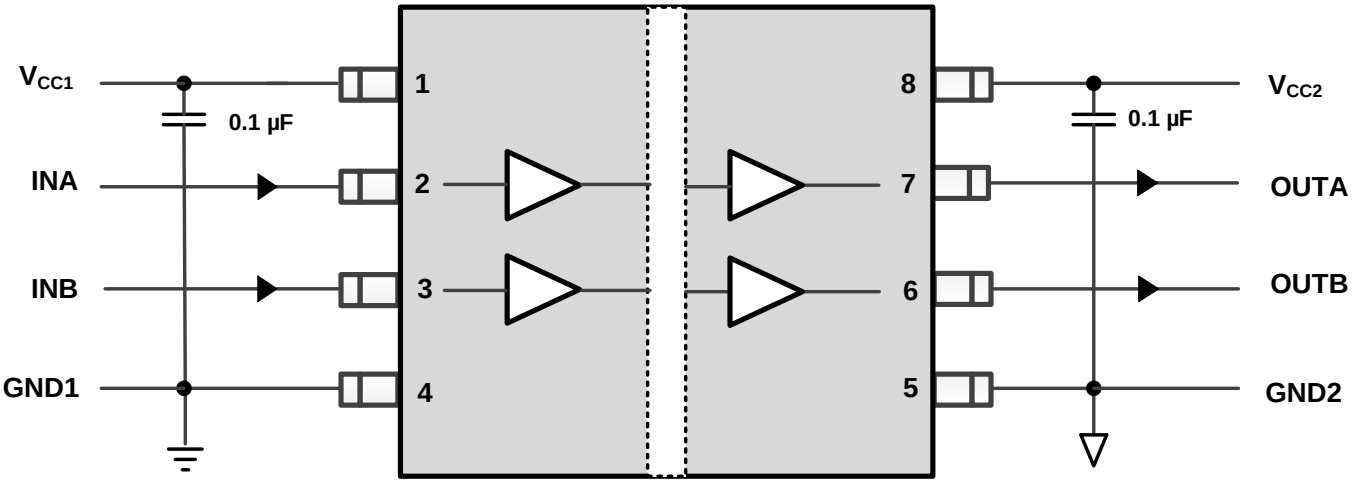


Figure 24. Typical ISO7420 Circuit Hookup

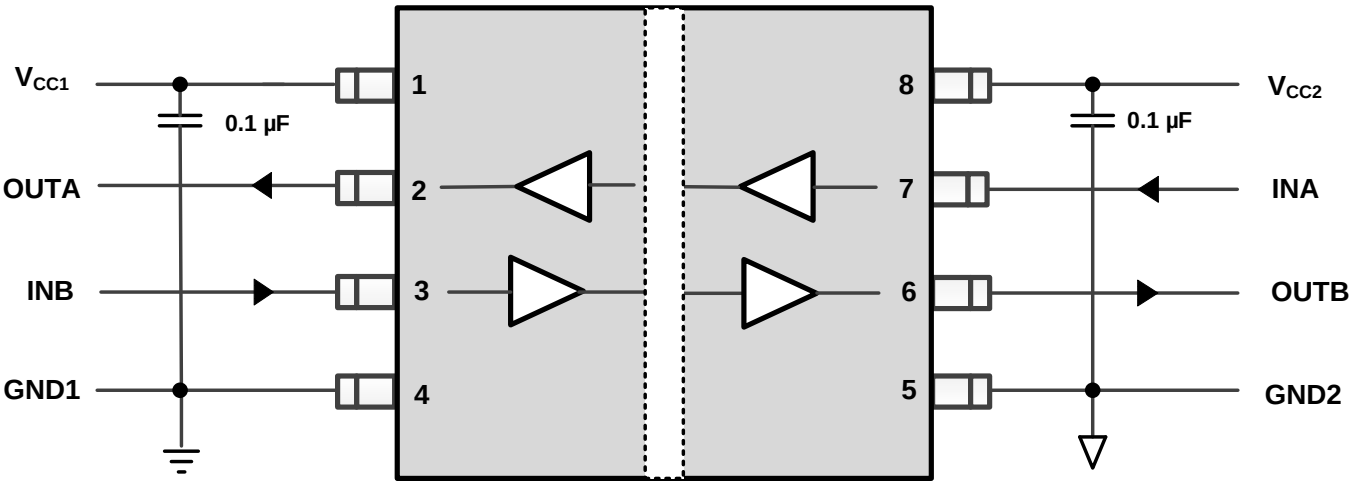


Figure 25. Typical ISO7421 Circuit Hookup

Typical Application (continued)

9.2.3 Application Curves

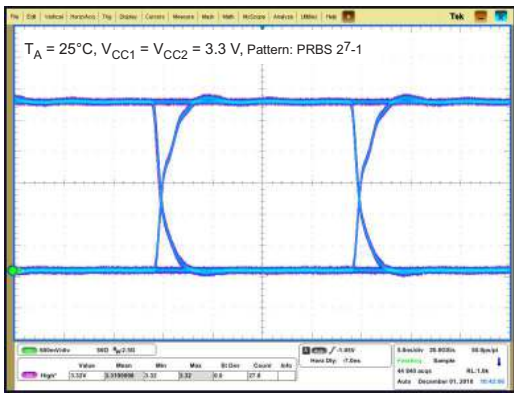


Figure 26. ISO7420FE Typical Eye Diagram at 50 MBPS, 3.3 V Operation

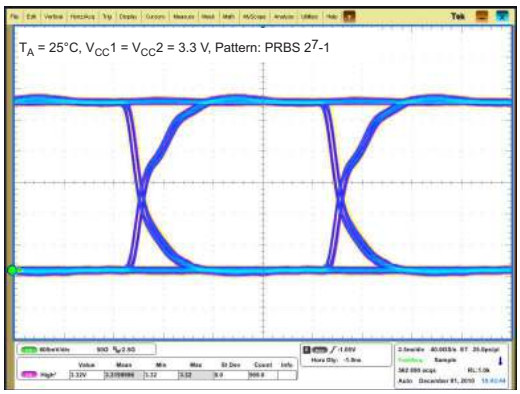


Figure 27. ISO7420FE Typical Eye Diagram at 100 MBPS, 3.3 V Operation

10 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, a 0.1 µF bypass capacitor is recommended at input and output supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments' SN6501. For such applications, detailed power supply design and transformer selection recommendations are available in SN6501 datasheet (SLLSEA0).

11 Layout

11.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 28). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power / ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, see Application Note *Digital Isolator Design Guide*, SLLA284.

11.1.1 PCB Material

For digital circuit boards operating below 150 Mbps, (or rise and fall times higher than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 epoxy-glass as PCB material. FR-4 (Flame Retardant 4) meets the requirements of Underwriters Laboratories UL94-V0, and is preferred over cheaper alternatives due to its lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and its self-extinguishing flammability-characteristics.

11.2 Layout Example

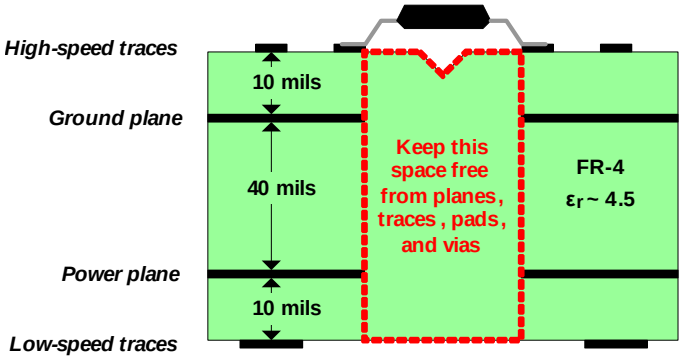


Figure 28. Recommended Layer Stack

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- *SN6501 Transformer Driver for Isolated Power Supplies*, SLLSEA0
- *Isolation Glossary*, SLLS353

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 3. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
ISO7420E	Click here	Click here	Click here	Click here	Click here
ISO7420FE	Click here	Click here	Click here	Click here	Click here
ISO7421E	Click here	Click here	Click here	Click here	Click here
ISO7421FE	Click here	Click here	Click here	Click here	Click here

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

DeviceNet, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO7420ED	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SO7420	Samples
ISO7420EDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SO7420	Samples
ISO7420FED	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7420F	Samples
ISO7420FEDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7420F	Samples
ISO7421ED	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SO7421	Samples
ISO7421EDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SO7421	Samples
ISO7421FED	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7421F	Samples
ISO7421FEDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7421F	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

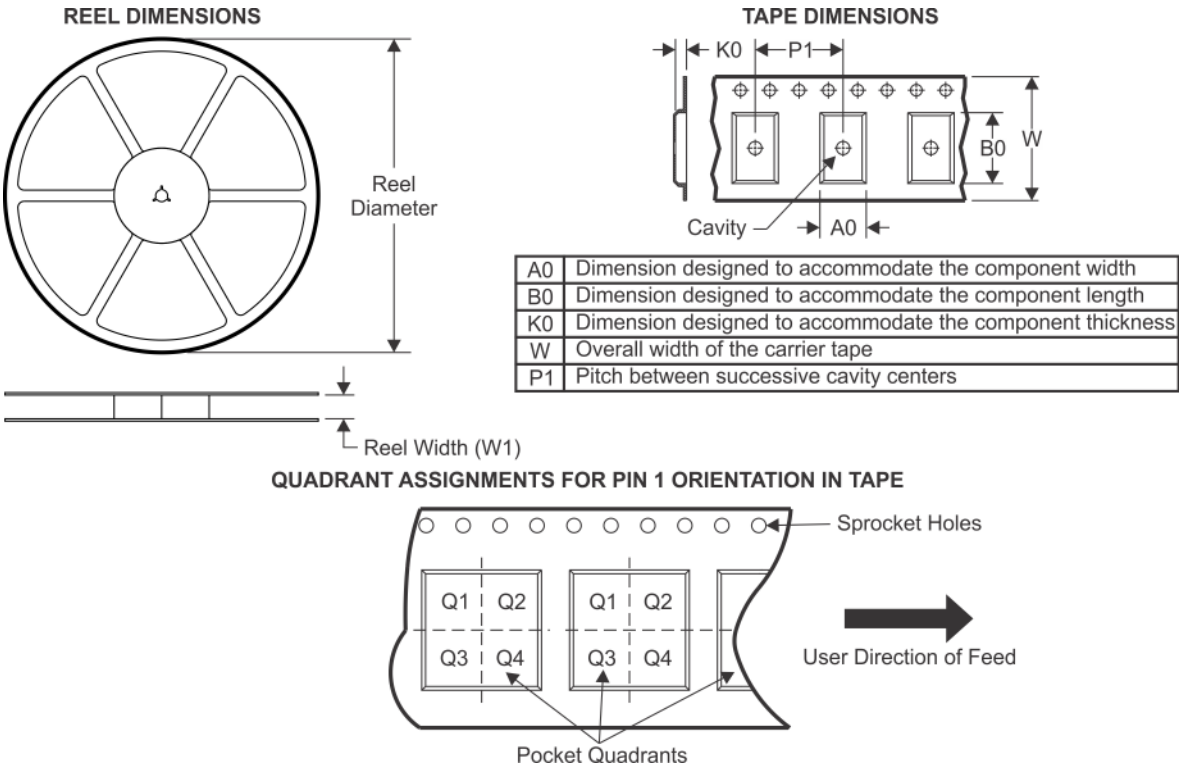
OTHER QUALIFIED VERSIONS OF ISO7421E :

- Automotive: ISO7421E-Q1

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

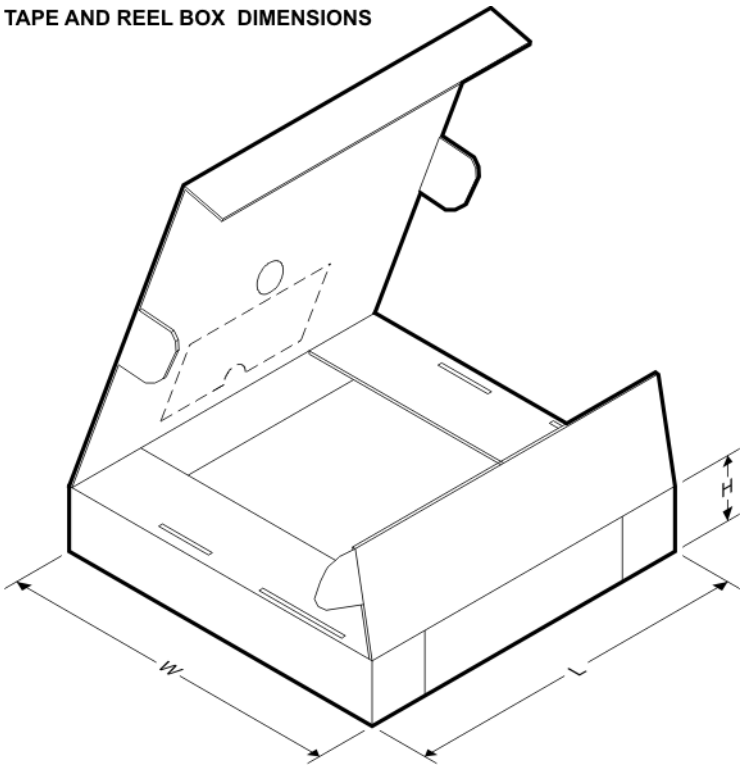


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7420EDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7420FEDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7421EDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7421FEDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

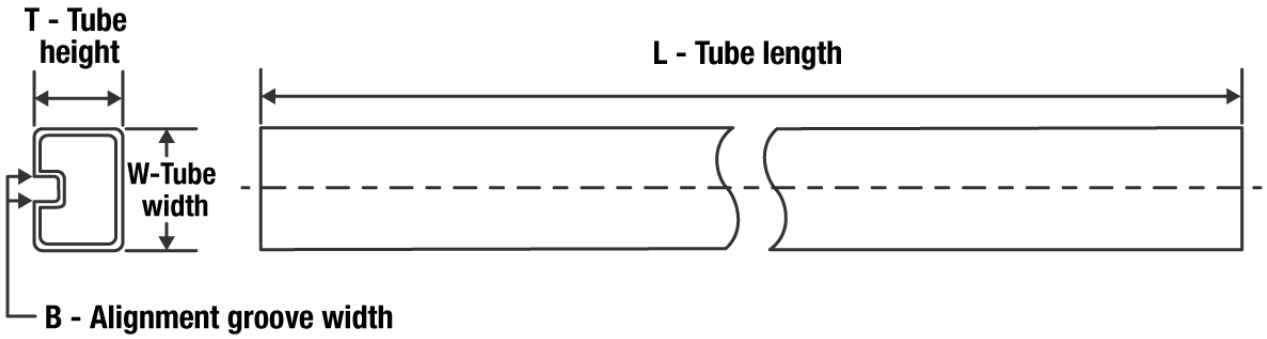
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

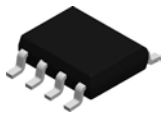
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7420EDR	SOIC	D	8	2500	350.0	350.0	43.0
ISO7420FEDR	SOIC	D	8	2500	350.0	350.0	43.0
ISO7421EDR	SOIC	D	8	2500	350.0	350.0	43.0
ISO7421FEDR	SOIC	D	8	2500	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ISO7420ED	D	SOIC	8	75	505.46	6.76	3810	4
ISO7420FED	D	SOIC	8	75	505.46	6.76	3810	4
ISO7421ED	D	SOIC	8	75	505.46	6.76	3810	4
ISO7421FED	D	SOIC	8	75	505.46	6.76	3810	4

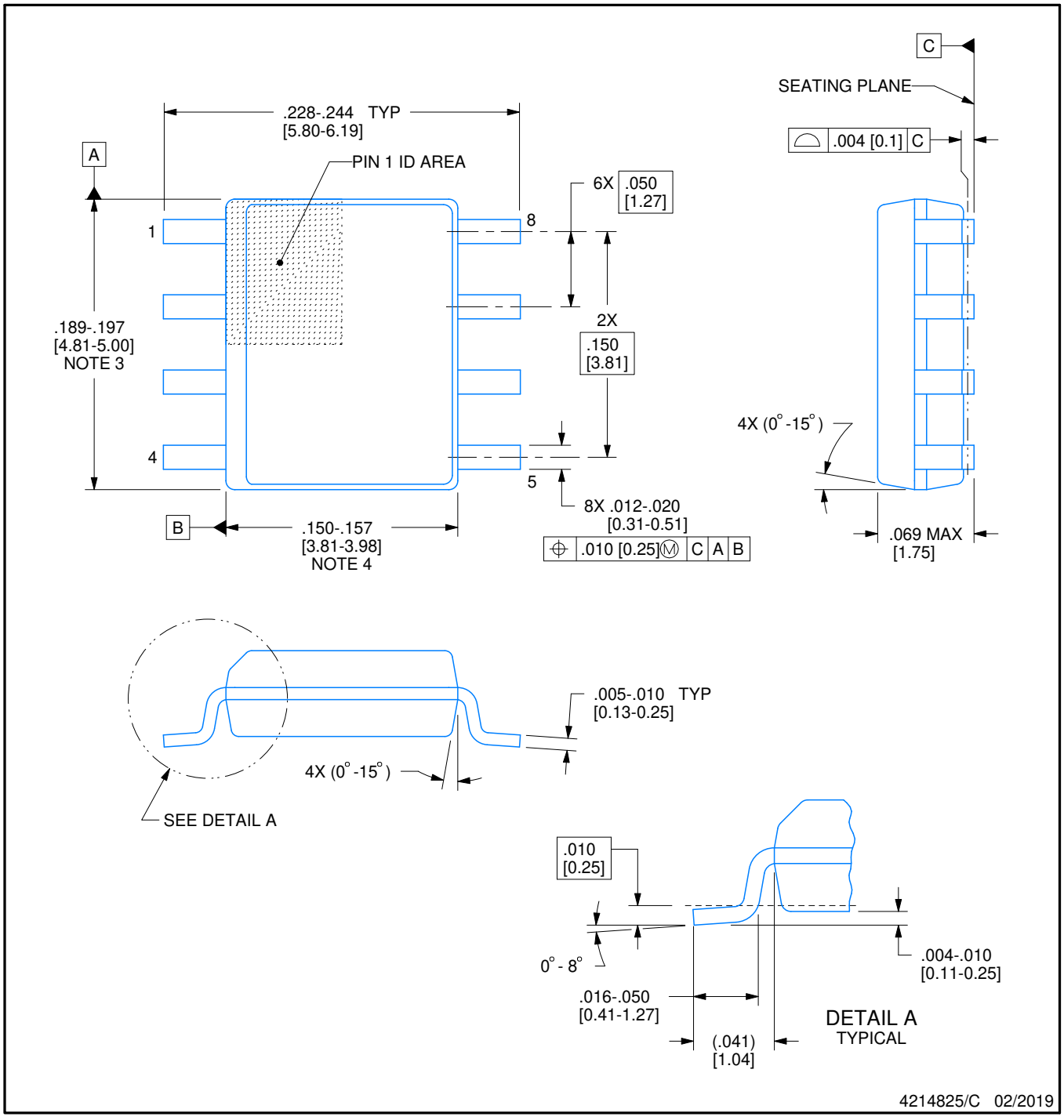


PACKAGE OUTLINE

D0008A

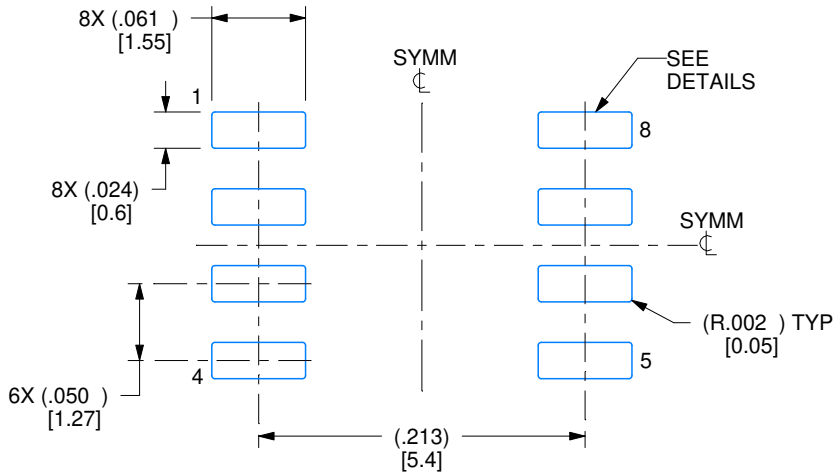
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

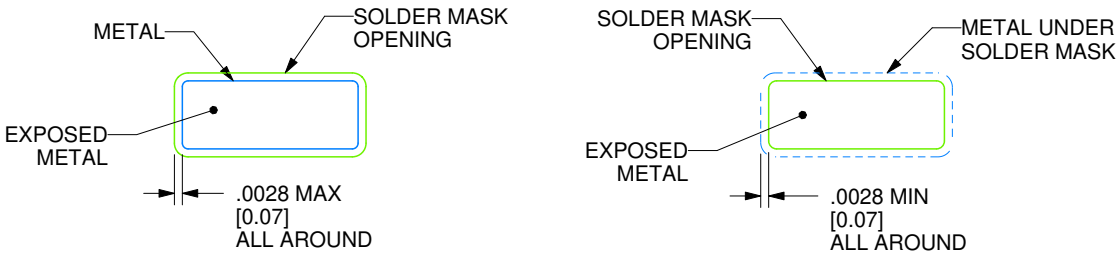


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

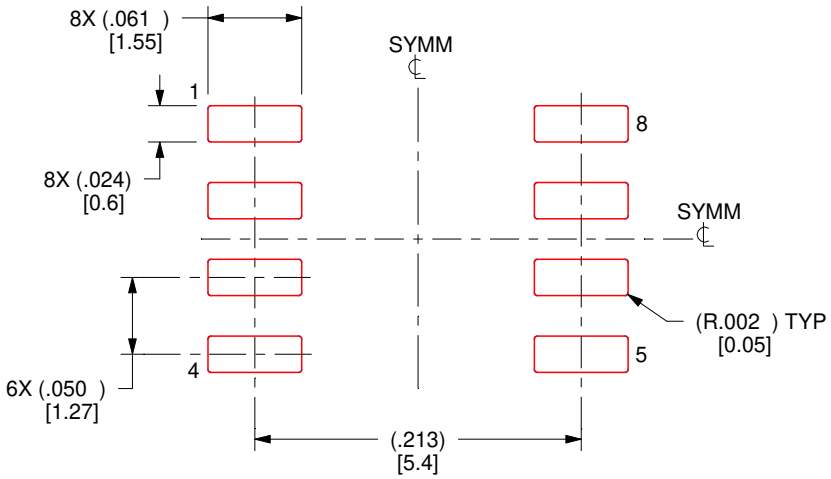
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265