

## DESCRIPTION

The MP7748S is a Class D Audio Amplifier for driving stereo speakers in single-ended configuration or a mono speaker in bridge-tied-load configuration. It is fully integrated audio amplifier which dramatically reduces solution size by integrating the following:

- 200mΩ power MOSFETs
- Startup / Shutdown pop elimination
- Short circuit protection circuits

The MP7748S is capable of delivering 30W per channel into 4Ω speaker in single-ended output structure, or delivering 60W into 8Ω speaker in bridge-tied-load output structure. MPS Class D Audio Amplifiers exhibit the high fidelity of a Class A/B amplifier at high efficiencies. The circuit is based on the MPS' proprietary variable frequency topology that delivers excellent linearity, fast response time and operates on a single power supply.

MP7748S features programmable VDD shutdown voltage for each channel by controlling the UVP node voltage. The default VDD shutdown (rising threshold) voltage is 8.4V if the UVP pin is NC.

The MP7748S is available in TSSOP28-Exposed Package.

## FEATURES

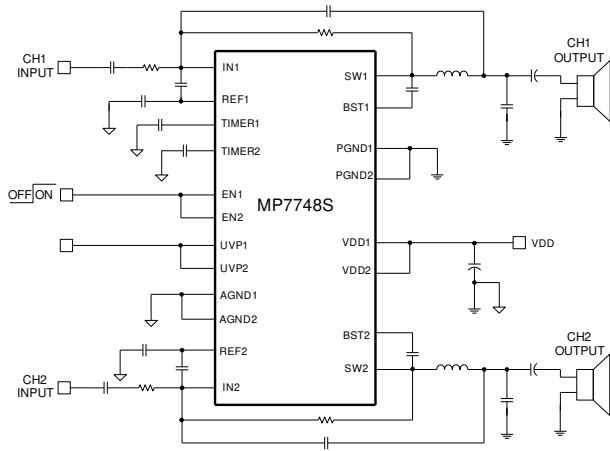
- 9.5V to 36V Operation from a Single Supply
- ±5.5A Peak Current Output
- Output Power at 30V and 10%THD:
  - Stereo Single Ended: 2 x 30W into 4Ω Load,
  - Bridge Tied Load: 60W into 8Ω Load
- THD+N = 0.02% at 1W, 8Ω
- > 90% Efficiency at 10%THD
- Low Noise (160μV with SE configuration, 145μV with BTL configuration)
- Switching Frequency Up to 1MHz
- Integrated Startup and Shutdown Pop Elimination Circuit
- Programmable UVP
- Thermal and Short Circuit Protection
- Integrated Power FETs
- Available in TSSOP28-Exposed Package

## APPLICATIONS

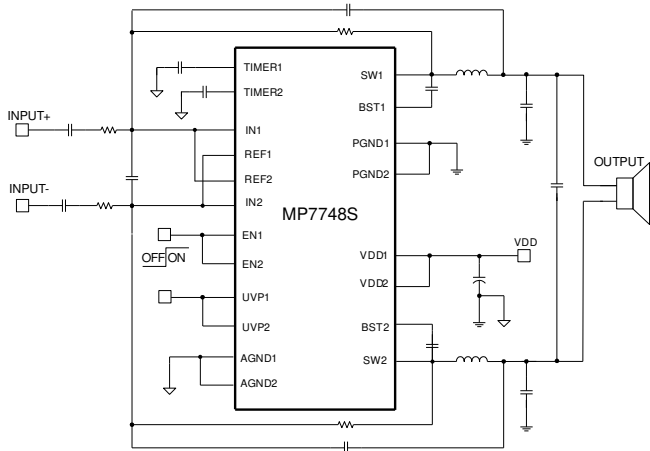
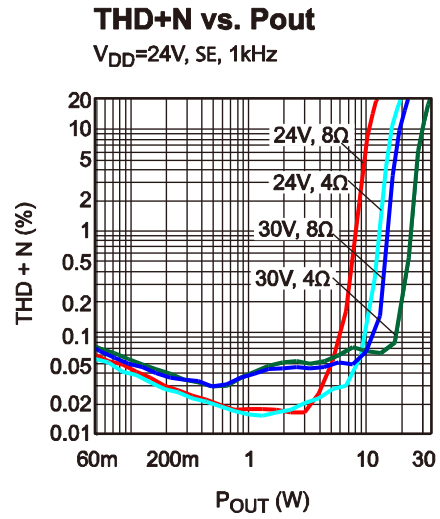
- Portable Docking Stations
- Surround Sound DVD Systems
- Televisions
- Flat Panel Monitors
- Multimedia Computers
- Home Stereo Systems

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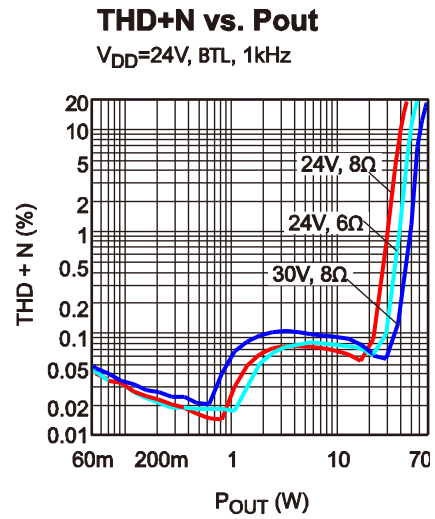
**TYPICAL APPLICATION**



**Stereo SE Application Circuit**



**Mono BTL Application Circuit**

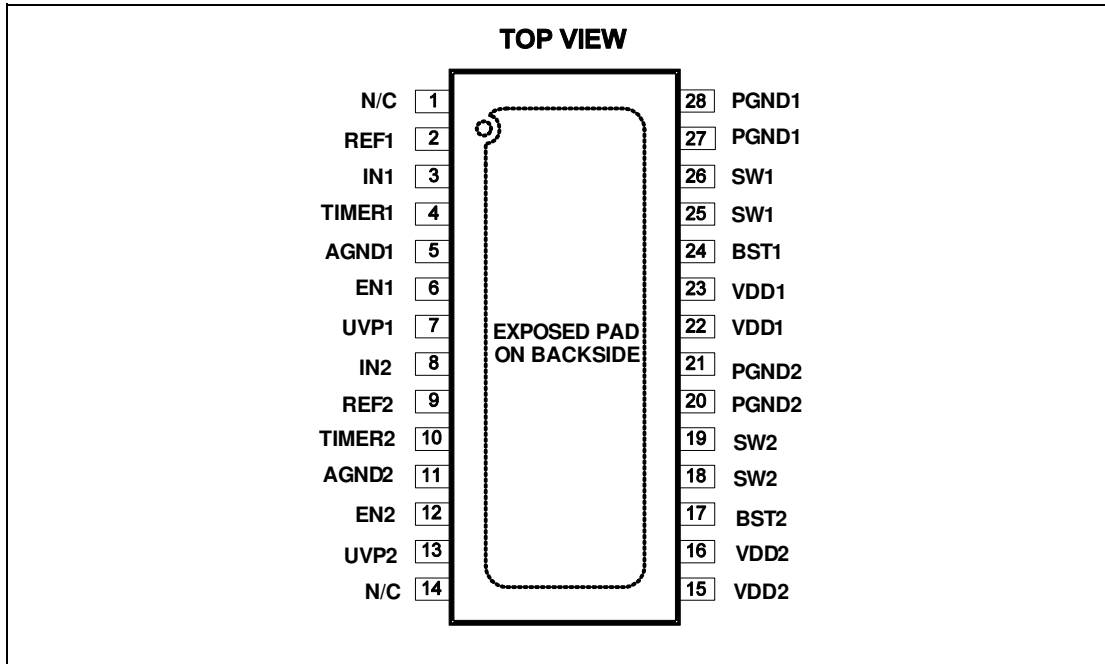


### ORDERING INFORMATION

| Part Number* | Package    | Top Marking |
|--------------|------------|-------------|
| MP7748SGF    | TSSOP28-EP | MP7748S     |

\* For Tape & Reel, add suffix -Z (e.g. MP7748SGF-Z).

### PACKAGE REFERENCE



#### ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>

|   |                                    |
|---|------------------------------------|
| Supply Voltage $V_{DD}$ .....                                       | 40V                                |
| BS Voltage.....   | $V_{SW} - 0.3V$ to $V_{SW} + 6.5V$ |
| $V_{UVP}$ , $V_{TIMER}$ , $V_{EN}$ .....                            | -0.3V to +6V                       |
| $V_{SW}$ .....  | -0.3V to $V_{DD} + 1V$             |
| $V_{REF}$ , $V_{IN}$ .....  | -0.3V to +34V                      |
| AGND to PGND.....   | -0.3V to +0.3V                     |
| Continuous Power Dissipation ( $T_A = +25^\circ C$ ) <sup>(2)</sup> | 3.9W                               |
| Junction Temperature.....   | 150°C                              |
| Lead Temperature.....   | 260°C                              |
| Storage Temperature.....  | -65°C to +150°C                    |

#### Recommended Operating Conditions <sup>(3)</sup>

|                                      |                 |
|--------------------------------------|-----------------|
| Supply Voltage $V_{DD}$ .....        | 9.5V to 36V     |
| Operating Junct. Temp ( $T_J$ )..... | -40°C to +125°C |

| Thermal Resistance <sup>(4)</sup> | $\theta_{JA}$ | $\theta_{JC}$ |
|-----------------------------------|---------------|---------------|
| TSSOP28-EP.....                   | 32.....       | 6..... °C/W   |

#### Notes:

- Exceeding these ratings may damage the device.
- The maximum allowable power dissipation is a function of the maximum junction temperature  $T_J$  (MAX), the junction-to-ambient thermal resistance  $\theta_{JA}$ , and the ambient temperature  $T_A$ . The maximum allowable continuous power dissipation at any ambient temperature is calculated by  $P_D$  (MAX) =  $(T_J$  (MAX) -  $T_A$ ) /  $\theta_{JA}$ . Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- The device is not guaranteed to function outside of its operating conditions.
- Measured on JESD51-7, 4-layer PCB.

**ELECTRICAL CHARACTERISTICS** (5, 6)

$V_{DD} = 24V$ ,  $V_{EN} = 5V$ ,  $T_A = +25^{\circ}C$ , unless otherwise noted.

| Parameters   | Symbol    | Condition                    | Min | Typ | Max | Units       |
|--|-----------|------------------------------|-----|-----|-----|-------------|
| Standby Current                                    |           | $V_{EN} = 0V, NIN=PIN=Float$ |     | 100 | 130 | $\mu A$     |
| Quiescent Current                                  | $I_Q$     | SW=Low                       |     | 3.1 | 3.5 | mA          |
| SW On Resistance                                   |           | Sourcing and Sinking         |     | 0.2 |     | $\Omega$    |
| Short Circuit Current                              |           | Sourcing and Sinking         | 4.5 | 5.5 | 6.5 | A           |
| EN Enable Threshold Voltage                        |           | $V_{EN}$ Rising              |     | 1.4 | 2.0 | V           |
|  |           | $V_{EN}$ Falling             | 0.4 | 1.0 |     | V           |
| EN Enable Input Current                            |           | $V_{EN} = 5V$                |     | 5   |     | $\mu A$     |
| External Undervoltage Detection                    | $V_{UVP}$ |                              | 2   | 2.2 | 2.4 | V           |
| External Undervoltage Detection Hysteresis Voltage | $V_{Hys}$ |                              |     | 0.3 |     | V           |
| Thermal Shutdown Trip Point                        |           | $T_J$ Rising                 |     | 150 |     | $^{\circ}C$ |
| Thermal Shutdown Hysteresis                        |           |                              |     | 30  |     | $^{\circ}C$ |

**Note:**

- 5) The device is not guaranteed to function outside its operating rating.
- 6) Electrical Characteristics are for the IC only with no external components except bypass capacitors.

## OPERATING SPECIFICATIONS <sup>(7)</sup>

Circuit of figure 5, single-ended output configuration,  $V_{DD} = 30V$ ,  $\text{Gain}=8.25V/V$ ,  $V_{EN} = 5V$ ,  $T_A = +25^\circ\text{C}$ , unless otherwise noted.

| Parameters              | Symbol | Condition   | Min                | Typ  | Max | Units         |             |
|-------------------------|--------|---|--------------------|------|-----|---------------|-------------|
| Standby Current         |        | $V_{EN} = 0V$   |                    | 100  |     | $\mu\text{A}$ |             |
| Quiescent Current       |        | Switching, no load  |                    | 22   |     | $\text{mA}$   |             |
| Power Output            |        | $f = 1\text{kHz}$ , THD+N = 10%, 4 $\Omega$ Load  |                    | 30   |     | W             |             |
|                         |        | $f = 1\text{kHz}$ , THD+N = 10%, 8 $\Omega$ Load  |                    | 17   |     | W             |             |
| THD+ Noise              |        | $P_{OUT} = 1W$ , $f = 1\text{kHz}$ , 4 $\Omega$ Load                                      |                    | 0.04 |     | %             |             |
|                         |        | $P_{OUT} = 1W$ , $f = 1\text{kHz}$ , 8 $\Omega$ Load                                      |                    | 0.02 |     | %             |             |
| Efficiency              |        | $f = 1\text{kHz}$ , $P_{OUT} = 30W$ , 4 $\Omega$ Load                                     |                    | 90   |     | %             |             |
|                         |        | $f = 1\text{kHz}$ , $P_{OUT} = 17W$ , 8 $\Omega$ Load                                     |                    | 94   |     | %             |             |
| Maximum Power Bandwidth |        |   |                    | 20   |     | $\text{kHz}$  |             |
| Dynamic Range           |        |   |                    | 96   |     | $\text{dB}$   |             |
| Noise Floor             |        | A-Weighted  |                    | 160  |     | $\mu\text{V}$ |             |
| Power Supply Rejection  |        | $V_{CC}=24V$ ,<br>Gain=8.25V/V,<br>$V_{RIPPLE}=200\text{mV}_{PP}$<br>$C_R=100\mu\text{F}$ | $f = 1\text{kHz}$  |      | -59 |               | $\text{dB}$ |
|                         |        |   | $f = 217\text{Hz}$ |      | -59 |               | $\text{dB}$ |

Circuit of figure 6, bridge-tied-load output configuration,  $V_{DD} = 30V$ ,  $\text{Gain}=15V/V$ ,  $V_{EN} = 5V$ ,  $T_A = +25^\circ\text{C}$ , unless otherwise noted.

| Parameters              | Symbol | Condition   | Min                | Typ  | Max | Units         |             |
|-------------------------|--------|---|--------------------|------|-----|---------------|-------------|
| Standby Current         |        | $V_{EN} = 0V$   |                    | 100  |     | $\mu\text{A}$ |             |
| Quiescent Current       |        | Switching, no load  |                    | 26   |     | $\text{mA}$   |             |
| Power Output            |        | $f = 1\text{kHz}$ , THD+N = 10%, 8 $\Omega$ Load                |                    | 60   |     | W             |             |
| THD+ Noise              |        | $P_{OUT} = 1W$ , $f = 1\text{kHz}$ , 8 $\Omega$ Load            |                    | 0.02 |     | %             |             |
| Efficiency              |        | $f = 1\text{kHz}$ , $P_{OUT} = 60W$ , 8 $\Omega$ Load           |                    | 94   |     | %             |             |
| Maximum Power Bandwidth |        |   |                    | 20   |     | $\text{kHz}$  |             |
| Dynamic Range           |        |   |                    | 103  |     | $\text{dB}$   |             |
| Noise Floor             |        | A-Weighted  |                    | 145  |     | $\mu\text{V}$ |             |
| Power Supply Rejection  |        | $V_{CC}=24V$ ,<br>Gain=15V/V,<br>$V_{RIPPLE}=200\text{mV}_{PP}$ | $f = 1\text{kHz}$  |      | -60 |               | $\text{dB}$ |
|                         |        |   | $f = 217\text{Hz}$ |      | -60 |               | $\text{dB}$ |

**Note:**

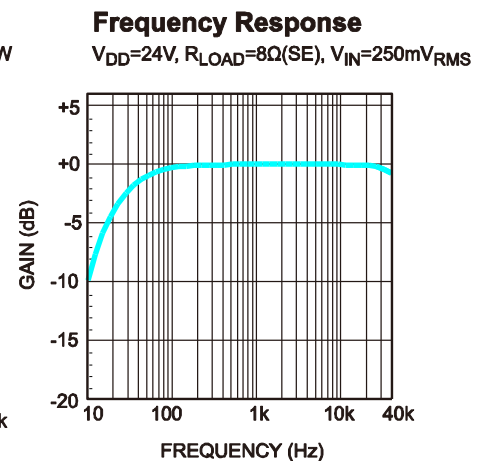
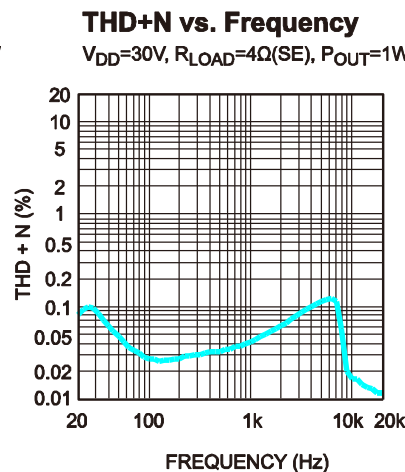
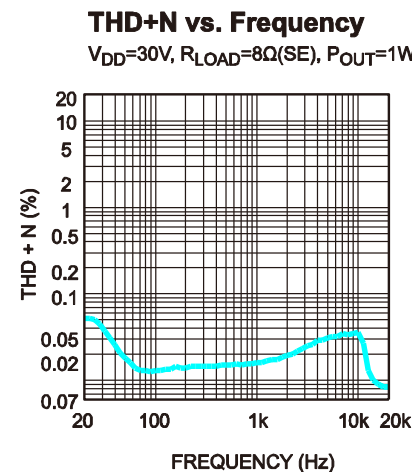
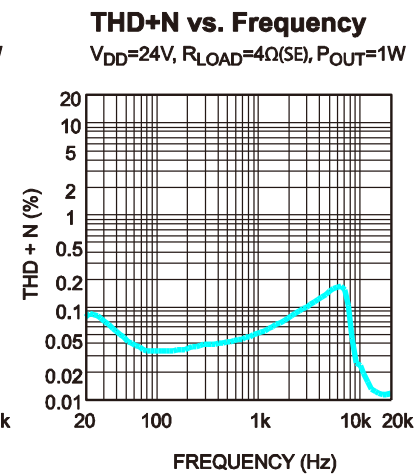
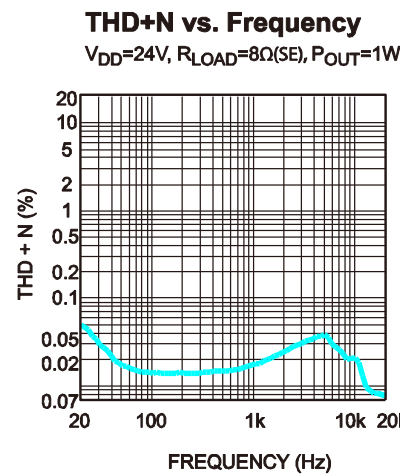
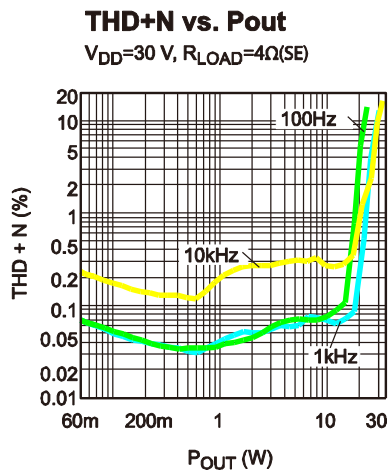
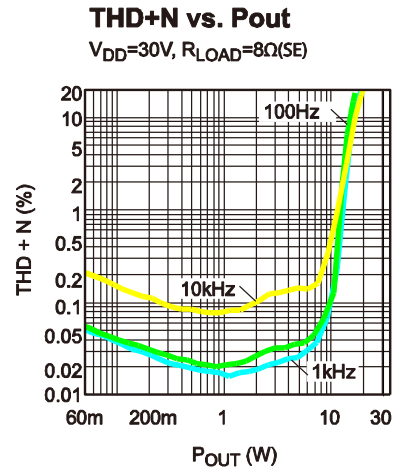
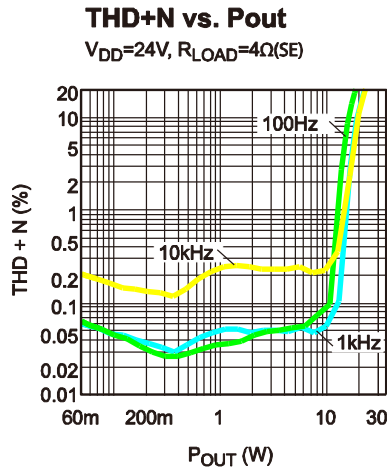
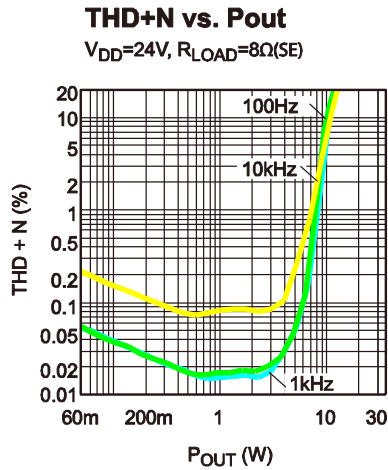
7) Operating Specifications are for the IC in Typical Application circuit.

## PIN FUNCTIONS

| Pin #  | Name        | Description  |
|--------|-------------|--|
| 1, 14  | N/C         | Not connected internally   |
| 2      | REF1        | Internal analog reference (VDD/2) for Amplifier 1. For SE configuration, connect a bypass capacitor from REF1 to AGND (10 $\mu$ F).  |
| 3      | IN1         | Inverting input for amplifier 1.   |
| 4      | TIMER1      | Internal timer input for Amplifier 1. Connect a capacitor from TIMER1 to AGND (2.2 $\mu$ F) to set the internal timer for startup pop elimination.                         |
| 5      | AGND1       | Analog ground for Amplifier 1. Connect AGND1 to AGND2. Connect PGND to AGND at a single point.   |
| 6      | EN1         | Enable input for Amplifier 1. Drive EN1 high to turn on the Amplifier 1, low to turn it off.   |
| 7      | UVP1        | Under-voltage protection reference input for Amplifier 1. Connect UVP1 to UVP2.  |
| 8      | IN2         | Inverting input for amplifier 2.   |
| 9      | REF2        | Internal analog reference (VDD/2) for Amplifier 2. For SE configuration, connect a bypass capacitor from REF2 to AGND (10 $\mu$ F).  |
| 10     | TIMER2      | Internal timer input for Amplifier 2. Connect a capacitor from TIMER2 to AGND (2.2 $\mu$ F) to set the internal timer for startup pop elimination.                         |
| 11     | AGND2       | Analog ground for Amplifier 2. Connect AGND2 to AGND1. Connect PGND to AGND at a single point.   |
| 12     | EN2         | Enable input for Amplifier 2. Drive EN2 high to turn on the Amplifier 2, low to turn it off.   |
| 13     | UVP2        | Under-voltage protection reference input for Amplifier 2. Connect UVP2 to UVP1.  |
| 15, 16 | VDD2        | Power supply input for Amplifier 2. Bypass VDD2 to PGND2 with a 1 $\mu$ F X7R capacitor (in addition to the main bulk capacitor), placed close to the VDD2 and PGND2 pins. |
| 17     | BST2        | High-side MOSFET bootstrap input for Amplifier 2. A capacitor from BST2 to SW2 supplies the gate drive current to the internal high-side MOSFET.                           |
| 18, 19 | SW2         | Switched power output for Amplifier 2.   |
| 20, 21 | PGND2       | Power ground for Amplifier 2. Connect PGND2 to PGND1. Connect PGND to AGND at a single point.  |
| 22, 23 | VDD1        | Power supply input for Amplifier 1. Bypass VDD1 to PGND1 with a 1 $\mu$ F X7R capacitor (in addition to the main bulk capacitor), placed close to the VDD1 and PGND1 pins. |
| 24     | BST1        | High-side MOSFET bootstrap input for Amplifier 1. A capacitor from BST1 to SW1 supplies the gate drive current to the internal high-side MOSFET.                           |
| 25, 26 | SW1         | Switched power output for Amplifier 1.   |
| 27, 28 | PGND1       | Power ground for Amplifier 1. Connect PGND1 to PGND2. Connect PGND to AGND at a single point.  |
|        | Exposed Pad | Connect exposed pad to GND plane for proper thermal performance.   |

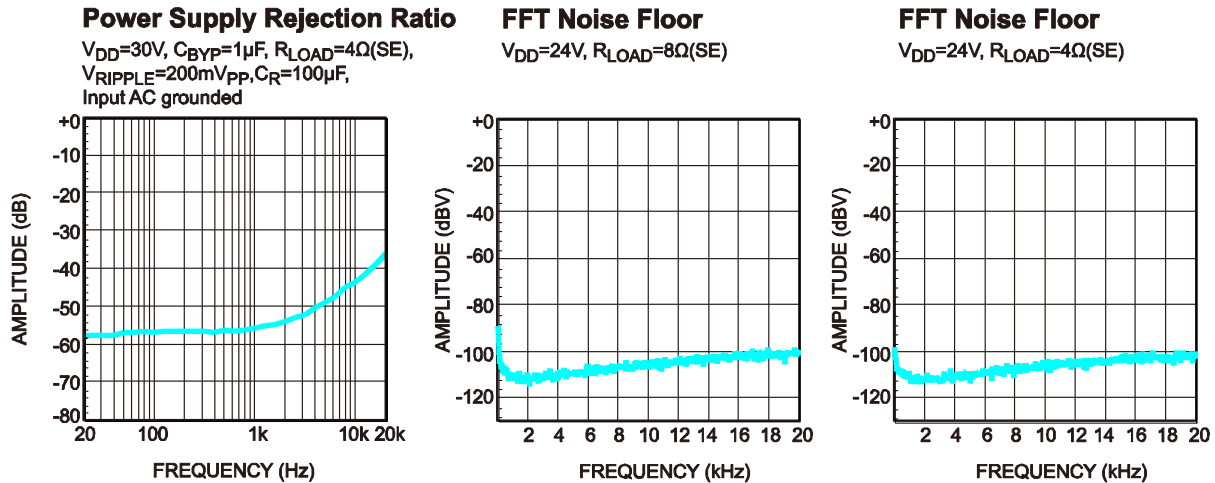
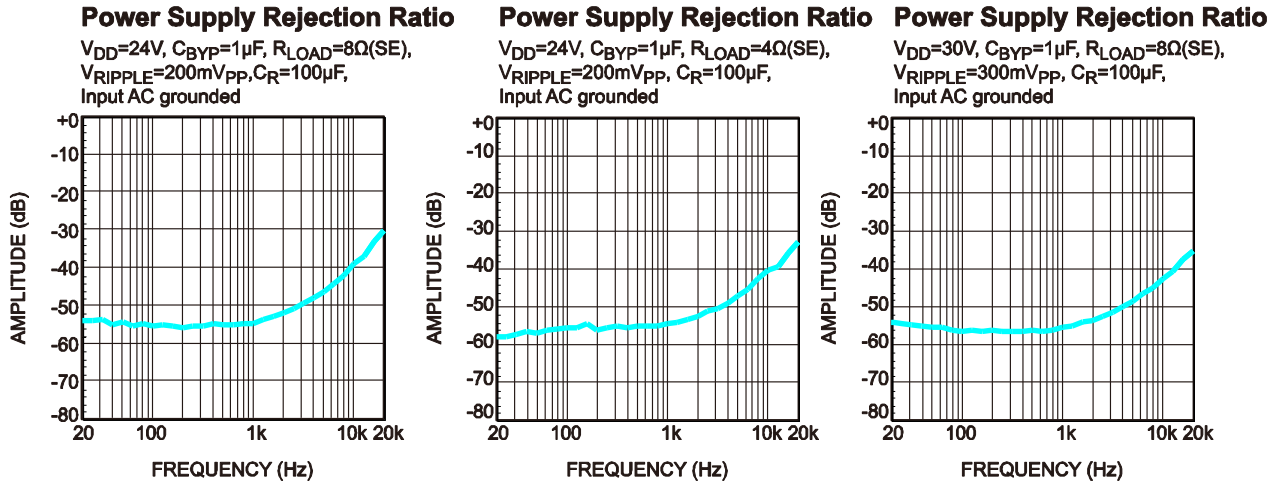
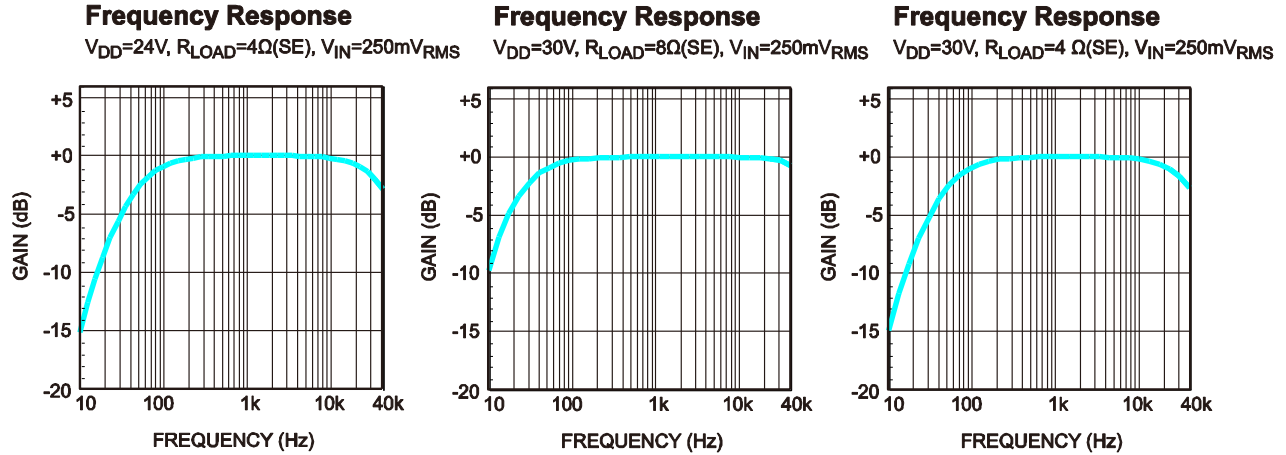
**TYPICAL PERFORMANCE CURVES**

Circuit of Figure 5, single-ended output configuration,  $V_{DD}=24V$ ,  $V_{EN}=5V$ ,  $A_V=8.2V/V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.



**TYPICAL PERFORMANCE CURVES (continued)**

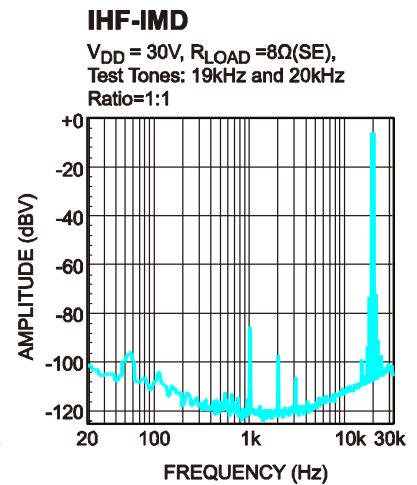
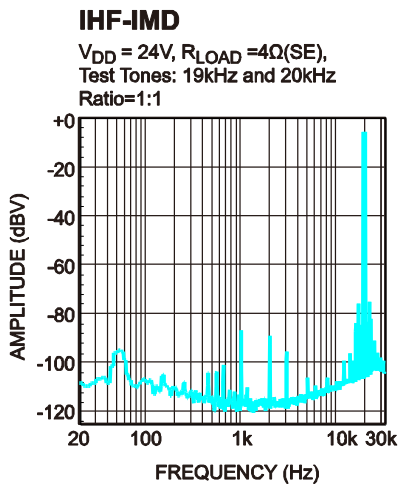
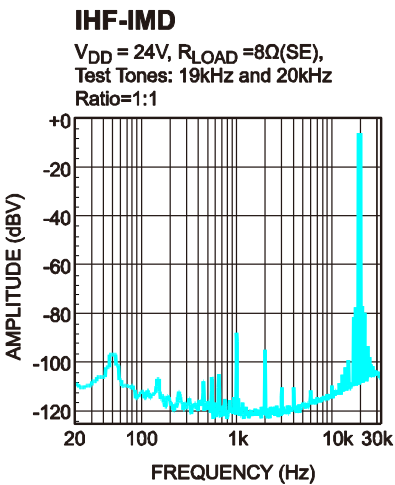
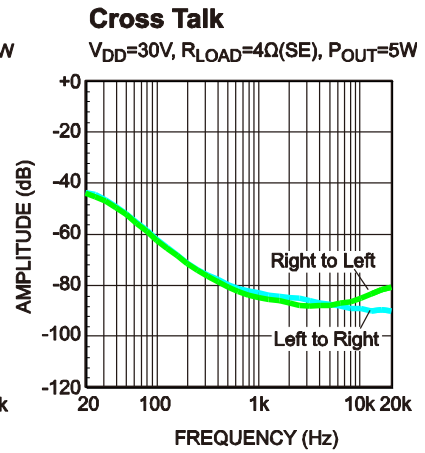
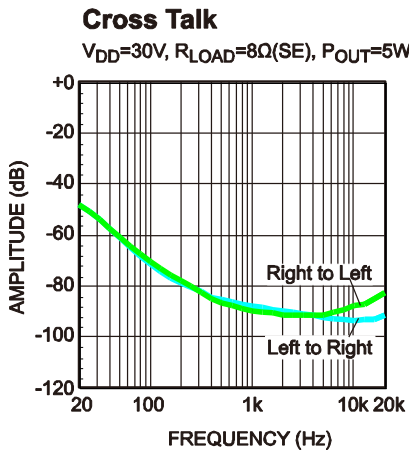
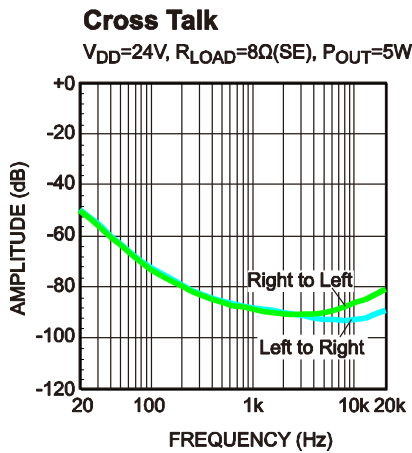
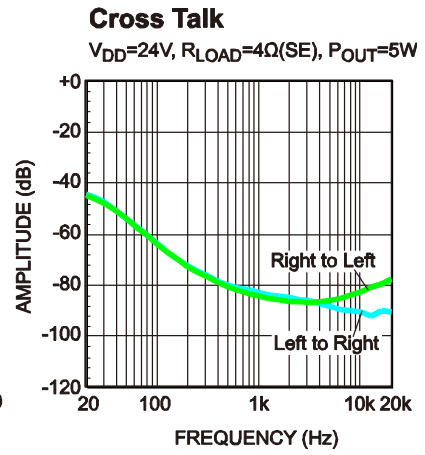
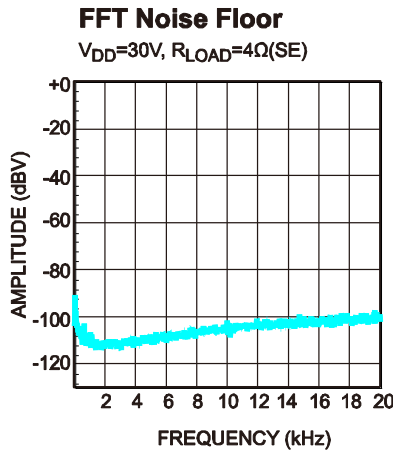
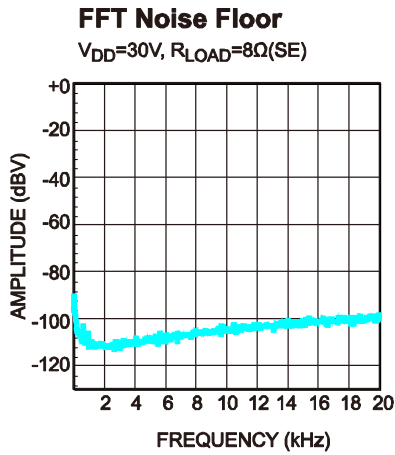
Circuit of Figure 5, single-ended output configuration,  $V_{DD}=24V$ ,  $V_{EN}=5V$ ,  $A_V=8.2V/V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.





**TYPICAL PERFORMANCE CURVES** *(continued)*

Circuit of Figure 5, single-ended output configuration,  $V_{DD}=24V$ ,  $V_{EN}=5V$ ,  $A_V=8.2V/V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.

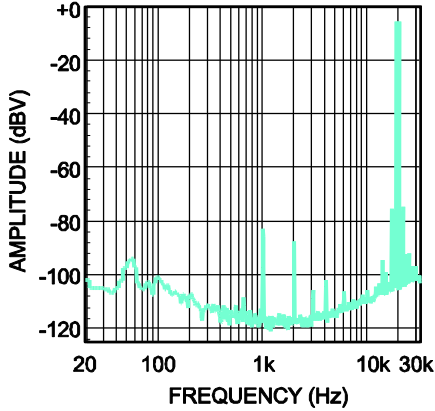


**TYPICAL PERFORMANCE CURVES** *(continued)*

Circuit of Figure 5, single-ended output configuration,  $V_{DD}=24V$ ,  $V_{EN}=5V$ ,  $A_V=8.2V/V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.

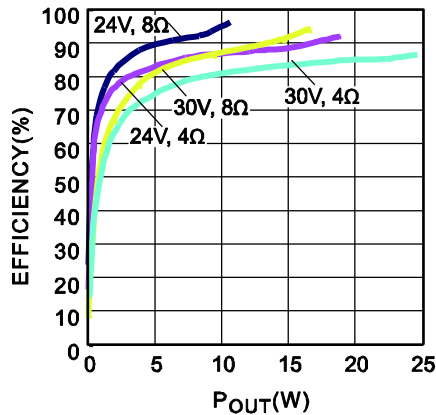
**IHF-IMD**

$V_{DD} = 30V$ ,  $R_{LOAD} = 4\Omega$ (SE),  
Test Tones: 19kHz and 20kHz  
Ratio=1:1



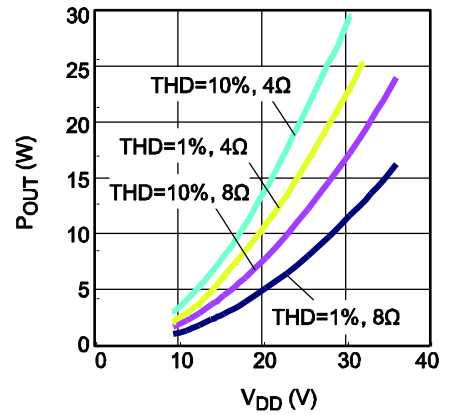
**Efficiency vs. P<sub>OUT</sub>**

Input Signal Frequency=1kHz



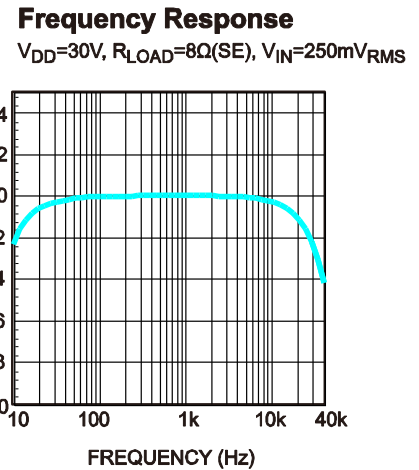
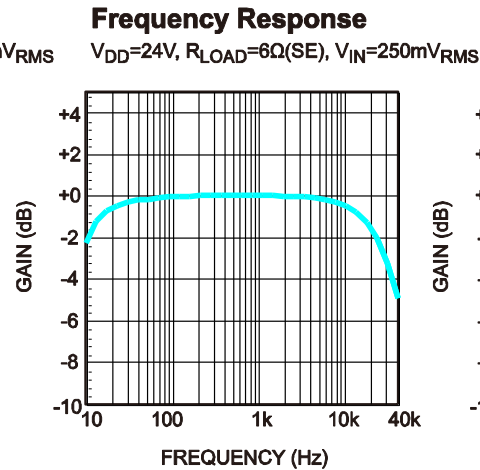
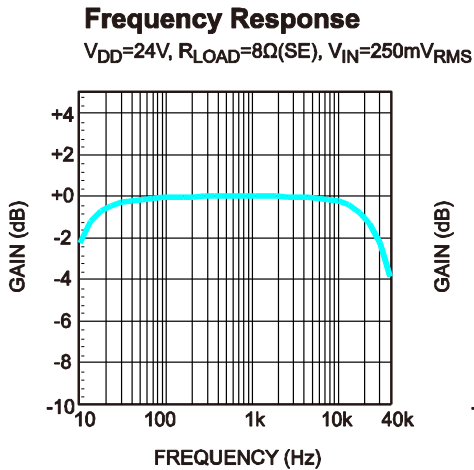
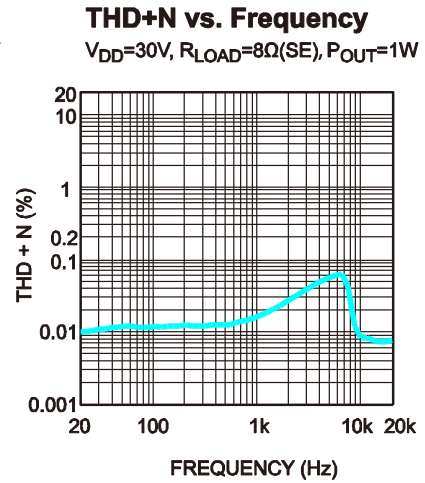
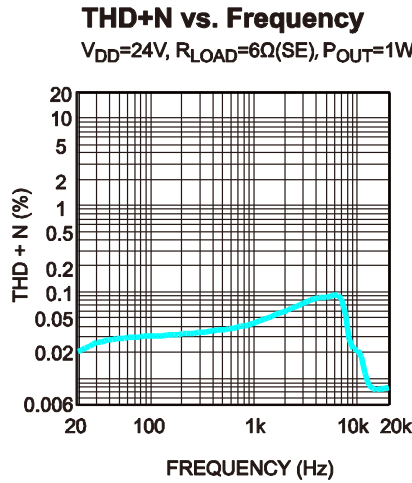
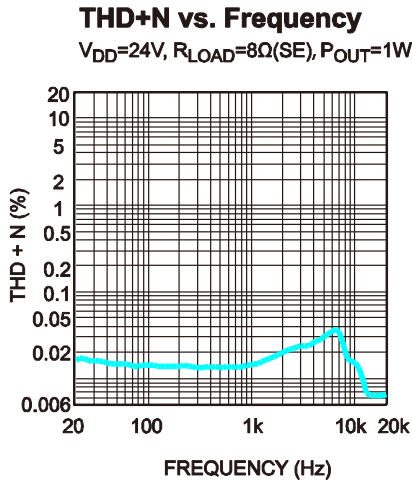
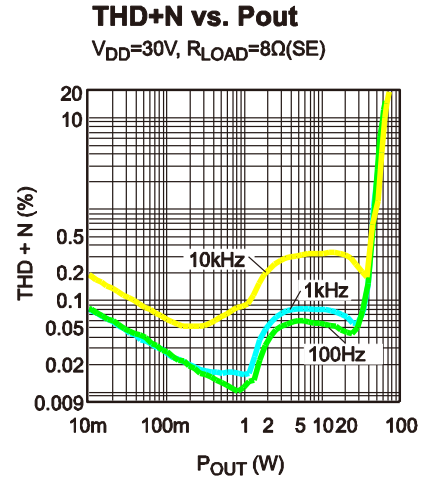
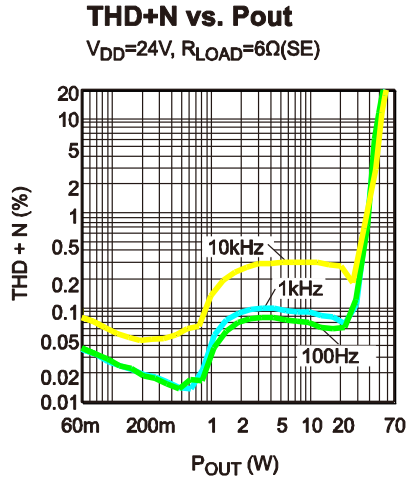
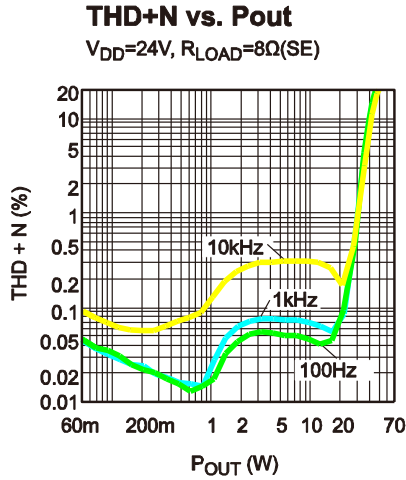
**P<sub>OUT</sub> vs. V<sub>DD</sub>**

Input Signal Frequency =1kHz  
the same P<sub>OUT</sub> for both channels



**TYPICAL PERFORMANCE CURVES (continued)**

Circuit of Figure 6, BTL output configuration,  $V_{DD}=24V$ ,  $V_{EN}=5V$ ,  $A_V=15V/V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.

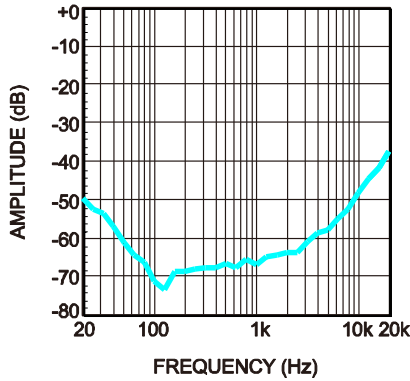


**TYPICAL PERFORMANCE CURVES** *(continued)*

Circuit of Figure 6, BTL output configuration,  $V_{DD}=24V$ ,  $V_{EN}=5V$ ,  $A_V=15V/V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.

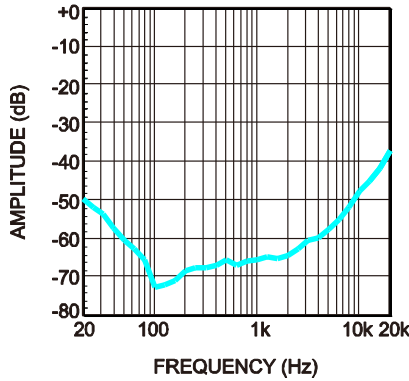
**Power Supply Rejection Ratio**

$V_{DD}=24V$ ,  $C_{BYP}=1\mu F$ ,  $R_{LOAD}=8\Omega(SE)$ ,  
 $V_{RIPPLE}=200mV_{PP}$ , Input AC grounded



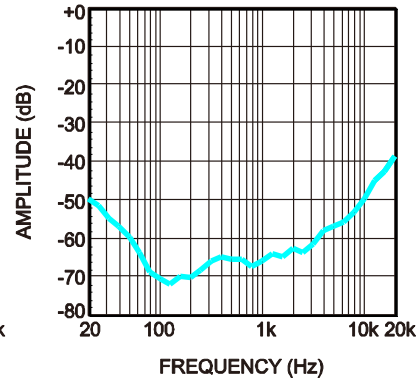
**Power Supply Rejection Ratio**

$V_{DD}=24V$ ,  $C_{BYP}=1\mu F$ ,  $R_{LOAD}=6\Omega(SE)$ ,  
 $V_{RIPPLE}=200mV_{PP}$ , Input AC grounded



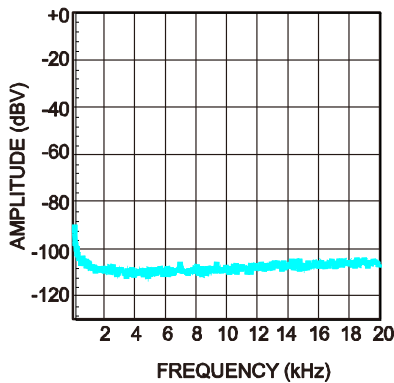
**Power Supply Rejection Ratio**

$V_{DD}=24V$ ,  $C_{BYP}=1\mu F$ ,  $R_{LOAD}=8\Omega(SE)$ ,  
 $V_{RIPPLE}=200mV_{PP}$ , Input AC grounded



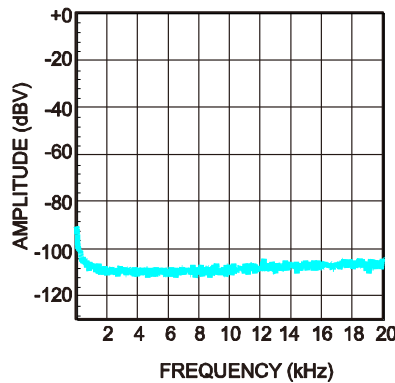
**FFT Noise Floor**

$V_{DD}=24V$ ,  $R_{LOAD}=8\Omega(SE)$



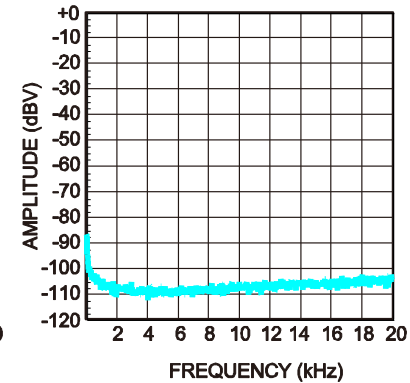
**FFT Noise Floor**

$V_{DD}=24V$ ,  $R_{LOAD}=6\Omega(SE)$



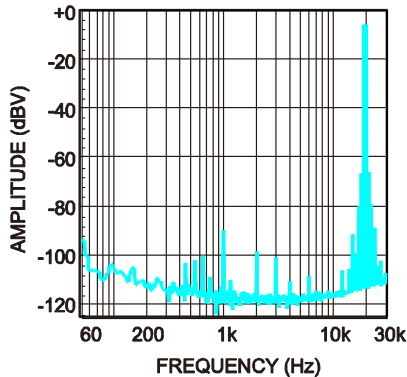
**FFT Noise Floor**

$V_{DD}=30V$ ,  $R_{LOAD}=8\Omega(SE)$



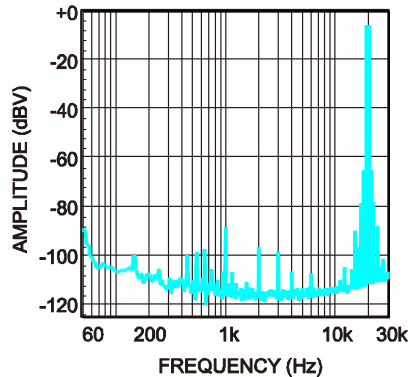
**IHF-IMD**

$V_{DD} = 24V$ ,  $R_{LOAD} = 8\Omega(SE)$ ,  
Test Tones: 19kHz and 20kHz  
Ratio=1:1



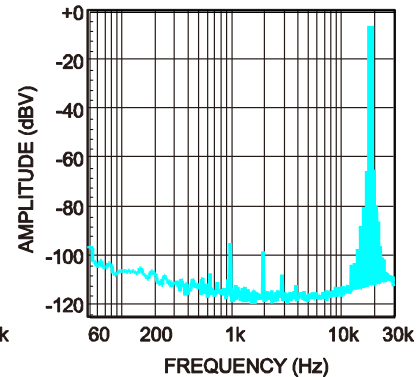
**IHF-IMD**

$V_{DD} = 24V$ ,  $R_{LOAD} = 6\Omega(SE)$ ,  
Test Tones: 19kHz and 20kHz  
Ratio=1:1



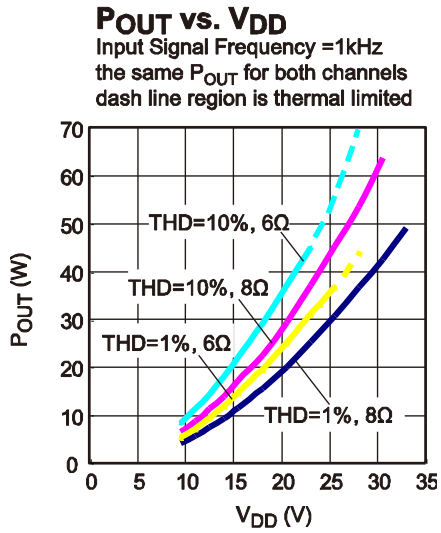
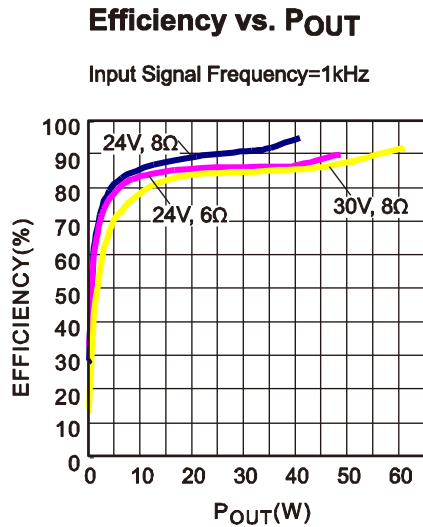
**IHF-IMD**

$V_{DD} = 30V$ ,  $R_{LOAD} = 8\Omega(SE)$ ,  
Test Tones: 19kHz and 20kHz  
Ratio=1:1

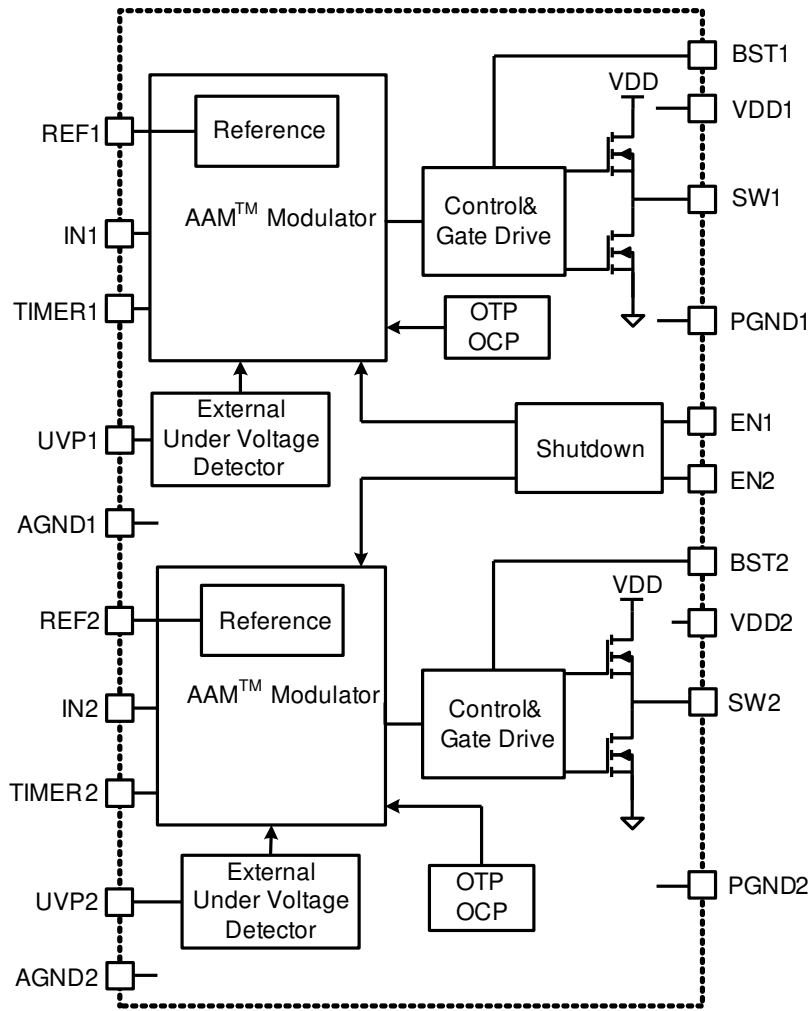


**TYPICAL PERFORMANCE CURVES** *(continued)*

Circuit of Figure 6, BTL output configuration,  $V_{DD}=24V$ ,  $V_{EN}=5V$ ,  $A_V=15V/V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.



**BLOCK DIAGRAM**



**Figure 1—Function Block Diagram**

## OPERATION

The MP7748S is a Class D Audio Amplifier for driving stereo speakers in single-ended configuration or a mono speaker in bridge-tied-load configuration. It uses the Monolithic Power Systems patented Analog Adaptive Modulation™ to convert the audio input signal into pulses. These pulses drive an internal high-current output stage and, when filtered through an external inductor-capacitor filter, reproduce the input signal across the load. Because of the switching Class D output stage, power dissipation in the amplifier is drastically reduced when compared to Class A, B or A/B amplifiers while maintaining high fidelity and low distortion.

REF1 and REF2 are the positive inputs of the two amplifiers. They are set to half the DC power supply input voltage ( $V_{DD}/2$ ) by the internal circuit. The input capacitor  $C_{IN}$  couple the AC signal at the input.

The amplifier voltage gain is set by the combination of the input resistor  $R_{IN}$  and the feedback resistor  $R_{FB}$  and is calculated by the equation:

$$AV = \frac{-R_{FB}}{R_{IN}}$$

Where: for Channel 1,  $R_{FB}=R_{FB1}$ ,  $R_{IN}=R_{IN1}$ ;

For Channel 2,  $R_{FB}=R_{FB2}$ ,  $R_{IN}=R_{IN2}$ .

The MP7748S includes four high-power MOSFETs wherein for each channel the output driver stage uses two 200mΩ N-channel MOSFETs to deliver the pulses to the LC output filter which in turn drives the load. To fully enhance the high-side MOSFET, the gate is driven to a voltage higher than the source by the bootstrap capacitor between SW and BS. While the output is driven low, the bootstrap capacitor is charged from  $V_{DD}$  through an internal circuit on the MP7748S. The gate of the high-side MOSFET is driven high from the voltage at BS, forcing the MOSFET gate to a voltage higher than  $V_{DD}$  and allowing the MOSFET to fully turn on, reducing power loss in the amplifier.

### Pop Elimination

The MP7748S integrates a source current function to charge the AC coupling capacitor  $C_{OUT1/2}$  for the SE output configuration and  $C_{IN1/2}$  at the start up moment. The start up source current slew rate is adjustable by selecting different capacitance of timer capacitor  $C_{TIMER1/2}$ . The larger the capacitance of the timer capacitor is, the smaller the start up current slew rate is. The recommended 1μF timer capacitor results in a start up current slew rate of approximately 20mA/350ms which would help to minimize the turn on pop.

After driving EN pin low, output SW will be set to high impedance immediately which would help to eliminate the turn off pop.

### Short Circuit/Overload Protection

The MP7748S has internal overload and short circuit protection. The currents in both the high-side and low-side MOSFETs are measured and if the current exceeds the 5.5A short circuit current limit, both MOSFETs are turned off. The MP7748S then restarts with the same power up sequence that is used for normal starting to prevent a pop from occurring after a short circuit condition is removed.

### Over-Temperature Shutdown

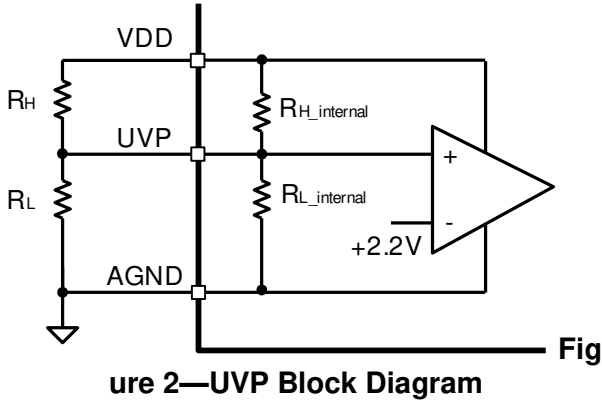
Thermal monitoring is also integrated into the MP7748S. If the die temperature rises above 150°C, all switches turn off. The temperature must fall below 120°C before normal operation resumes, with the same power-up sequence used to prevent popping noise.

### Enable Function

The MP7748S EN input is an active high enable control. To enable the MP7748S, drive EN with a 2.0V or higher voltage. To disable the amplifier, drive it below 0.4V. While the MP7748S is disabled, the  $V_{DD}$  operating current is around 100μA and the output driver MOSFETs are turned off.

**Programmable UVP**

MP7748S integrate programmable UVP function, which can be used to shutdown the MP7748S to escape the pop, by controlling the UVP node voltage. The VDD shutdown voltage can be flexibly adjusted by the external resistor, as shown in the figure 2.



If external resistor  $R_H$  and  $R_L$  is low enough (e.g.  $R_H, R_L < 50k\Omega$ ) compared with internal resistor, the VDD shutdown voltage (rising threshold) can be calculated by the equation:

$$V_{VDD\_shutdown} \approx 2.2 * \frac{(R_H + R_L)}{R_L}$$

If the UVP pin is NC, the default VDD shutdown voltage (rising threshold) is 8.4V since there is internal voltage divided circuit.

For example, please see the table 1 for recommended UVP setting for reduce the power off pop.

**Table 1: Recommended  $R_H$  and  $R_L$  for proper UVP setting.**

| VDD (V) | VDD_shutdown (V) | $R_H$ | $R_L$ |
|---------|------------------|-------|-------|
| 12      | 8.6              | 15k   | 5.1k  |
| 24      | 19               | 39k   | 5.1k  |
| 36      | 26               | 56k   | 5.1k  |



## APPLICATION INFORMATION

### Component Selection

The MP7748S uses a minimum number of external components to complete a stereo SE or mono BTL Class D audio amplifier. The circuit in Figure 5 (stereo SE application circuit) and Figure 6 (mono BLT application circuit) are optimized for a 30V power supply. This circuit should be suitable for most applications. Use the following sections to design custom circuits.

### Setting the Voltage Gain

The maximum output-voltage swing is limited by the power supply. To achieve the maximum output power, set the gain such that the maximum input signal results in the maximum output voltage swing.

For a single-ended (SE) output configuration, the maximum output voltage  $V_{OUT(PK)}$  is  $V_{DD}/2$ . For a bridge-tied-load (BTL) output configuration, the maximum output voltage  $V_{OUT(PK)}$  is  $V_{DD}$ . For a given input signal voltage, where  $V_{IN(PK)}$  is the peak input voltage, the maximum voltage gain is:

$$A_V(MAX) = \frac{V_{OUT(PK)}}{V_{IN(PK)}}$$

This voltage-gain setting results in the peak output voltage approaching its maximum for the maximum input signal. In some cases the amplifier is allowed to overdrive slightly, allowing the THD to increase at high power levels, and so a higher gain than  $A_V(max)$  is required.

### Setting the Switching Frequency

The idle switching frequency (the switching frequency when no audio input is present) is a function of several variables: The supply voltage  $V_{DD}$ , the integral capacitor  $C_{INT}$  and the feedback resistor  $R_{FB}$ . Lower switching frequencies result in greater inductor ripple, causing more quiescent output voltage ripple, and increasing the output noise and distortion. Higher switching frequencies result in greater power loss. The optimum quiescent switching frequency is approximately 600kHz. When used to drive stereo speakers in single-ended configuration, set right channel to an idle switching frequency greater than 50kHz plus the left channel's

switching frequency by using a different timing capacitor  $C_{INT}$ . For details, refer to the Table for recommended SE output configuration design, and Table 3 for recommended BTL output configuration design.

**Table 2: Switching Frequency Setting For SE Output Configuration**

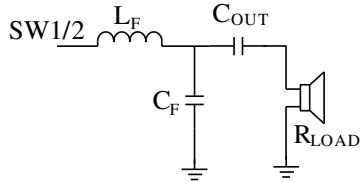
| $V_{DD}$<br>(V) | Gain<br>(V/V) | $R_{FB}$<br>(k $\Omega$ ) | $R_{IN}$<br>(k $\Omega$ ) | Left<br>channel    |                    | Right<br>channel   |                    |
|-----------------|---------------|---------------------------|---------------------------|--------------------|--------------------|--------------------|--------------------|
|                 |               |                           |                           | $C_{INT1}$<br>(nF) | $F_{SW1}$<br>(kHz) | $C_{INT2}$<br>(nF) | $F_{SW2}$<br>(kHz) |
| 12              | 10            | 100                       | 10                        | 1.8                | 694                | 1.5                | 774                |
| 12              | 20            | 100                       | 4.99                      | 1.8                | 694                | 1.5                | 782                |
| 24              | 10            | 150                       | 15                        | 2.7                | 653                | 2.2                | 720                |
| 24              | 20            | 150                       | 7.5                       | 2.7                | 654                | 2.2                | 723                |
| 24              | 30            | 150                       | 4.99                      | 2.7                | 657                | 2.2                | 723                |
| 30              | 10            | 150                       | 15                        | 3.3                | 653                | 2.7                | 743                |
| 30              | 20            | 150                       | 7.5                       | 3.3                | 654                | 2.7                | 745                |
| 30              | 30            | 150                       | 4.99                      | 3.3                | 659                | 2.7                | 747                |
| 36              | 10            | 150                       | 15                        | 5.6                | 588                | 3.9                | 665                |
| 36              | 20            | 150                       | 7.5                       | 5.6                | 590                | 3.9                | 667                |
| 36              | 30            | 150                       | 4.99                      | 5.6                | 592                | 3.9                | 670                |

**Table 3: Switching Frequency Setting for BTL Output Configuration**

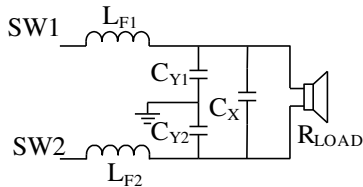
| $V_{DD}$<br>(V) | Gain<br>(V/V) | $R_{FB}$<br>(k $\Omega$ ) | $R_{IN}$<br>(k $\Omega$ ) | $C_{INT}$<br>(nF) | $F_{SW}$<br>(kHz) |
|-----------------|---------------|---------------------------|---------------------------|-------------------|-------------------|
| 12              | 10            | 100                       | 10                        | 1.0               | 686               |
| 12              | 20            | 100                       | 4.99                      | 1.0               | 693               |
| 24              | 10            | 150                       | 15                        | 1.0               | 660               |
| 24              | 20            | 150                       | 7.5                       | 1.0               | 669               |
| 24              | 30            | 150                       | 4.99                      | 1.0               | 674               |
| 30              | 10            | 150                       | 15                        | 1.2               | 670               |
| 30              | 20            | 150                       | 7.5                       | 1.2               | 672               |
| 30              | 30            | 150                       | 4.99                      | 1.2               | 677               |

**Choosing the Output LC Filter**

The inductor-capacitor (LC) filter converts the pulses at SW to the output voltage that drives the speaker. There are two kinds of LC filter structure depending on the output configuration.



**Figure 3: SE Filter Configuration**



**Figure 4: BTL Filter Configuration**

Where:

$$L_F = L_{F1} + L_{F2},$$

$$C_F = C_X + \frac{C_{Y1} \times C_{Y2}}{C_{Y1} + C_{Y2}},$$

$$L_{F1} = L_{F2};$$

$$C_{Y1} = C_{Y2}$$

The characteristic frequency of the LC filter needs to be high enough to allow high frequency audio to the output, yet needs to be low enough to filter out high frequency products of the pulses from the SW pin. The characteristic frequency of the LC filter is:

$$f_0 = \frac{1}{2 \times \pi \times \sqrt{L_F \times C_F}}$$

The quality factor (Q) of the LC filter is important: If this is too low, output noise will increase; if this is too high, then peaking may occur at high frequencies and reduce the passband flatness. The circuit Q is set by the load resistance (speaker resistance, typically 4Ω or 8Ω). Q is calculated as:

$$Q = \frac{R_{LOAD}}{\omega_0 \times L_F} = \frac{R_{LOAD}}{2\pi \times f_0 \times L_F}$$

$\omega_0$  is the characteristic frequency in radians/second and  $f_0$  is in Hz. Use an LC filter with Q between 0.7 and 1.

The type of inductor and capacitor used in the LC filter greatly affects the output ripple and noise. Use a film capacitor and an inductor with sufficient power rating to supply the output current to the load. The inductor must exhibit soft saturation characteristics: If the inductor exhibits hard saturation, it should operate well below the saturation current. Use toroidal cores made of gapped ferrite, MPP, powdered iron, or similar materials. If using either an open or shielded bobbin ferrite core for multi-channel designs, make sure that the start windings of each inductor align (all starting toward the SW pin, or all starting toward the output) to prevent crosstalk or other channel-to-channel interference.

**Output Coupling Capacitor for SE Output**

The output AC coupling capacitor— $C_{OUT}$ —serves to pass only the amplified AC signal from the LC filter to the load and to block DC signals. The combination of the coupling capacitor,  $C_{OUT}$  and the load resistance results in a first-order high-pass filter. Select  $C_{OUT}$  so that the required minimum frequency passes. The output corner frequency (-3dB point),  $f_{OUT}$ , can be calculated as:

$$f_{OUT} = \frac{1}{2 \times \pi \times R_{LOAD} \times C_{OUT}}$$

Set the output corner frequency ( $f_{OUT}$ ) at or below the minimum required frequency.

The output coupling capacitor carries the full load current, so chose a capacitor such that its ripple current rating is greater than the maximum load current. Use low-ESR aluminum electrolytic capacitors for best results.

**Input Coupling Capacitor**

The input coupling capacitors  $C_{IN1}$  and  $C_{IN2}$  pass only the AC signal at the input. For a typical system application, the source input signal centers around the circuit ground, while the MP7748S input is at half the power supply voltage ( $V_{DD}/2$ ). The input coupling capacitor transmits the AC signal from the source

to the MP7748S while blocking the DC voltage. Choose an input coupling capacitor such that the corner frequency ( $f_{IN}$ ) is less than the passband frequency. The corner frequency is calculated as:

$$f_{IN} = \frac{1}{2 \times \pi \times R_{IN} \times C_{IN}}$$

### Timer capacitor

The start-up source current slew rate is related to the timing capacitor  $C_{TIMER}$  and SW voltage: The higher SW voltage is, the smaller charge current slew rate is. The larger the  $C_{TIMER}$  capacitance is, the longer the start-up time is. Select a  $C_{TIMER}$  value larger than 312nF, so the start-up current slew rate would be small which helps eliminate the turn-on pop. The recommended 1 $\mu$ F capacitor  $C_{TIMER}$  results in a start-up current slew rate of approximately 20mA/350ms.

### Power Source

For maximum output power, the amplifier circuit requires a regulated external power source. A high power-supply voltage can deliver more power to a given load resistance, but a power-source voltage exceeding the maximum voltage of 36V can damage the MP7748S. The MP7748S's power supply rejection is excellent, though power-supply noise can pass to the output, so care must be taken to minimize power supply noise within the pass-band frequencies. Bypass the power supply with a large capacitor (typically aluminum electrolytic) along with a smaller 1 $\mu$ F ceramic capacitor at the MP7748S  $V_{DD}$  supply pins.

### PCB Layout

Circuit layout is critical for optimal performance, low output distortion, and noise. Duplicate the EVB layout for best results. For layout changes, follow these guidelines and use Figure 7 and Figure 8 as references.

1) Place the following components as close to the MP7748S as possible:

#### *Bootstrap Capacitors*

$C_{BS1}$  and  $C_{BS2}$  supply the gate drive current to the internal HS-FET. Place  $C_{BS1}$  as close to BST1/2 pin and SW1/2 pin as possible.

Likewise, place  $C_{BS2}$  as close to BST2 pin and SW2 pins as possible.

#### *Power Supply Bypass Capacitors*

$C_{BYP1}$  and  $C_{BYP2}$  carry the transient current for the switching power stage. To avoid overstressing the MP7748S and excessive output noise, place  $C_{BYP1}$  as close to the VDD1 pins and PGND1 pins as possible, and place  $C_{BYP2}$  as close to the VDD2 pins and PGND2 pins as possible.

#### *Integral Capacitors*

$C_{INT}$  sets the amplifier switching frequencies and are typically on the order of a few nF. Place the integral capacitor  $C_{INT}$  as close to the corresponding input as possible to reduce distortion and noise. For example, place  $C_{INT1}$  as close to pins 2 and 3 as possible at SE output configuration.

#### *Reference Bypass Capacitors for SE Output*

When used with SE output, CR1 and CR2 filter the  $\frac{1}{2}$  VDD reference voltages. Place  $C_{R1}$  and  $C_{R2}$  as close to the IC as possible to improve power supply rejection and reduce distortion and noise at the output.

2) The Inductor-Capacitor (LC) filter converts the pulse train at SW to the output voltage that drives the speaker. Please keep the filter capacitor close to the inductor.

3) When laying out the PCB, use two separate ground planes—analogue ground (AGND) and power ground (PGND)—and connect the two grounds together at a single point (usually around the bulk bypass capacitor) to prevent noise injection into the amplifier input to reduce distortion.

4) Keep the sensitive feedback signal trace on the input side and shield the trace with the AGND plane. Make sure that any traces carrying the switch node (SW) voltages are routed far from any input signal traces. If the trace must run near the SW trace near the input, shield the input with a ground plane between the traces. Physically separate each channel to prevent crosstalk. Make sure that all inductors used on a single circuit board have the same orientation.

Route each power supply from the source to each channel individually, not serially. This prevents channel-to-channel coupling through the power supply input.

### **Electro-Magnetic Interference (EMI) Considerations**

Due to the switching nature of Class D amplifiers, care must be taken to minimize the effects of electromagnetic interference from the amplifier. However, proper component selection and careful attention to circuit layout can minimize the effects of the EMI due to the amplifier switching.

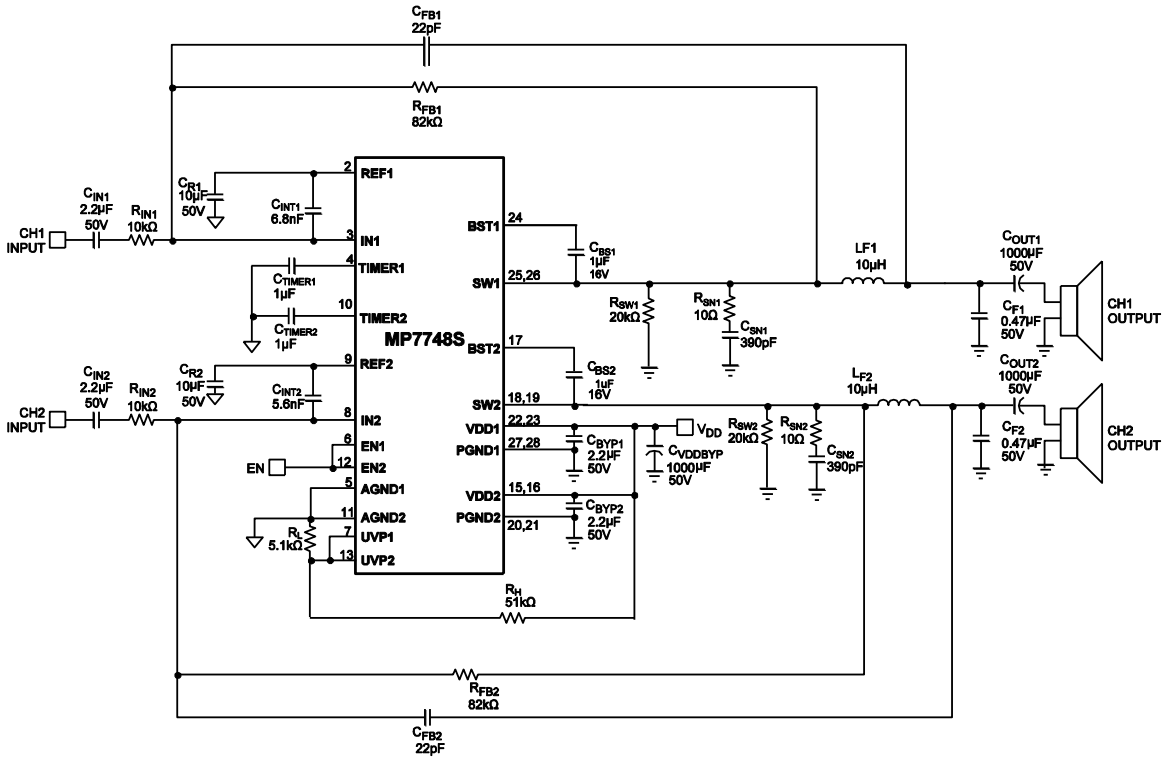
The power inductors are a potential source of radiated emissions. For the best EMI performance, use toroidal inductors, since the magnetic field is well-contained inside the core.

However toroidal inductors can be expensive to wind. For a more economical solution, use shielded-gapped-ferrite or shielded-ferrite-bobbin-core inductors. These inductors typically do not contain the EM field as well toroidal inductors, but can achieve a better balance between good EMI performance with low cost.

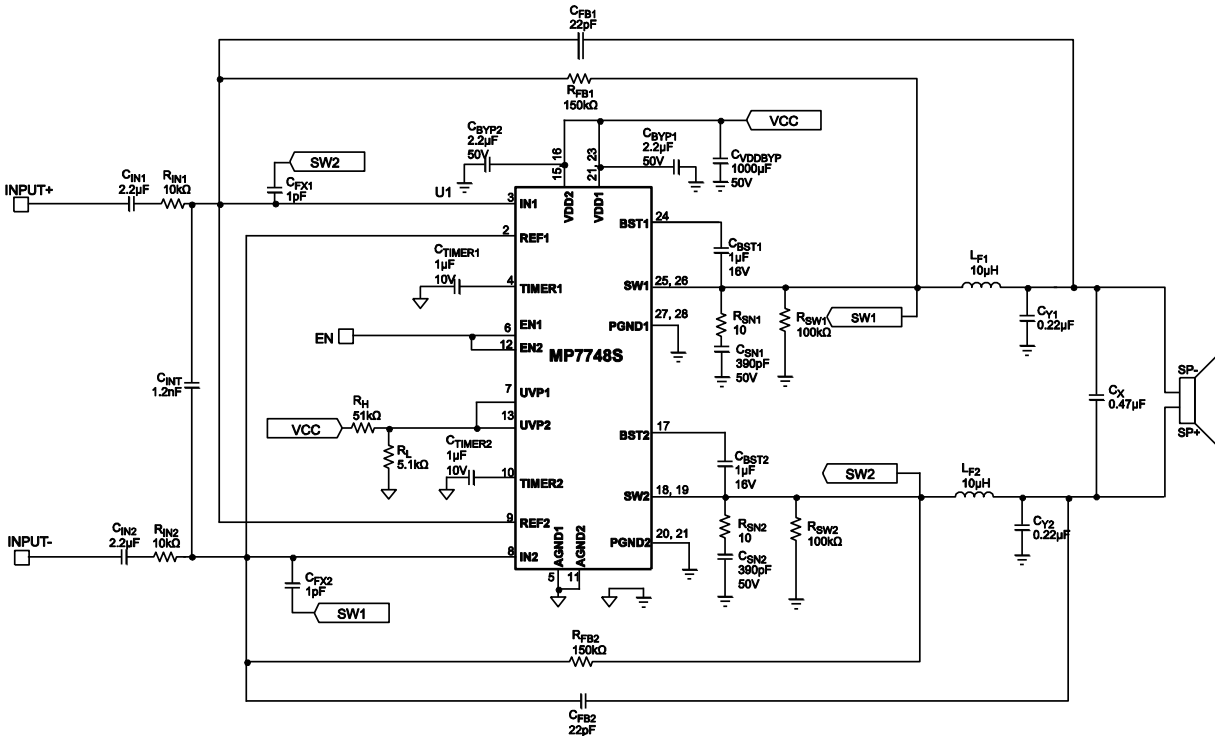
The size of high-current loops that carry rapidly changing currents must be minimized: Make sure that the  $V_{DD}$  bypass capacitors are as close to the MP7748S as possible.

Nodes that carry rapidly changing voltage, such as SW, need to be made as small as possible. If sensitive traces run near a trace connected to SW, place a ground shield between the traces.

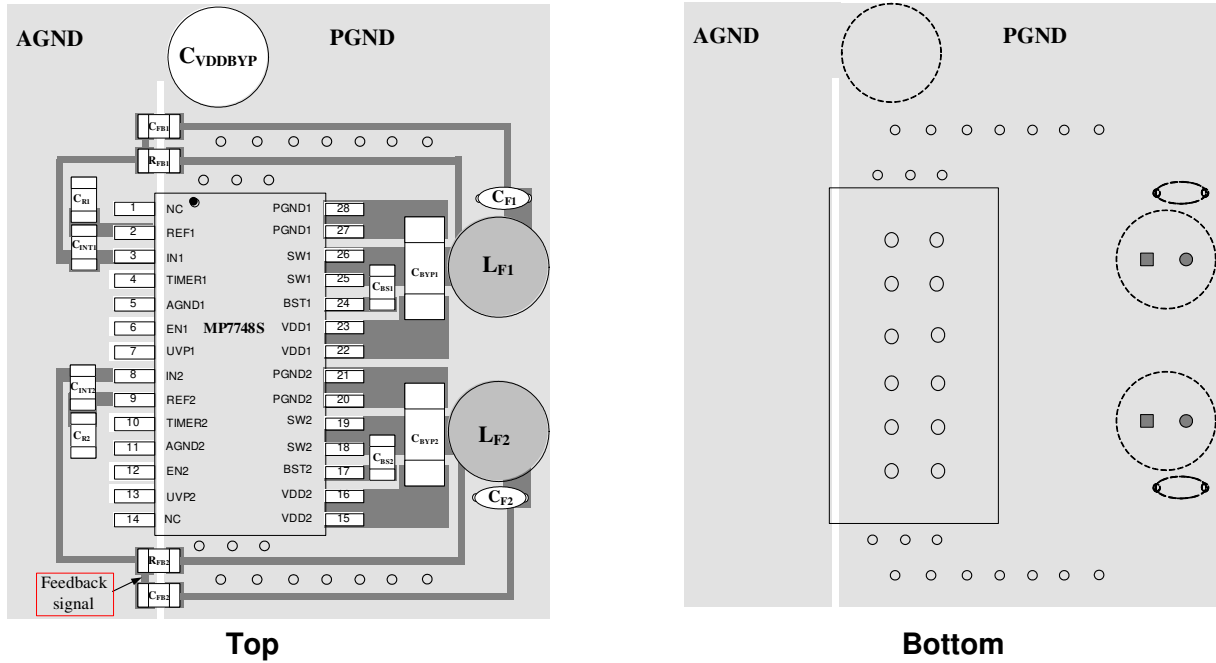
**TYPICAL APPLICATION CIRCUITS**



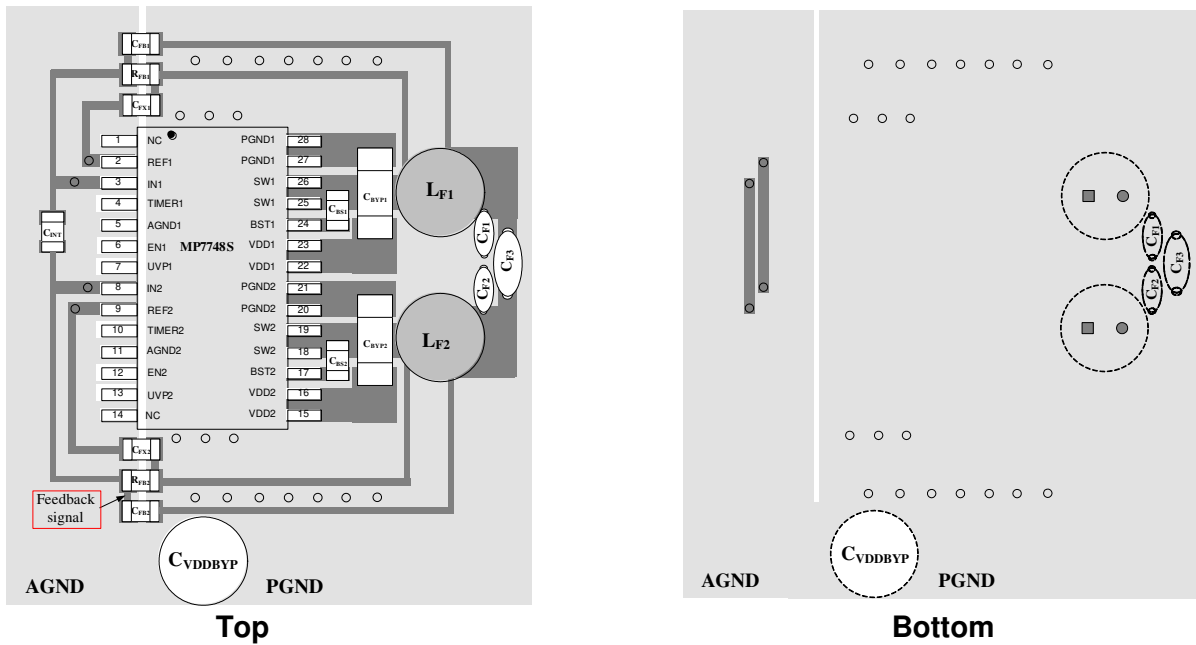
**Figure 5—30V VDD Stereo SE Typical Application Circuit**



**Figure 6—30V VDD mono BTL Typical Application Circuit**



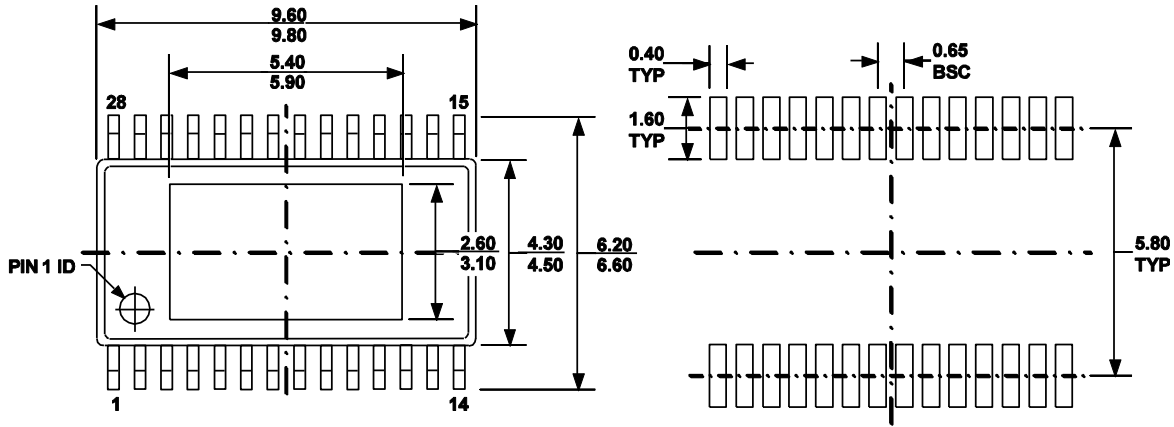
**Figure 7—Stereo SE Reference PCB Layout**



**Figure 8—Mono BTL Reference PCB Layout**

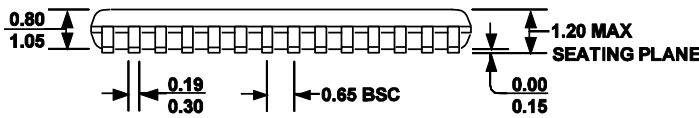
**PACKAGE INFORMATION**

**TSSOP28-EP**

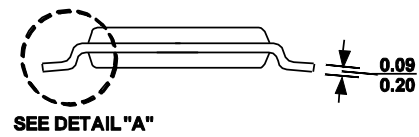


**TOP VIEW**

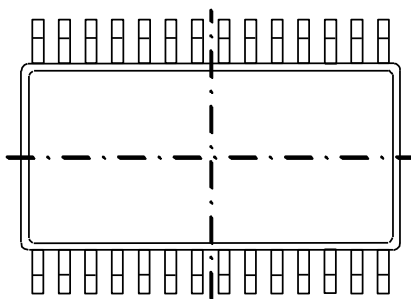
**RECOMMENDED LAND PATTERN**



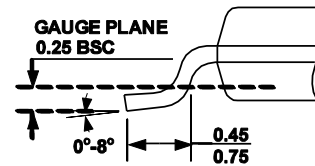
**FRONT VIEW**



**SIDE VIEW**



**BOTTOM VIEW**



**DETAIL "A"**

**NOTE:**

- 1) ALL DIMENSIONS ARE IN MILLIMETERS
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX
- 5) JEDEC REFERENCE IS MO-153.
- 6) DRAWING IS NOT TO SCALE

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