A8509

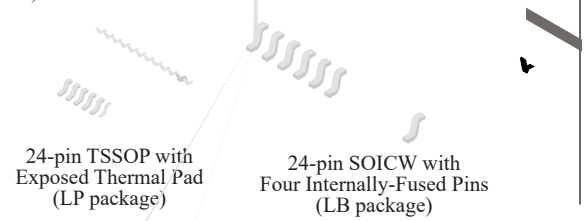
Wide Input Voltage Range, High Efficiency 4-Channel Fault Tolerant LED Driver

FEATURES AND BENEFITS

- Four integrated high current sinks for LED strings; can be tied together for even higher currents
- Fixed frequency current mode control with integrated gate driver / boost controller; powerful gate driver to drive an external N-channel MOSFET allows significant scaling capability on the number of LEDs per string
- Parallel operation with one boost controller (master) and up to three additional slave controllers; can run up to 16 strings of LEDs while populating only a single master boost regulator
- Active current sharing between LED strings for 0.7% accuracy and 0.8% matching
- Wide input voltage range: 9 to 40 V
- Internal bias supply for single-supply operation (typically V_{IN} = 12 or 24 V)
- Separate Enable and PWM pins as interface for Enable and PWM Dimming functions
- FSET / SYNC function to either set the boost converter switching frequency or synchronize at up to 800 kHz
- Protection Features
  - Open or shorted LED pin protection
  - Open Schottky protection
  - Pulse-by-pulse current limit
  - Overtemperature protection (OTP)

PACKAGES

(Not to scale)



24-pin TSSOP with Exposed Thermal Pad (LP package)

24-pin SOICW with Four Internally-Fused Pins (LB package)

DESCRIPTION

The A8509 is a multi-output white LED driver for backlighting LCD panels. It integrates a current-mode boost controller and four individual current sinks.

The boost controller architecture allows for significant scaling of boost voltage to optimize the solution for the required number of LEDs per string. The FSET/SYNC pin either sets the required boost switching frequency or synchronizes the value in the range of 300 to 800 kHz.

The LED sink current value is set by an external ISET resistor (see figure 1). The four LED sinks can also be combined to achieve even higher current per LED string.

The A8509 provides protection against output shorts and overvoltage, open or shorted LED pins, and overtemperature. A dual-level, pulse-by-pulse current limit function provides soft-start and protects the external current switch against high current overloads. As an option, the A8509 can drive an external P-FET interfaced to the $\overline{\text{FAULT}}$ pin to disconnect the input supply from the system in the event of short-to-ground in the boost converter.

Package options are 24-pin TSSOP (suffix LP) and SOICW (LB) packages. The TSSOP has an exposed thermal pad, and the SOICW has four internally fused pins, for enhanced thermal dissipation. Both packages are lead (Pb) free, with 100% matte tin leadframe plating.

Typical Application

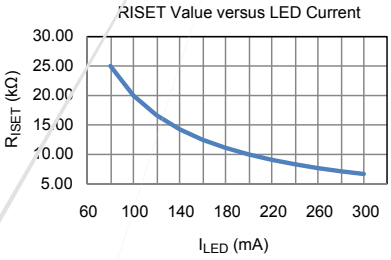
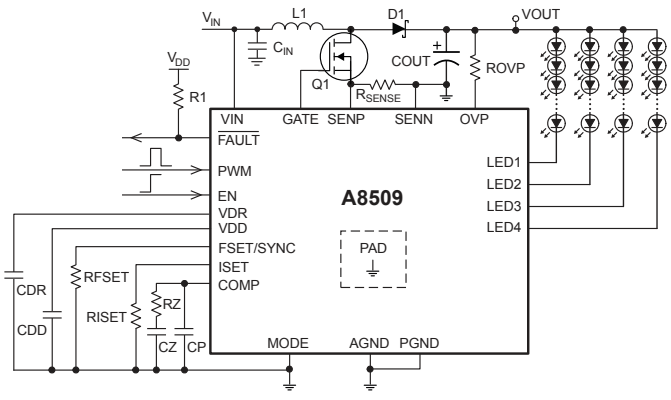


Figure 1. Typical application circuit showing 4 channels of LEDs; RZ-CZ optional (component list shown in the Typical Applications section)



ABSOLUTE MAXIMUM RATINGS*

Characteristic	Symbol	Notes	Rating	Unit
LEDx Pin Voltage	V_{LEDx}		–0.3 to 55	V
OVP Pin Voltage	V_{OVP}		–0.3 to 60	V
VIN Pin Voltage	V_{IN}		–0.3 to 40	V
$\overline{\text{FAULT}}$ Pin Voltage	V_{FAULT}		–0.3 to 40	V
COMP, EN, FSET/SYNC, ISET, MODE, PWM, SENN, SENP, and VDD Pin Voltage	–		–0.3 to 5.5	V
GATE, VDR Pin Voltage	–		–0.3 to 8	V
Operating Ambient Temperature	T_A	G temperature range	–40 to 105	°C
Maximum Junction Temperature	T_J(max)		150	°C

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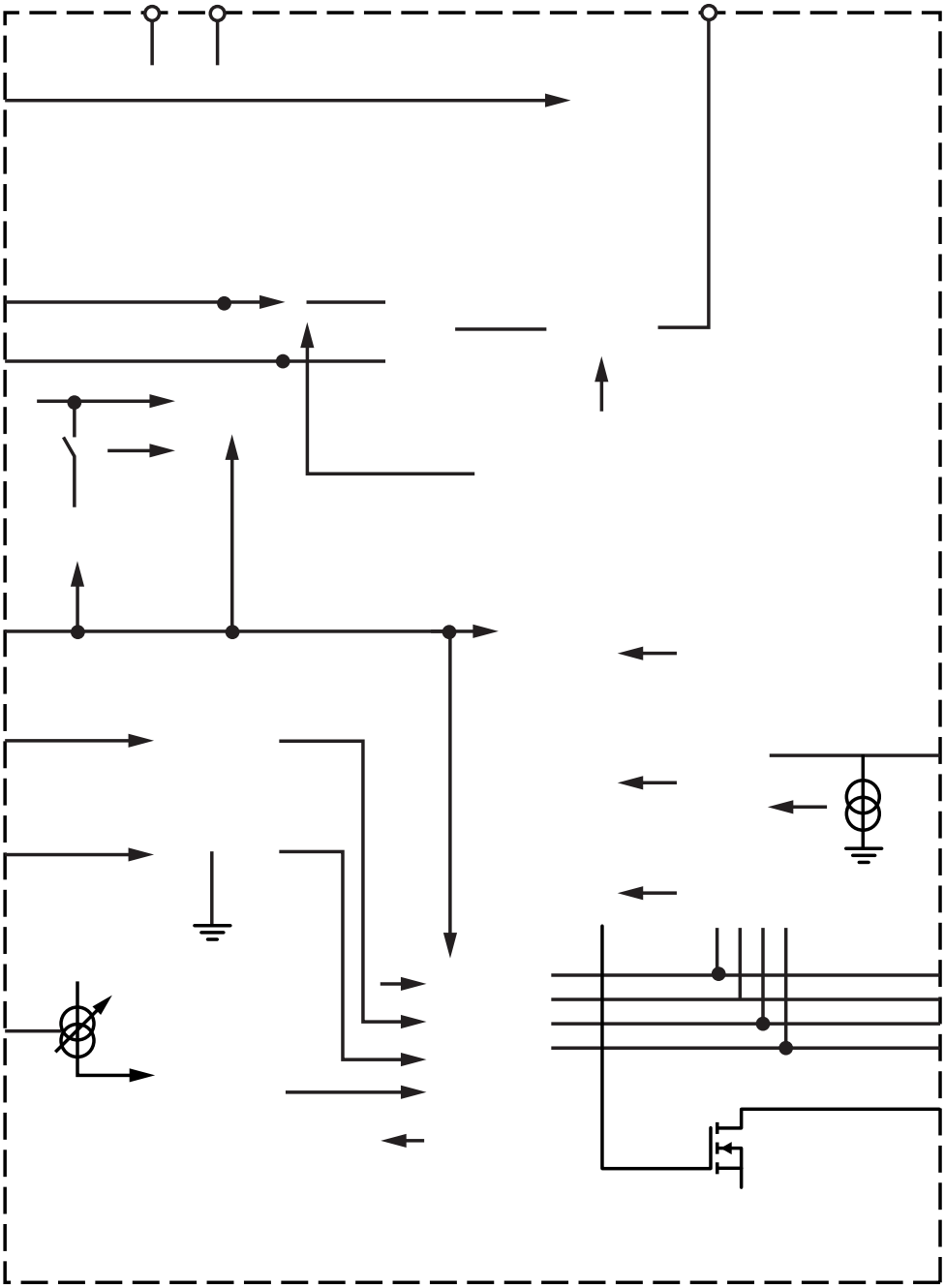
FUNCTIONAL BLOCK DIAGRAM



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Pinout Diagrams

Terminal List Table

Name	Number		Function
	LB	LP	
AGND	18, 19	18, 19	LED ground.
COMP	4	5	Output of the error amplifier and compensation node. Connect a compensation network from this pin to ground.
EN	8	7	Enable for the A8509.
$\overline{\text{FAULT}}$			

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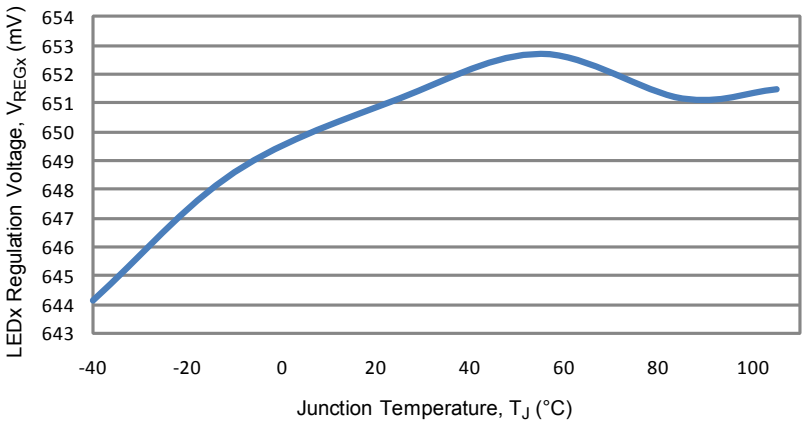

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FUNCTIONAL DESCRIPTION

Enabling the IC

The IC turns on when a logic high signal is applied on the EN pin, and the input voltage present on the VIN pin is greater than the 8.5 V necessary to clear the UVLO ($V_{UVLOrise}$) threshold. Before the LEDs are enabled, the A8509 driver goes through a system check to determine if there are any possible fault conditions that might prevent the system from functioning correctly.

Powering Op: LED Pin short-to-GND Check

After the VIN pin goes above the UVLO threshold, and a high signal is present on the EN pin, the IC proceeds to check if any LEDx pins are shorted to GND and/or are not used. Each unused pin should be connected to GND with a 2.4 kΩ pull-down resistor.

After the voltage threshold on the LEDx pins exceeds 120 mV, a timer of 1536 clock cycles (2 ms at 800 kHz switching frequency, see figure 2) is applied during which the A8509 determines the status of the pins. Any unused pin connected to GND with the pull-down resistor will be taken out of regulation at this point and will not contribute to the boost regulation loop (see figure 3). A typical example is shown in figure 4. When a pin is connected to GND through a 2.4 kΩ resistor, the voltage on that LEDx pin during the LED detection period is about 200 mV. This is shown in figure 2.

If an LEDx pin is shorted to ground such that LEDx pin voltage is < 100 mV, the A8509 will not proceed with soft-start until the short is removed from the LEDx pin. This prevents the A8509

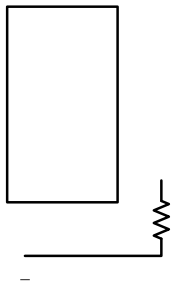

Figure 4. Channel select setup: (left) channel LED4 not used, (right) using all channels.

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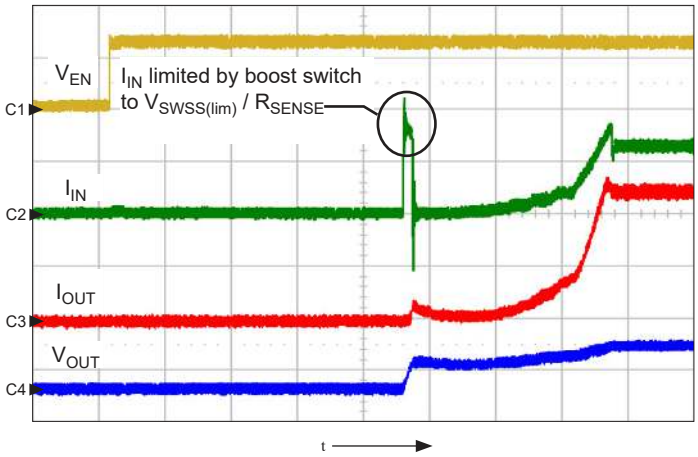

Figure 6. Start-up operation, individual LEDx current = 120 mA, boost sense resistor = 0.020 Ω; shows V_{EN} (ch1, 2 V/div.), I_{IN} (ch2, 1 A/div.), I_{OUT} (ch3, 200 mA/div.), and V_{OUT} (ch4, 20 V/div.), t = 500 µs/div.

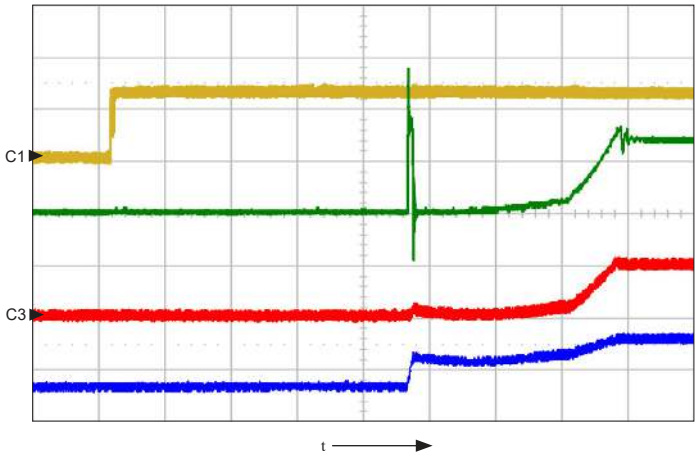

Figure 7. Start-up operation, individual LEDx current = 240 mA, boost sense resistor = 0.010 Ω; shows V_{EN} (ch1, 2 V/div.), I_{IN} (ch2, 2 A/div.), I_{OUT} (ch3, 1 A/div.), and V_{OUT} (ch4, 20 V/div.), t = 500 µs/div.

Figure 8. Normal start-up behavior; shows VEN (ch1, 2 V/div.), V_{COMP} (ch2, 2 V/div.), I_{IN} (ch3, 1 V/div.), and V_{OUT} (ch4, 10 V/div.), t = 500 µs/div.

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Frequency Selection

The switching frequency on the boost regulator is set by connecting a resistor between the FSET/SYNC pin and ground. The switching frequency range is 300 to 800 kHz, with example values of:

R_{FSET} Value (kΩ)	Switching Frequency, f_{SW} (kHz)
7.5	800
10	600

The relationship of R_{FSET} and f_{SW} is shown in figure 9.

The FSET/SYNC pin has short-to-ground protection. If the FSET/SYNC pin is held low for more than 4 µs typical, the A8509 will stop switching and disable the LEDx pins (see figures 10 and 11). If the FSET/SYNC pin is released at any time after 7 µs, the A8509 will proceed to soft-start but will not perform the LED detection phase.

Figure 10. Shutdown when the FSET/SYNC pin is shorted to ground; shows V_{OUT} (ch1, 10 V/div.), $V_{FSET/SYNC}$ (ch2, 1 V/div.), I_{IN} (ch3, 2 A/div.), and I_{OUT} (ch4, 500 mA/div.), t = 200 µs/div.

Synchronization

The A8509 can also be synchronized by using an external clock connected to the FSET/SYNC pin. The synchronization function of IC was designed to work with a push-pull type of clock driver. The amplitude of the clock signal should be between 1.5 and 3.3 V. The synchronization clock should have duty cycles that meet the minimum on/off times. Figure 12 shows the timing for a synchronization clock into the A8509 at 800 kHz. The 150 ns minimum on-time and 150 ns minimum off-time are

Figure 11. Zoomed-in view of figure 9, showing quick shutdown when FSET/SYNC shorted to ground, preventing IC running at very high frequency; shows V_{OUT} (ch1, 10 V/div.), $V_{FSET/SYNC}$ (ch2, 1 V/div.), I_{IN} (ch3, 2 A/div.), and I_{OUT} (ch4, 1 A/div.), t = 10 µs/div.

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indicated by the specifications for $t_{PWSYNCON}$ and $t_{PWSYNCOFF}$. Thus any pulse with a duty cycle of 19% to 85% at 800 kHz will synchronize the IC.

It is recommended to also use the RFSET resistor with the external clock signal. If a synchronization clock is lost during operation, the IC will revert to the preset switching frequency that is set by the RFSET resistor. In this configuration the preset frequency does not have any restrictions other than the normal operating range of 300 to 800 kHz. During the changeover period the IC stops switching for an approximately 5 µs period to allow for the synchronization detection circuitry to switch over to external preset switching frequency.

Although examples shown in figures 13 and 14 are extreme cases of clock-to-resistor frequency changes, it is recommended that actual applications do not have such large switching frequency changes. In most applications the RFSET resistor and clock frequency should be very close to each other in terms of frequency. Setting the frequencies close together will prevent the system from experiencing large changes on frequency-dependent signals and components, such as the inductor ripple current and the compensation resistor and capacitor.

LED Current Setting and LED Dimming

The maximum LED current can be up to 300 mA per channel. The LED current is set through the RISET resistor connected between the ISET pin and ground. The I_{LED} current is set according to the following formula:

$$R_{ISET} = (1.000 / I_{LED}) \times 2320 \quad (2)$$

where R_{ISET} is in Ω, and I_{LED} is in A. This sets the maximum current through the LEDs, referred to as the *100% current*. Standard R_{ISET} values are as follows:

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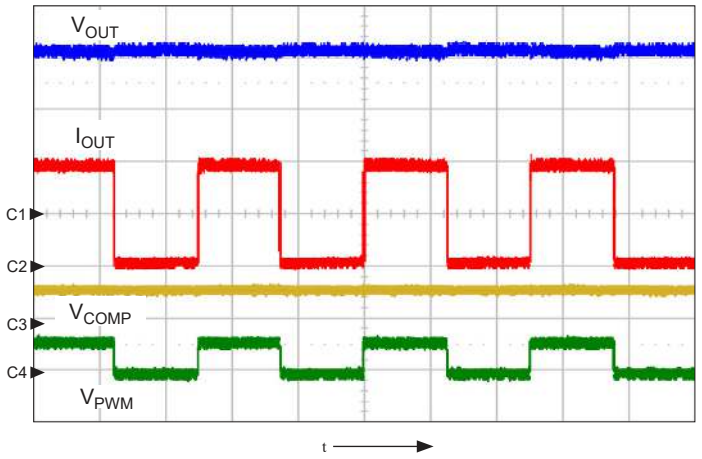
The cited values are for 1% tolerance resistors. If the calculated value was not present, the next lowest value of 1% resistor was chosen.

PWM Dimming

Applying an external PWM signal on the PWM pin performs PWM dimming. When the PWM pin is pulled high, the A8509 enables the LEDx pins to sink 100% current. When PWM is pulled low, the boost converter and LEDx sinks are turned off. The compensation (COMP) pin is floated, and critical internal circuits are kept active.

The typical PWM dimming frequencies fall between 100 and 1000 Hz. Figures 15 and 16 show examples of dimming at 50% and 0.5% duty cycles.



Analog Dimming

The A8509 can also be dimmed by using an external DAC or other voltage source applied either directly to the ground side of the RISET resistor or through an external resistor to the ISET pin (see figure 17). The ISET current can be varied in the range between 34 µA and 130 µA.

• For a single-resistor configuration (panel A of figure 17), the ISET current is controlled by the following formula:

$$I_{SET} = \frac{V_{ISET} - V_{DAC}}{R_{ISET}}$$

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Boost Switch Overcurrent Protection

The boost switch is protected with pulse-by-pulse current limiting set by the external RSENSE resistor. There also is a secondary current limit that is sensed on the boost switch.

Setting the Current Sense Resistor

The current sense resistor (see figure 18) is set according to the following formula:

$$I_{LIM} = \frac{V_{SENP}}{R_{SENSE}} \quad (5)$$

where V_{SENP} is found in the Electrical Characteristics table, and R_{SENSE} is the current sense resistor value.

The current limit is calculated by the following formula:

$$I_{LIM} = I_{IN}(max) + \frac{\Delta I_L}{2} \quad (6)$$

where $I_{IN}(max)$ is the maximum input current, and ΔI_L is the inductor current ripple.

Current Sense Resistor Routing

The current sense resistor must be routed as a differential pair to minimize measurement accuracy errors. For most current sense resistors, the resistance is measured between the inside edges of the mounting pads of the RSENSE resistor.

Figure 19 shows correct differential current sensing connections to the A8509. The individual current sense traces are kept short and side-by-side to get proper signal voltage levels. The trace for the positive sense pin (SENP) must be routed to the inside edge of the mounting pad on the high side of RSENSE. The trace for the negative sense pin (SENN) must be routed to the inside edge of the mounting pad on the ground side of RSENSE.

It should be noted that when designing the PCB layout, the trace for the negative sense pin (SENN) is often automatically merged with the ground flood fill and with the mounting pad on the the negative senoutinglETe o0 an the inside edge

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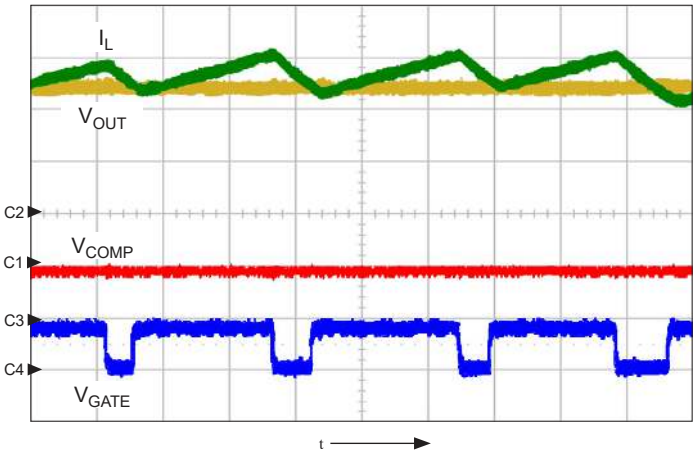
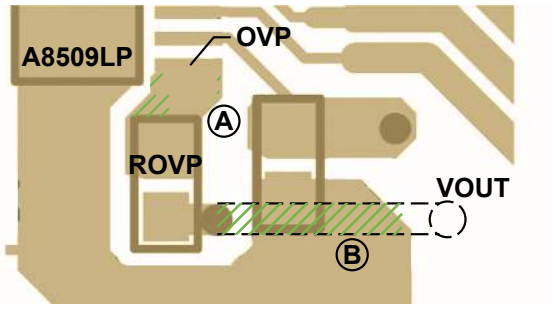
Pulse-By-Pulse Current Limit

Figure 21 illustrates the normal waveform for the current sense signal. The pulse-by-pulse current limit is designed to limit the current through the external MOSFET to prevent failure. When the V_{SENSEP} threshold is reached, the IC stops switching to allow the inductor current to fall. Operation of pulse-by-pulse current limiting is shown in figure 22.

Figure 21. Current sense signal (V_{SENSE}) during normal operation, showing large spikes that are filtered out by a blanking period to avoid false overcurrent tripping; R_{SENSE} = 10 mΩ; shows inductor current I_L (ch1, 1 A/div.), V_{SENSE}





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LED Open Detect

When any LED string opens, the boost control circuit increases the output voltage until it reaches the overvoltage protection level. The OVP event causes any LED string that is below regulation level to be disabled. After disabling the open string, the output voltage returns to normal operating voltage. An EN low signal will reset the LED string regulation lock.

Figure 25 shows a typical overvoltage condition when the output voltage is disconnected from the LED load. Figure 26 shows an extended view of the same situation. Figure 27 shows an OVP condition created by a single open LED string.

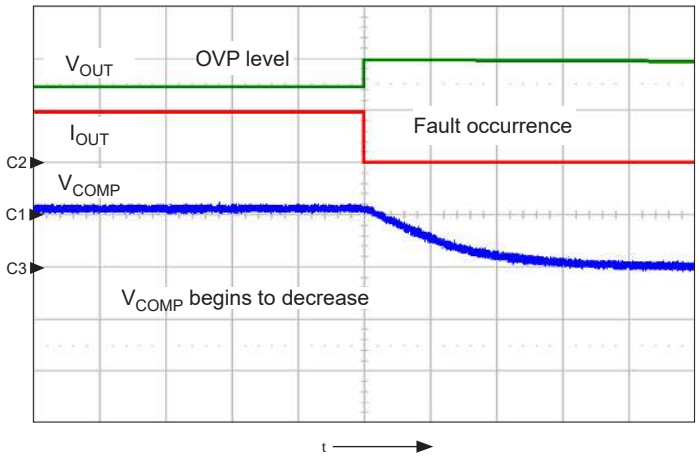

Figure 25. OVP operation with all LEDx pins open. V_{OUT} rises to the overvoltage level and stays there until the IC is shut down; shows V_{OUT} (ch1, 20 V/div.), I_{OUT} (ch2, 1 A/div.), and V_{COMP} (ch3, 2 V/div.), t = 2 ms/div.

Undervoltage Protection (UVP)

If the output voltage is shorted to ground the OVP pin will sense an undervoltage condition (UVP). When UVP is sensed, the IC sets the Fault flag low which, if used to interface to the output-disconnect switch, will shut off the P-FET device. Figure 28 is a schematic showing the input disconnect switch implementation.

Figure 28. Simplified schematic of an external disconnect switch implementation.

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The waveforms in figure 29 show the operation of the disconnect feature.

LED Short Detect

All LEDx pins are rated for 55 V, thus allowing LEDx pin-to-VOUT short protection in case of a connector short. Any LEDx pin that has a voltage exceeding V_{LEDSC} will be removed from operation. This is to prevent the IC dissipating too much power by having a large voltage present on the LEDx pins.

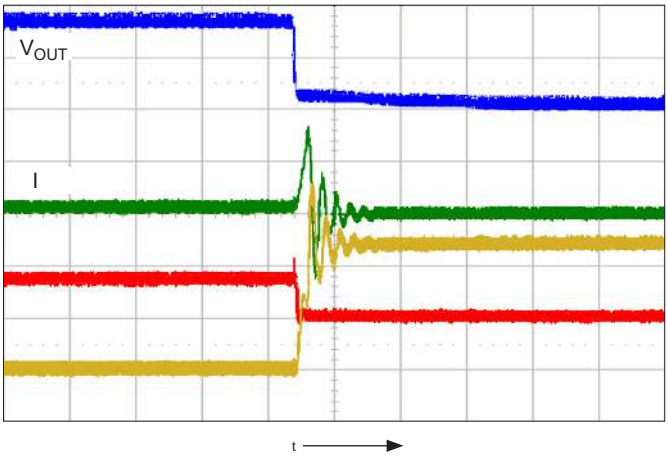

Figure 29. Input disconnect switch shutdown during an output short condition; shows V_{OUT} (ch1, 20 V/div.), I_{IN} (ch2, 10 A/div.), $\overline{FAULT}$ (ch3, 5 V/div.), and PMOS device V_{GATE} (ch4, 5 V/div.), t = 50 µs/div.

Input UVLO

When V_{IN} rises above the UVLO threshold ($V_{UVLO(th)}$), the A8509 is enabled. It is disabled when V_{IN} falls below $V_{UVLO(th)} - V_{UVLO(hys)}$ for more than 2 µs. This lag is to avoid shutdown because of momentary glitches in the power supply.

VDD and VDR

The VDD pin provides the regulated bias supply for the internal circuits. A capacitor with a value in the range 0.1 to 1 µF should be used to decouple the internal analog and digital circuitry.

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The VDR circuit provides power to the gate driver of the A8509. For VDR the decoupling capacitor value should fall in the range 0.47 to 1 µF. A 1 µF capacitor is recommended.

Shutdown

If the EN pin is pulled low, the IC will shut down immediately.

Fault Protection During Operation

The A8509 device constantly monitors the state of the system to determine if any fault conditions occur during normal operation. The response to a triggered fault condition is summarized in table 1. The possible fault conditions that the part can detect are:

- Open LED pin
- Shorted inductor with second level switch current protection
- VOUT short-to-ground
- ISET pin short-to-ground
- FSET pin short-to-ground
- Shorted LED
- Open Schottky diode
- Short Schottky diode protection with second level switch current protection
- Thermal shutdown (TSD)
- Overvoltage protection (OVP)

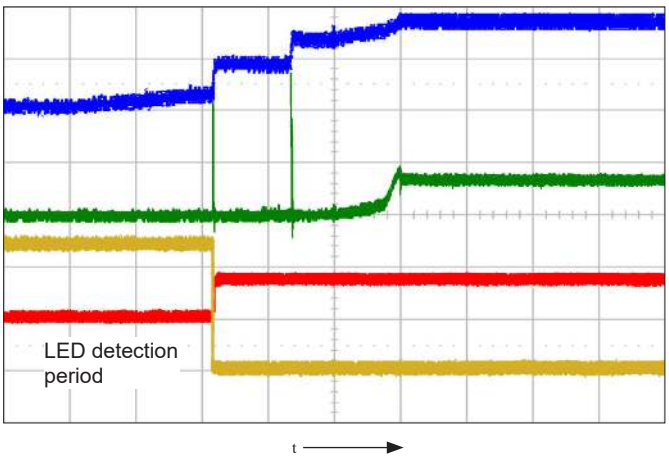

Figure 31. Input disconnect switch power-up: (1) V_{OUT} charges via 10 kΩ resistor, (2) I_{IN} current spike from charging COUT when the PMOS is enabled; shows V_{OUT} (ch1, 20 V/div.), I_{IN} (ch2, 2 A/div.), $\overline{FAULT}$ (ch3, 5 V/div.), and PMOS device V_{GATE} (ch4, 5 V/div.), t = 2 ms/div.

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Table 1. Fault Modes

Fault Name	Type	Active	Fault Flag Set	Description	Boost	Sink driver
Primary switch current protection (pulse-by-pulse current limit)	Auto-restart	Always	No	This fault condition is triggered by the pulse-by-pulse current limit when the SENSP pin voltage exceeds V_{SENSEP}.	Off for a single cycle	On
Secondary switch current limit	Latched	Always	Yes	When the current through the boost switch TEMC /hen the current through the boost switch TEMC /h		

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APPLICATION INFORMATION

Paralleling More Than One A8509

The A8509 can be paralleled together by using a single boost converter (master) to provide output power for up to a total of four A8509s (slaves). The MODE pin of each device must be tied to the VDD pin of the same device for proper mode selection. In this mode, the $\overline{\text{FAULT}}$ pins and the COMP pins become a bi-direction signal bus for the system to communicate.

At initial power-up, each IC will release a pull-down resistor on the COMP pin and start in soft-start mode. When 200 mV is detected on the COMP pin, the master will then switch to normal mode. Also, for proper operation all of the $\overline{\text{FAULT}}$ pins must be tied together to prevent the parallel ICs from powering-up into a shorted LEDx pin situation. While the $\overline{\text{FAULT}}$ pins are pulled low, the system will not proceed with start-up.

Below is a simple list of necessary connections for the master, to ensure proper parallel operation (refer to Application C in the Typical Applications section):

- COMP pin
- VOUT node
- $\overline{\text{FAULT}}$ pin

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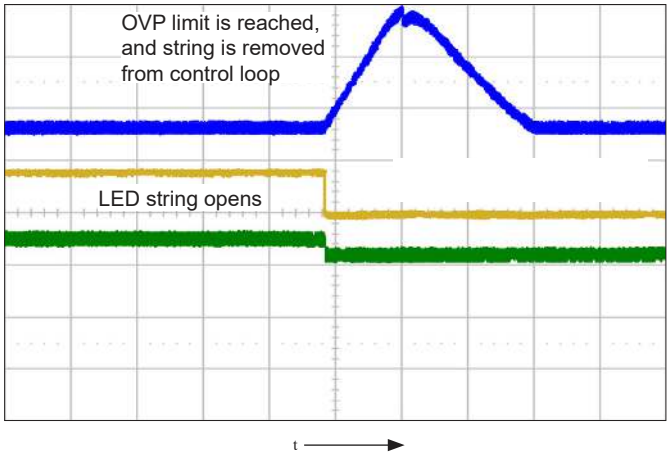

Figure 32. Proper OVP setting for the master and slave configuration. The master OVP is set higher than the slave, shows V_{OUT} (ch1, 2 V/div.), pin voltage V_{LEDx} (ch2, 2 V/div.), and I_{OUT} (ch3, 200 mA/div.), t = 2 ms/div.

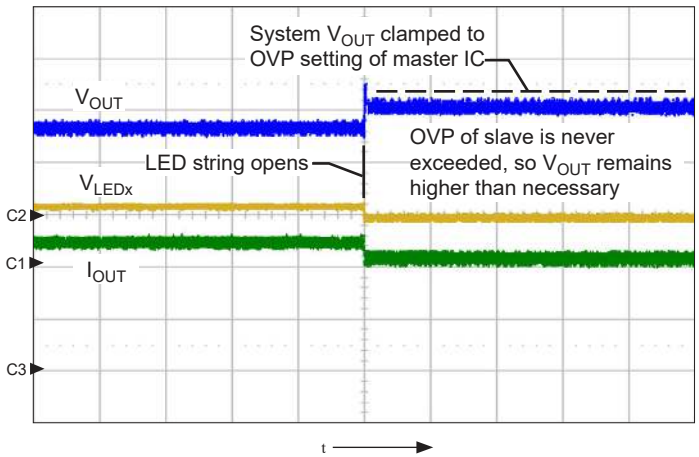

Figure 33. OVP on the master IC is set too low and the IC does not respond properly to the open LED condition on the slave IC; shows V_{OUT} (ch1, 10 V/div.), V_{LEDx} (ch2, 5 V/div.), and I_{OUT} (ch3, 200 mA/div.), t = 100 ms/div.

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Design Example

This section provides a method for selecting component values when designing an application using the A8509.

Assumptions: For the purposes of this example, the following are given as the application requirements:

- V_{IN}: 10 to 16 V
- Quantity of LED channels, #CHANNELS: 4
- Quantity of series LEDs per channel, #SERIESLEDS : 10
- LED current per channel, I_{LED}: 240 mA
- $V_{f(240)}$ at 240 mA: 3.2 V (max)
- f_{SW} : 600 kHz
- T_A(max): 65°C
- PWM dimming frequency: 200 Hz, 1% duty cycle

Step 1: Connect LEDs to pins LED1 through LED4.

Step 2: Determine the LED current by setting resistor R_{ISET}. To do so, apply equation 2:

$$\begin{aligned} R_{ISET} &= (1.000 / I_{LED}) \times 2320 \\ &= (1.000\ V / 0.240\ A) \times 2320 \\ &= 9.67\ k\Omega \end{aligned}$$

Choose a 9.53 kΩ resistor.

STEP 3: Determine the OVP resistor. The OVP resistor is connected between the OVP pin and the output voltage of the converter. The first step is to determine the maximum voltage based on the LED requirements. Then the regulation voltage of 650 mV should be added, along with 2 V for noise and regulation. Given the regulation voltage (V_{LED}) of the A8509 is 650 mV, the minimum required voltage can be determined as follows:

$$\begin{aligned} V_{OUT(OVP)} &= \#SERIESLEDS \times V_{f(240)} + V_{LED} + 2\ V \qquad (10) \\ &= 10 \times 3.2\ V + 0.650\ V + 2\ V \\ V_{OUT(OVP)(min)} &= 34.65\ V \end{aligned}$$

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The minimum input current can be calculated as:

$$I_{IN}(\min) = \frac{V_{OUT} \times I_{OUT}}{V_{IN}(\max) \times \eta} \quad (15)$$

$$= \frac{34.65\ V \times 0.960\ A}{16\ V \times 0.90}$$

$$= 2.31\ A$$

STEP 4c: Determining the inductor value. To assure that the inductor operates in continuous conduction mode, the value of inductor must be set such that $^1/_2$ of the inductor ripple current is not greater than the average minimum input current.

As a first pass, take I_{ripple} to be 30% of the maximum inductor current:

$$\Delta I_L = I_{IN}(\max) \times (I_{ripple} / I_{IN}(\max)) \quad (16)$$

$$= 3.72\ A \times 0.30$$

$$= 1.1\ A$$

Check to make sure that $^1/_2$ of the inductor ripple current is less than $I_{IN}(min)$:

$$I_{IN}(\min) > \frac{1}{2} \times \Delta I_L$$

$$2.31\ A > 0.56\ A$$

The inductor value can be calculated as:

$$L = \frac{V_{IN}(\min) \times \text{[illegible]} \times 20\ m}{\Delta I_L \times f_{SW}}$$

$$=$$

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The reverse voltage rating should be such that, during any operation condition, the voltage rating of the device is larger than the maximum output voltage. In this case, the maximum output voltage is $V_{OUT(OVP)}$.

The peak current through the diode is:

$$I_{d(peak)} = I_{IN}(max) + \Delta I_{Lused} \quad (23)$$

$$= 3.72\ A + 0.56\ A$$

$$= 4.28\ A$$

The other major component in determining the switching diode is the reverse current characteristic of the diode. This characteristic is especially important when PWM dimming is implemented. During PWM off-time the boost converter is not switching. This results in a slow bleeding-off of the output voltage due to leakage currents (I_R). I_R, or reverse current, can be a huge contributor especially at high temperatures. On the diode that was selected in this design, the current varies between 1 and 100 µA.

STEP 7: Choosing the output capacitors. The output capacitors must be chosen such that they can provide filtering for both the boost converter and for the PWM dimming function. The biggest factor that contributes to the size of the output capacitor is PWM dimming frequency and the PWM duty cycle. Another major contributor is leakage current (I_{LK}). This current is the combination of the OVP current sense as well as the reverse current of the switching diode.

In this design the PWM dimming frequency is 200 Hz and the minimum duty cycle is 1%. Typically, the voltage variation on the output during PWM dimming must be less than 250 mV (V_{COUT}) so that no audible hum can be heard:

$$= I_{LK}\times$$

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Typical Applications

Designator	Description	Part Number	Manufacturer
CDD	0.1 µF / 10 V	GRM2195C1H104JA01D	Murata
CDR	1 µF / 16 V	DRM188R61A105K	Murata
C_{IN}	4.7 µF / 50 V	GRM32ER71H475KA88L	Murata
COUT	10 µF / 50 V	GRM32ER71H475KA88L	Murata
CP	1 µF / 16V	GRM188R61A474K	Murata
CZ	DNP		
D1	60 V / 5 A Schottky	CMSH5-60-AMI	Central Semi
L1	10 µH / 5 A	74477110	Wurth Electronics
Q1	NMOS	FQD13N06LTM	Faichild
R1	100 kΩ		

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Typical Applications

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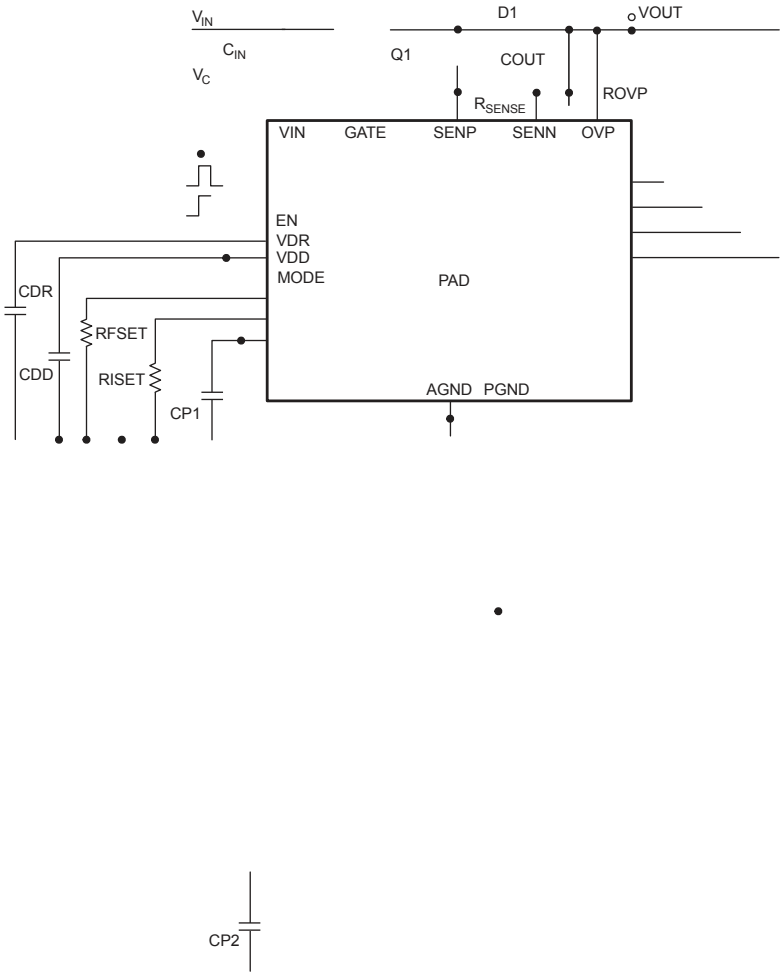

Application C. Parallel operation of two A8509s; overvoltage protection on master must be set higher than the OVP on the slave

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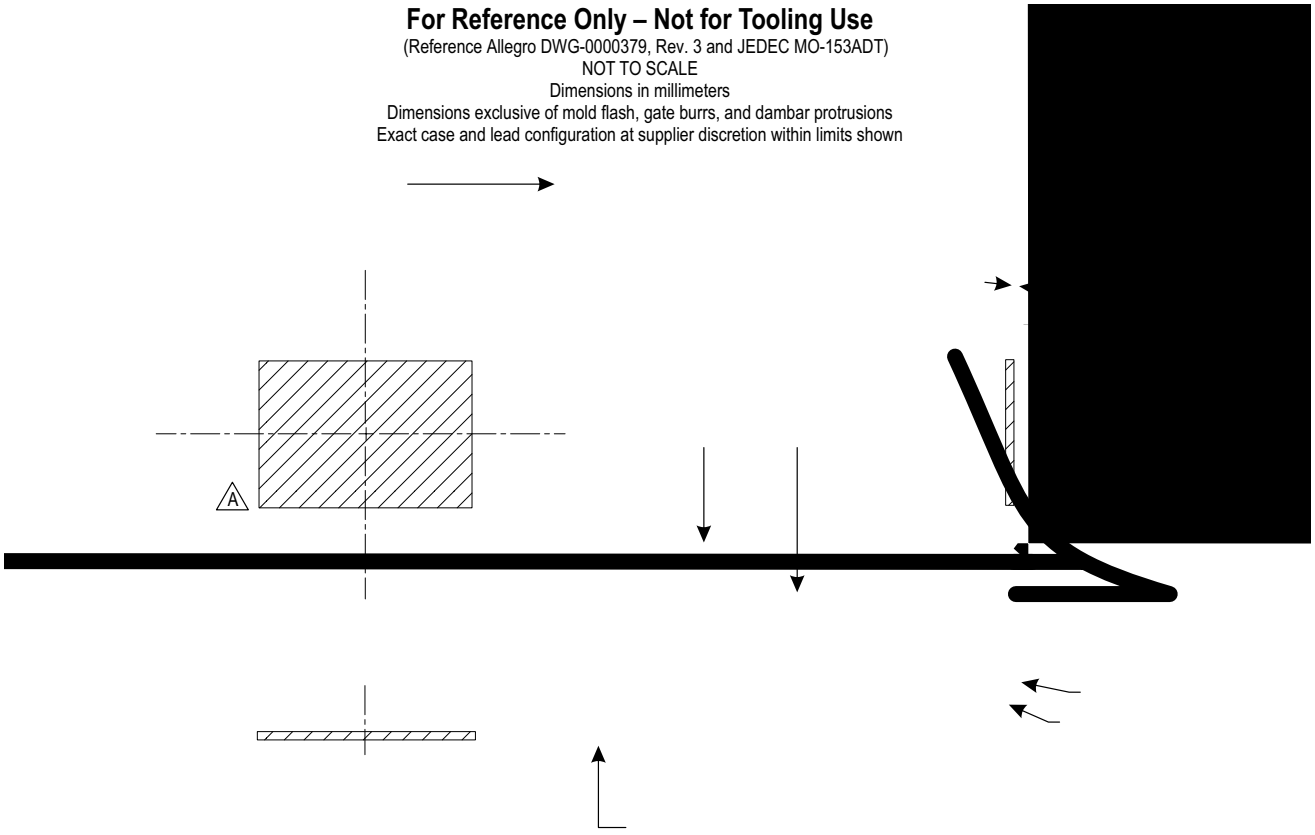
Package LP, 24-Pin TSSOP with Exposed Thermal Pad

For Reference Only – Not for Tooling Use
(Reference Allegro DWG-0000379, Rev. 3 and JEDEC MO-153ADT)
NOT TO SCALE
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



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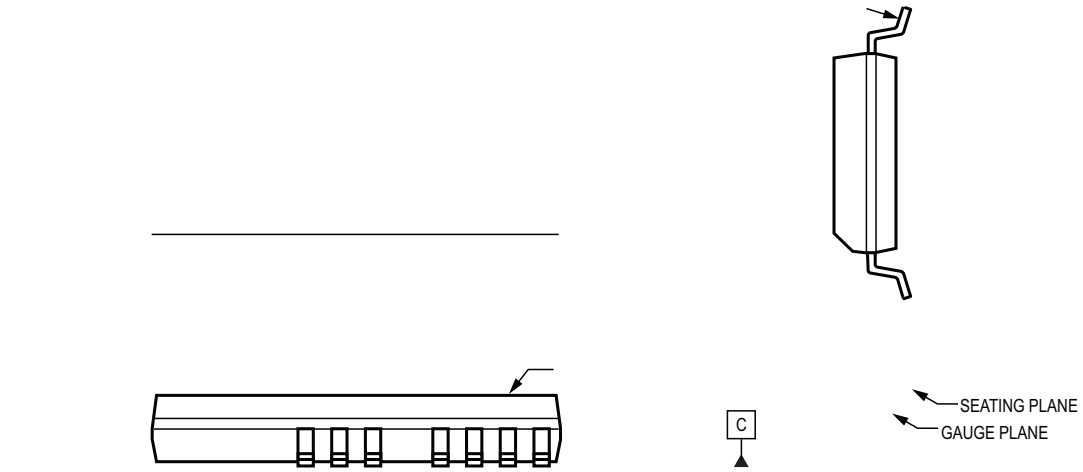
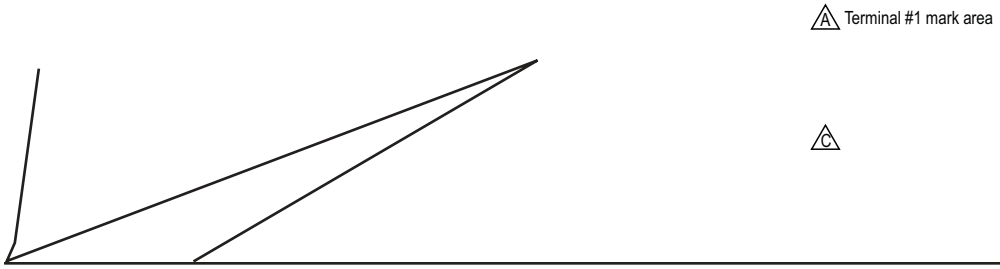
Package LB, 24-Pin SOICW with Exposed Thermal Pad

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000388, Rev. 1 and JEDEC MS-013AD)
NOT TO SCALE
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown
Internal configuration of fused pins is device-dependent





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Revision History

Number	Date	Description
–	June 19, 2011	Initial release
1	May 14, 2020	Minor editorial updates
2	May 11, 2022	Updated LP package drawing (page 27); added LB package drawing (page 28); minor editorial updates

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