



STL55NH3LL

N-channel 30 V, 0.0079 Ω , 15 A, PowerFLAT™ (6x5)
ultra low gate charge STripFET™ Power MOSFET

Features

Type	V _{DSS}	R _{DS(on)} max	I _D
STL55NH3LL	30 V	< 0.0088 Ω	15 A

- Improved die-to-footprint ratio
- Very low profile package (1mm max)
- Very low thermal resistance
- Very low gate charge
- Low threshold device

Application

- Switching applications

Description

This application specific Power MOSFET is the latest generation of STMicroelectronics unique "STripFET™" technology. The resulting transistor is optimized for low on-resistance and minimal gate charge. The chip scaled PowerFLAT™ package allows a significant board space saving, still boosting the performance.

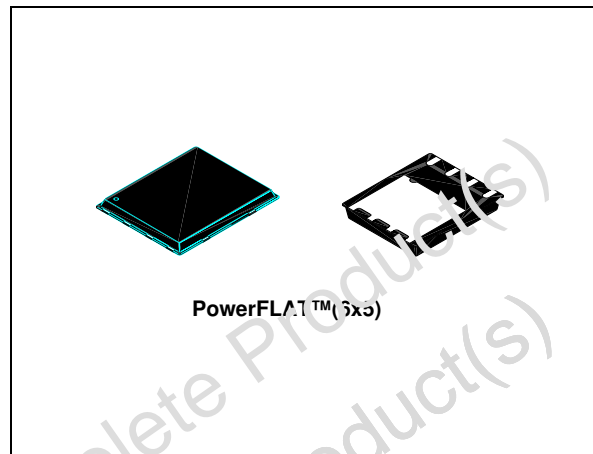


Figure 1. Internal schematic diagram

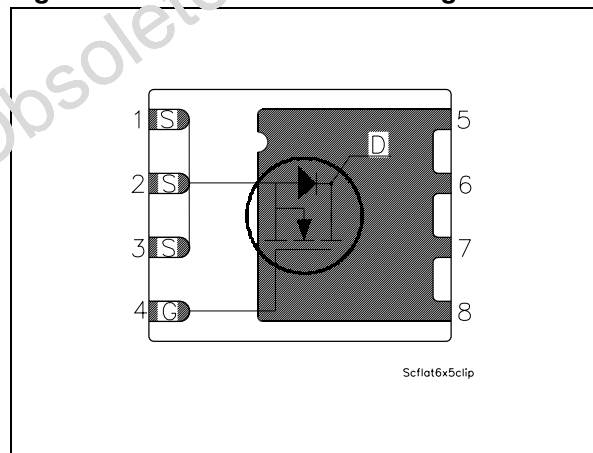


Table 1. Device summary

Order code	Marking	Package	Packaging
STL55NH3LL	L55NH3LL	PowerFLAT™ (6x5)	Tape and reel

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Obsolete Product(s) - Obsolete Product(s)
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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	30	V
$V_{GS}^{(1)}$	Gate-source voltage	± 16	V
$V_{GS}^{(2)}$	Gate-source voltage	± 18	V
$I_D^{(3)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	55	A
$I_D^{(3)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	36	A
$I_{DM}^{(4)}$	Drain current (pulsed)	60	A
$I_D^{(5)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	15	A
$I_D^{(5)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	9.4	A
$P_{TOT}^{(5)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	4	W
$P_{TOT}^{(3)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	60	W
	Derating factor	0.03	W/°C
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150	°C

1. Continuous mode
2. Guaranteed for test time $\leq 15\text{ ms}$
3. The value is rated according R_{th-jc}
4. Pulse width limited by safe operating area
5. The value is rated according $R_{thj-pcb}$

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case (drain)	2.08	°C/W
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-ambient	31.3	°C/W

1. When mounted on FR-4 board of 1inch², 2oz Cu, $t < 10\text{ sec}$

Table 4. Avalanche data

Symbol	Parameter	Value	Unit
I_{AV}	Not-repetitive avalanche current (pulse width limited by $T_J\text{ Max}$)	7.5	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$, $I_D = I_{AV}$, $V_{DD} = 24\text{ V}$, $L = 6\text{ mH}$)	150	mJ

2 Electrical characteristics

($T_{CASE}=25^{\circ}C$ unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250 \mu A, V_{GS} = 0$	30			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{max rating},$ $V_{DS} = \text{max rating @ } 125^{\circ}C$			1 10	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 16 V$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	1		2.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10 V, I_D = 7.5 A$ $V_{GS} = 8 V, I_D = 7.5 A$ $V_{GS} = 4.5 V, I_D = 7.5 A$		0.0079 0.0079 0.009	0.0088 0.0088 0.0115	Ω Ω Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25 V, f = 1 \text{ MHz},$ $V_{GS} = 0$		965		pF
C_{oss}	Output capacitance			285		pF
C_{rss}	Reverse transfer capacitance			38		pF
Q_c	Total gate charge	$V_{DD} = 15 V, I_D = 15 A$		9	12	nC
Q_{gs}	Gate-source charge	$V_{GS} = 4.5 V$		3.7		nC
Q_{gd}	Gate-drain charge	(see Figure 16)		3		nC
Q_{gs1}	Pre V_{th} gate-to-source charge	$V_{DD} = 15 V, I_D = 15 A$		2.5		nC
Q_{gs2}	Post V_{th} gate-to-source charge	$V_{GS} = 4.5 V$		1.2		nC
R_G	Gate input resistance	$f = 1 \text{ MHz}$ Gate DC Bias = 0 Test signal level = 20 mV open drain	0.5	1.5	2.5	Ω

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD}=15\text{ V}$, $I_D=7.5\text{ A}$, $R_G=4.7\ \Omega$, $V_{GS}=4.5\text{ V}$ (see Figure 18)		15		ns
t_r	Rise time			32		ns
$t_{d(off)}$	Turn-off delay time			18		ns
t_f	Fall time			8.5		ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current				5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				60	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=15\text{ A}$, $V_{GS}=0$			1.3	V
t_{rr}	Reverse recovery time	$I_{SD}=15\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD}=20\text{ V}$, $T_J=150\text{ }^\circ\text{C}$ (see Figure 17)		24		ns
Q_{rr}	Reverse recovery charge			17.4		nC
I_{RRM}	Reverse recovery current			1.45		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

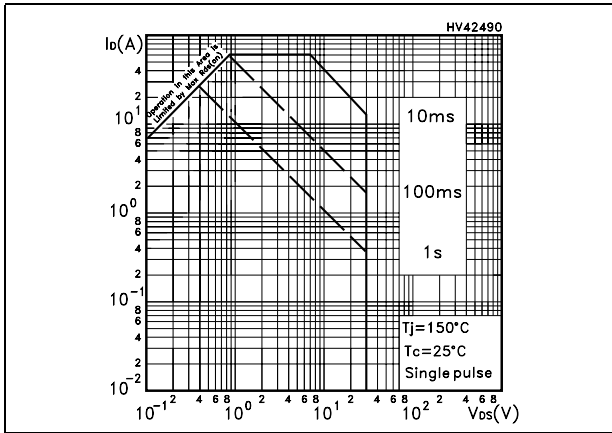


Figure 3. Thermal impedance

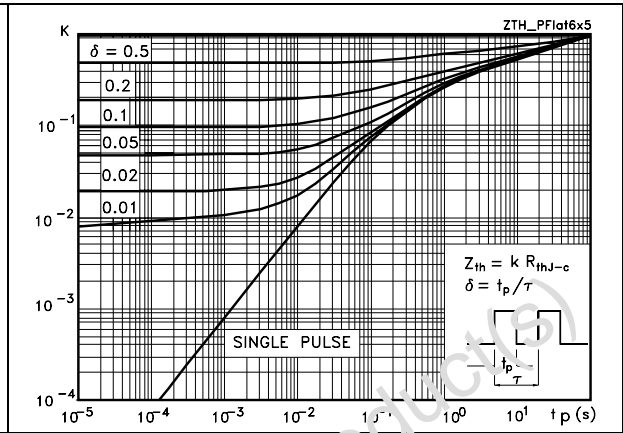


Figure 4. Output characteristics

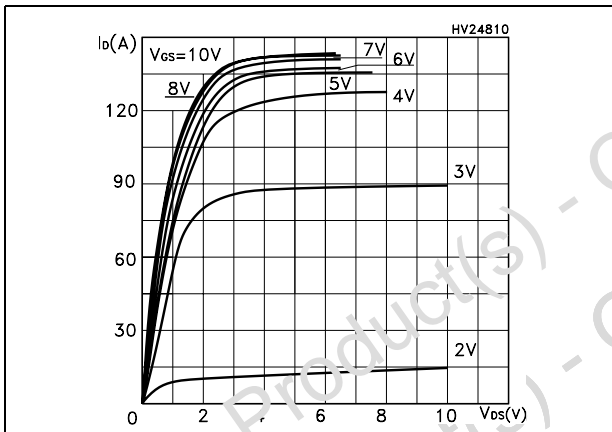


Figure 5. Transfer characteristics

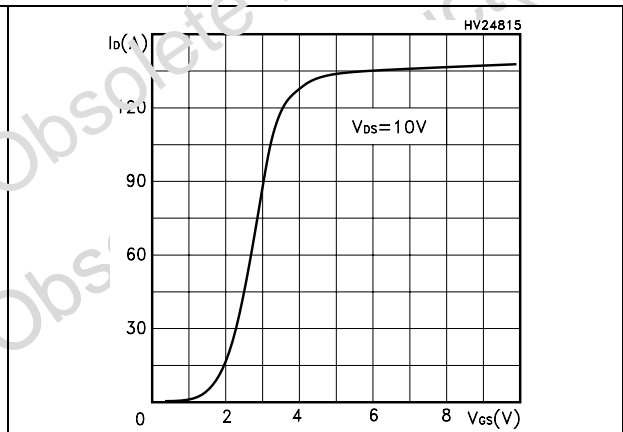


Figure 6. Normalized $B_{V_{DS}}$ vs temperature

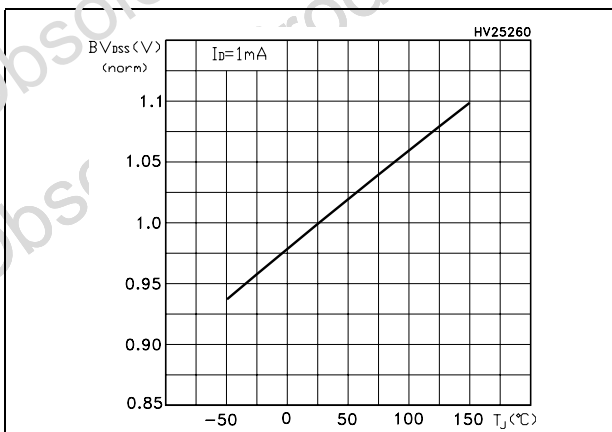


Figure 7. Static drain-source on resistance

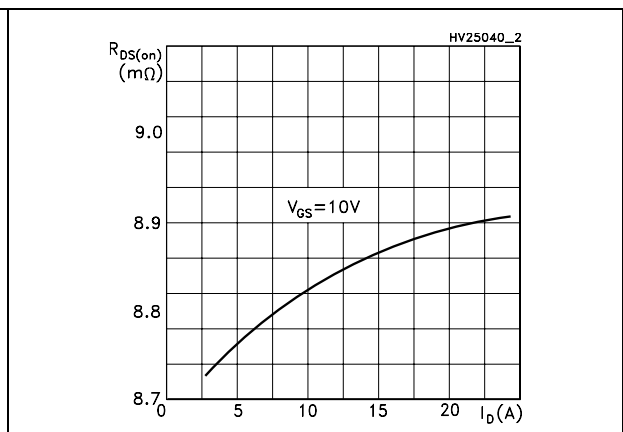


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

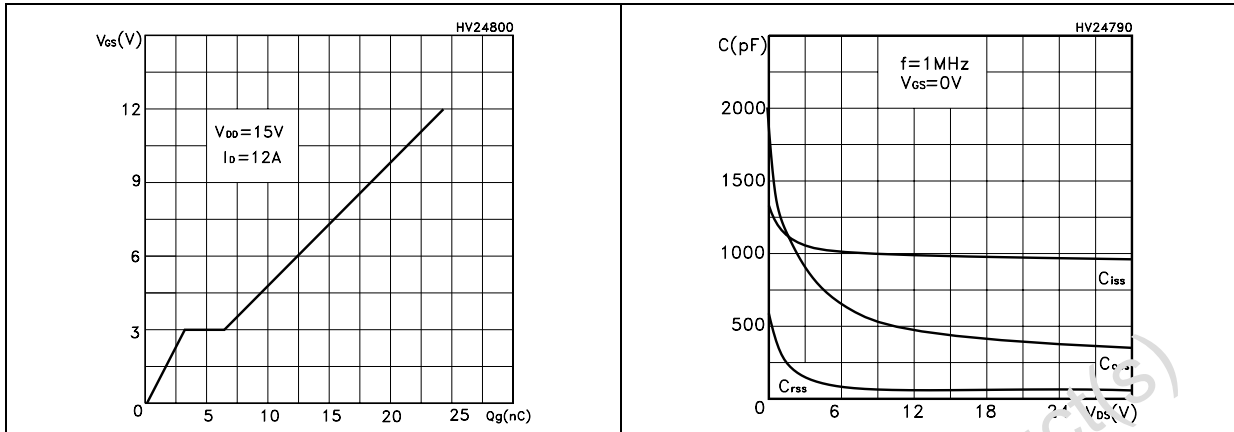


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature

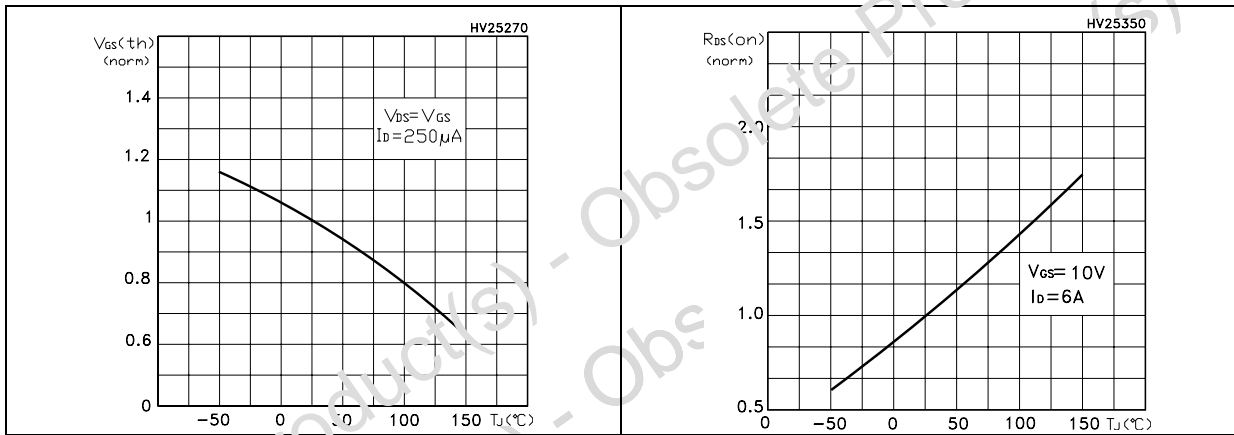


Figure 12. Source-drain diode forward characteristics Figure 13. Avalanche energy vs starting t_j

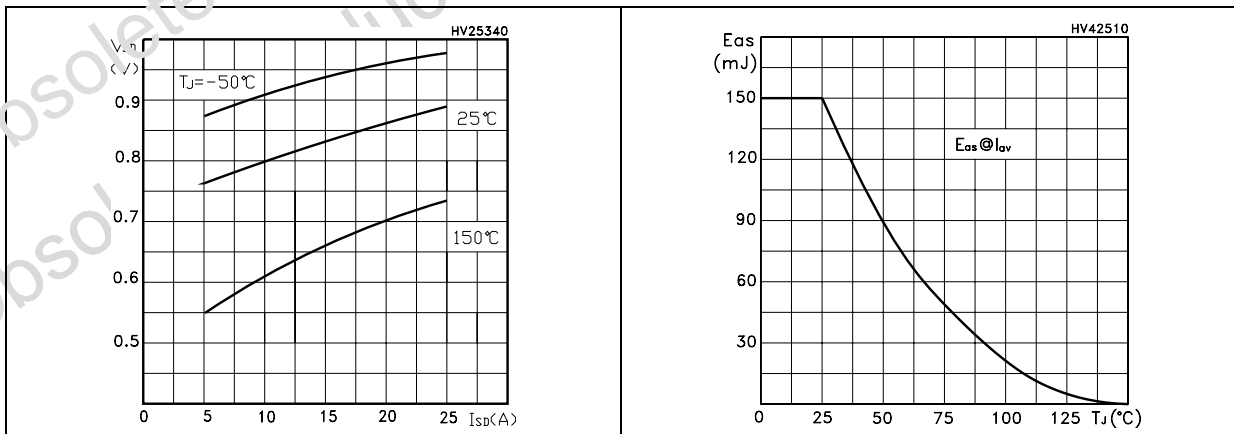
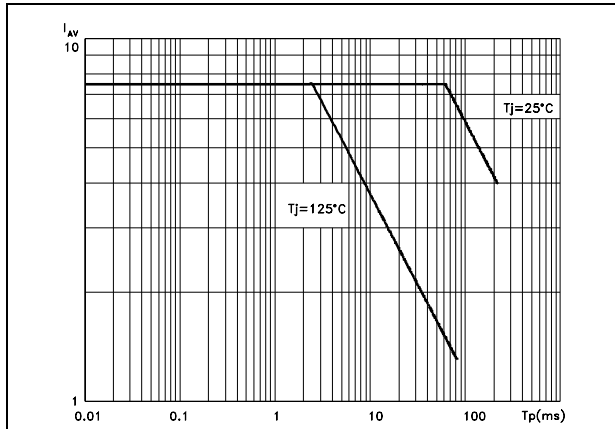


Figure 14. Allowable I_{AV} vs time in avalanche



The previous curve gives the single pulse safe operating area for unclamped inductive loads, under the following conditions:

$$P_{D(AVE)} = 0.5 \cdot (1.3 \cdot B_{VDSS} \cdot I_{AV})$$

$$E_{AS(AR)} = P_{D(AVE)} \cdot t_{AV}$$

Where:

I_{AV} is the allowable current in avalanche

$P_{D(AVE)}$ is the average power dissipation in avalanche (single pulse)

t_{AV} is the time in avalanche

3 Test circuits

Figure 15. Switching times test circuit for resistive load

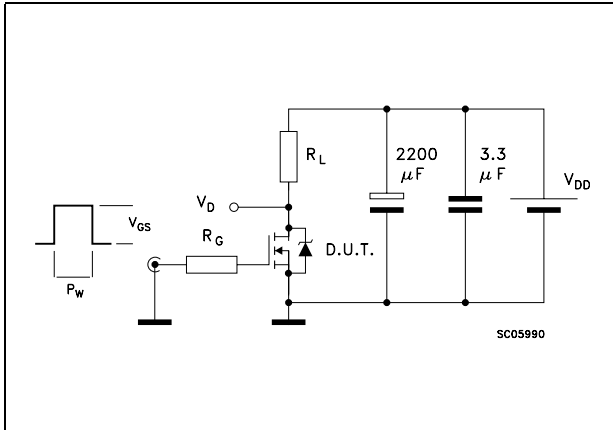


Figure 16. Gate charge test circuit

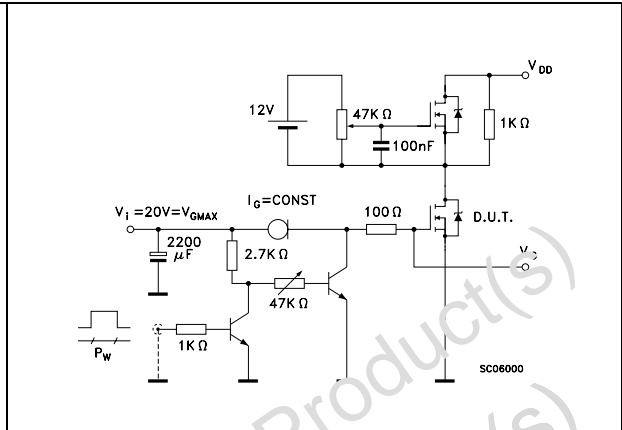


Figure 17. Test circuit for inductive load switching and diode recovery times

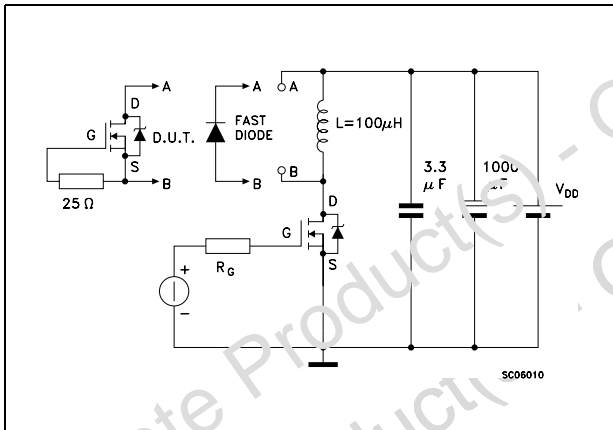


Figure 18. Unclamped inductive load test circuit

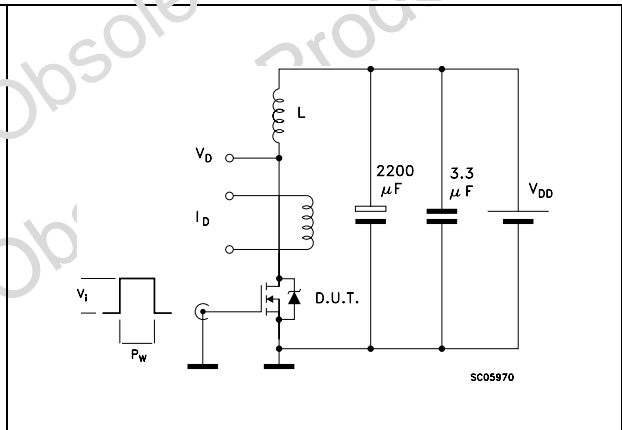


Figure 19. Unclamped inductive waveform

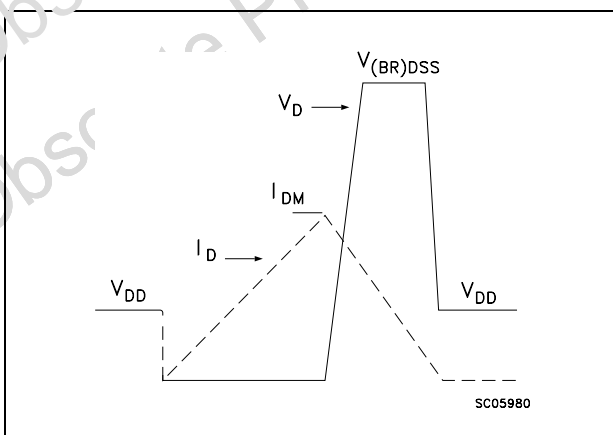


Figure 20. Switching time waveform

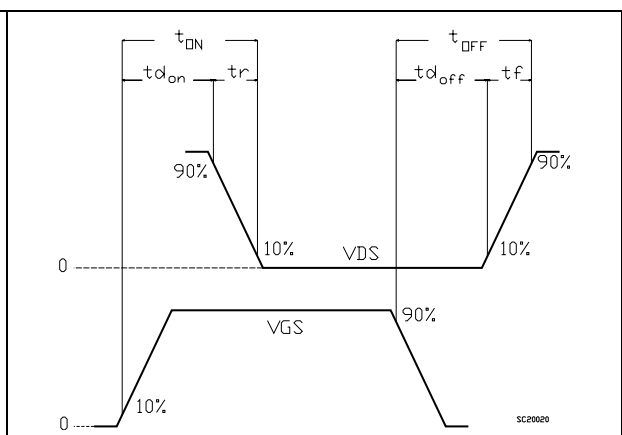
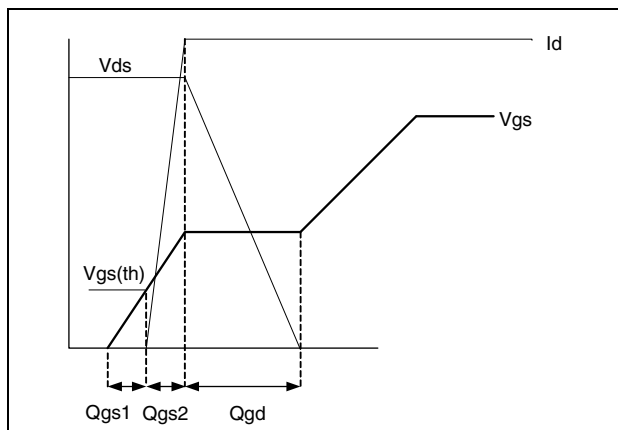


Figure 21. Gate charge waveform



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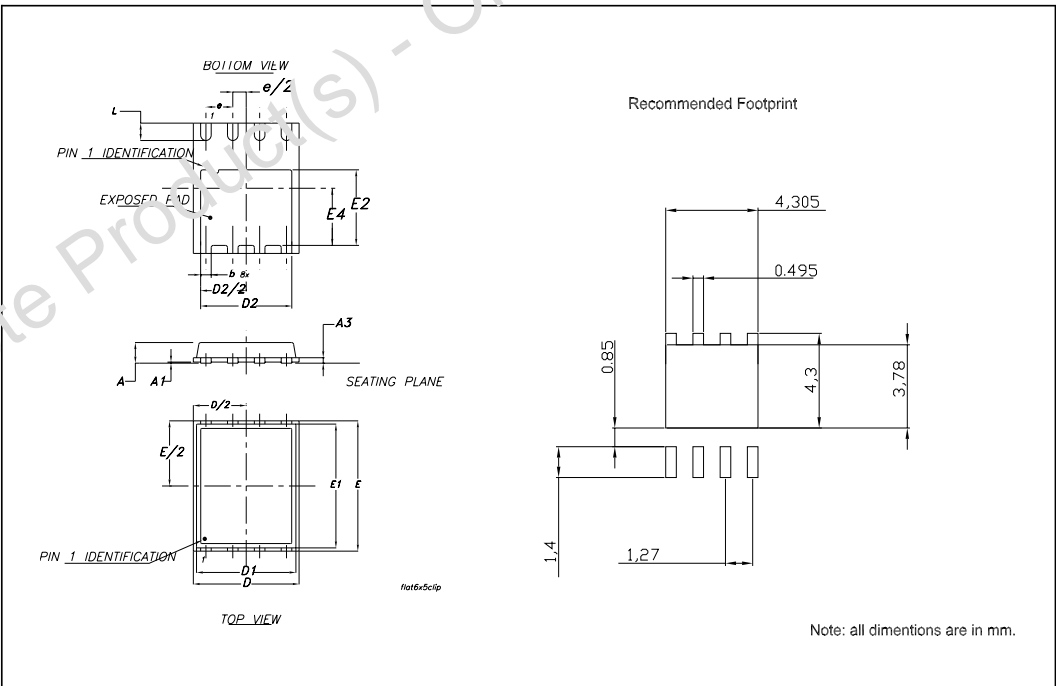
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

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PowerFLAT™ (6x5) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	0.80	0.83	0.93	0.031	0.032	0.036
A1		0.02	0.05		0.0007	0.0019
A3		0.20			0.007	
b	0.35	0.40	0.47	0.013	0.015	0.018
D		5.00			0.196	
D1		4.75			0.187	
D2	4.15	4.20	4.25	0.163	0.165	0.167
E		6.00			0.236	
E1		5.75			0.227	
E2	3.43	3.48	3.53	0.135	0.137	0.139
E4	2.58	2.63	2.68	0.103	0.105	0.105
e		1.27			0.050	
L	0.70	0.80	0.90	0.027	0.031	0.035



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
18-Mar-2008	1	First release.
05-May-2008	2	Corrected Table 1: Device summary
07-May-2008	3	Update Figure 6: Normalized B_{VDSS} vs temperature

Obsolete Product(s) - Obsolete Product(s)
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