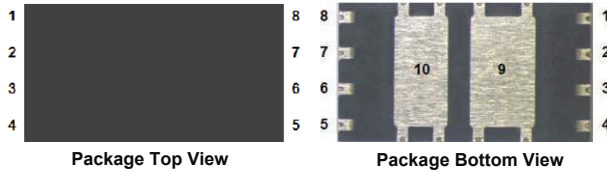


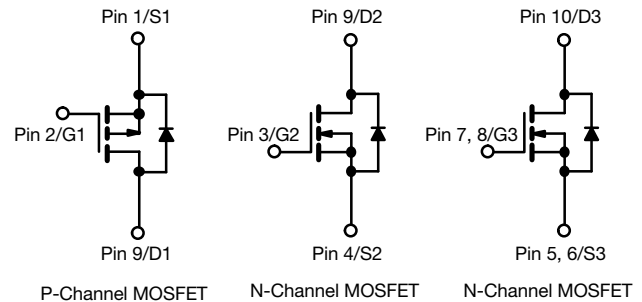
40 V N- and P-Channel Common Drain MOSFET Pair and 200 V N-Channel MOSFET


FEATURES

- Optimized triple die package
- TrenchFET® power MOSFET
- 100 % R_g and UIS tested
- AEC-Q101 qualified
- Material categorization:
for definitions of compliance please see
www.vishay.com/doc?99912



PRODUCT SUMMARY			
	N-CH 2	P-CH 1	N-CH 3
V _{DS} (V)	40	-40	200
R _{DS(on)} (Ω) at V _{GS} = 10 V	0.0092	0.030	0.060
R _{DS(on)} (Ω) at V _{GS} = 4.5 V	0.0135	0.048	-
I _D (A)	30	-30	20
Q _g typ. (nC)	25.5	30.2	14
Configuration	N- and p-pair		
Package	Triple die		



ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	N-CH 2	P-CH 1	N-CH 3	UNIT	
Drain-source voltage	V _{DS}	40	-40	200	V	
Gate-source voltage	V _{GS}	20	20	20		
Continuous drain current (T _J = 175 °C)	I _D	T _C = 25 °C	30	-30	20	A
		T _C = 125 °C	30	-30	11	
Pulsed drain current (t = 300 μs)	I _{DM}	120	-120	60		
Continuous source drain current	I _S	T _C = 25 °C	30	-30	20	
		T _C = 125 °C	30	-30	11.4	
Single pulse avalanche current	I _{AS}	26.5	-25	20		
Single pulse avalanche energy	E _{AS}	35	31	20	mJ	
Maximum power dissipation	P _D	T _C = 25 °C	48	48	60	W
		T _C = 125 °C	16	16	20	
Operating junction and storage temperature range	T _J , T _{stg}	-55 to +175			°C	

THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	N-CH 2	P-CH 1	N-CH 3	UNIT
Junction-to-case (drain)	R _{thJC}	2.6	2.6	2.4	°C/W

Notes

- Package limited, T_C = 25 °C
- Surface mounted on 1" x 1" FR4 board
- t = 10 s
- See solder profile (www.vishay.com/doc?73257). The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components



SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	N-Ch 2	40	-	-	V
		$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	P-Ch 1	-40	-	-	
		$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	N-Ch 3	200	-	-	
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	N-Ch 2	1.5	2.0	2.5	V
		$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	P-Ch 1	1.5	2.0	2.5	
		$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	N-Ch 3	2.5	3.0	3.5	
Gate-source leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$	N-Ch 2	-	-	± 100	nA
			P-Ch 1	-	-	± 100	
			N-Ch 3	-	-	± 100	
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}$	N-Ch 2	-	-	1	mA
		$V_{DS} = -40\text{ V}, V_{GS} = 0\text{ V}$	P-Ch 1	-	-	-1	
		$V_{DS} = 200\text{ V}, V_{GS} = 0\text{ V}$	N-Ch 3	-	-	1	
		$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$	N-Ch 2	-	-	50	
		$V_{DS} = -40\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$	P-Ch 1	-	-	-50	
		$V_{DS} = 200\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$	N-Ch 3	-	-	50	
On-state drain current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	N-Ch 2	25	-	-	A
		$V_{DS} \leq 5\text{ V}, V_{GS} = -10\text{ V}$	P-Ch 1	-25	-	-	
		$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	N-Ch 3	20	-	-	
Drain-source on-state resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 9.8\text{ A}$	N-Ch 2	-	0.0077	0.0092	Ω
		$V_{GS} = -10\text{ V}, I_D = -6\text{ A}$	P-Ch 1	-	0.0220	0.0300	
		$V_{GS} = 10\text{ V}, I_D = 5\text{ A}$	N-Ch 3	-	0.0500	0.0600	
		$V_{GS} = 4.5\text{ V}, I_D = 8.9\text{ A}$	N-Ch 2	-	0.0940	0.0135	
		$V_{GS} = 4.5\text{ V}, I_D = -4.7\text{ A}$	P-Ch 1	-	0.0360	0.0480	
Forward transconductance ^a	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 9.8\text{ A}$	N-Ch 2	-	65	-	S
		$V_{DS} = -15\text{ V}, I_D = 6\text{ A}$	P-Ch 1	-	16	-	
		$V_{DS} = 15\text{ V}, I_D = 19\text{ A}$	N-Ch 3	-	19	-	
Dynamic ^b							
Input capacitance	C_{iss}	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	N-Ch 2	-	1474	-	pF
		$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	P-Ch 1	-	1302	-	
		$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	N-Ch 3	-	1450	-	
Output capacitance	C_{oss}	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	N-Ch 2	-	218	-	pF
		$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	P-Ch 1	-	222	-	
		$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	N-Ch 3	-	116	-	
Reverse transfer capacitance	C_{rss}	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	N-Ch 2	-	89	-	pF
		$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	P-Ch 1	-	154	-	
		$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	N-Ch 3	-	9	-	
Total gate charge	Q_g	$V_{DS} = 20\text{ V}, V_{GS} = 10\text{ V}, I_D = 10\text{ A}$	N-Ch 2	-	23	-	nC
		$V_{DS} = -20\text{ V}, V_{GS} = -10\text{ V}, I_D = -10\text{ A}$	P-Ch 1	-	30.2	-	
		$V_{DS} = 100\text{ V}, V_{GS} = 10\text{ V}, I_D = 10\text{ A}$	N-Ch 3	-	14	-	
Gate-source charge	Q_{gs}	$V_{DS} = 20\text{ V}, V_{GS} = 10\text{ V}, I_D = 10\text{ A}$	N-Ch 2	-	4.4	-	nC
		$V_{DS} = -20\text{ V}, V_{GS} = -10\text{ V}, I_D = -10\text{ A}$	P-Ch 1	-	4.1	-	
		$V_{DS} = 100\text{ V}, V_{GS} = 10\text{ V}, I_D = 10\text{ A}$	N-Ch 3	-	4.4	-	
Gate-drain charge	Q_{gd}	$V_{DS} = 20\text{ V}, V_{GS} = 10\text{ V}, I_D = 10\text{ A}$	N-Ch 2	-	4.3	-	nC
		$V_{DS} = -20\text{ V}, V_{GS} = -10\text{ V}, I_D = -10\text{ A}$	P-Ch 1	-	7.4	-	
		$V_{DS} = 100\text{ V}, V_{GS} = 10\text{ V}, I_D = 10\text{ A}$	N-Ch 3	-	5	-	
Gate resistance	R_g	$f = 1\text{ MHz}$	N-Ch 2	-	-	2.1	Ω
			P-Ch 1	-	-	9.5	
			N-Ch 3	-	-	2.9	



SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Dynamic ^b							
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 20\text{ V}, R_L = 2\ \Omega$ $I_D = 10\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\ \Omega$	N-Ch 2	-	8	-	ns
		$V_{DD} = -20\text{ V}, R_L = 2\ \Omega$ $I_D = -10\text{ A}, V_{GEN} = -10\text{ V}, R_g = 1\ \Omega$	P-Ch 1	-	7	-	
		$V_{DD} = 100\text{ V}, R_L = 5.2\ \Omega$ $I_D = 10\text{ A}, V_{GEN} = 10\text{ V}, R_g = 2.5\ \Omega$	N-Ch 3	-	10	-	
Rise time	t_r	$V_{DD} = 20\text{ V}, R_L = 2\ \Omega$ $I_D = 10\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\ \Omega$	N-Ch 2	-	12	-	
		$V_{DD} = -20\text{ V}, R_L = 2\ \Omega$ $I_D = -10\text{ A}, V_{GEN} = -10\text{ V}, R_g = 1\ \Omega$	P-Ch 1	-	9	-	
		$V_{DD} = 100\text{ V}, R_L = 5.2\ \Omega$ $I_D = 10\text{ A}, V_{GEN} = 10\text{ V}, R_g = 2.5\ \Omega$	N-Ch 3	-	3	-	
Turn-off delay time	$t_{d(off)}$	$V_{DD} = 20\text{ V}, R_L = 2\ \Omega$ $I_D = 10\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\ \Omega$	N-Ch 2	-	22	-	
		$V_{DD} = -20\text{ V}, R_L = 2\ \Omega$ $I_D = -10\text{ A}, V_{GEN} = -10\text{ V}, R_g = 1\ \Omega$	P-Ch 1	-	43	-	
		$V_{DD} = 100\text{ V}, R_L = 5.2\ \Omega$ $I_D = 10\text{ A}, V_{GEN} = 10\text{ V}, R_g = 2.5\ \Omega$	N-Ch 3	-	15	-	
Fall time	t_f	$V_{DD} = 20\text{ V}, R_L = 2\ \Omega$ $I_D = 10\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\ \Omega$	N-Ch 2	-	10	-	
		$V_{DD} = -20\text{ V}, R_L = 2\ \Omega$ $I_D = -10\text{ A}, V_{GEN} = -10\text{ V}, R_g = 1\ \Omega$	P-Ch 1	-	19	-	
		$V_{DD} = 100\text{ V}, R_L = 5.2\ \Omega$ $I_D = 10\text{ A}, V_{GEN} = 10\text{ V}, R_g = 2.5\ \Omega$	N-Ch 3	-	2	-	
Source-Drain Diode Ratings and Characteristics							
Pulsed current	I_{SM}		N-Ch 2	-	-	120	A
			P-Ch 1	-	-	-120	
			N-Ch 3	-	-	50	
Forward voltage	V_{SD}	$I_S = 6.5\text{ A}, V_{GS} = 0\text{ V}$	N-Ch 2	-	0.79	-	V
		$I_S = -3.4\text{ A}, V_{GS} = 0\text{ V}$	P-Ch 1	-	-0.78	-	
		$I_S = 19\text{ A}, V_{GS} = 0\text{ V}$	N-Ch 3	-	0.9	-	

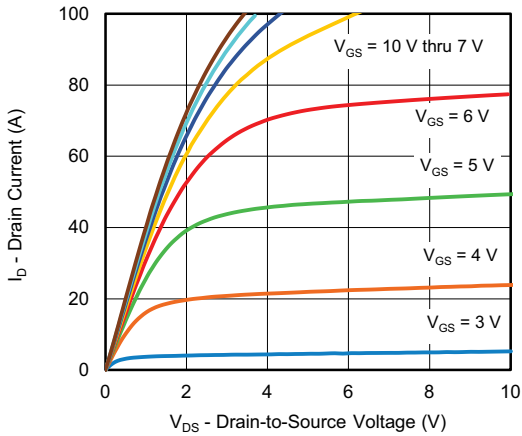
Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\ \%$
- b. Guaranteed by design, not subject to production testing

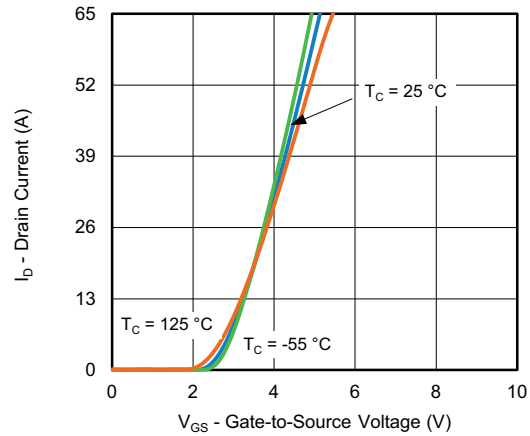
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



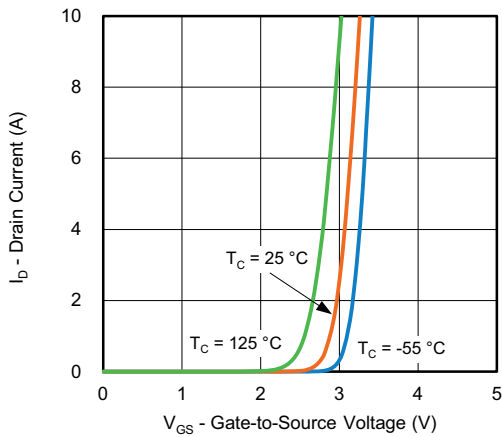
CHANNEL-1 TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



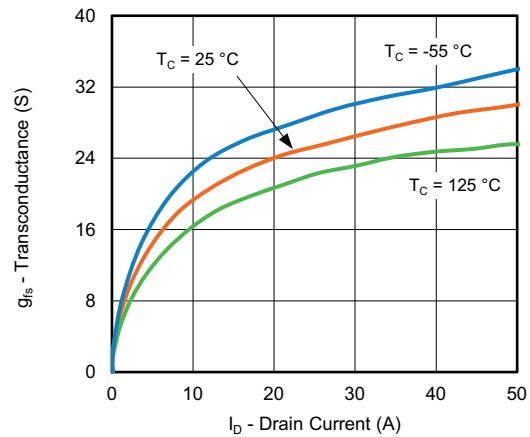
Output Characteristics



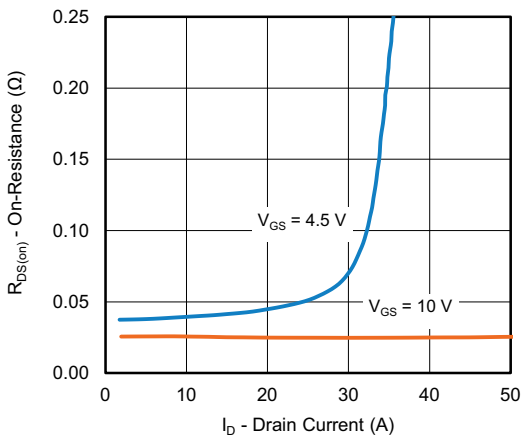
Transfer Characteristics



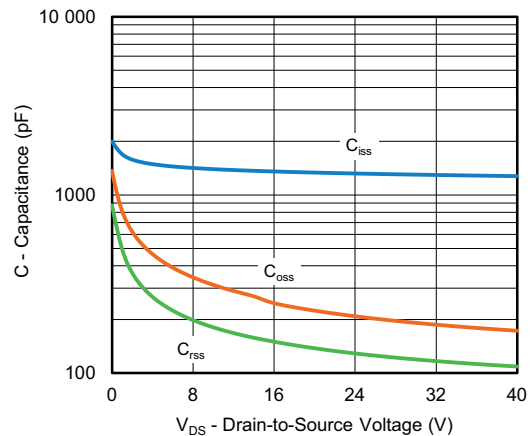
Transfer Characteristics



Transconductance



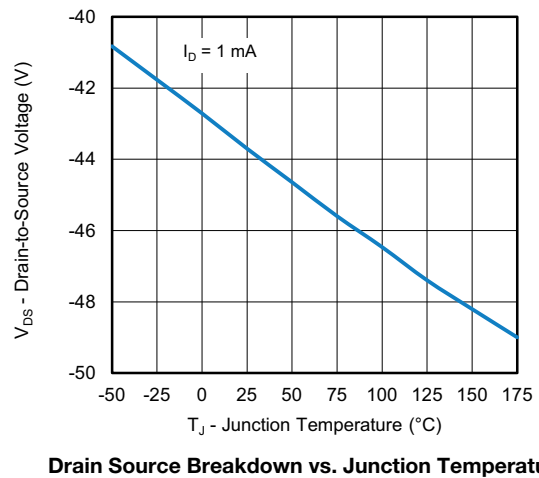
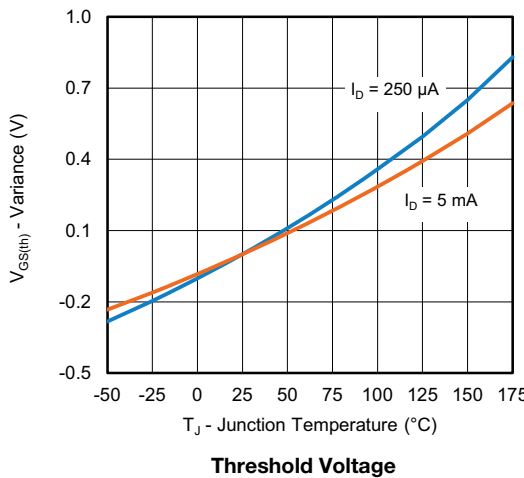
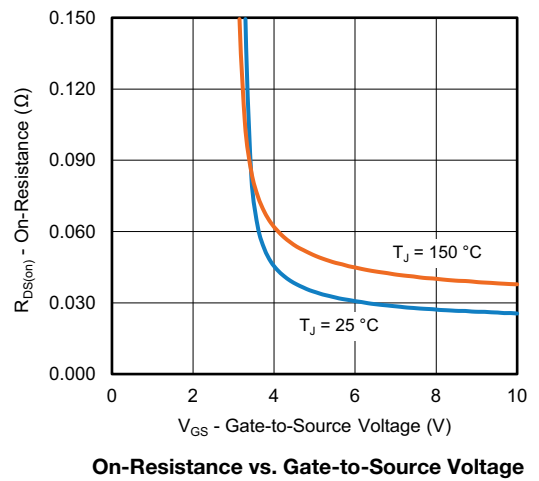
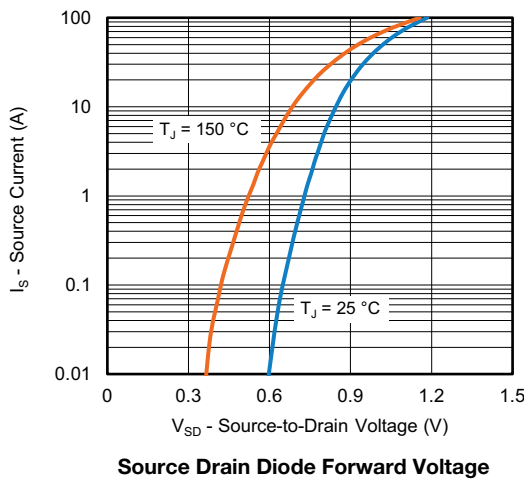
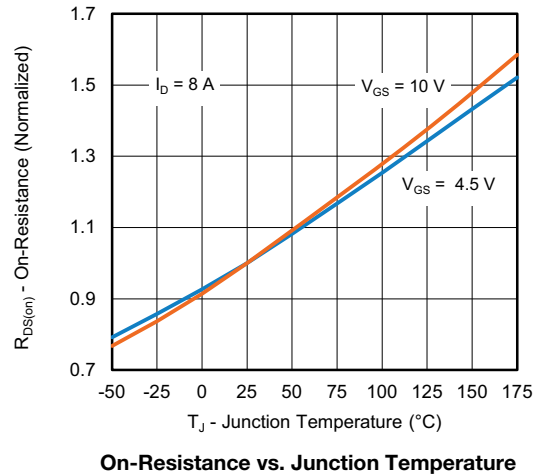
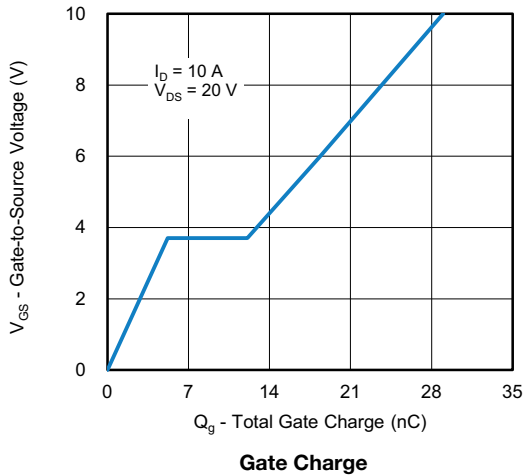
On-Resistance vs. Drain Current



Capacitance

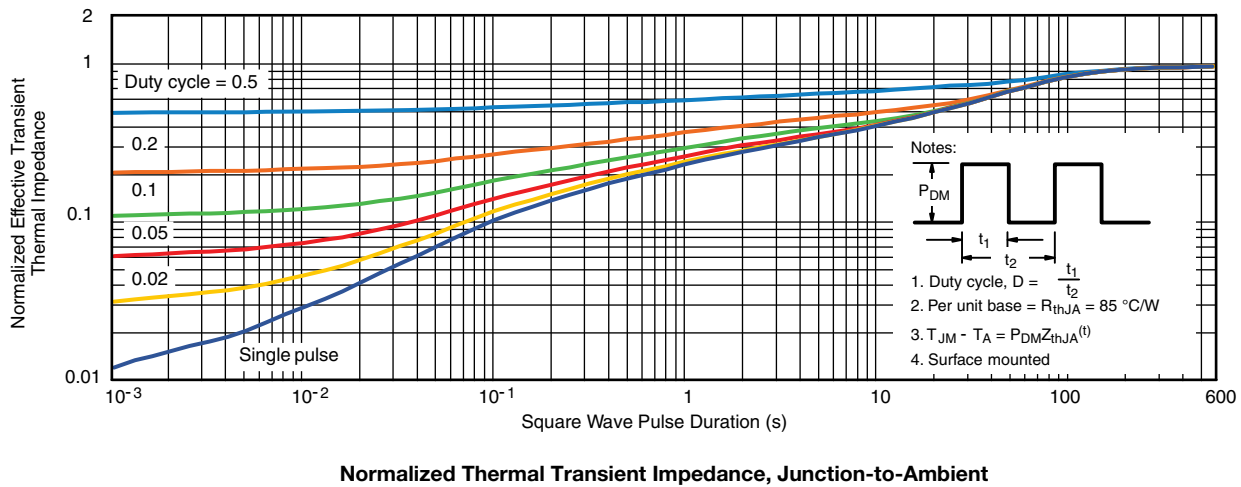
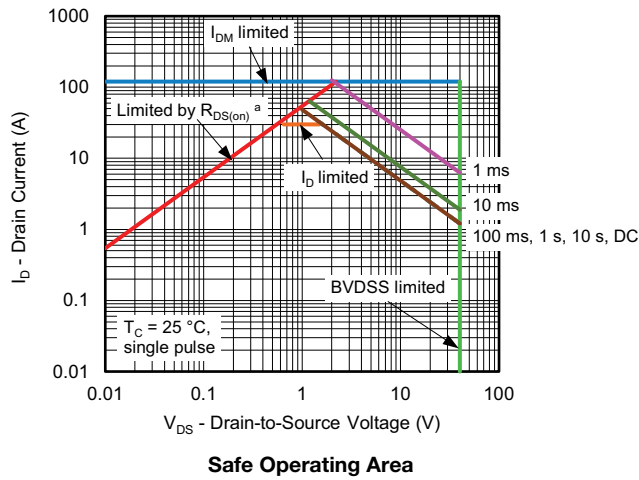


CHANNEL-1 TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)





CHANNEL-1 TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)

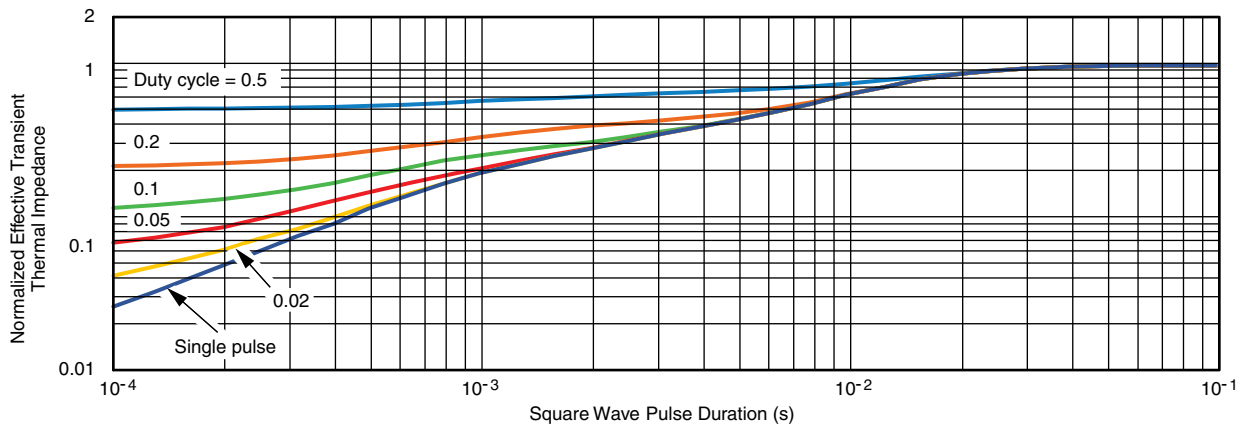


Note

a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified



CHANNEL-1 TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



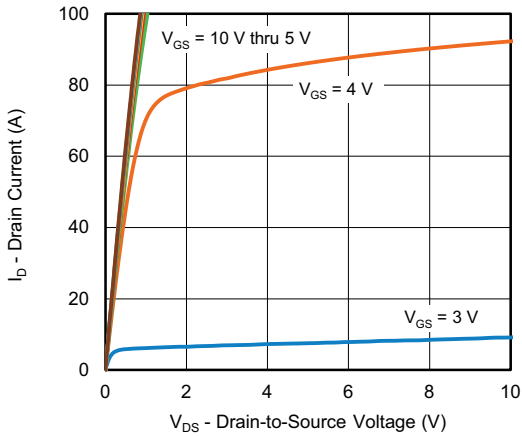
Normalized Thermal Transient Impedance, Junction-to-Case

Note

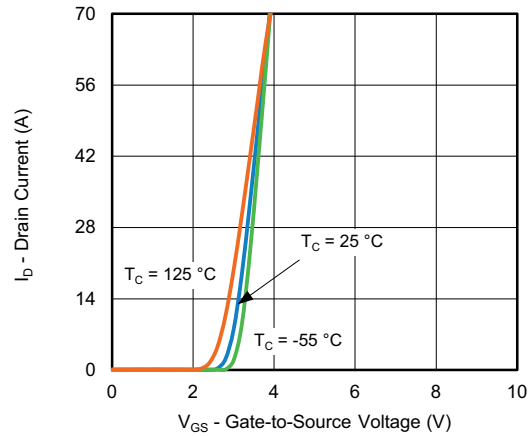
- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
 - Normalized Transient Thermal Impedance Junction-to-Case (25 °C)are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions



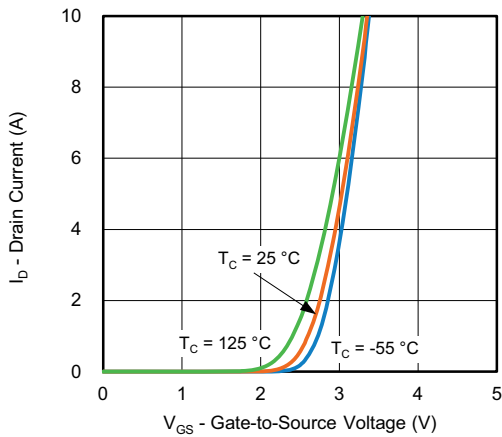
CHANNEL-2 TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



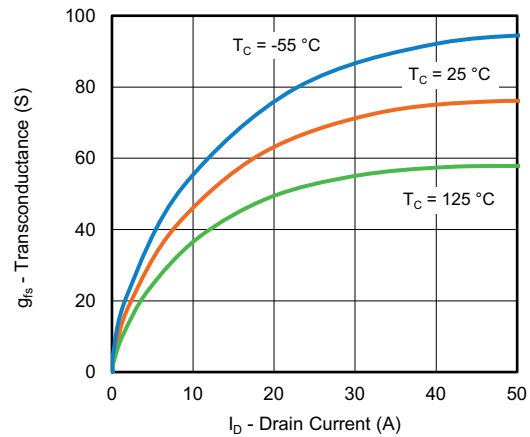
Output Characteristics



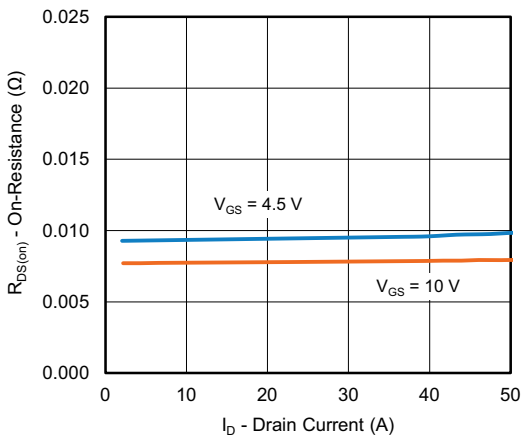
Transfer Characteristics



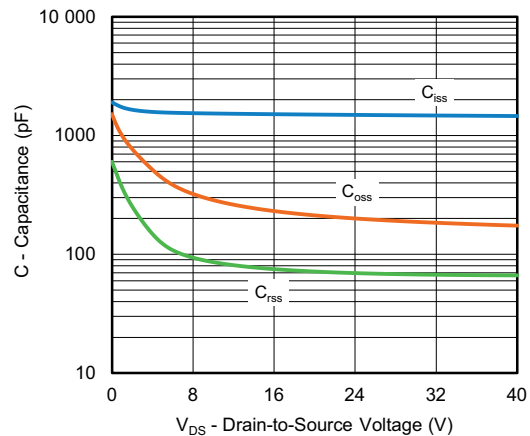
Transfer Characteristics



Transconductance



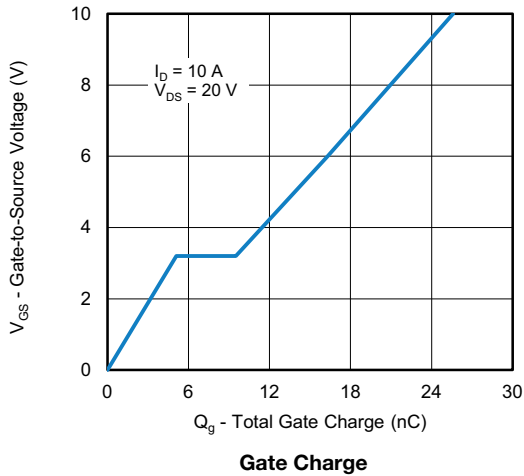
On-Resistance vs. Drain Current



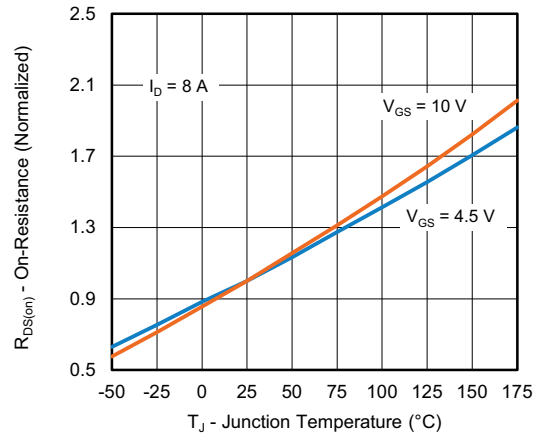
Capacitance



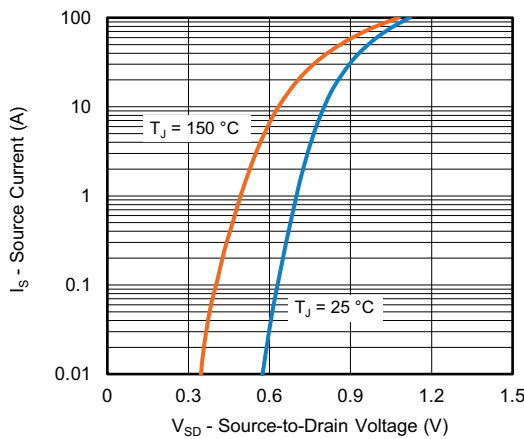
CHANNEL-2 TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



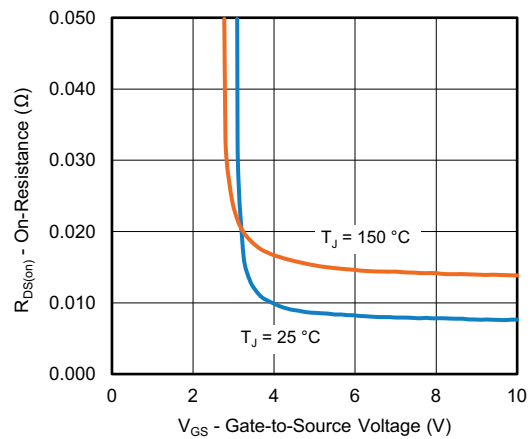
Gate Charge



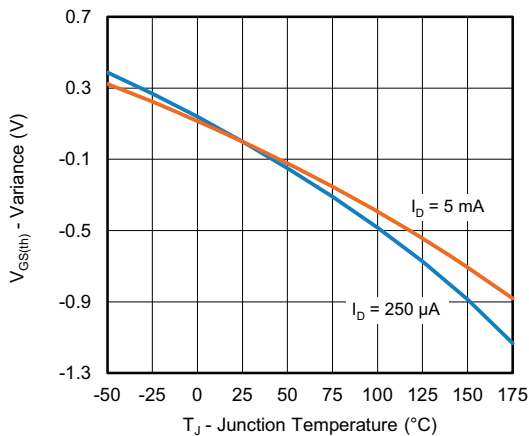
On-Resistance vs. Junction Temperature



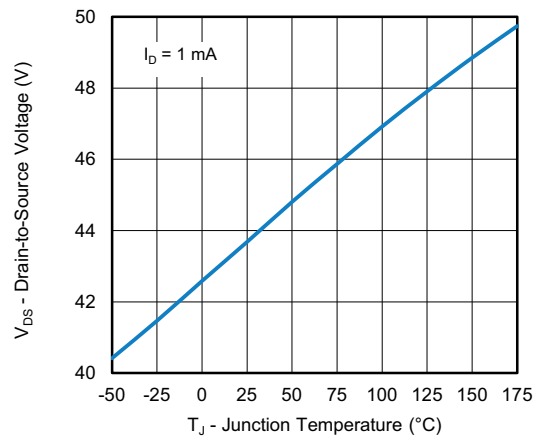
Source Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



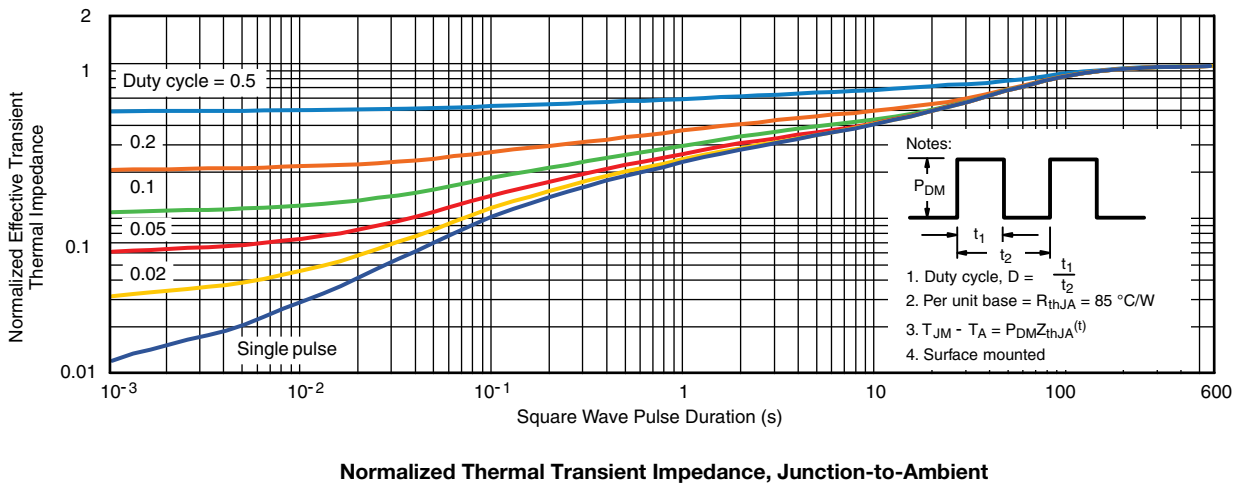
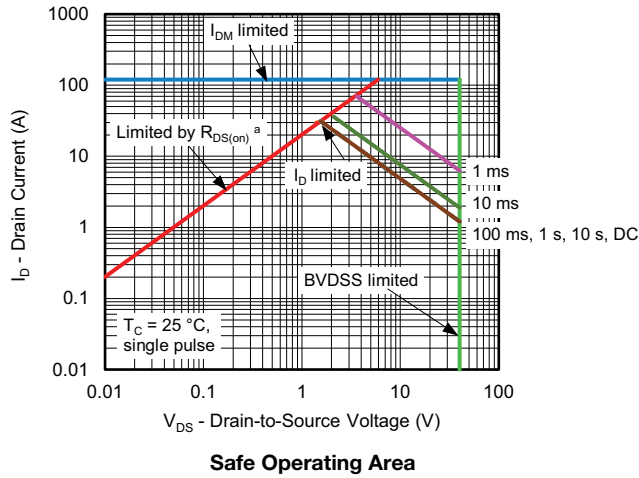
Threshold Voltage



Drain Source Breakdown vs. Junction Temperature



CHANNEL-2 TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)

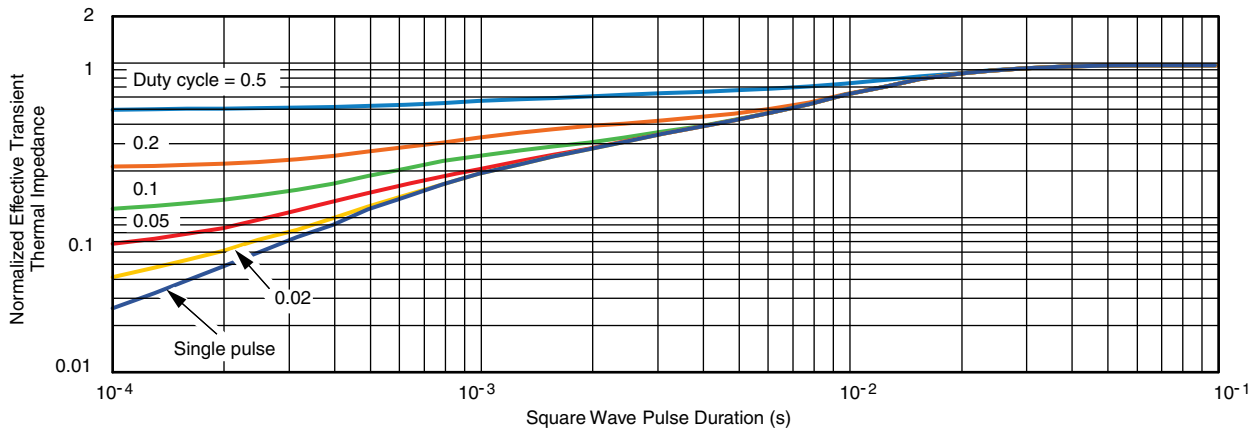


Note

a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified



CHANNEL-2 TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



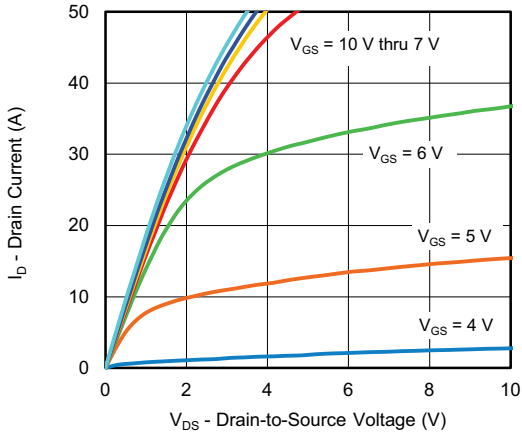
Normalized Thermal Transient Impedance, Junction-to-Case

Note

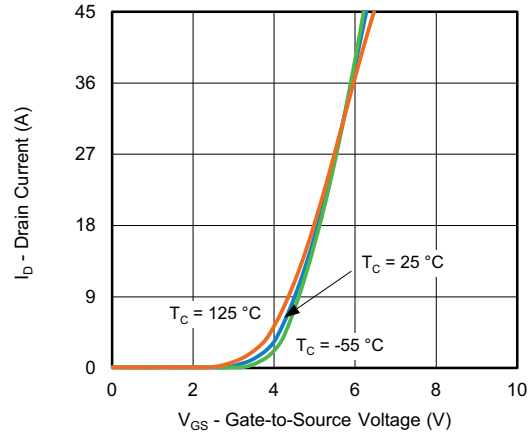
- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
 - Normalized Transient Thermal Impedance Junction-to-Case (25 °C)
 are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions



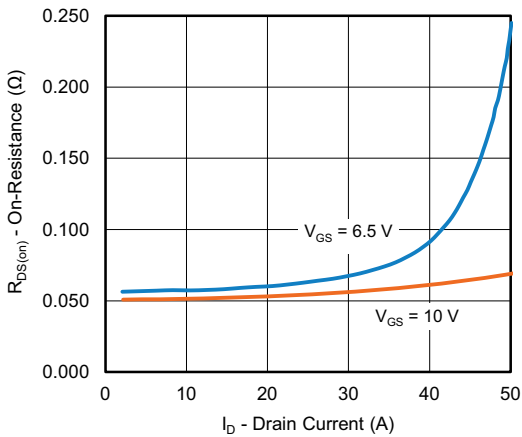
CHANNEL-3 TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



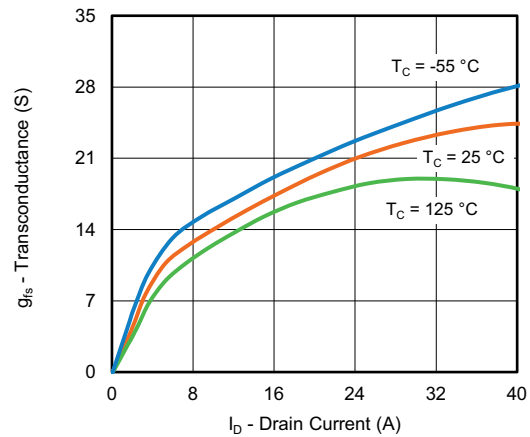
Output Characteristics



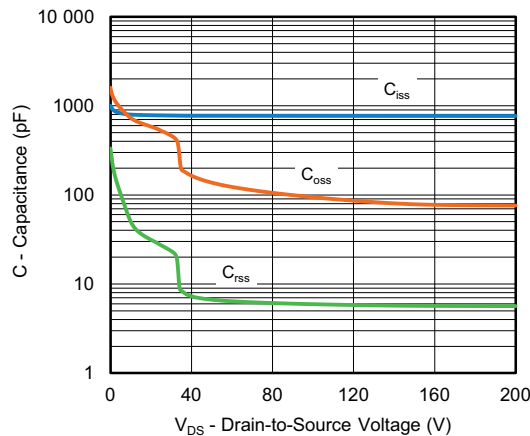
Transfer Characteristics



On-Resistance vs. Drain Current



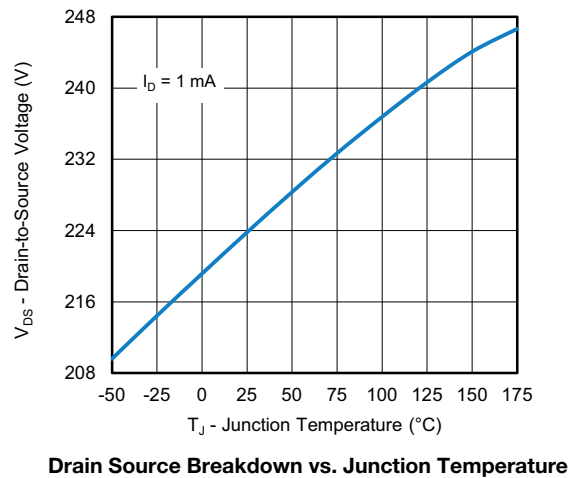
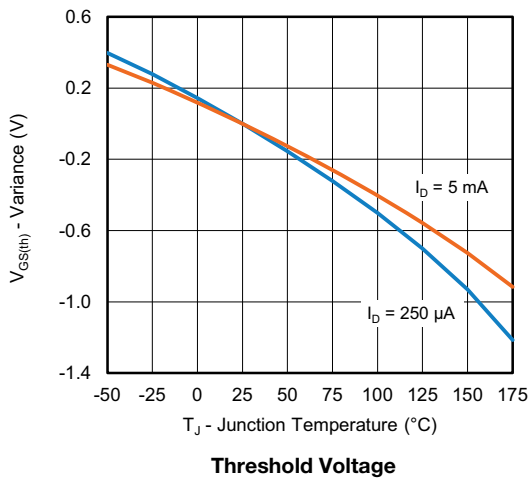
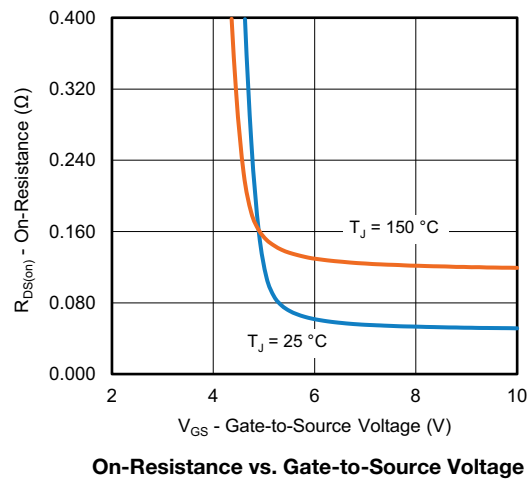
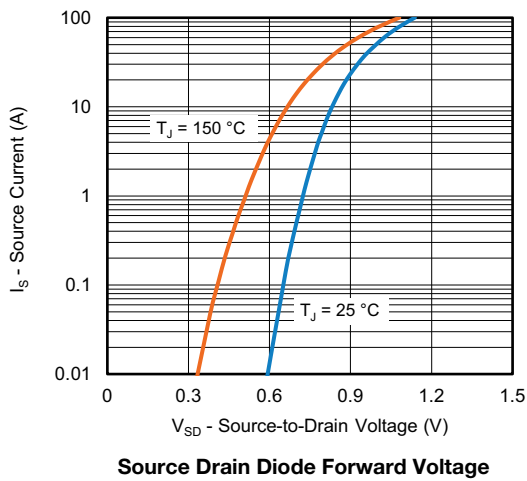
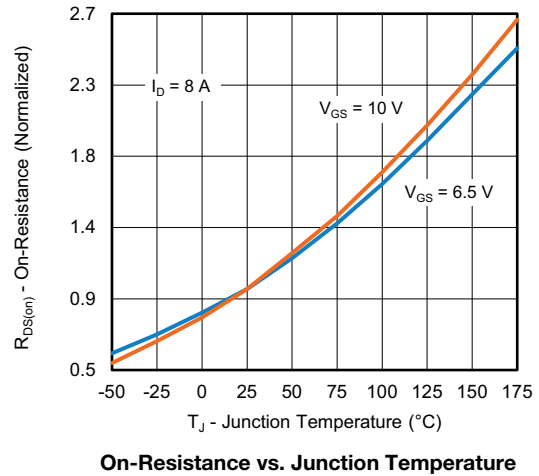
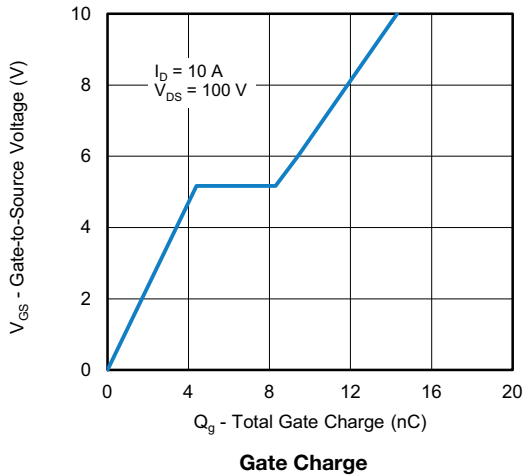
Transconductance



Capacitance

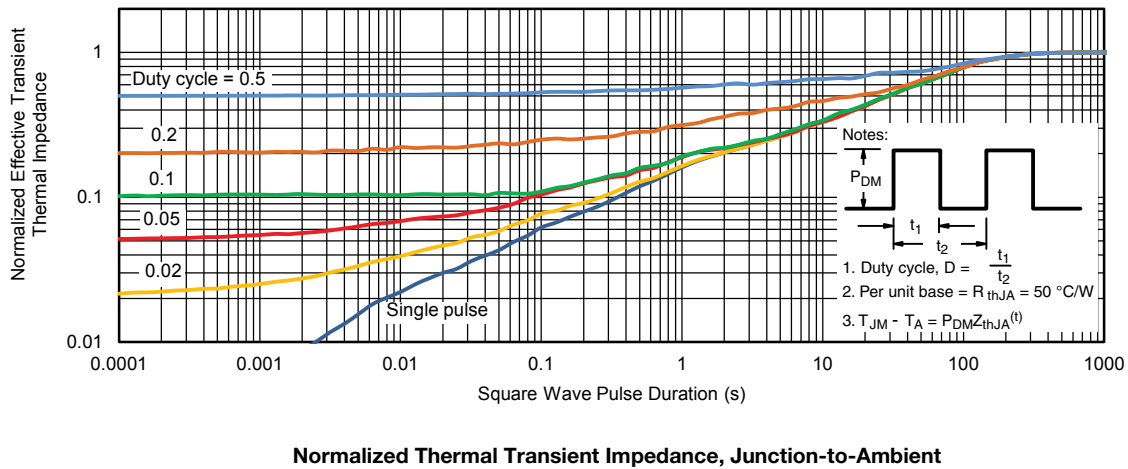
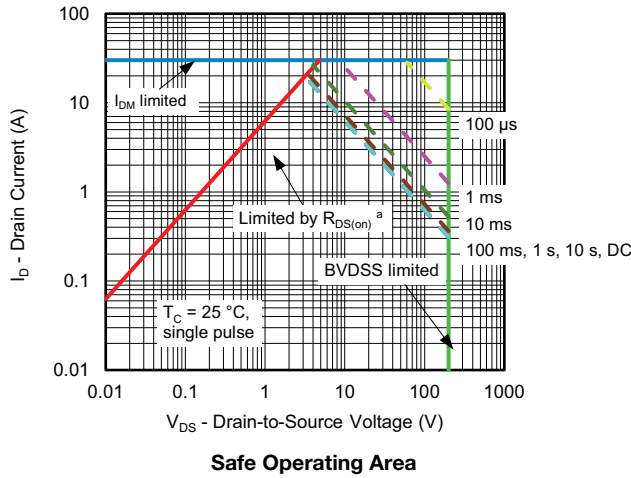


CHANNEL-3 TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)





CHANNEL-3 TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)

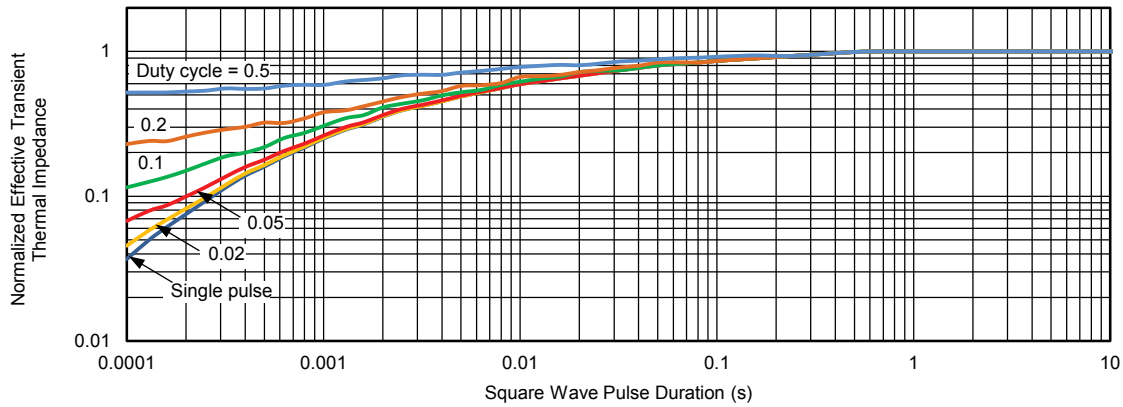


Note

a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified



CHANNEL-3 TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
 - Normalized Transient Thermal Impedance Junction-to-Case (25 °C)
 are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

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