HARRIS SEMICONDUCTOR
HARRIS · RCA · GE · INTERSIL

ICL7675/ICL7676
Switched-Mode Power Supply Controller Set

GENERAL DESCRIPTION

The ICL7675/7676 two-chip set provides the necessary control circuitry for regulation of a single-ended, transformer coupled, flyback type switching power supply. Specifically designed to operate in this type of configuration, the Harris controller chip set is trimmed to provide a regulated 5V output.

The two chips comprise a primary side controller and a secondary side controller. Referring to Figure 3, the output of the primary side controller drives the power MOSFET switch in the primary leg of the transformer. The switch is always turned off at a time corresponding to the falling edge of the internal system clock at a frequency of 50kHz. Following an initial soft-start cycle, the switch is turned on at a time corresponding to a pulse received from the secondary side controller via a pulse transformer. The secondary side controller detects the power switch turn-off at the secondary of the transformer and initiates a time-out sequence with a duration directly proportional to the output voltage being sensed. A pulse generated at the end of the time-out period is fed back through the pulse transformer to the primary side controller, thereby completing the control loop.

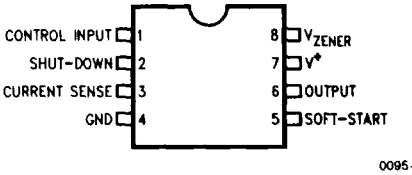
Power for the primary side controller may be taken from the high voltage DC input to the power transformer via a resistor which feeds current to the on-chip zener diode. This eliminates the need for a separate power supply for the controller. Excessive current in the power MOSFET switch is detected at one end of a resistor in series with the source of the MOSFET, forcing the primary side controller into the soft-start mode.

FEATURES

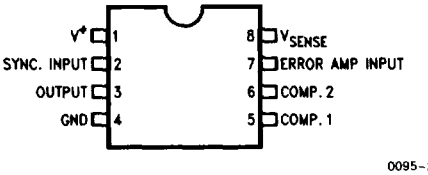
- **Output Voltage of 5V ± 5% Under All Conditions**
- **Simple Low Current Pulse Transformer Feedback**
- **Power Switch Over-Current Protection**
- **Soft-Start**
- **No Off-Chip Trimming Required**
- **Minimum External Components**
- **Low Supply Current**
- ***Output Duty Cycle—5% to 75%***

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICL7675CPA	0°C to +70°C	8 Lead MINIDIP
ICL7675CJA	0°C to +70°C	8 Lead CERDIP
ICL7675IPA	−25°C to +85°C	8 Lead MINIDIP
ICL7675MJA	−55°C to +125°C	8 Lead CERDIP
ICL7676CPA	0°C to +70°C	8 Lead MINIDIP
ICL7676MJA	−55°C to +125°C	8 Lead CERDIP



ICL7675
Package Outline (PA, JA)



ICL7676
Package Outline (PA, JA)

Figure 1: Pin Configurations

302072-002

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

ICL7675

Supply Voltage (V^+ to GND) 16V
Voltage on any pin ..... (V^+ + 0.3) to (GND − 0.3) V

ICL7676

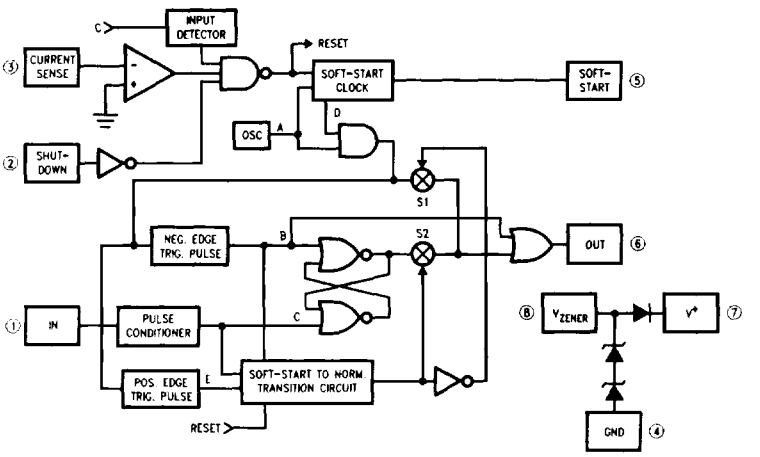
Supply Voltage (V_{sense} to GND) 16V
Voltage on any pin ..... (V_{sense} + 0.3) to (GND − 0.3) V

ICL7675 & ICL7676

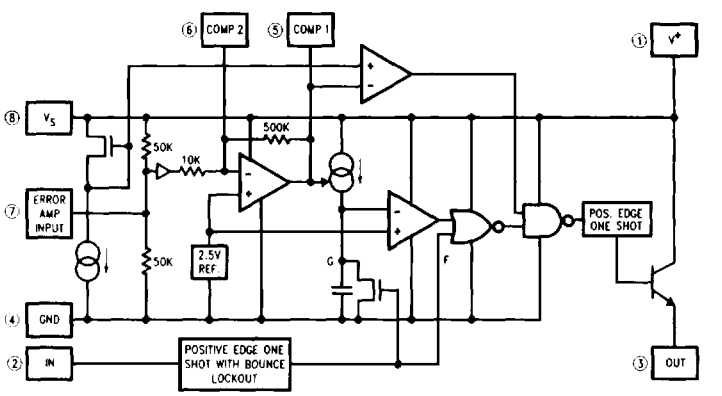
Lead Temperature (Soldering, 10 sec) ..... 300°C
Storage Temperature Range ..... − 65°C to + 150°C

Operating Temperature Range
ICL767XC ..... 0°C to + 70°C
ICL767XI ..... − 25°C to + 85°C
ICL767XM ..... − 55°C to + 125°C
Continuous Total Power Dissipation (T_A = 25°C)
CERDIP Package ..... 500 mW
Plastic Package ..... 375 mW

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*



ICL7675



ICL7676

Figure 2: Functional Diagrams

NOTE: All typical values have been characterized but are not tested.

ICL7675
ELECTRICAL CHARACTERISTICS

Unless otherwise stated: Pins 1, 2, 3, and 4 are connected to GND; Pin 7 is connected to V^+; all other pins are open; $V^+ = 13.5V$

Parameter	Test Conditions	Limits												Units
		$T_A = +25°C$			$0°C < T_A < +70°C$			$-25°C < T_A < +85°C$			$-55°C < T_A < +125°C$			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Oscillator: Frequency		42		58	41		59	40		60	38		62	kHz
Temp. Stability						0.1			0.1			0.1		%/°C
Output: Fall Time (Note 1)	R_O = 10M, C_O = 500 pF		100	150			170			180			200	ns
Rise Time (Note 1)	R_O = 10M, C_O = 500 pF		100	150			170			180			200	ns
Voltage	Output Low, $I_O = -5$ mA		0.2	0.3			0.33			0.35			0.40	V
	Output High, $I_O = +5$ mA	12.8			12.8			12.7			12.6			V
Control Input: Leakage Current			0.01	10			50			50			100	nA
Threshold		9.5		11.0	9.0		11.0	8.5		11.5	8.5		12.0	V
Shut-Down: Leakage Current			0.01	10			50			50			100	nA
Threshold		9.5		11.5	9.4		11.8	9.3		12.0	9.2		12.5	V
Soft-Start: Time-out	Open Pin		8											ms
Current Limiting: Sense Voltage		420		600	390		630	370		640	300		700	mV
Sense Voltage Temperature Coefficient						0.6			0.6			0.6		mV/°C
V_{zener}: Forward Voltage (Pin 8)		13.5	13.8	14.3										V
Forward Voltage Temperature Coefficient						7			7			7		mV/°C
V^+ Supply Voltage (Pin 7)			13.2											V
Supply Current	No Output Load			1.2			1.3			1.4			1.5	mA

NOTE 1: This parameter is guaranteed by design and is not tested in production.

NOTE: All typical values have been characterized but are not tested.

ICL7676
ELECTRICAL CHARACTERISTICS

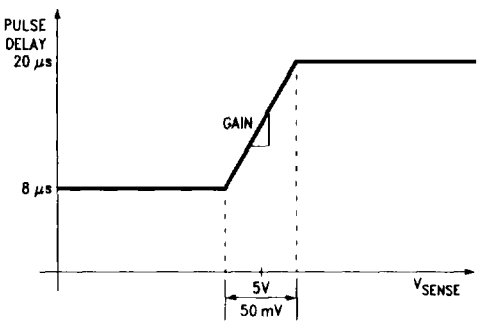
Unless otherwise stated: Pins 2 and 4 are connected to GND; Pins 1 and 8 are connected to V_{sense}; all other pins are open; $V^+ = 5V$

Parameter	Test Conditions	Limits									Units
		$T_A = +25°C$			$0°C < T_A < +70°C$			$-55°C < T_A < +125°C$			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Power Supply: Output Voltage	15 μs Pulse Delay (Note 2)	4.9		5.1							V
Temp. Stability						100			100		mV
Sync Input: Threshold		1.2		2.4	1.2		2.4	1.2		2.4	V
Leakage			0.01	10			50			100	nA
Output: Voltage	Output High	4.35			4.3			4.1			V
Pulse Current		15			14			10			mA
Pulse Width		0.55		1.0	0.5		1.0	0.25		1.0	μs
Min. Pulse Delay	50kHz Clock at Input			9			9			12	μs
Max. Pulse Delay	50kHz Clock at Input	20			20			20			μs
Gain	Time-Out/V_{sense}	90	140		70			50			μs/V
V_{sense} Input Current (Note 3)	$V_{sense} = 5.0V$, No Load			1.0			1.1			1.5	mA

NOTE 2: This corresponds to a 25% duty cycle at the output of the ICL7675.

3: This parameter is equivalent to device supply current.

TYPICAL PERFORMANCE CHARACTERISTICS



Pulse Delay vs V_{sense}

NOTE All typical values have been characterized but are not tested.

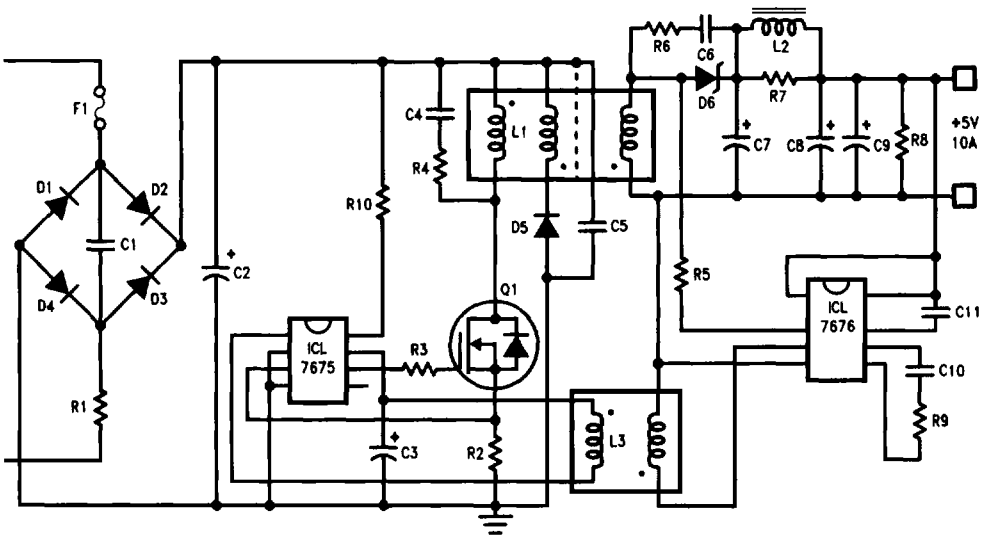


Figure 3: System Schematic

C1	0.022 μF/400V	R1	Thermistor	D1-4	1N4004
C2	330 μF/200V	R2	.47Ω/2W	D5	1N4937
C3	470 μF/16V	R3	10Ω/.125W	D6	MBR1035
C4	180 pF/500V	R4	1.5 kΩ/2W		
C5	0.022 μF/400V	R5	10 kΩ/.25W	L1	Lp = 5.1 mH
C6	39 pF/500V	R6	10Ω/.5W		n = 1/14
C7	11,000 μF/6.3V	R7	3.9Ω/.5W	L2	20 μH
C8	4.7 μF/16V	R8	10Ω/5W	L3	47 μH
C9	.047 μF/10V	R9	68 kΩ/.25W		n = 1/3
C10	2200 pF/500V	R10	75 kΩ/.5W	Q1	GE IRF821
C11	270 pF/500V				

Table 1: Example Component Values for SMPS System

NOTE: All typical values have been characterized but are not tested

DETAILED DESCRIPTION

Refer to the system schematic (Figure 3), timing diagram (Figure 4) and the individual controller functional diagrams (Figure 2) for the following discussion.

Secondary Side Controller

The secondary side controller, ICL7676, is required to provide an output pulse that will cause the primary side controller, ICL7675, to turn the MOSFET power switch on in the primary leg of the power supply transformer. This pulse must occur at a time such that the resultant switch duty cycle causes the output of the power supply to be regulated at precisely 5V. The circuit accomplishes this by amplifying the difference between a fraction of the output voltage and an internally generated reference voltage and using that output to control a ramp generator. When the output of the ramp generator reaches the reference voltage level, a comparator triggers a monostable giving a fixed width pulse at the output of the controller. A positive transition at the power supply transformer secondary, corresponding to power switch turn-off, triggers a one-shot with a bounce lock-out feature that prevents any false triggering due to excessive ringing at this node. The output of this one-shot resets the ramp generator by turning on a MOS transistor across the ramp capacitor. Also, if the ramp voltage has not reached the comparator threshold, the one-shot triggers the output monostable. This ensures that a pulse is sent to the primary side controller every cycle. Variations in the output voltage are detected and cause an increase or decrease in the current supplied to the ramp capacitor. This causes a change in the capacitor ramp rate at point G in Figure 2 and a consequent change in the time when the comparator threshold crossover occurs, generating an output pulse from the ICL7676. The output pulse's position is thereby modulated relative to the input trigger in direct proportion to the power supply voltage. The direction of change is such that when the resultant duty cycle at the output of the ICL7675 corrects the power supply voltage, a negative feedback control loop is formed that maintains the desired output voltage.

Primary Side Controller

The primary side controller, ICL7675, must process the incoming pulse from the secondary side controller, ICL7676, and combine this with the internally generated oscillator waveform to produce a driving signal for the MOSFET switch. Initially, however, a soft-start circuit determines the driving signal waveform. Therefore, there must also be a circuit which directs the orderly transition from soft-start to normal operation. When the power supply is first turned on, a power-up-reset circuit initializes the soft-start clock and sets switch S1 on and switch S2 off, as shown in Figure 2. The soft-start's slowly increasing duty cycle waveform is fed through an AND gate and through switch S1 to the output buffer. Meanwhile, the transition circuit continuously monitors the relative position in time between the incoming pulse from the secondary side controller and the leading edge from the clock waveform. When the duty cycle of the soft-start clock has increased to the point where its positive edge occurs earlier than the input pulse, then the transition circuit gives control of the output switch drive to the feedback loop by turning off S1 and turning on S2. Now the negative edge of the clock resets the flip-flop, turning off the power switch, and the input pulse sets the flip-flop, turning on the power switch. The negative edge of the soft-start clock is synchronized to the negative edge of the oscillator and occurs at a fixed frequency of 50kHz. The soft-start clock's output duty cycle gradually increases from zero to 100%, but when ANDed with the 75% duty cycle waveform of the oscillator, the maximum duty cycle of the resultant waveform is limited to 75% as well.

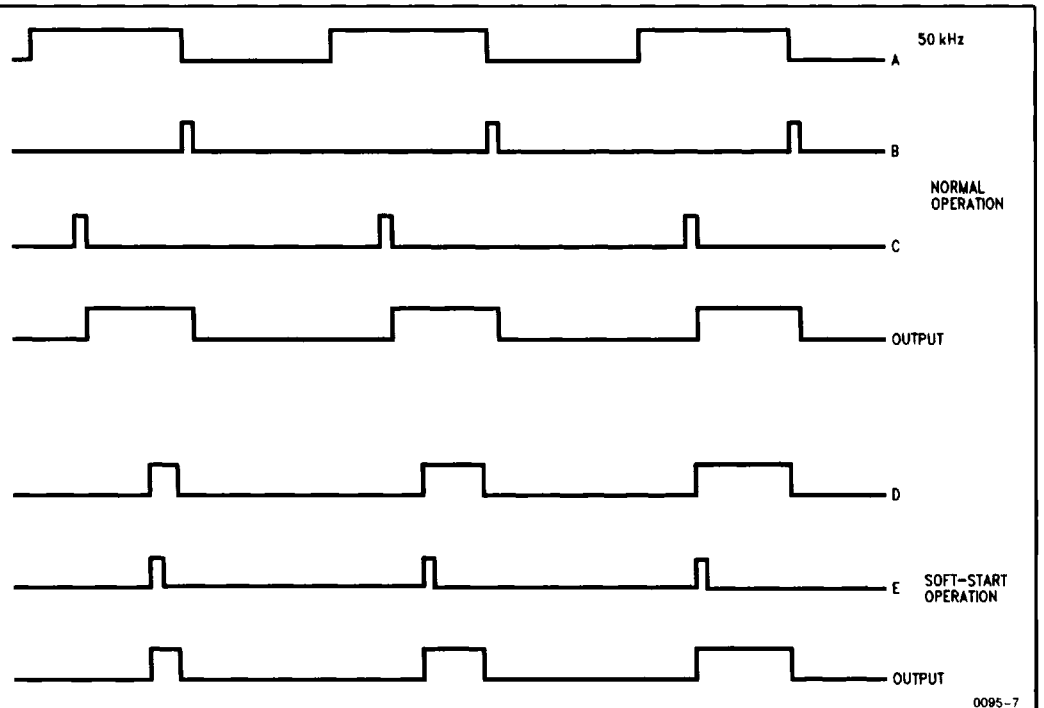
Soft-Start Cycle

The soft-start cycle time is fixed at about 15 ms. It can be increased somewhat by adding capacitance to pin 5. If no pulse is received from the secondary side controller, the primary side controller will reset, initiating the soft-start sequence. It will continue to recycle through the soft-start sequence until a pulse is received. As long as a pulse is received within one eighth cycle after the falling edge of the system clock, an approximately 0.5 μs pulse will appear at the output to drive the power switch. This allows for delays in the feedback loop which might cause the controlling pulse to arrive late.

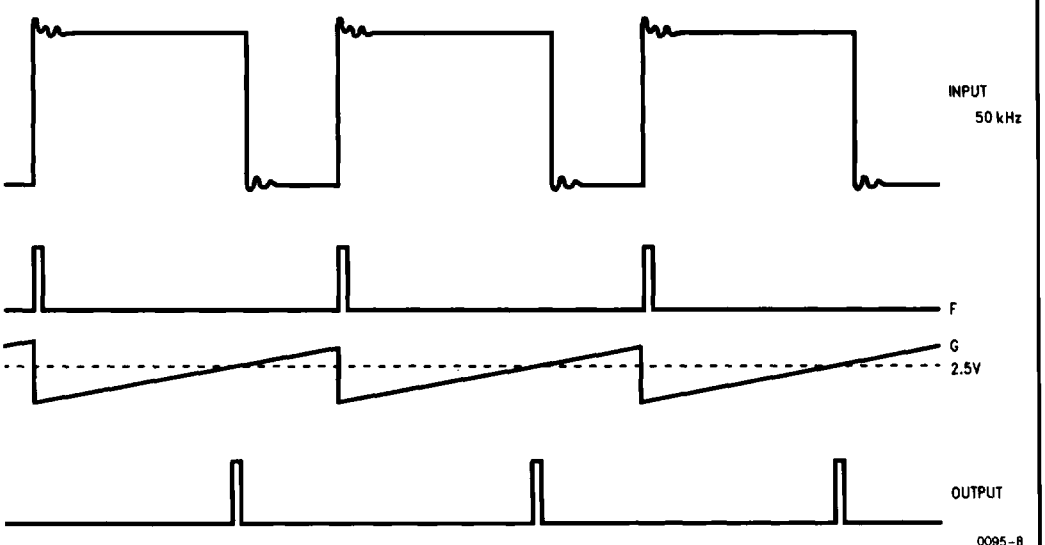
Other Features

The external resistor R2, connected between the I_{sense} pin and ground and placed in series with the power MOSFET switch, senses an over-current fault condition, tripping a comparator which shuts down the output. After the fault condition has been removed, the power supply will pass through the soft-start cycle before returning to normal operation. There is also a shut-down pin that when forced high will shut down the output. An on-chip zener diode and rectifying diode combination, connected through a dropping resistor to the high DC input voltage of the power supply, provides power to the circuit.

NOTE: All typical values have been characterized but are not tested.



ICL7675 Timing Diagram



ICL7676 Timing Diagram

Figure 4: 7675/7676 Timing Diagrams

NOTE: All typical values have been characterized but are not tested.

APPLICATIONS

Refer to the system schematic (Figure 3) for the following discussion of a flyback converter.

The input bridge rectifier and filter circuit converts the 115V AC line to 163V DC. The unregulated high voltage DC is applied across a GE IRF 821 Power FET (Q1) and the primary of transformer L1. The Power FET acts as a switch, opening and closing in response to the gate drive signal from the output of the ICL7675 controller. When Q1 opens, the energy stored in L1 is transferred to the secondary and through diode D6 into C7. This is characteristic of the flyback converter. The ICL7676 monitors the voltage across C7 and sends a variable time delay pulse through pulse transformer L3 to the ICL7675 with a delay proportional to the voltage sensed. The ICL7675 translates the pulse into a variable duty-cycle 50kHz output signal which drives the gate of the Power FET Q1 "ON" and "OFF" thereby closing the negative feedback loop.

The flyback converter topology is best suited for power levels below 150W due to the high ripple current produced across capacitor C7. This topology is favored because of its simplicity. Output voltage control is achieved by varying the ratio of ON to OFF time for Q1, and can be expressed as follows:

$$V_O = V_{C2}\, N \frac{t_{on}}{t_{off}} - V_{D6} - I_O R_S$$

where:

V_{C2} = Voltage across C2
V_{D6} = Forward drop across D6
I_O = Output current
R_S = Output series resistance
N = Turns ratio of L1 (secondary/primary)

This applies for continuous mode operation where the current in L1 never falls to zero during a clock cycle. For light loads, discontinuous conduction may occur. The primary inductance of L1 required to assure continuous mode operation at a light load $I_{O(min)}$ is:

$$L_p = \frac{t^2_{on(min)} \times V^2_{C1(max)} \times f}{2(V_O + V_{D6} + I_O R_S)\, I_{O(min)}}$$

For $I_{O(min)}$ = 10% of full load at high line:

$$L_p = \frac{(6 \times 10^{-6})^2 \times (185)^2 \times (50 \times 10^3)}{(2)\,(6)\,(1)} = 5.1\ \text{mH}$$

This inductance can be obtained on a gapped ferrite 'E' core which offers an excellent (performance)/(cost) ratio. The air gap is required to prevent saturation at low line and maximum current.

Neglecting voltage spikes due to leakage inductance, drain to source voltage stress for Q1 is:

$$V_{ds} = \frac{V_O + V_{D6} + I_O R_S}{N} + V_{C2}$$

A turns ratio N = 1/14 limits V_{ds} to a safe value at high line. A catch winding clamps voltage spikes across the Power FET at turn off. The winding should be bifilar wound with the primary to minimize leakage inductance. An electrostatic shield will improve isolation between primary and secondary.

The network composed of L2 and C8 at the output provides additional filtering by attenuating high frequency spikes and ripple. The corner frequency for the LC filter is approximately 20kHz which effectively attenuates 50kHz and higher order harmonics. Inductor L2 is shunted by 3.9Ω R7 to reduce the output "Q" and minimize output ringing. For critical damping: $R = \sqrt{L/C}$. Diode D6 is a fast recovery Schottky doide. It has a low V_d and is snubbed by resistor R6 and capacitor C6 to limit the dV/dt and overshoot. The diode D5 is also a fast recovery diode which is connected to the catch winding of transformer L1. This protects the power FET Q1 from potentially damaging voltage spikes.

Switching Losses

Power FETs behave like ideal switches and are very well suited for high frequency switching power supply applications. The fast turn-on and turn-off of the power MOSFET results in very low switching losses. In this application the turn-off losses are essentially zero, due in part to the presence of snubber network C4 and R4. And the worst case turn-on losses are less than two watts.

Energy: $W = \int_0^t V_{ds}(t)\, I_d(t)\, dt$

where: $V_{ds}(t) = 10^9\, t$

$I_d(t) = 12.5 \times 10^6\, t$

$W = 12.5 \times 10^{15} \int_0^{200\ ns} t^2\, dt$

Integrating:

$$W = 12.5 \times 10^{15} \frac{t^3}{3} \qquad \text{where: } t = 200 \times 10^{-9}$$

and Power:

$$P = W \times F \qquad \text{where: } F = 50\ \text{kHz}$$

$$\text{Power} = 12.5 \times 10^{15} \left[\frac{(2 \times 10^{-7})^3}{3}\right] 5 \times 10^4$$

$$= 1.67\ \text{Watts}$$

Because the power MOSFET has very high current gain it can be driven directly from the ICL7675. This is highly advantageous because it simplifies the circuitry and reduces overall system manufacturing costs.

Control Loop Design

The control loop for a transformer coupled flyback converter is similar to the boost converter from which it is derived. The presence of an LC resonant filter with its steep 180 degree phase rolloff and a right-half plane zero in the loop transfer function makes frequency compensation a non-trivial exercise. However, the design of the control loop can be made easier if not simpler with the proper tools. The mathematical equation representing the power mesh equivalent transfer function may be reduced to a model which can be entered into SPICE, a widely used circuit simulation program, or any other simulation software being used. The equation for the modulator-power mesh portion of the control loop may be expressed as:

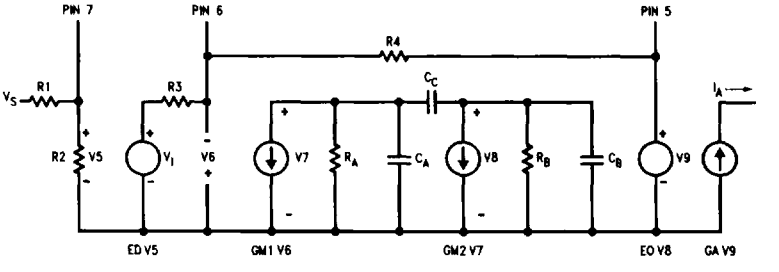
$$\frac{V_O}{D(1-D)}\left[1 - \frac{sn^2 DL_p}{(1-D)^2 R_O}\right]\frac{T(1-D)^2}{C_r V_{ref}}$$

NOTE: All typical values have been characterized but are not tested

where:

- D = Duty cycle
- n = Transformer turns ratio
- L_p = Primary inductance
- R_0 = Load resistance
- T = Clock period
- C_r = Internal ramp capacitance = 40 pF
- V_{ref} = Internal reference voltage = 2.5V

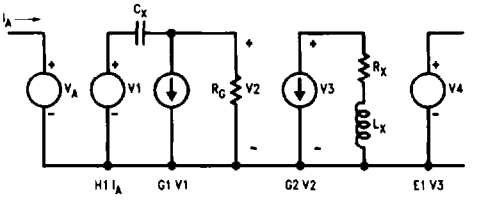
A model representing this equation is shown in Figure 5B. Combined with the output filter shown in Figure 5C, and the error amp shown in Figure 5A, a computer simulation can be used to determine the optimum combination of components for a stable design that still provides adequate response to external disturbances. Note that in the output filter, the effective primary inductance and inductor series resistance are multiplied by $n^2/(1-D)^2$. In the example here, a combination of lead compensation provided by C11 and lag compensation provided by R9 and C10 gave the desired response.



Valid for frequencies < 200 kHz

GM1 = 0.4 MV	R_B = 500 kΩ	R1 = 50 kΩ	E0 = ED = 1
GM2 = 0.15 MV	C_B = 20 pF	R2 = 50 kΩ	GA = 6.67 μV
R_A = 1.0 MΩ	C_C = 10 pF	R3 = 11.94 kΩ	
C_A = 4 pF		R4 = 500 kΩ	

Figure 5A: Error Amp Model



$$\frac{V4}{I_A} = \frac{E1 \cdot G1 \cdot G2 \times H1 \times R_G \left[1 - s\frac{C_X}{G1}\right]\left(R_X + s L_X\right)}{1 + s R_G C_X}$$

$$R_G = G1 = R_X = G2 = H1 = 1$$

$$C_X = L_X = \frac{n^2 D L_p}{(1-D)^2}$$

$$E1 = \frac{V_0}{D(1-D)} \times \frac{T(1-D)^2}{C_r V_{ref}}$$

Figure 5B: Control Loop Model

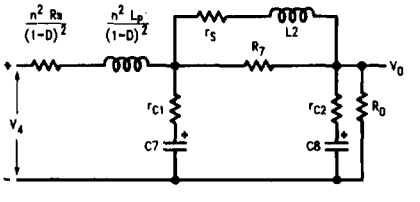


Figure 5C: Output Filter Model

NOTE: All typical values have been characterized but are not tested.