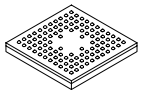
Order this document by MC13760PP/D

MOTOROLA intelligence everywhere | digital dna

MC13760

MULTI–PROTOCOL TRANSCEIVER

SEMICONDUCTOR TECHNICAL DATA



PLASTIC PACKAGE
CASE 1285
(BGA–104)

Product Preview

GSM/DCS/TDMA/AMPS Multi-Protocol Transceiver

The MC13760 Multi–Protocol, Multi–Band Digital Transceiver IC combines, on a single Advanced BiCMOS chip, the major building blocks required for next generation multi–purpose, multi–band wireless products. The device includes the majority of the circuitry necessary for IF signal processing between the RF front end and the DSP and backend. The MC13760 contains two fractional–N synthesizers, a re–configurable zero IF receiver with programmable bandwidth, receive A/D conversion, multi–rate data interface to the baseband DSP, direct launch digital modulator, full transmit support circuits, and general purpose support circuits such as D/A and A/D converters, battery save and tri–state control switches.

Intended for use in a combined GSM/TDMA/AMPS/iDEN portable wireless phone product in the 800/900/1800/1900 MHz bands. The MC13760 can be used over a wide range of RF and IF frequencies. The main PLL prescaler input is usable to over 2.0 GHz and the IF quadrature downconverter operates up to 400 MHz.

The MC13760 has separate receive IF inputs and a common zero–IF IQ receiver for TDMA and for GSM accommodating the receiver architectural need to use different IF frequencies and filters without the need for additional switches.

- Receiver Functions for all GSM/DCS/TDMA IS–136/AMPS Modes and Frequencies Including GPRS
- Direct Interface to Motorola Baseband Processors, such as the DSP56690 through a Common Programming and Data Interface
- Main Three Accumulator (24–Bit) Fractional–N Synthesizer
  - Resolution Capability of 6.0 Hz
  - Dual–Mode Charge Pump Output for TDMA TX VCO and all RX
  - Independent Charge Pump Output for the GSM/DCS TX VCO
  - GMSK Lookup ROM for Direct Transmission in GSM/DCS Mode
  - Digital 16–Bit Automatic Frequency Control
- Secondary Three Accumulator (24–Bit) Fractional–N Synthesizer for use as an Accurate Frequency–Corrected Clock in GSM, or as an Additional Low Frequency LO
- Coarse Tuning of the VCO(s) via a 6–Bit D/A with Adapt
- Operates at 2.75 V Deep Sleep Mode with Current as low as 50 μA
- Versatile Frequency Generation including Linear and Constant Envelope Modulation Paths, Ramp and Power Level Control, Direct Gain Control of the RFPA in the TDMA Mode
- D/A Conversion of TDMA TXI and TXQ
- Reference Crystal Oscillator with a Buffered Output, Compensation/Fine Tuning via 9–Bit D/A
- Receiver Gain Adjustment and Bandwidth Down to 6.0 kHz Programmed over the SPI Bus
- A/D Conversion of RXI and RXQ to 8–Bit or 10–Bit Resolution
- Types of Applications
  - GSM/DCS/TDMA/AMPS Global Roaming Multiband Cellular Telephone
  - VHF/UHF 2–Way or Trunked Radio, iDEN, Tetra, or Satellite Communication Radios or Telephones
  - Hand–Held Wireless PDA's
  - Wireless LAN's, Industrial Devices, ISM Band Products
  - Any New Device Containing Some Combination of the Above Functions

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC13760	T_A = –40 to 85°C	BGA–104

Figure 1. MC13760 Detailed Block Diagram

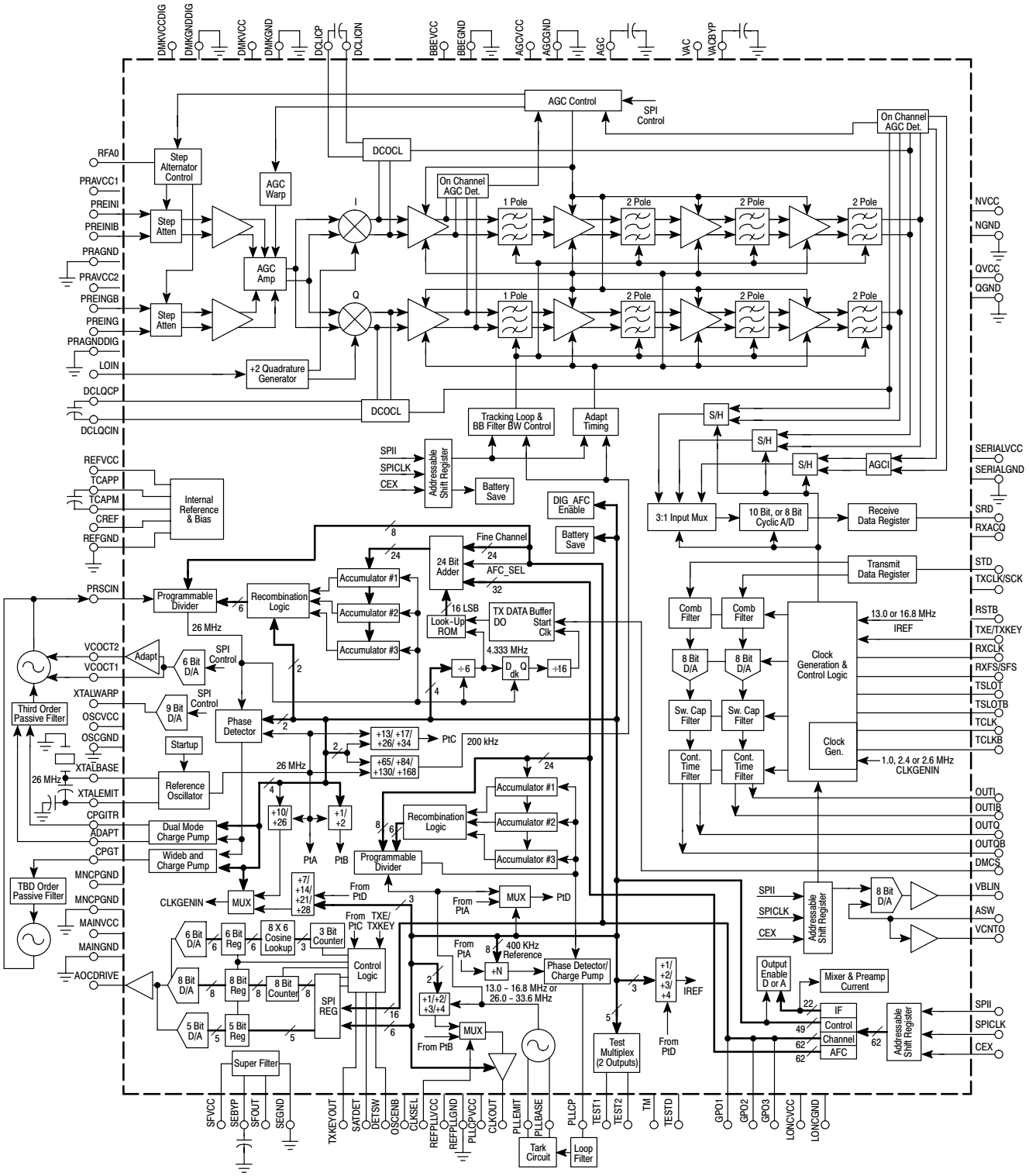


Table 1. BGA Contact Identification

BALL #	BALL NAME	DESCRIPTION	SIGNAL TYPE
A1	PRAGNDDIG	Ground for the preamp substrate.	Ground
A2	PRAGND	Ground for the preamp.	Ground
A3	PREINGB	GSM IF preamp input.	RF Input
A4	PREINIB	TDMA IF preamp input.	RF Input
A5	BBFGND	Ground for the baseband filters.	Ground
A6	DCLQCP	DC Offset Correction Loop (input) capacitor – Q channel	Analog Input
A7	CREF	Bypass capacitor for the bandgap regulator.	Analog
A8	OUTQ	TDMA Q channel analog transmit data.	Analog Output
A9	OUTIB	TDMA I channel analog transmit data.	Analog Output
A10	TSLOTB	TDMA low level transmit slot.	Analog Output
A11	TSLOT	TDMA low level transmit slot.	Analog Output
B1	RFA0	RF attenuator 0 control line. (This line is a driver for an external RF attenuator.)	Digital Output
B2	DMXGND	Ground for the mixer.	Ground
B3	PREING	GSM IF preamp input.	RF Input
B4	PREINI	TDMA IF preamp input.	RF Input
B5	PRAVCC2	Supply for the preamp output stage.	Supply 2.775 V
B6	DCLICP	DC Offset Correction Loop (input) capacitor – I channel	Analog Input
B7	GPO3/test_so2	SPI port expansion 3. Or scan data output for MODROM module.	Digital Output
B8	TCAPP	Differential reference capacitor.	Analog
B9	REFGND	Ground for the internal reference.	Ground
B10	REFVCC	Supply for the internal reference.	Supply 2.775 V
B11	TCLK	TDMA low level transmit clock.	Analog Output
C1	DMXVCC	Supply for the mixer.	Supply 2.775 V
C2	DMXGNDDIG	Ground for the mixer substrate and quadrature generator.	Ground
C3	PRAVCC1	Supply for the preamp.	Supply 2.775 V
C4	BBFVCC	Supply for the baseband filters.	Supply 2.775 V
C5	DCLICIN	DC Offset Correction Loop (output) capacitor – TDMA – I channel	Analog Output
C6	DCLQCIN	DC Offset Correction Loop (output) capacitor – TDMA – Q channel	Analog Output
C7	TCAPM	Differential reference capacitor.	Analog
C8	OUTQB	TDMA Q channel analog transmit data.	Analog Output
C9	CLKSEL	Selects the source for the clock output to the digital circuitry of the radio as either the crystal reference/divided crystal reference or the Step Up PLL/divided Step Up PLL. A low on this pin selects the crystal reference/divided crystal reference. A high on this pin selects the Step Up PLL/divided Step Up PLL. Integrated weak pulldown.	Digital Input
C10	TCLKB	TDMA low level transmit clock.	Analog Output
C11	QGND	Quiet analog ground for the PA D/A and the data processing circuits.	Ground
D1	LOIN	Input port for the second LO VCO signal.	RF Input
D2	DMXVCCDIG	Supply for the quadrature generator.	Supply 2.775 V
D3	TEST2/EERQ	Test input/MUX 2 output. (Various signals are buffered and MUX'd to this pin. Output signal is determined by programming of test bits.) Or with EER active, TDMA Q channel transmit data.	Analog Test Point
D4	TEST1/EERI	Test input/MUX 1 output. (Various signals are buffered and MUX'd to this pin. Output signal is determined by programming of test bits.) Or with EER active, TDMA I channel transmit data.	Analog Test Point
D6	PKGGND1	Ground for the package flag (no direct connection to die).	Pkg Ground
D8	OUTI	TDMA I channel analog transmit data.	Analog Output
D9	TESTD/GPO4	Digital test point. (Various digital signals are MUX'd to this pin. Output is determined by programming of test bits.) Or SPI port expansion 4.	Digital Test Point Digital Output

Table 1. BGA Contact Identification (continued)

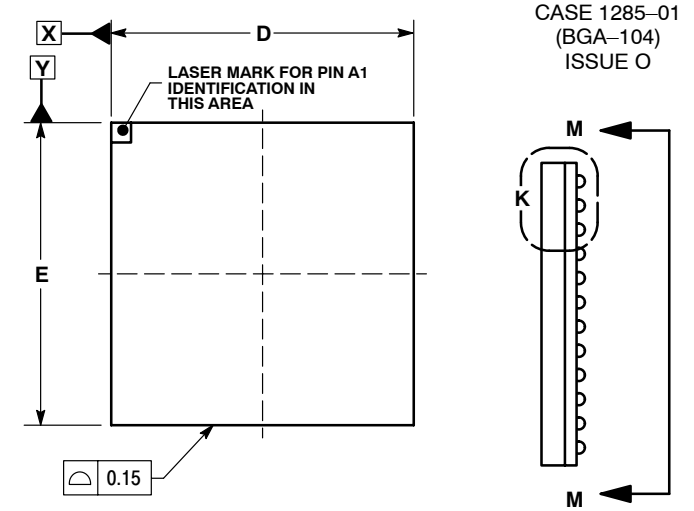
BALL #	BALL NAME	DESCRIPTION	SIGNAL TYPE
D10	QVCC	Quiet analog supply for the PA D/A and the data processing circuits.	Supply 2.775 V
D11	NGND	Noisy analog ground for the VCO D/A, AOC D/A and the data processing circuits.	Ground
E1	VAG	Analog ground.	Analog
E2	AGCGND	Ground for the AGC.	Ground
E3	VAGBYP	Bypass capacitor for the analog ground voltage.	Analog
E9	NVCC	Noisy analog supply for the VCO D/A, AOC D/A and the data processing circuits.	Supply 2.775 V
E10	RSTB	Reset. Low true input. Integrated weak pullup.	Digital Input
E11	TM	Enable for the internal scan test.	Digital Input
F1	AGCVCC	Supply for the AGC.	Supply 2.775 V
F2	TXKEYOUT/test_so4	Conditioned TXKEY out. Or scan data output for reference clock module.	Digital Output
F3	AGC	Capacitor for the TDMA AGC.	Analog
F4	PKGGND2	Ground for the package flag (no direct connection to die).	Pkg Ground
F8	PKGGND3	Ground for the package flag (no direct connection to die).	Pkg Ground
F9	PLLCPVCC	Supply for the Step Up PLL phase detector and charge pump.	Supply 5.0 V
F10	CLKOUT	Clock output to the digital circuitry of the radio. Ranges are 13.0 to 16.8 MHz, or 26.0 to 33.6 MHz. The actual frequency provided will depend upon the configuration of the Step Up PLL and the SPI selected configuration of the MC13760.	Analog Output
F11	PLLCP	Charge pump output for the Step Up PLL.	Analog Output
G1	PRSCIN	Main LO prescaler input.	RF Input
G2	MAINGND	Ground for the main prescaler and divider.	Ground
G3	AOCDRIVE	Output to the PA bias circuitry drive input. (Output drive impedance is 620 Ohms.)	Analog Output
G9	PLLEMIT	Emitter of the oscillator transistor for the Step Up PLL.	RF Output
G10	REFPLLVCC	Supply for the Step Up PLL VCO and dividers.	Supply 2.775 V
G11	PLLBASE/vco_clk	Base of the oscillator transistor for the Step Up PLL. Or scan clock input for VCO clock zone.	RF Input
H1	SATDET/test_si4	Input indicating saturation. Or scan data input for reference clock module.	Digital Input
H2	GPO2/test_so8	SPI port expansion 2. Or Main PLL Adapt Timer output. Or scan data output for SSI module.	Digital Output
H3	MAINVCC	Supply for the main prescaler and divider.	Supply 2.775 V
H4	MNCPVCC	Supply for the main phase detector and charge pump.	Supply 5.0 V
H6	PKGGND4	Ground for the package flag (no direct connection to die).	Pkg Ground
H8	TXE/TXKEY/test_si8	Transmit slot enable in TDMA mode; digital input to start/stop the PA Control sequence in GSM mode. Or scan data input for SSI module.	Digital Input
H9	RXACQ/test_si7	Serial bus enable. Or scan data input for 5 bit and 8 bit xtal clock dividers.	Digital Input
H10	REFPLLGND	Ground for the Step Up PLL.	Ground
H11	SERIALVCC	Supply for the SSI and SPI serial communication ports.	Supply 1.8 — 2.775V
J1	GPO1/test_so1	SPI port expansion 1. Or Coarse Tune Adapt Timer output. Or scan data output for main Frac–N.	Digital Output
J2	VCOCT2	High current (ADAPT) output of the 6 bit main RX VCO Coarse Tune D/A.	Analog Output
J3	DETSW/test_si1	Output to the PA control circuitry power range input (open drain). Or scan data input for main Frac–N.	Analog Output
J4	SFVCC	Supply for the super filter.	Supply 2.775 V
J5	ASW/sc_inp1	TDMA antenna switch control input. Or scan data input for reference clock Frac–N accumulator module.	Digital Input

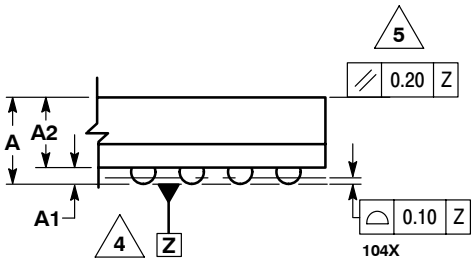
Table 1. BGA Contact Identification (continued)

BALL #	BALL NAME	DESCRIPTION	SIGNAL TYPE
J6	VCNTO	TDMA RFPA gain control voltage output.	Analog Output
J7	OSCVCC	Supply for the crystal oscillator.	Supply 2.775 V
J8	XTALWARP	Output of the 9 bit WARP D/A to be used for compensation/correction of the reference crystal frequency.	Analog Output
J9	OSCENB	Digital input used to control the crystal oscillator circuit. A logic low selects the internal oscillator. Integrated weak pulldown.	Digital Input
J10	RXCLK/test_so3	SSI RX clock in GSM mode; not used in TDMA mode. Or scan data output for transmit power amp control module.	Digital Output
J11	SRD/test_so6	SSI receive data. Or scan data output for Adapt Generator module.	Digital Output
K1	VCOCT1	Low current output of the 6 bit main RX VCO Coarse Tune D/A.	Analog Output
K2	MNCPGND	Ground for the main phase detector and charge pump.	Ground
K3	SFGND	Ground for the super filter.	Ground
K4	SFBYP	Bypass capacitor for the super filter. (1.0 μf)	Analog
K5	OSCGND	Ground for the crystal oscillator.	Ground
K6	XTALBASE/sc_clk26	Crystal oscillator base. Or scan clock input for xtal clock zone.	RF Input
K7	LOGICVCC	Supply for the main synthesizer logic, adapt control and test MUXs.	Supply 2.775 V
K8	CEX	Digital input that latches in the SPI data. (Low Active)	Digital Input
K9	SPICLK	SPI clock input.	Digital Input
K10	STD/test_si3	SSI transmit data. Or scan data input for transmit.	Digital Input
K11	TXCLK/SCK/test_so5	Bit clock for TX data transfer in GSM mode. Bit clock for RX and TX data transfer in TDMA mode. Or scan data output for reference clock Frac–N accumulator module.	Digital Output
L1	ADAPT	Synthesizer output to adapt the loop filter for the main PLL.	Analog Output
L2	CPGT	Charge pump output for the main TX LO (GSM).	Analog Output
L3	CPGITR	Charge pump output for the main RX LO (GSM, TDMA TX and RX).	Analog Output
L4	SFOUT	Super filter output. (45 mA max) (bypass with 0.01 μf)	Analog Output
L5	VBLIN	TDMA RFPA bias control voltage output.	Analog Output
L6	XTALEMIT	Crystal oscillator emitter.	RF Output
L7	LOGICGND	Ground for the main synthesizer logic, adapt control and test MUXs.	Ground
L8	SERIALGND	Ground for the SSI and SPI serial communication ports.	Ground
L9	SPII	SPI data input.	Digital Input
L10	DMCS/test_si2	Digital input that starts the GSM TX modulation. Or scan data input for MODROM module.	Digital Input
L11	RXFS/SFS/test_so7	RX SSI frame sync in GSM mode; SSI frame sync in TDMA mode. Or scan data output for 5 bit and 8 bit xtal clock dividers.	Digital Output

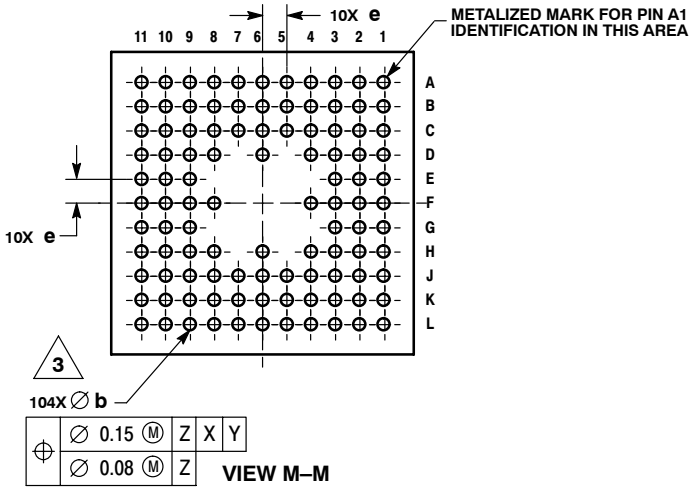
OUTLINE DIMENSIONS

PLASTIC PACKAGE
CASE 1285–01
(BGA–104)
ISSUE O





DETAIL K
ROTATED 90° CLOCKWISE



VIEW M–M

NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

	MILLIMETERS	
DIM	MIN	MAX
A	1.25	1.60
A1	0.21	0.40
A2	1.16 REF	
b	0.35	0.45
D	10.00 BSC	
E	10.00 BSC	
e	0.80 BSC	

How to reach us:
USA/EUROPE/Locations Not Listed: Motorola Literature Distribution;
P.O. Box 5405, Denver, Colorado 80217. 1–303–675–2140 or 1–800–441–2447

Technical Information Center: 1–800–521–6274

JAPAN: Motorola Japan Ltd.; SPS, Technical Information Center, 3–20–1, Minami–Azabu. Minato–ku, Tokyo 106–8573 Japan. 81–3–3440–3569

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Centre, 2, Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong. 852–26668334

HOME PAGE: http://www.motorola.com/semiconductors/

MOTOROLA