

Quad TTL to MECL Translator

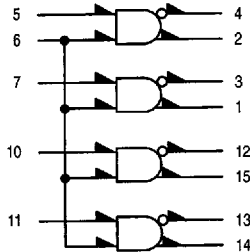
The MC10124 is a quad translator for interfacing data and control signals between a saturated logic section and the MECL section of digital systems. The MC10124 has TTL compatible inputs, and MECL complementary open-emitter outputs that allow use as an inverting/ non-inverting translator or as a differential line driver. When the common strobe input is at the low logic level, it forces all true outputs to a MECL low logic state and all inverting outputs to a MECL high logic state.

Power supply requirements are ground, +5.0 Volts, and -5.2 Volts. Propagation delay of the MC10124 is typically 3.5 ns. The dc levels are standard or Schottky TTL in, MECL 10,000 out.

An advantage of this device is that TTL level information can be transmitted differentially, via balanced twisted pair lines, to the MECL equipment, where the signal can be received by the MC10115 or MC10116 differential line receivers. The MC10124 is useful in computers, instrumentation, peripheral controllers, test equipment, and digital communications systems.

$P_D = 380 \text{ mW typ/pkg (No Load)}$
 $t_{pd} = 3.5 \text{ ns typ (+ 1.5 Vdc in to 50% out)}$
 $t_r, t_f = 2.5 \text{ ns typ (20\%--80\%)}$

LOGIC DIAGRAM



Gnd = PIN 16
 VCC (+5.0Vdc) = PIN 9
 VEE (-5.2Vdc) = PIN 8

MC10124



L SUFFIX
CERAMIC PACKAGE
CASE 620-10

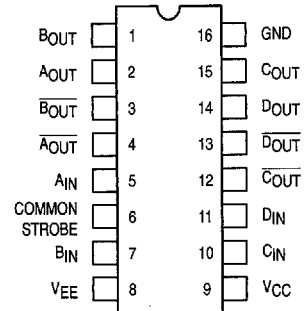


P SUFFIX
PLASTIC PACKAGE
CASE 648-08



FN SUFFIX
PLCC
CASE 775-02

DIP
PIN ASSIGNMENT



Pin assignment is for Dual-in-Line Package.
 For PLCC pin assignment, see the Pin Conversion
 Tables on page 6-11.

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ELECTRICAL CHARACTERISTICS

| Characteristic | Symbol | Pin Under Test | Test Limits | | | | | | Unit | |
|--|-------------------|----------------|-------------|--------|--------|-----|--------|--------|--------|------|
| | | | -30°C | | +25°C | | | +85°C | | |
| | | | Min | Max | Min | Typ | Max | Min | | Max |
| Negative Power Supply Drain Current | I _E | 8 | | 72 | | | 66 | | 72 | mAdc |
| Positive Power Supply Drain Current | I _{CCH} | 9 | | 16 | | | 16 | | 18 | mAdc |
| | I _{CCL} | 9 | | 25 | | | 25 | | 25 | mAdc |
| Reverse Current | I _R | 6 | | 200 | | | 200 | | 200 | μAdc |
| | | 7 | | 50 | | | 50 | | 50 | |
| Forward Current | I _F | 6 | | -12.8 | | | -12.8 | | -12.8 | mAdc |
| | | 7 | | -3.2 | | | -3.2 | | -3.2 | |
| Input Breakdown Voltage | BV _{in} | 6 | 5.5 | | 5.5 | | | 5.5 | | Vdc |
| | | 7 | 5.5 | | 5.5 | | | 5.5 | | |
| Clamp Input Voltage | V _I | 6 | | -1.5 | | | -1.5 | | -1.5 | Vdc |
| | | 7 | | -1.5 | | | -1.5 | | -1.5 | |
| High Output Voltage | V _{OH} | 1 | -1.060 | -0.890 | -0.960 | | -0.810 | -0.890 | -0.700 | Vdc |
| | | 3 | -1.060 | -0.890 | -0.960 | | -0.810 | -0.890 | -0.700 | |
| Low Output Voltage | V _{OL} | 1 | -1.890 | -1.675 | -1.850 | | -1.650 | -1.825 | -1.615 | Vdc |
| | | 3 | -1.890 | -1.675 | -1.850 | | -1.650 | -1.825 | -1.615 | |
| High Threshold Voltage | V _{OHA} | 1 | -1.080 | | -0.980 | | | -0.910 | | Vdc |
| | | 3 | -1.080 | | -0.980 | | | -0.910 | | |
| Low Threshold Voltage | V _{OLA} | 1 | | -1.655 | | | -1.630 | | -1.595 | Vdc |
| | | 3 | | -1.655 | | | -1.630 | | -1.595 | |
| Switching Times (50Ω Load) | | | | | | | | | | ns |
| Propagation Delay (+3.5Vdc to 50%) ¹ | t ₆₊₁₊ | 1 | 1.5 | 6.8 | 1.0 | 3.5 | 6.0 | 1.0 | 6.0 | |
| | t ₆₋₁₋ | 1 | 1.0 | 6.0 | 1.0 | 3.5 | 6.0 | 1.5 | 6.8 | |
| | t ₇₊₁₊ | 1 | 1.5 | 6.8 | 1.0 | 3.5 | 6.0 | 1.0 | 6.0 | |
| | t ₇₋₁₋ | 1 | 1.0 | 6.0 | 1.0 | 3.5 | 6.0 | 1.5 | 6.8 | |
| | t ₇₊₃₋ | 3 | 1.5 | 6.8 | 1.0 | 3.5 | 6.0 | 1.0 | 6.0 | |
| | t ₇₋₃₊ | 3 | 1.0 | 6.0 | 1.0 | 3.5 | 6.0 | 1.5 | 6.8 | |
| Rise Time (20 to 80%) | t ₁₊ | 1 | 1.0 | 4.2 | 1.1 | 2.5 | 3.9 | 1.1 | 4.3 | |
| Fall Time (20 to 80%) | t ₁₋ | 1 | 1.0 | 4.2 | 1.1 | 2.5 | 3.9 | 1.1 | 4.3 | |

1. See switching time test circuit. Propagation delay for this circuit is specified from +1.5Vdc in to the 50% point on the output waveform. The +3.5Vdc is shown here because all logic and supply levels are shifted 2 volts positive.

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ELECTRICAL CHARACTERISTICS (continued)

| | | | TEST VOLTAGE VALUES (Volts) | | | | | Gnd |
|--|-------------------|----------------|---|--------------------|-------------------|-------------------|----------------|----------------------|
| | | | V _{IH} | V _{ILmax} | V _{IHA'} | V _{ILA'} | V _F | |
| @ Test Temperature | | | | | | | | |
| -30°C | | | +4.0 | +0.40 | +2.00 | +1.10 | +0.40 | |
| +25°C | | | +4.0 | +0.40 | +1.80 | +1.10 | +0.40 | |
| +85°C | | | +4.0 | +0.40 | +1.80 | +0.90 | +0.40 | |
| Characteristic | Symbol | Pin Under Test | TEST VOLTAGE APPLIED TO PINS LISTED BELOW | | | | | Gnd |
| | | | V _{IH} | V _{ILmax} | V _{IHA'} | V _{ILA'} | V _F | |
| Negative Power Supply Drain Current | I _E | 8 | | | | | | 16 |
| Positive Power Supply Drain Current | I _{CCH} | 9 | 5,6,7,10,11 | | | | | 16 |
| | I _{CCL} | 9 | | | | | | 5,6,7,10,11,16 |
| Reverse Current | I _R | 6 7 | | | | | 5,7,10,11 6 | 16 16 |
| Forward Current | I _F | 6 7 | 5,7,10,11 6 | | | | 6 7 | 16 16 |
| Input Breakdown Voltage | BV _{in} | 6 7 | | | | | | 5,7,10,11,16 6,16 |
| Clamp Input Voltage | V _I | 6 7 | | | | | | 16 16 |
| High Output Voltage | V _{OH} | 1 3 | 6,7 | 6,7 | | | | 16 16 |
| Low Output Voltage | V _{OL} | 1 3 | 6,7 | 6,7 | | | | 16 16 |
| High Threshold Voltage | V _{OHA} | 1 3 | 6 6 | | 7 | 7 | | 16 16 |
| Low Threshold Voltage | V _{OLA} | 1 3 | 6 6 | | 7 | 7 | | 16 16 |
| Switching Times (50Ω Load) | | | +6.0 V | Pulse In | Pulse Out | | | +2.0 V |
| Propagation Delay (+3.5Vdc to 50%) ¹ | t ₆₊₁₊ | 1 | 7 | 6 | 1 | | | 16 |
| | t ₆₋₁₋ | 1 | 7 | 6 | 1 | | | 16 |
| | t ₇₊₁₊ | 1 | 6 | 7 | 1 | | | 16 |
| | t ₇₋₁₋ | 1 | 6 | 7 | 1 | | | 16 |
| | t ₇₊₃₋ | 3 | 6 | 7 | 3 | | | 16 |
| | t ₇₋₃₊ | 3 | 6 | 7 | 3 | | | 16 |
| Rise Time (20 to 80%) | t ₁₊ | 1 | 6 | 7 | 1 | | | 16 |
| Fail Time (20 to 80%) | t ₁₋ | 1 | 6 | 7 | 1 | | | 16 |

1. See switching time test circuit. Propagation delay for this circuit is specified from +1.5Vdc in to the 50% point on the output waveform. The +3.5Vdc is shown here because all logic and supply levels are shifted 2 volts positive.

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ELECTRICAL CHARACTERISTICS (continued)

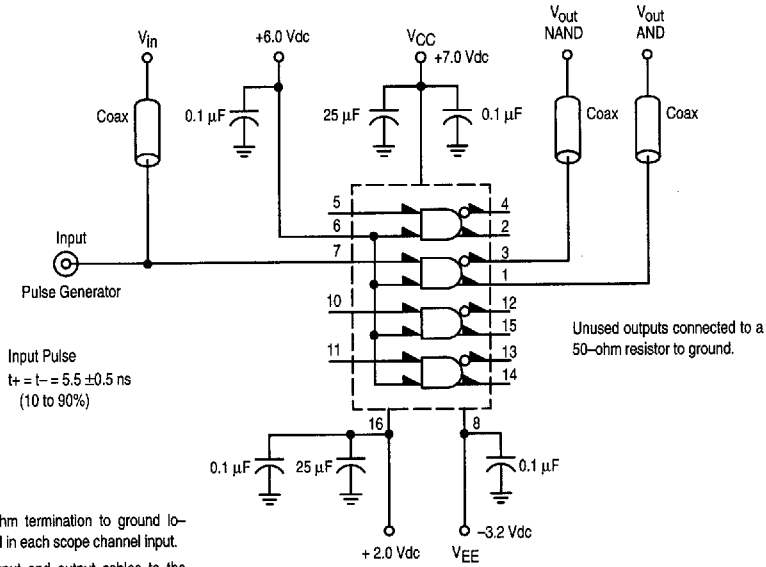
| | | | TEST VOLTAGE VALUES (Volts) | | | (mA) | | |
|---|-------------------|----------------|---|-----------------|-----------------|----------------|-----------------|----------------|
| | | | V _R | V _{CC} | V _{EE} | I _I | I _{in} | |
| @ Test Temperature | | | | | | | | |
| | | | -30°C | +2.40 | +5.00 | -5.2 | -10 | +1.0 |
| | | | +25°C | +2.40 | +5.00 | -5.2 | -10 | +1.0 |
| | | | +85°C | +2.40 | +5.00 | -5.2 | -10 | +1.0 |
| Characteristic | Symbol | Pin Under Test | TEST VOLTAGE APPLIED TO PINS LISTED BELOW | | | | | Gnd |
| | | | V _R | V _{CC} | V _{EE} | I _I | I _{in} | |
| Negative Power Supply Drain Current | I _E | 8 | | 9 | 8 | | | 16 |
| Positive Power Supply Drain Current | I _{CCH} | 9 | | 9 | 8 | | | 16 |
| | I _{CCL} | 9 | | 9 | 8 | | | 5,6,7,10,11,16 |
| Reverse Current | I _R | 6 | 6 | 9 | 8 | | | 16 |
| | | 7 | 7 | 9 | 8 | | | 16 |
| Forward Current | I _F | 6 | | 9 | 8 | | | 16 |
| | | 7 | | 9 | 8 | | | 16 |
| Input Breakdown Voltage | BV _{in} | 6 | | 9 | 8 | | 6 | 5,7,10,11,16 |
| | | 7 | | 9 | 8 | | 7 | 6,16 |
| Clamp Input Voltage | V _I | 6 | | 9 | 8 | 6 | | 16 |
| | | 7 | | 9 | 8 | 7 | | 16 |
| High Output Voltage | V _{OH} | 1 | | 9 | 8 | | | 16 |
| | | 3 | | 9 | 8 | | | 16 |
| Low Output Voltage | V _{OL} | 1 | | 9 | 8 | | | 16 |
| | | 3 | | 9 | 8 | | | 16 |
| High Threshold Voltage | V _{OHA} | 1 | | 9 | 8 | | | 16 |
| | | 3 | | 9 | 8 | | | 16 |
| Low Threshold Voltage | V _{OLA} | 1 | | 9 | 8 | | | 16 |
| | | 3 | | 9 | 8 | | | 16 |
| Switching Times (50Ω Load) | | | | +7.0 V | -3.2 V | | | +2.0 V |
| Propagation Delay (+3.5Vdc to 50%) ¹ | t ₆₊₁₊ | 1 | | 9 | 8 | | | 16 |
| | t ₆₋₁₋ | 1 | | 9 | 8 | | | 16 |
| | t ₇₊₁₊ | 1 | | 9 | 8 | | | 16 |
| | t ₇₋₁₋ | 1 | | 9 | 8 | | | 16 |
| | t ₇₊₃₋ | 3 | | 9 | 8 | | | 16 |
| | t ₇₋₃₊ | 3 | | 9 | 8 | | | 16 |
| Rise Time (20 to 80%) | t ₁₊ | 1 | | 9 | 8 | | | 16 |
| Fall Time (20 to 80%) | t ₁₋ | 1 | | 9 | 8 | | | 16 |

1. See switching time test circuit. Propagation delay for this circuit is specified from +1.5Vdc in to the 50% point on the output waveform. The +3.5Vdc is shown here because all logic and supply levels are shifted 2 volts positive.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

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SWITCHING TIME TEST CIRCUIT



50-ohm termination to ground located in each scope channel input. All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

NOTE: All power supply and logic levels are shown shifted 2 volts positive.

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