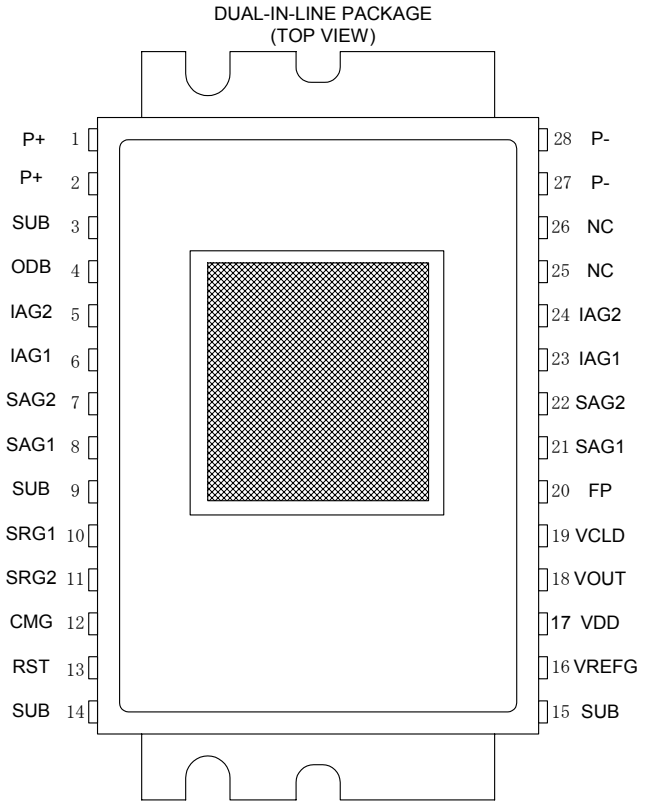
- **Very Low Noise, Very High Sensitivity, Electronically Variable Charge Domain Gain**
- **High Resolution, 2/3-in Format, Solid State Charge-Coupled Device (CCD) Frame Transfer Image Sensor for low light level applications with 30-Frame/s readout speed.**
- **1,006,008 Pixels per Field**
- **Frame Memory**
- **1004 (H) x 1002 (V) Active Pixels in Image Sensing Area Compatible With Electronic Centering**
- **Multimode Readout Capability**
  - **Progressive Scan**
  - **Line Summing**
  - **Pixel Summing**
- **Serial Register 0-8V Clocking (except CMG gate)**
- **Continuous Electronic Exposure Control from 1/30 s to 1/5,000 s**
- **8.0 um Square Pixels**
- **Advanced Lateral Overflow Drain**
- **Low Dark Current**



- **High Photo response Uniformity Over a Wide Spectral Range**
- **Solid State Reliability With No Image Burn-in, Residual Imaging, Image Distortion, Image Lag, or Microphonics**
- **Package with peltier cooler**

Description

The TC285SPD is a 1004x1002 30-Frame/s readout, frame-transfer CCD image sensor designed for use in black and white, bio-medical, and special-purpose applications requiring high sensitivity, high speed, high resolution, and low noise.

The TC285SPD is a new device of the *IMPACTRON*™ family of very-low noise, high sensitivity, high-speed, and high-resolution image sensors that multiply charge directly in

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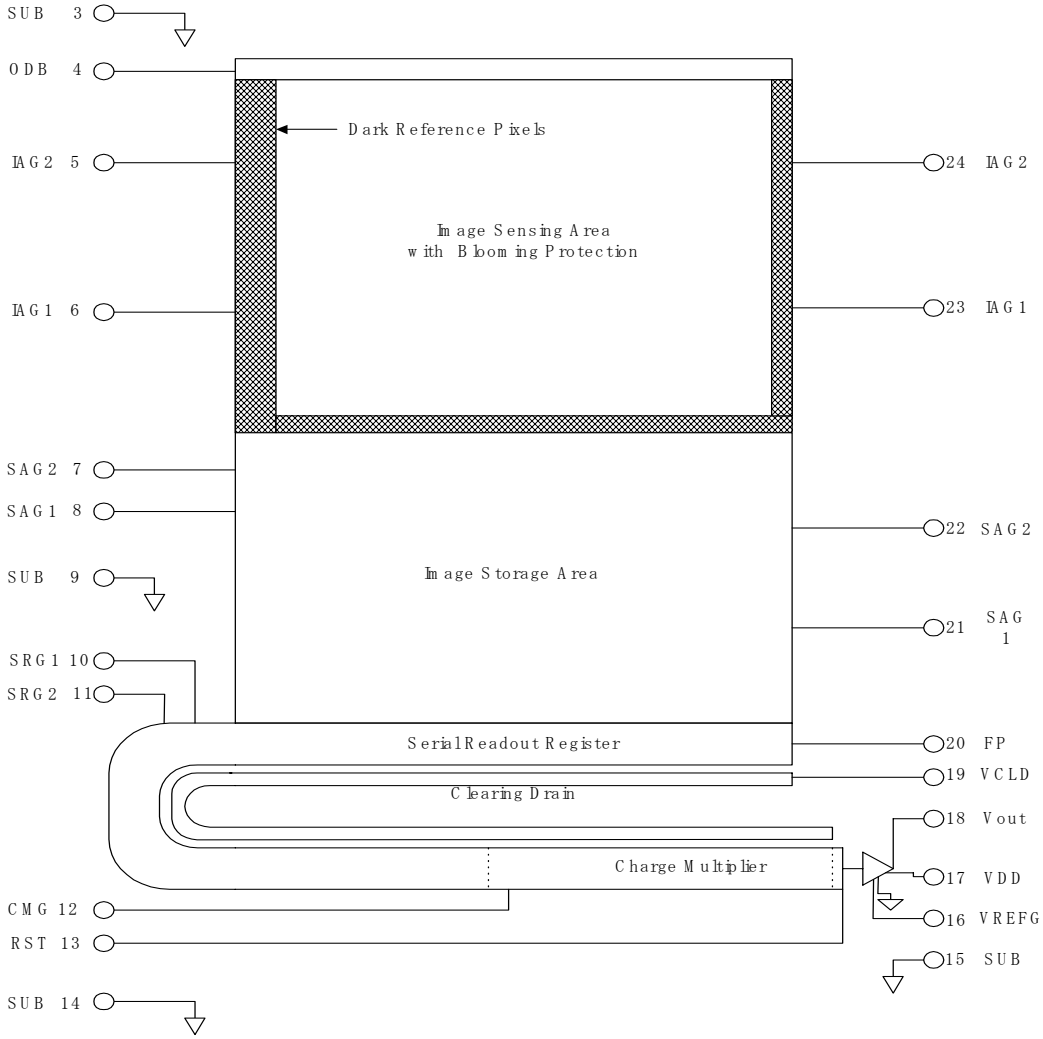
the charge domain before conversion to voltage. The charge carrier multiplication (CCM) is achieved by using a low-noise single-carrier, impact ionization process that occurs during repeated carrier transfers through high field regions. Applying multiplication pulses to specially designed gates activates the CCM. The amount of multiplication gain is adjustable depending on the amplitude of multiplication pulses. The device function resembles the function of an image intensifier implemented in solid state.

The image-sensing area of the TC285SPD is configured into 1002 lines with 1004 pixels in each line. 28 pixels are reserved in each line for dark reference. The blooming protection is based on an advanced lateral overflow drain concept that does not reduce NIR response. The sensor can be operated in the progressive scan mode and can capture a full 1,006,008 pixels in one image field. The frame transfer from the image sensing area to the memory area is accomplished at a high rate that minimizes image smear. The electronic exposure control is achieved by clearing the unwanted charge from the image area using a short positive pulse applied to the anti-blooming drain. This marks the beginning of the integration time, which can be arbitrarily shortened from its nominal length. After charge is integrated and stored in the memory it is available for readout in the next cycle. This is accomplished by using a unique serial register design that includes special charge multiplication pixels.

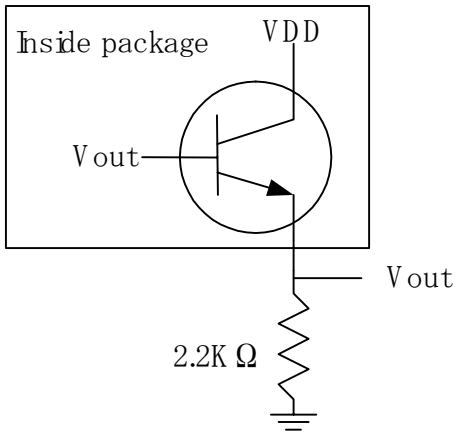
The TC285SPD sensor is built using TI-proprietary advanced Split-Gate Virtual-Phase CCD (SGVPCCD) technology, which provides devices with wide spectral response, high quantum efficiency (QE), low dark current, and high response uniformity.

This MOS device contains limited built-in ESD protection. During storage or handling, the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to Vss. Under no circumstances should pin voltages exceed absolute maximum ratings. Avoid shorting OUT to Vss during operation to prevent damage to the amplifier. The device can also be damaged if the output and ADB terminals are reverse-biased and excessive current is allowed to flow. Specific guidelines for handling devices of this type are contained in the publication “Guidelines for Handling Electrostatic-Discharge-Sensitive (ESD) Devices and Assemblies” available from Texas Instruments.

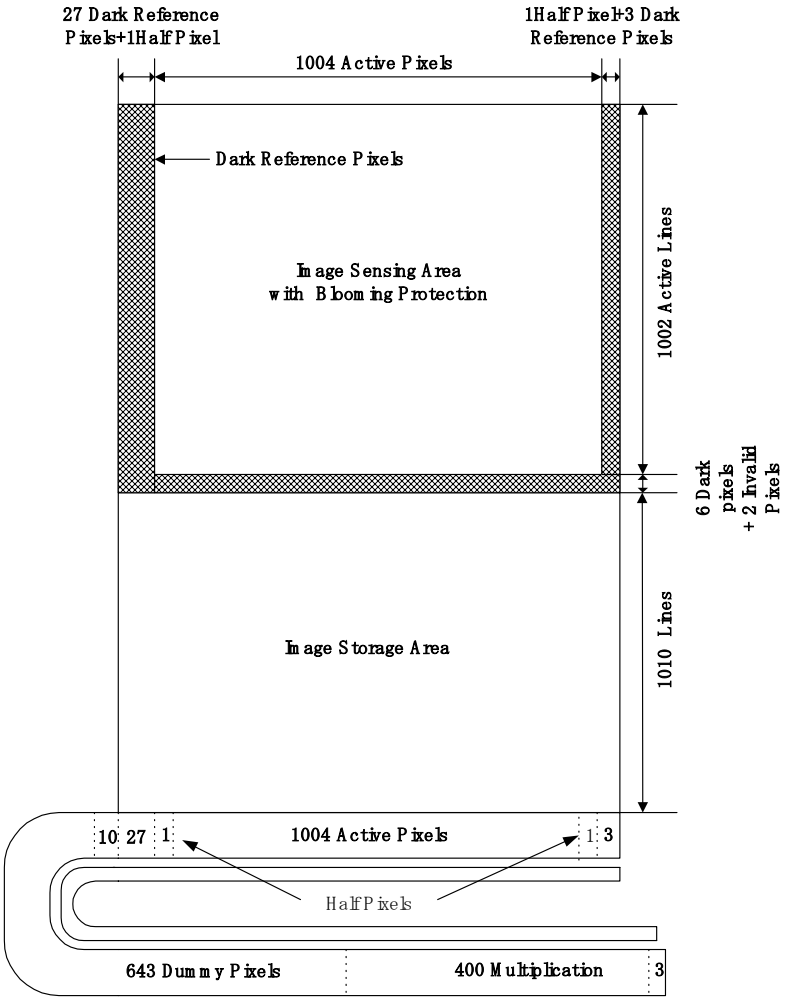
Functional block diagram



** TC285SPD includes an output bipolar transistor in the package. For a proper operation it is necessary to connect a 2.2kOhm-loading resistor externally to the VOUT pin.


Inside package
VDD
Vout
Vout
2.2K Ω

Sensor Topology diagram



Terminal functions

Terminal name	No.	I/O	Description
VDD	17	I	Supply voltage for amplifiers
VCLD	19	I	Supply voltage for Clearing drain & ESD circuits
IAG1	6,23	I	Image area gate-1
IAG2	5,24	I	Image area gate-2
ODB	4	I	Supply voltage for anti-blooming drain
OUT	18	O	Output signal, multiplier channel
SAG1	8,21	I	Storage area gate-1
SAG2	7,22	I	Storage area gate-2
SRG1	10	I	Serial register gate-1
SRG2	11	I	Serial register gate-2
CMG	12	I	Charge multiplication gate
RST	13	I	Reset gate
FP	20	I	Field plate (See Figure 3)
VREFG	16	I	Amplifier reference gate
SUB	3,9,14,15	-	Chip substrate
P+	1,2	-	Peltier cooler power supply -positive
P-	27,28	-	Peltier cooler power supply -negative

Detailed description

The TC285SPD consists of five basic functional blocks: The image-sensing area, the image–storage area, the serial register, the charge multiplier, and the charge detection node with buffer amplifier. The location of each of these blocks is identified in the functional block diagram.

Image-sensing and storage areas

Figure 1 and Figure 2 show the pixel cross-section with potential-well diagram and top views of pixels in the image-sensing and storage areas. As light enters the silicon in the image-sensing area, electrons are generated and collected in potential wells of the pixels. Applying a suitable dc bias to the anti blooming drain provides blooming protection. The electrons that exceed a specific level, determined by the ODB bias, are drained away from the pixels. If it is necessary to remove all previously accumulated charge from the wells a short positive pulse is applied to the drain. This marks the beginning of the new integration period. After the integration cycle is completed, charge is quickly transferred into the memory where it waits for readout. The lines can be read out from the memory in a sequential order to implement progressive scan. 28 columns at the left edge and 4 columns at the right edge of the image-sensing area are shielded from the incident light. These pixels provide the dark reference used in subsequent video-processing circuits to restore the video-black level. Additionally, 6 dark lines, located between the image sensing area and the image-storage area, were added to the array for isolation.

Advanced lateral overflow drain

The advanced lateral overflow drain structure is shared by two neighboring pixels in each line. By varying the DC bias of the anti-blooming drain it is possible to control the blooming protection level and trade it for well capacity. Applying a pulse to the drain, approximately 6V above the nominal level, for a minimum of 100μs(3H), removes all charge from the pixels. This feature permits precise control of the integration time on a frame-by-frame basis. The single-pulse clearing capability also reduces smear by eliminating accumulated charge in pixels before the start of the integration period (single sided smear).

Serial register and charge multiplier

The serial register of TC285SPD image sensor consists of only poly-silicon gates. It operates at high speed, being clocked from 0V to 8V. This allows the sensor to work at 30 frames/s. The serial register is used for transporting charge stored in the pixels of the memory lines to the output amplifier. The TC285SPD device has a serial register with twice the standard length. The first half has a conventional design that interfaces with the memory as it would in any other CCD sensor. The second half, however, is unique and includes 400 charge multiplication stages with a number of dummy pixels that are needed to transport charge between the active register blocks and the output amplifier. Charge is multiplied as it progresses from stage to stage in the multiplier toward the charge detection node. The charge multiplication level depends on the amplitude of the multiplication pulses (approximately 15V~22V) applied to the multiplication gate. Due to the double length of the register, first 2 lines in each field or frame scan do not contain valid data and should be discarded.

Charge detection node and buffer amplifier

The last element of the charge detection and readout chain is the charge detection node with the buffer amplifier. The charge detection node is using a standard Floating Diffusion (FD) concept followed by an on-chip dual-stage source-follower buffer. Another bipolar transistor (third stage) has been included in the sensor package to improve the driving capability at high speed. A load for the bipolar transistor (2.2kOhm) needs to be connected externally from the package output pin to SUB. Applying a pulse to the RST pin resets the detection node. Pixel charge summing function can be easily implemented by skipping the RST pulses. To achieve the ultimate sensor performance it is necessary to eliminate kTC noise. This is typically accomplished by using CDS (correlated double sampling) processing techniques. *IMPACTRON*™ devices have the potential for detecting single electrons (photons) when cooled or when sufficiently short integration times are used.

Absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage range, Vss: VDD, VCLD (see Note1) …… 0V to + 15V
Supply voltage range, Vss: ODB…… 0V to + 22V
Supply voltage range, Vss: FP, VREFG …… 0V to + 8V
Input voltage range, Vi: IAG, SAG……. …… - 8V to + 8V
Input voltage range, Vi: SRG, RST…… 0V to + 10V
Input voltage range, Vi: CMG …… -5V to + 23V
Supply voltage range, Vcool: P+ (see Note2)…….. 0V to + 7V
Supply current range, Icool: P+ (see Note2) …… 0A to 1.8A
Operating free-air temperature range, Ta …… -10°C to 45°C
Storage temperature range, Tstg …… -30°C to 85°C
Operating case temperature range ……..…..…..……-10°C to 55°C
Dew point of package inside gas (see Note2)…….…..…… Less than -20°C

* Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect the device reliability.

Note 1: All voltage values are with respect to substrate terminal.
Note 2: Peltier cooler generates heat during cooling process. To keep the case temperature range, the heat must be removed through an external heat sink. See Figure 12 for reference of CCD temperature vs Icool. In order to avoid condensation upon the surface do not cool the CCD to less than -20 degrees C.
Be careful when attaching external heat sink to package. Fastening it too strongly may crack or puncture the package, making it susceptible to moisture or humidity.

Recommended operating conditions

Description				MIN	NOM	MAX	UNIT
Substrate bias, Vss					0		V
Supply voltage, Vdd*	VDD, VCLD			13.5	14.0	14.5	
	ODB	For blooming control		4.9	5.2	5.5	
		For clearing		12.0	12.5	13.0	
	FP				1.5		
	VREFG **			5.0	5.5	6.0	
Input voltage, Vi *	IAG1***		High	3.2	3.5	3.8	V
			Low	-6.0	-5.7	-5.4	
	IAG2***		High	2.9	3.2	3.5	
			Low	-6.0	-5.7	-5.4	
	SAG1***		High	3.2	3.5	3.8	
			Low	-6.0	-5.7	-5.4	
	SAG2***		High	2.9	3.2	3.5	
			Low	-6.0	-5.7	-5.4	
	SRG1		High	7.5	7.8	8.1	
			Low		0.0		
	SRG2		High	7.5	7.8	8.1	
			Low		0.0		
	CMG****		High	7.0		22.0	
			Low	-4.1	-3.8	-3.5	
	RST		High	5.5	6.0	6.5	
			Low		0.0		
Clock Frequency, fck	IAG1, IAG2, SAG1, SAG2				1.0		MHz
	SRG1, SRG2, CMG ,RST				35.0		
Load capacitance	OUT					6.0	pF
Inside dew point of a package*****						-20	°C
Operating free-air temperature				-10	25	45	°C

* Fine-tuning of input voltages may be required to obtain the best charge transfer efficiency.
** For proper operation it is necessary to keep VREFG bias lower than RST High voltage
*** Refer to Figure 6 for a description of the waveforms applied to IAG and SAG by typical driver circuits operated at the H and L voltage settings specified in these recommended operating conditions.
**** Charge multiplication gain depends on high level of the CMG and temperature. See figure 10.
***** -20 degrees should be the minimum temperature of the cooled CCD.

Electrical characteristics over recommended operating ranges of supply voltage at operating free-air temperature (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
Charge multiplication gain**		1	200	2000**	-
Excess noise factor for typical CCM gain (Note 3)		1	1.4		-
Dynamic range without CCM gain			66		dB
Dynamic range with typical CCM gain (Note 4)			72		dB
Charge conversion gain without CCM gain (Note 5)			14		uV/e
τ Signal-response delay time (Note6)			16		ns
Output resistance（Note 7）			320		Ω
Amp. Noise-equivalent signal without CCM gain *			20		e
Amp. Noise-equivalent signal with typ. CCM gain *				1.0	e
Response linearity with no CCM gain			1		-
Response linearity with typ. CCM gain			1		-
Charge-transfer efficiency (Note 8)	Parallel transfer	0.99994		1.0	
	Serial transfer	0.99994		1.0	-
Supply current without output bipolar transistor current			2.7	4	mA
Ci Input capacitance	IAG1		12.8		nF
	IAG2		13.5		
	IAG1-IAG2		6.8		
	SAG1		13.9		
	SAG2		14.5		
	SAG1-SAG2		7.78		
	SRG1		86.0		pF
	SRG2		69.0		
	CMG		24.0		
	ODB		3,000		
	RST		10		
	FP		127		
	VREFG		10		

All typical values are at Ta = 25 °C unless otherwise noted.
** Maximum CCM gain is not guaranteed.
* The values in the table are quoted using CDS = Correlated Double Sampling. CDS is a signal processing technique that improves performance by minimizing undesirable effects of reset noise.

Notes: 3. Excess Noise Factor "F" is defined as the ratio of noise sigma after multiplication divided by M times the noise sigma before multiplication where M is the charge multiplication gain.
4. Dynamic Range is –20 times the logarithm of the noise sigma divided by the saturation–output signal amplitude.
5. Charge conversion factor is defined as the ratio of output signal to input number of electrons.
6. Signal-response delay time is the time between the falling edge of the SRG1 pulse and the output-signal valid state.
7. Since the output bipolar transistor is carried out to the package, output resistance cannot be measured.

8. Charge transfer efficiency is one minus the charge loss per transfer in the CCD register. The test is performed in the dark using either electrical or optical input.

Optical characteristics

Ta = 25°C, Integration time = 16.67ms(unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
Sensitivity with typical CCM gain (Note 9)	No IR filter		5600		V/Lx*s
	With IR filter		700		
Sensitivity without CCM gain (Note 9)	No IR filter		28		V/Lx*s
	With IR filter		3.5		
Saturation signal output no CCM gain (Note 10)			600		mV
Saturation signal output Anti blooming Enable no CCM gain(Note 10)			180		
Saturation signal output with typ. CCM gain (Note10)			1100		
Zero input offset output (Note 11)			90		
Blooming overload ratio (Note 12)			1000:1		-
Image area well capacity			40k		
Smear (Note 13)			-44		dB
Dark current (Note 14)*			0.005	0.02	nA/cm^2
Dark signal (Note 15)*			0.005	0.02	mV
Dark-signal uniformity (Note 16)				0.3	mV
Dark-signal shading (Note 17)				0.2	mV
Spurious non-uniformity	Dark			10.0	mV
	Illuminated	-30%		30%	-
Column uniformity (Note 18)				1.5%	-
Electronic-shutter capability		1/5000		1/30	s

Notes:
9. Light source temperature is 2856 °K. The IR filter used is CM500 1mm thick.
10. Saturation is the condition in which further increase in exposure does not lead to further increases in output signal.
11. Zero input offset is the residual output signal measured from the reset level with no input charge present. This level is not caused by the dark current and remains approximately constant independent of temperature. It may vary with the amplitude of SRG1.
12. Blooming is the condition in which charge induced by light in one element spills over to the neighboring elements.
13. Smear is the measure of error signal introduced into the pixels by transferring them through the illuminated region into the memory. The illuminated region is 1/10 of the image area height. The value in the table is obtained for the integration time of 16.66ms and 1.0 MHz vertical clock transfer frequency.
14. Dark current depends on temperature and approximately doubles every 8 C^o. Dark current is also multiplied by CCM operation. The value given in the table is with the multiplier turned off and it is a calculated value.
15. Dark signal is actual device output measured in dark.
16. Dark signal uniformity is the sigma of difference of two neighboring pixels taking from all the image area pixels.
17. Dark signal shading is the difference between maximum and minimum of 5 pixel median taken anywhere in the array.
18. Column uniformity is obtain by summing all the lines in the array, finding the maximum of the difference of two neighboring columns anywhere in the array, and dividing the result by number of lines.

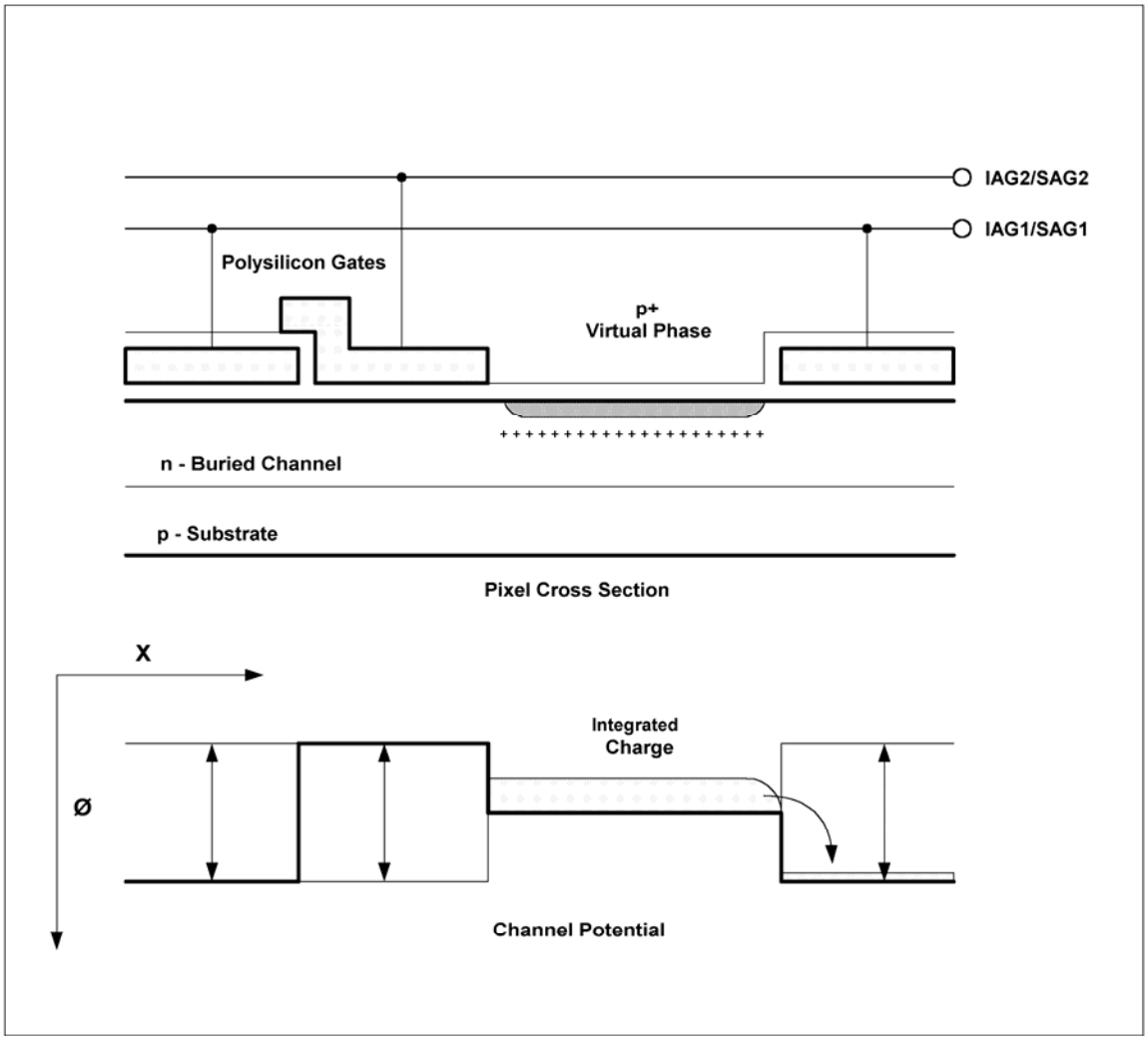


FIGURE 1. Image Aarea and Storage Area Pixel Cross Section with Potential Diagram

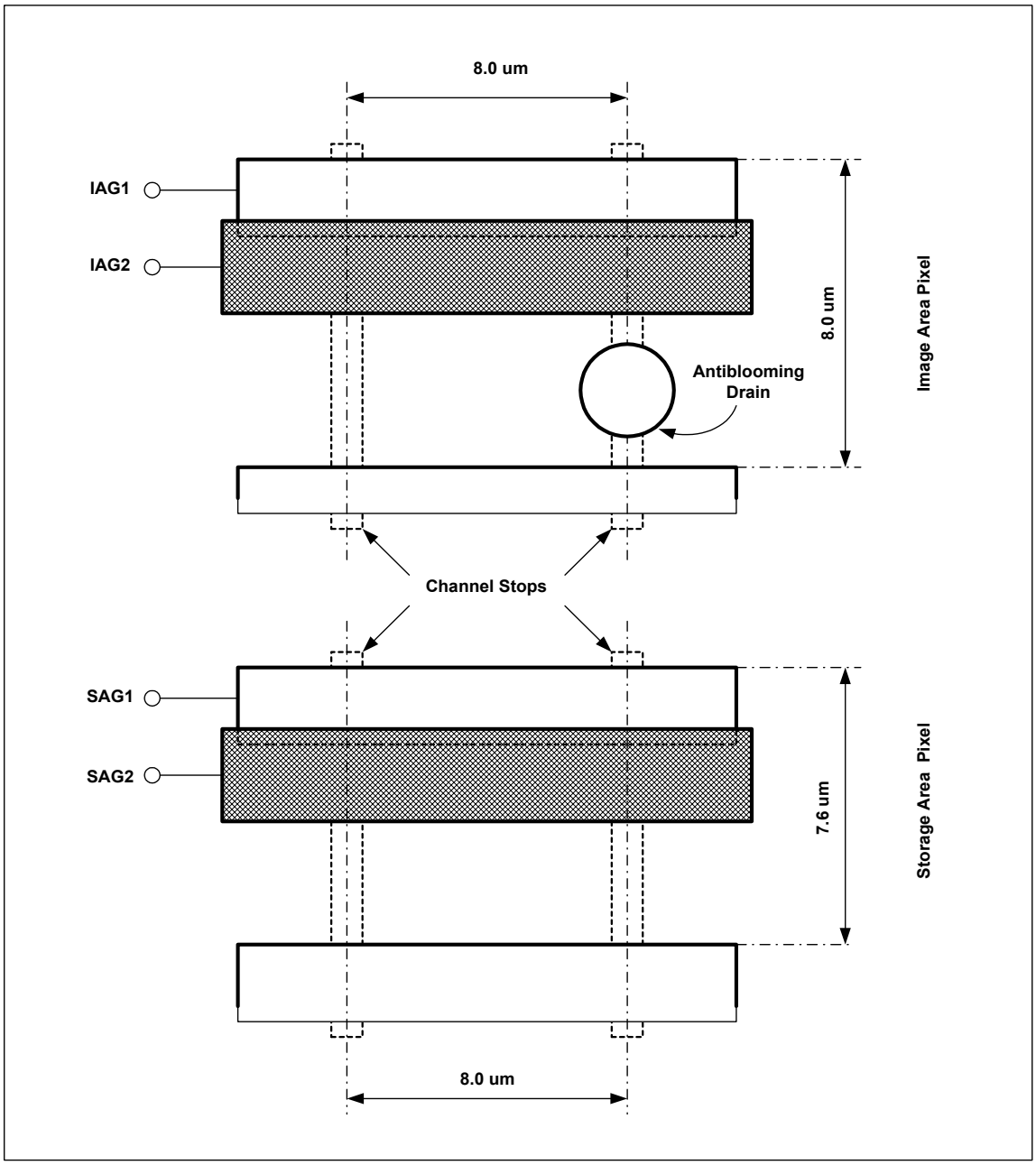
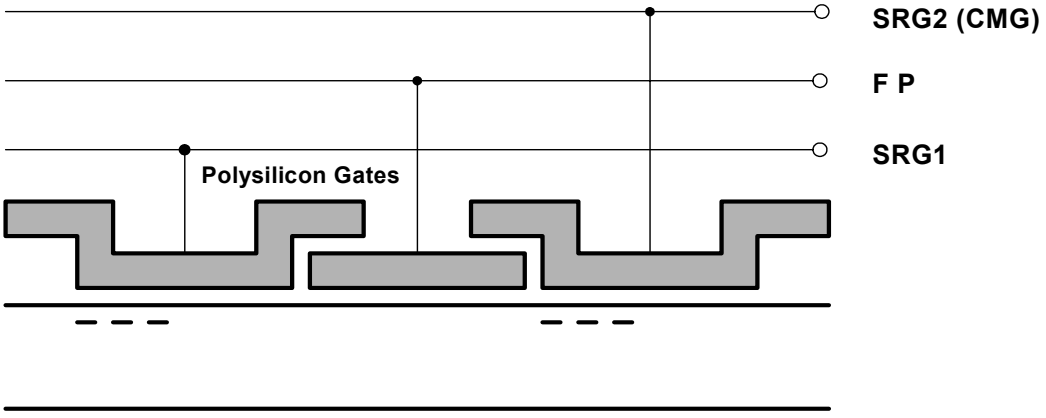
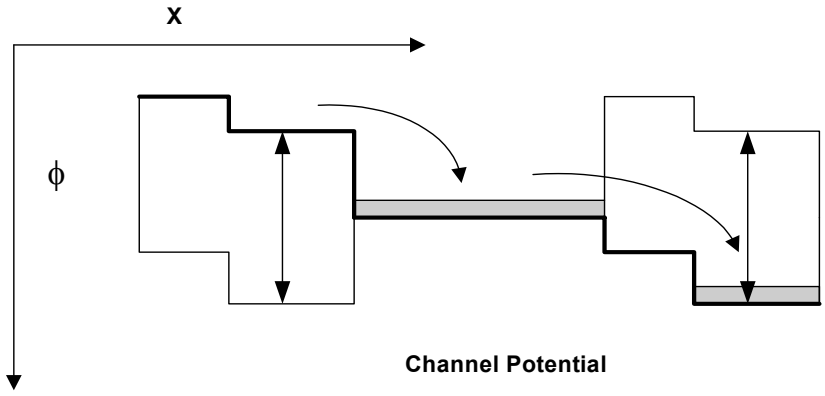


FIGURE 2. Image Area and Memory Area Pixel Topologies



Pixel Cross Section



Channel Potential

FIGURE 3. Serial Register Pixel Cross Section

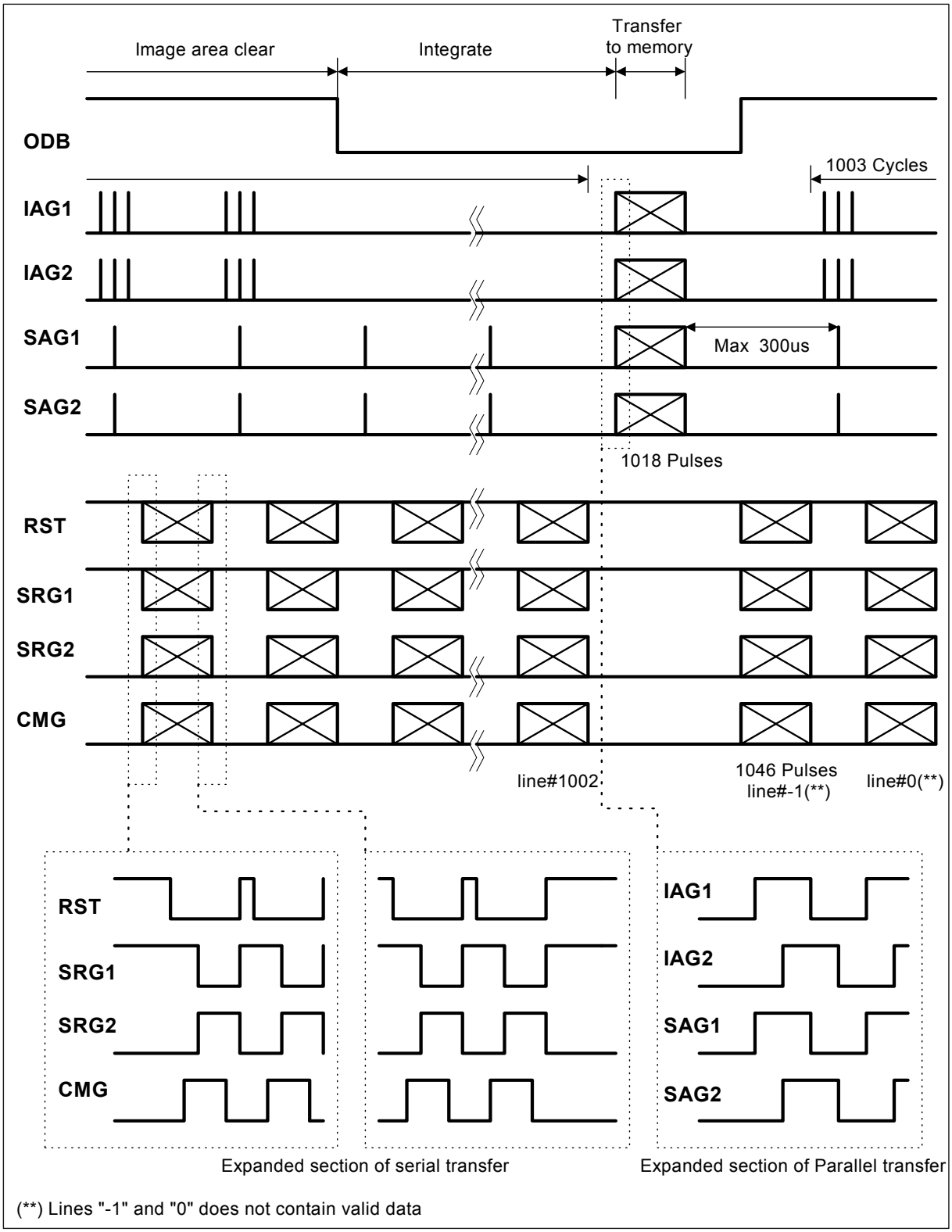
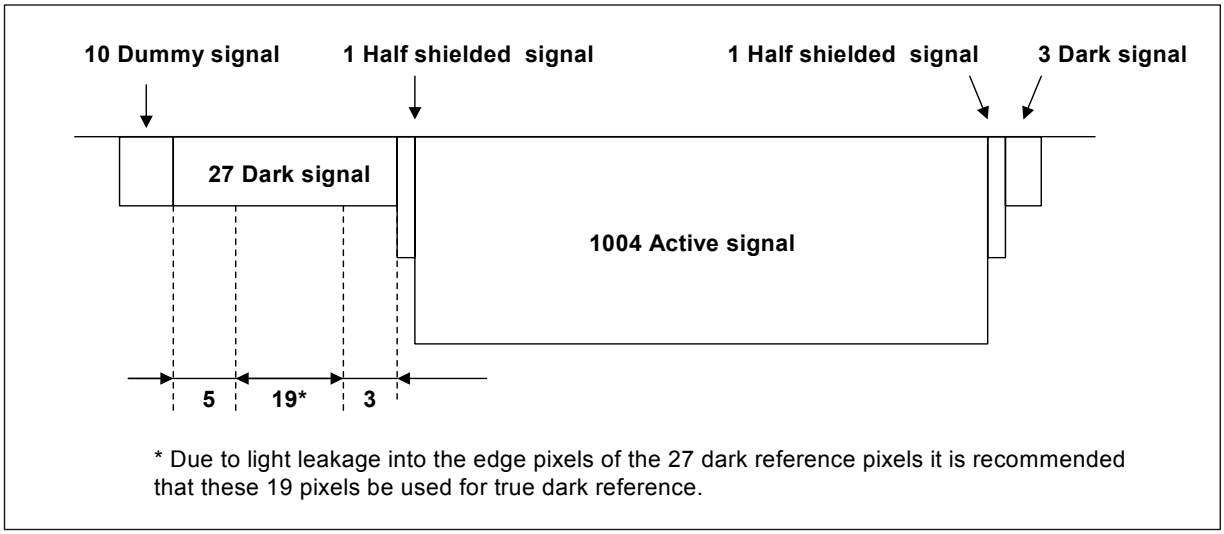


FIGURE 4. Progressive Scan Timing



* Due to light leakage into the edge pixels of the 27 dark reference pixels it is recommended that these 19 pixels be used for true dark reference.

FIGURE 5. Composition of output signal for a line

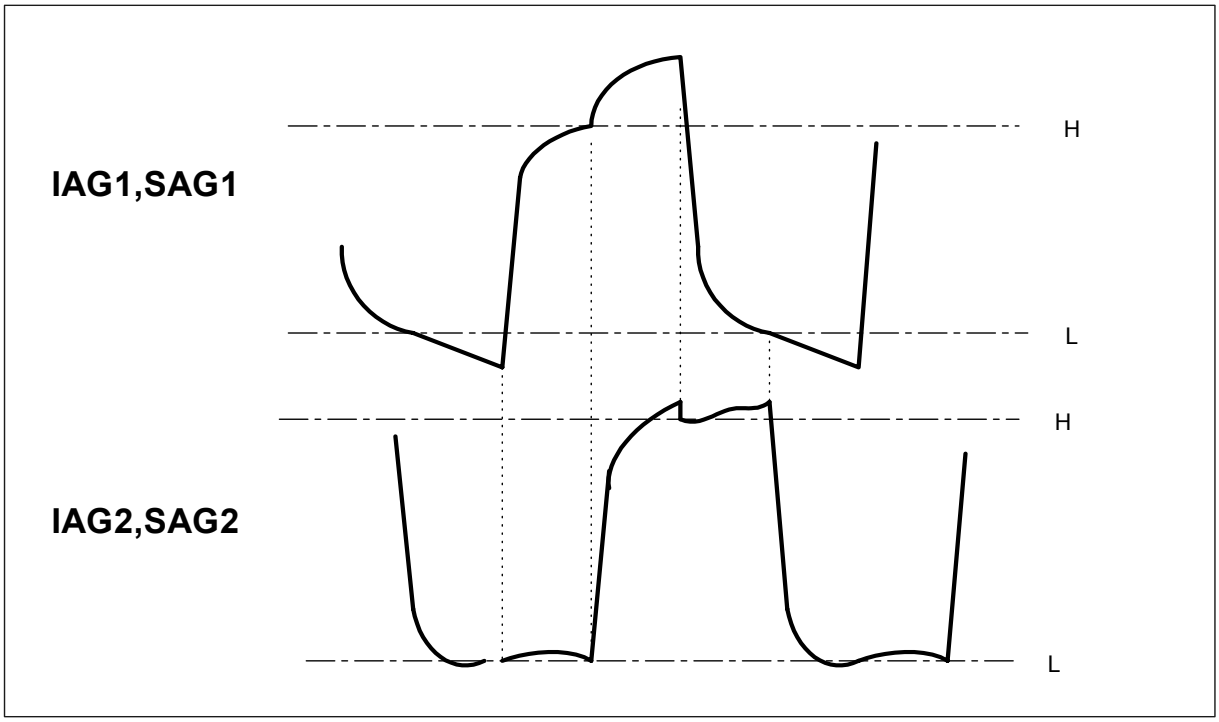
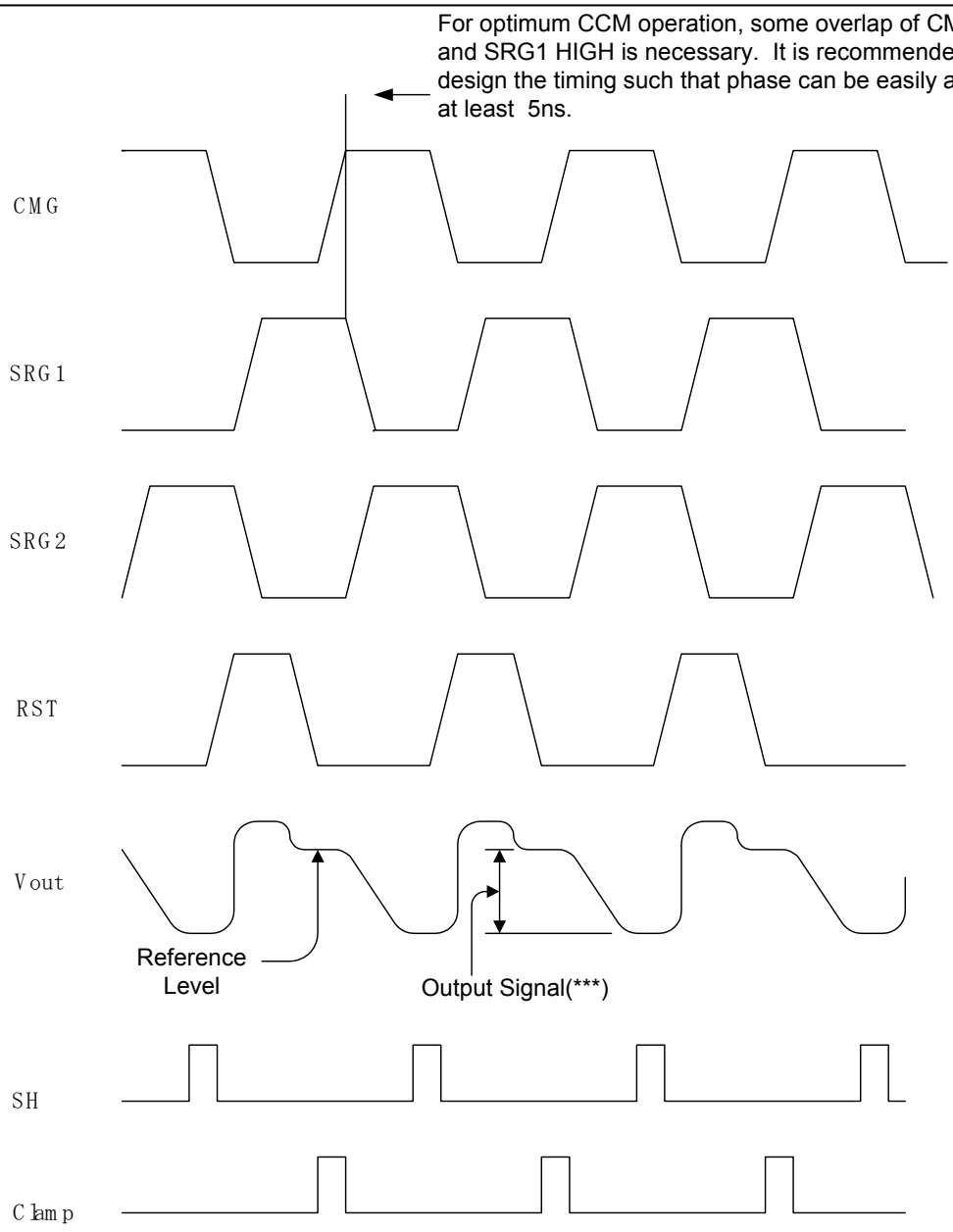


FIGURE 6. An example of parallel transfer waveform by typical driver circuit



(***) Output signal may not go all the way to zero. A zero offset of up to 100 mV may be present.

FIGURE 7. Detailed Serial Register Clock Timing for CDS Implementation.

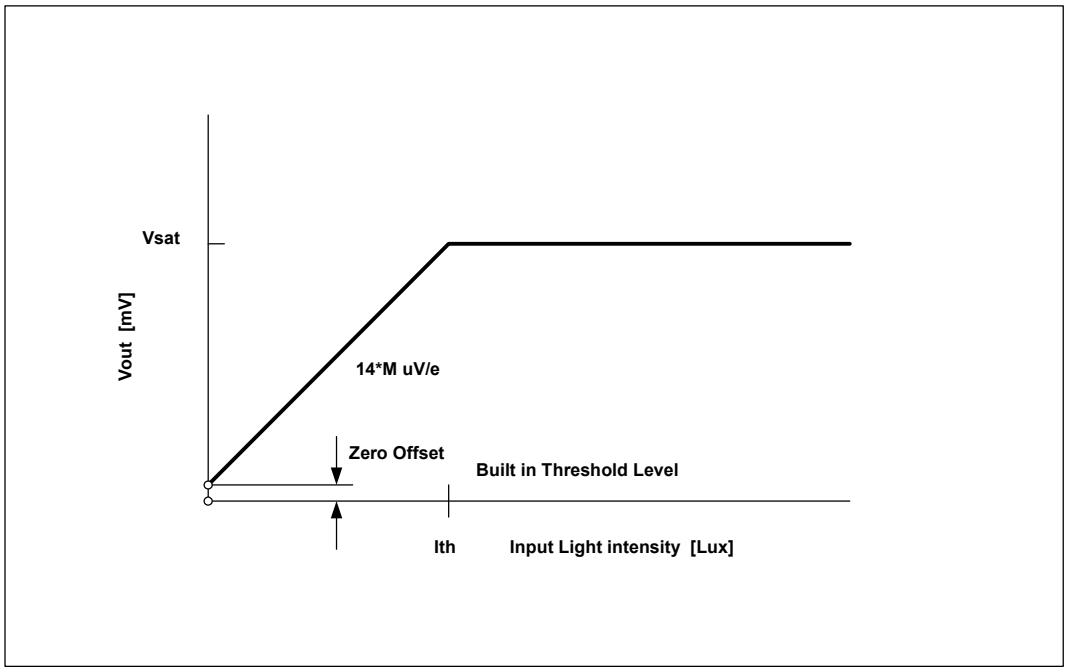


FIGURE 8. Photon Transfer Characteristic of CCD Outputs

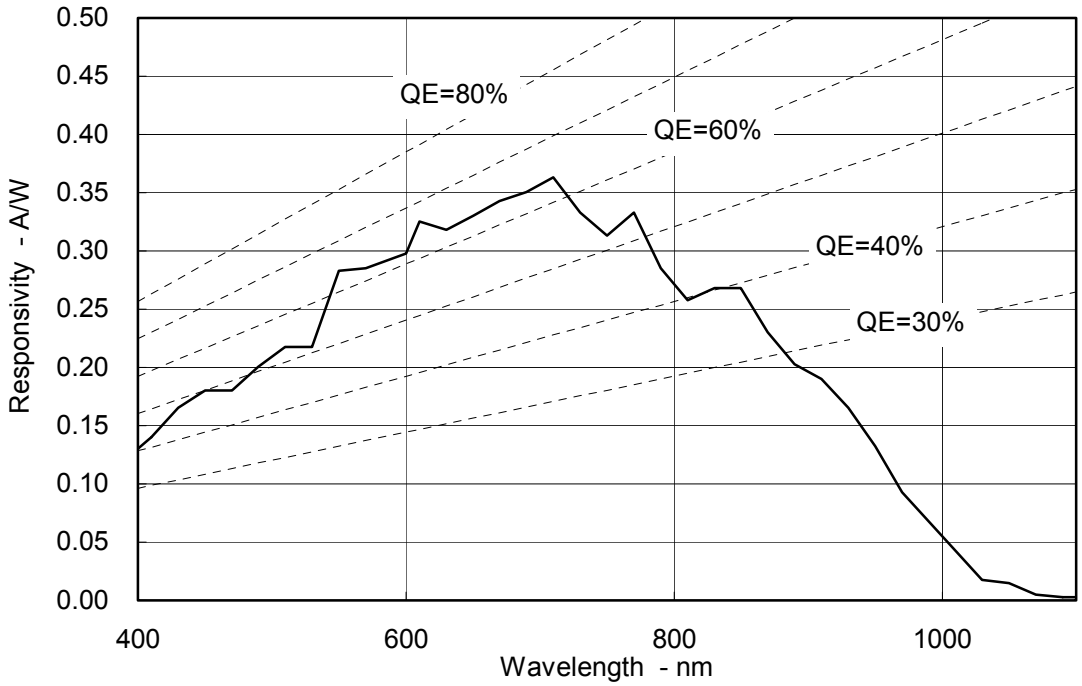
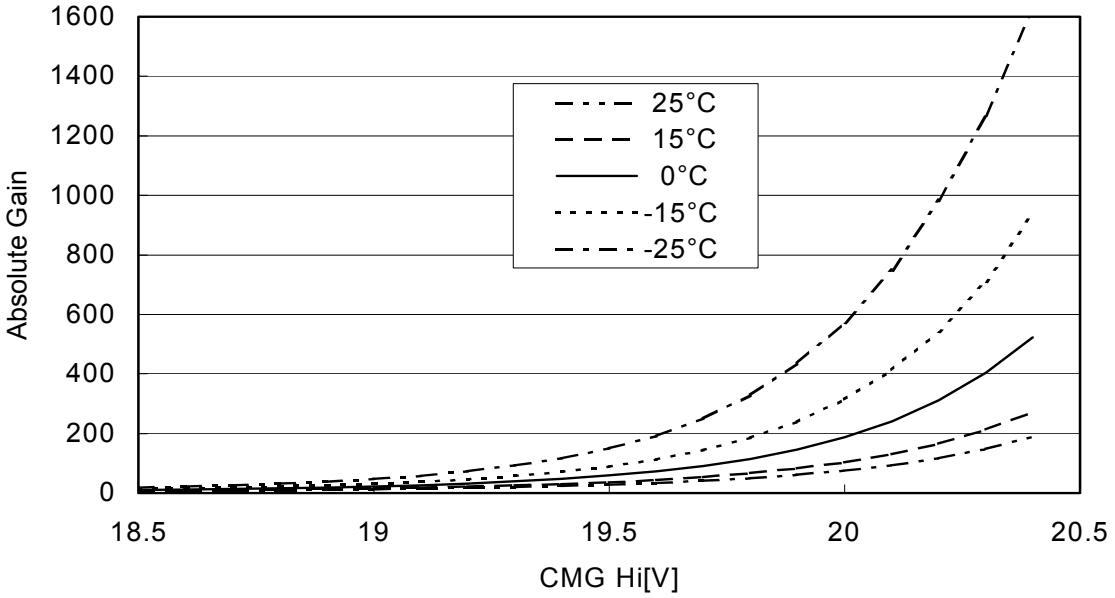


FIGURE 9. Typical Spectral Response

FIGURE 10. Typical CM gain as function of CMG high voltage



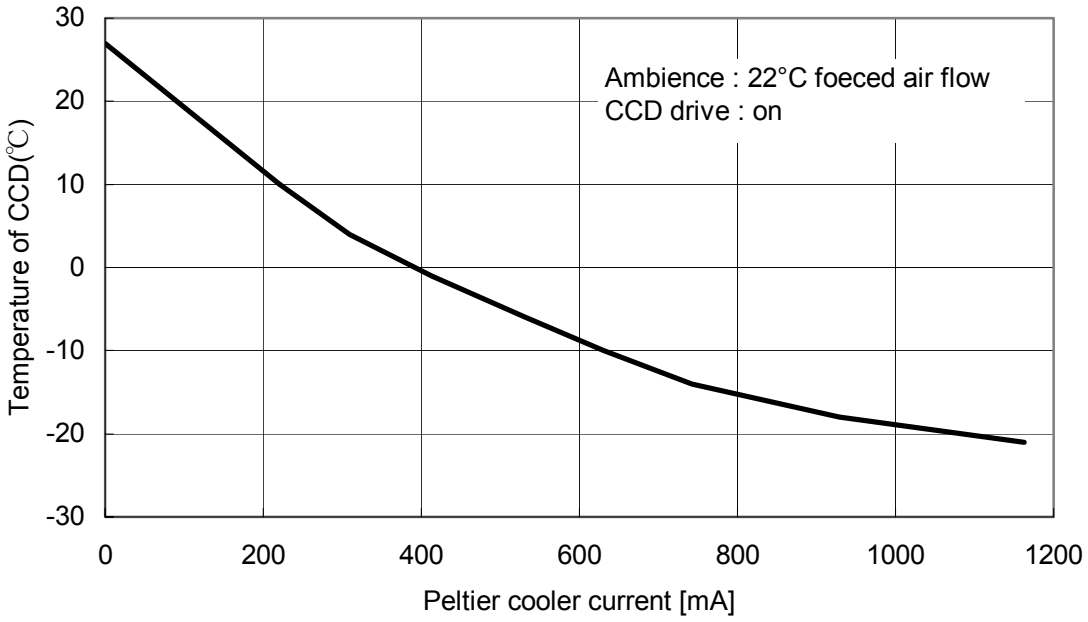


FIGURE 12. Typical cooling capability

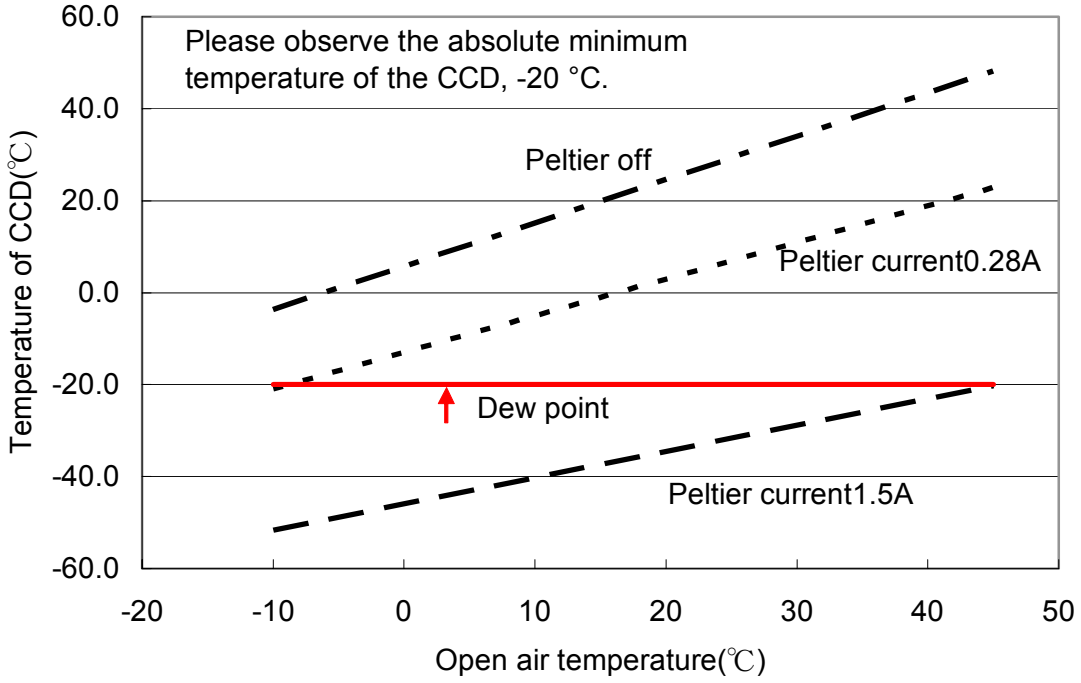
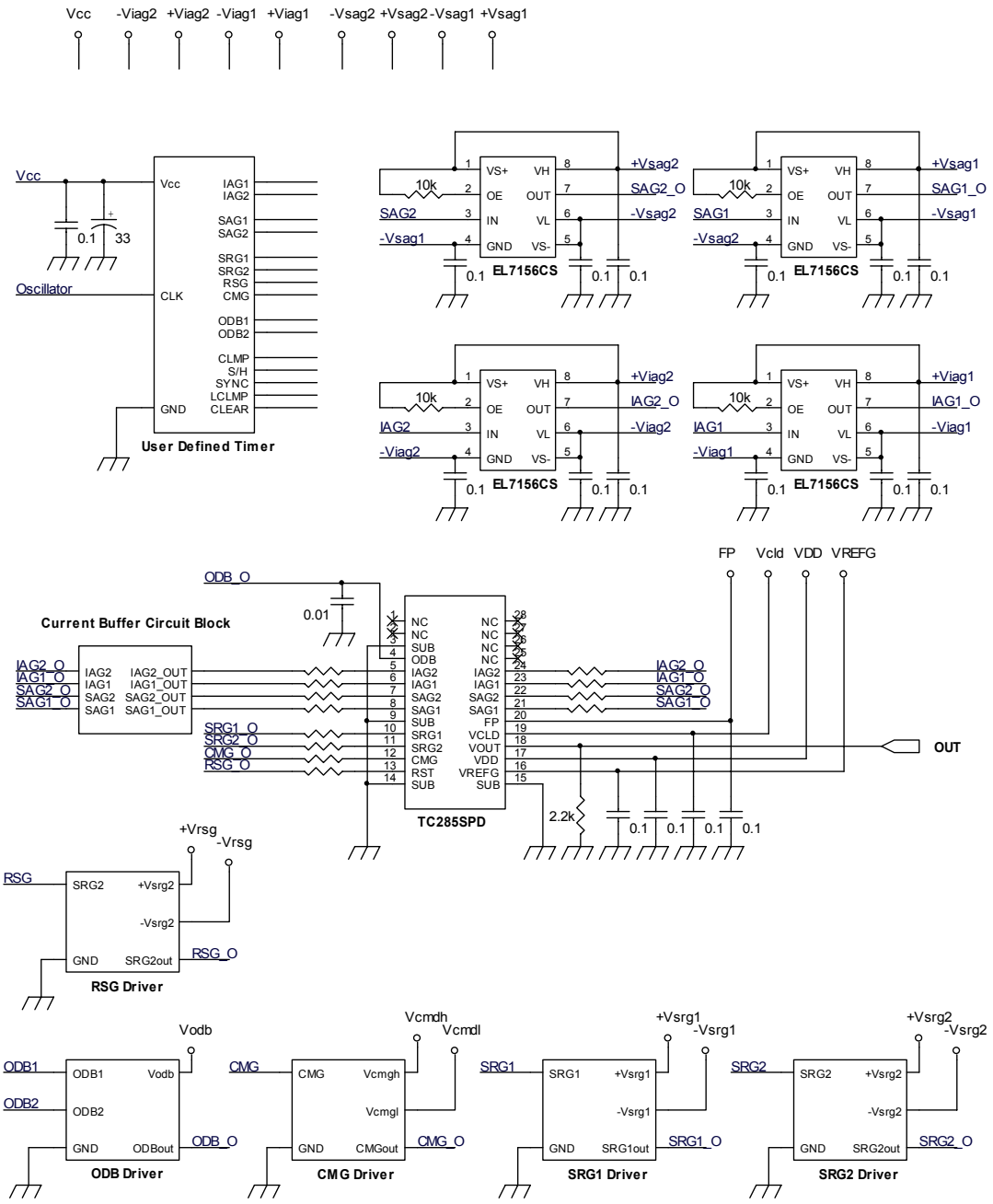


FIGURE 13. TC285-B0 Typical cooling characteristic

A heat dissipation board was attached to the back of the CCD package for measurement purposes.



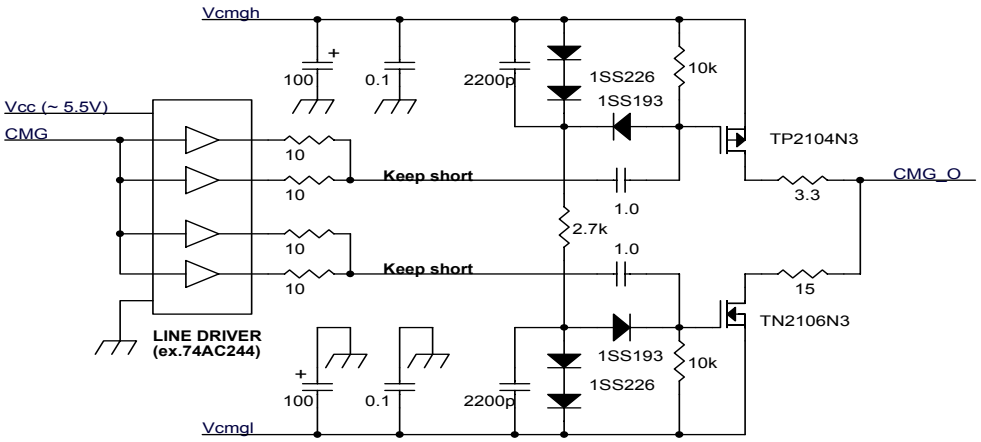
Notes: **A. All values are in Ohms and Microfarads unless otherwise noted.**

B. TI recommends AC coupled system for coupling to the next video processing circuits.

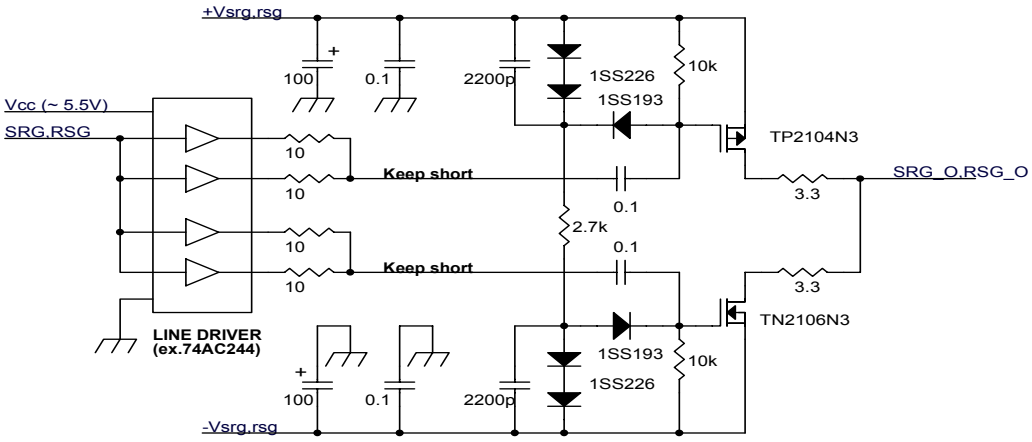
C. Damping resister on each driver lines are defined by the condition of user designed board (1.0 ~ 10 ohm recommended).

D. Please shift the GND levels of IAG and SAG at the output of "User Defined Timer" from GND to their appropriate -V as specified in the data sheet before inputting those signals into the EL7156CS driver ICs.

FIGURE 15. Typical Application Circuit Diagram



CMG Driver Circuit



SRG,RSG Driver Circuit

Notes: **A. All values are in Ohms and Microfarads unless otherwise noted.**

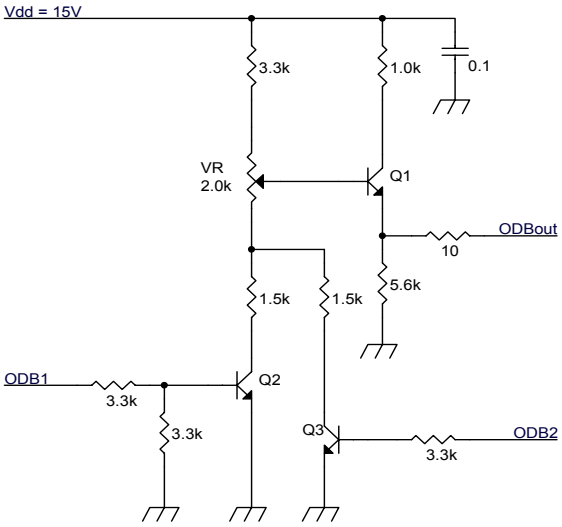
B. These circuits are implemented on TI's EVM285SPD with negative-swing.

C. In these circuits, line driver IC before AC couple should drive over 5.5V swing because of certain switching for discrete MOS-FETs (TP2104,TN2106).

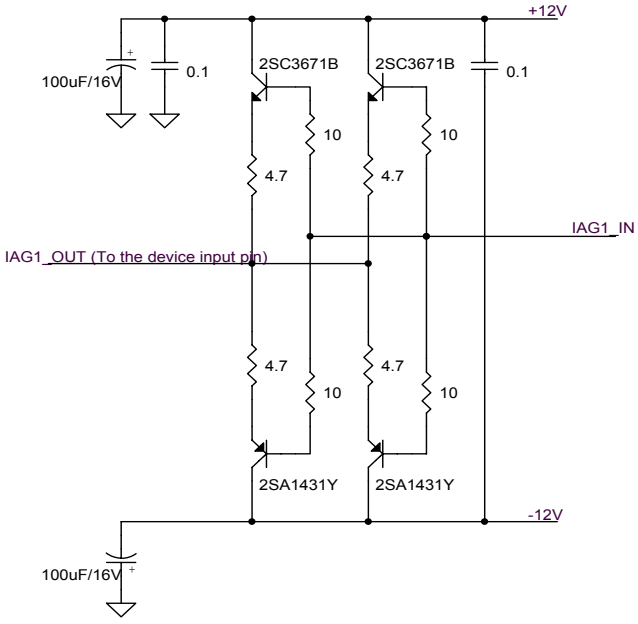
D. In these circuits, pre-driver line distance from line driver IC output to AC couple input should keep as short as it can.

E. The EL7156CS (Intersil/Elantec) driver is an acceptable alternative to the discreet SRG circuit shown.

FIGURE 16. Typical CMG and SRG Driver Circuits



ODB Driver Circuit



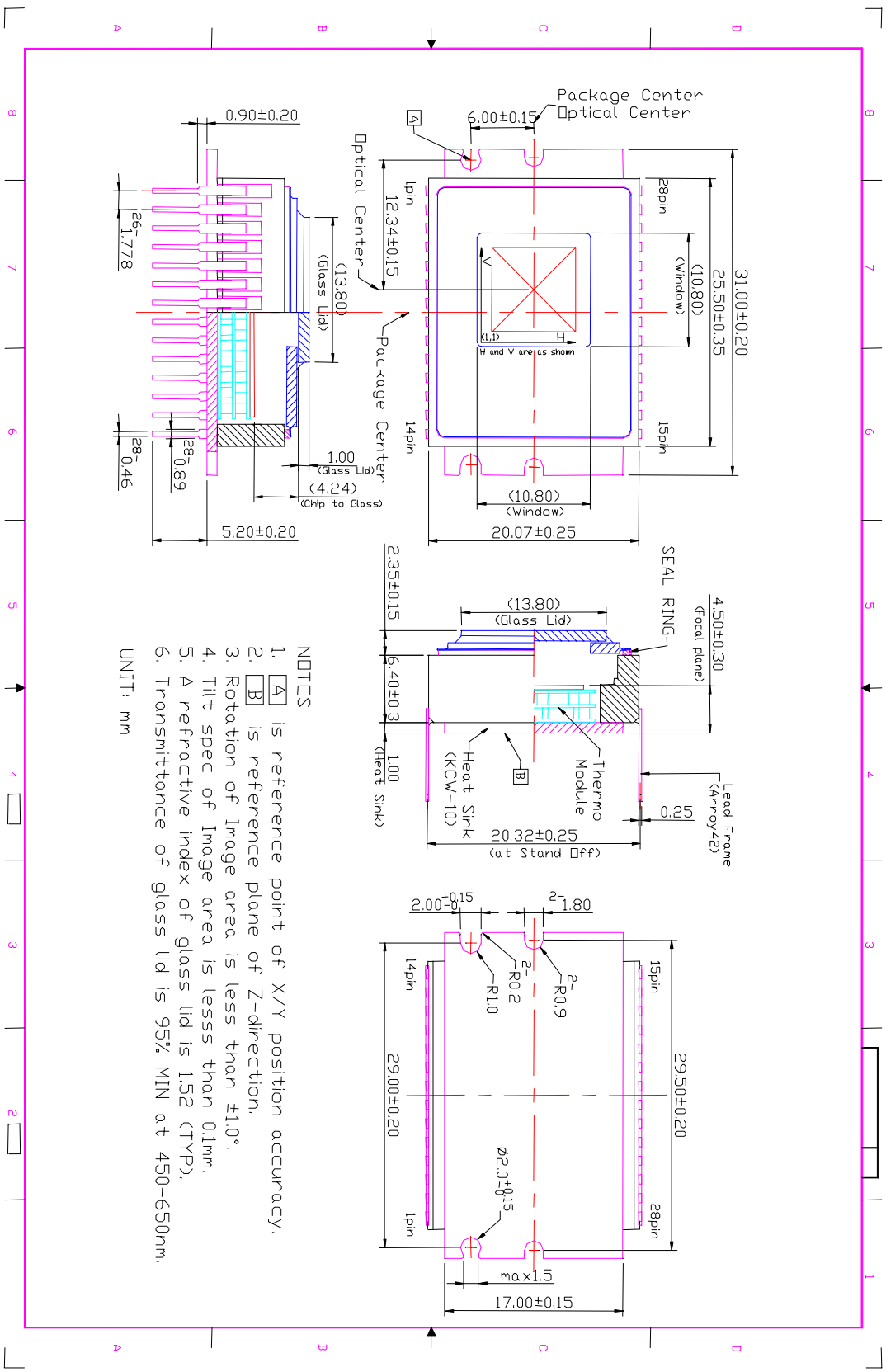
Current Bufferr Circuit
(For IAG1, same as the other gate)

Notes: A. All values are in Ohms and Microfarads unless otherwise noted.

FIGURE 17. Typical ODB Driver and Parallel Current Buffer Circuit

Mechanical data

The package for the TC285SPD consists of a ceramic base, a glass window, and a 28-pin lead frame. The glass window is hermetically sealed to the package. The package leads are configured in a dual-in-line arrangement and fit into mounting holes with 1,78 mm center-to-center spacing. The TC285SPD sensor also contains a bipolar transistor inside the package. The transistor load (2.2kOhm) needs to be connected to the VOUT pin externally.



NOTES

1. A is reference point of X/Y position accuracy.
2. B is reference plane of Z-direction.
3. Rotation of Image area is less than ±1.0°.
4. Tilt spec of Image area is lesss than 0.1mm.
5. A refractive index of glass lid is 1.52 (TYP).
6. Transmittance of glass lid is 95% MIN at 450-650nm.

UNIT: mm

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