MC74LVX132

Product Preview

Quad 2-Input NAND Schmitt Trigger

The MC74LVX132 is an advanced high speed CMOS Schmitt NAND trigger fabricated with silicon gate CMOS technology.

Pin configuration and function are the same as the MC74LVX00, but the inputs have hysteresis.

The internal circuit is composed of multiple stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

- High Speed: t_{PD} = 5.8ns (Typ) at V_{CC} = 3.3V
- Low Power Dissipation: I_{CC} = 2μA (Max) at T_A = 25°C
- Power Down Protection Provided on Inputs
- Low Noise: V_{OLP} = 0.5V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V

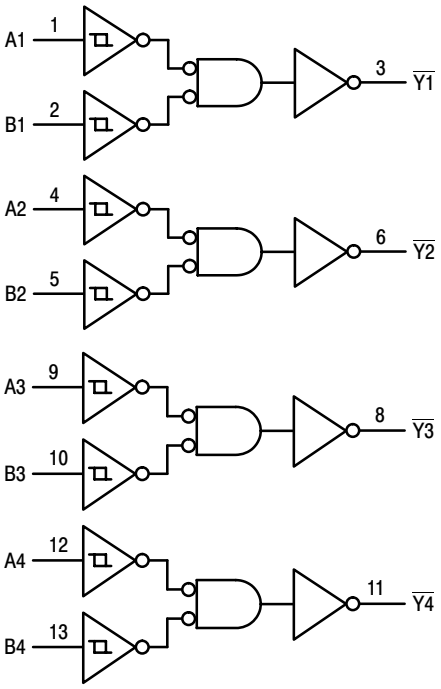

Figure 1. Logic Diagram

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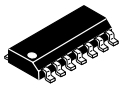
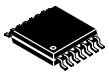
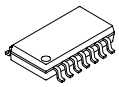


14–LEAD SOIC
D SUFFIX
CASE 751A



14–LEAD TSSOP
DT SUFFIX
CASE 948G



14–LEAD SOIC EIAJ
M SUFFIX
CASE 965

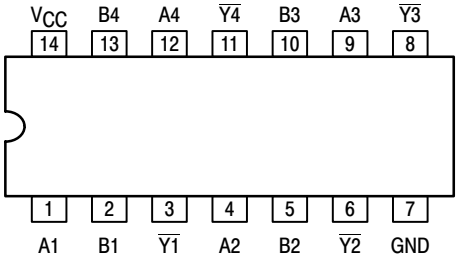


Figure 2. Pin Connection and Marking Diagram (Top View)

For detailed package marking information, see the Marking Diagram section on page 350 of this data sheet.

ORDERING INFORMATION

Device	Package	Shipping
MC74LVX132D	SOIC	55 Units/Rail
MC74LVX132DT	TSSOP	96 Units/Rail
MC74LVX132M	SOIC EIAJ	50 Units/Rail

FUNCTION TABLE

A Input	B Input	$\overline{Y}$ Output
L	L	H
L	H	H
H	L	H
H	H	L

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +7.0	V
V_{IN}	DC Input Voltage		−0.5 to +7.0	V
V_{OUT}	DC Output Voltage		−0.5 to V_{CC} +0.5	V
I_{IK}	DC Input Diode Current	V_I < GND	−20	mA
I_{OK}	DC Output Diode Current	V_O < GND	±20	mA
I_{OUT}	DC Output Sink Current		±25	mA
I_{CC}	DC Supply Current per Supply Pin		±50	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature under Bias		+150	°C
θ_{JA}	Thermal Resistance	SOIC TSSOP	250	°C/W
P_D	Power Dissipation in Still Air at 85°C	SOIC TSSOP	250	mW
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating	Oxygen Index: 30% – 35%	UL–94–VO (0.125 in)	
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 1.) Machine Model (Note 2.) Charged Device Model (Note 3.)	> 2000 > 200 N/A	V
$I_{Latch–Up}$	Latch–Up Performance	Above V_{CC} and Below GND at 85°C (Note 4.)	±300	mA

Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.

1. Tested to EIA/JESD22–A114–A.
2. Tested to EIA/JESD22–A115–A.
3. Tested to JESD22–C101–A.
4. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply Voltage		2.0	3.6	V
V_I	Input Voltage	(Note 5.)	0	5.5	V
V_O	Output Voltage	(HIGH or LOW State)	0	5.5	V
T_A	Operating Free–Air Temperature		−40	+125	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate	V_{CC} = 3.0 V ±0.3 V	0	100	ns/V

5. Unused inputs may not be left open. All inputs must be tied to a high– or low–logic input voltage level.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = ≤ 85°C		T_A = ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V_{T+}	Positive Threshold Voltage (5)		2.0 3.0 3.6	1.15 1.50 1.70	1.31 1.82 2.12	1.60 2.25 2.60	1.15 1.50 1.70	1.60 2.25 2.60	1.15 1.50 1.70	1.60 2.25 2.60	V
V_{T-}	Negative Threshold Voltage (5)		2.0 3.0 3.6	0.30 0.75 1.00	0.64 1.13 1.46	0.9 1.45 1.90	0.30 0.75 1.00	0.90 1.45 1.90	0.30 0.75 1.00	0.90 1.45 1.90	V
V_H	Hysteresis Voltage (5)		2.0 3.0 3.6	0.30 0.30 0.35	0.70 0.76 0.69	1.30 1.50 1.60	0.30 0.30 0.35	1.30 1.50 1.60	0.30 0.30 0.35	1.30 1.50 1.60	V
V_{OH}	Minimum High–Level Output Voltage V_{IN} = V_{IH} or V_{IL}	I_{OH} = – 50μA I_{OH} = – 50μA I_{OH} = – 4mA	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		1.9 2.9 2.34		V
V_{OL}	Maximum Low–Level Output Voltage V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA I_{OL} = 50μA I_{OL} = 4mA	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44		0.1 0.1 0.52	V
I_{in}	Maximum Input Leakage Current	V_{in} = 5.5V or GND	3.6			± 0.1		± 1.0		± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{in} = V_{CC} or GND	3.6			2.0		20		20	μA

AC ELECTRICAL CHARACTERISTICS (Input t_r = t_f = 3.0ns)

Symbol	Parameter	Test Conditions		T_A = 25°C			T_A = ≤ 85°C		T_A = ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, A or B to $\overline{Y}$	V_{CC} = 2.7V	C_L = 15pF C_L = 50pF		7.0 10.0	11.0 16.0	1.0 1.0	13.0 18.7	1.0 1.0	15.0 20.0	ns
		V_{CC} = 3.3 ± 0.3V	C_L = 15pF C_L = 50pF		5.8 8.3	10.6 15.4	1.0 1.0	12.5 17.5	1.0 1.0	14.5 19.5	
t_{OSHL}, t_{OSLH}	Output to Output Skew (Note 6.)	V_{CC} = 2.7V	C_L = 50pF			1.5		1.5		1.5	ns
		V_{CC} = 3.3 ± 0.3V	C_L = 50pF			1.5		1.5		1.5	
C_{in}	Maximum Input Capacitance				4	10		10		10	pF

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Note 6.)	11	pF

6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/4$ (per gate). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input t_r = t_f = 3.0ns, C_L = 50pF, V_{CC} = 5.0 V)

Symbol	Characteristic	T_A = 25°C		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.3	0.5	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	–0.3	–0.5	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

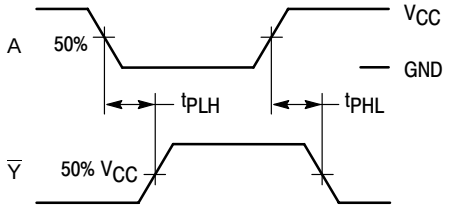
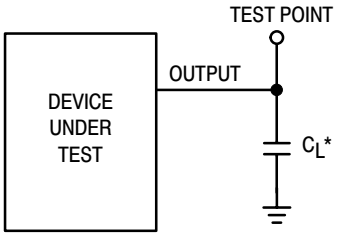


Figure 3. Switching Waveforms



*Includes all probe and jig capacitance

Figure 4. Test Circuit

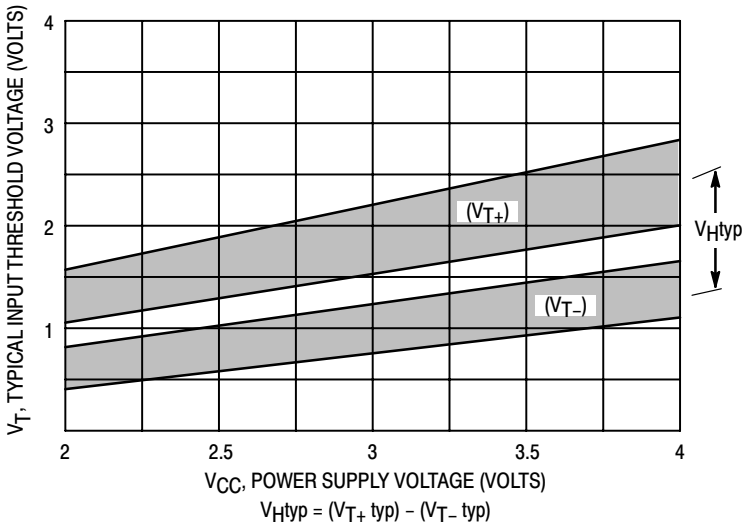
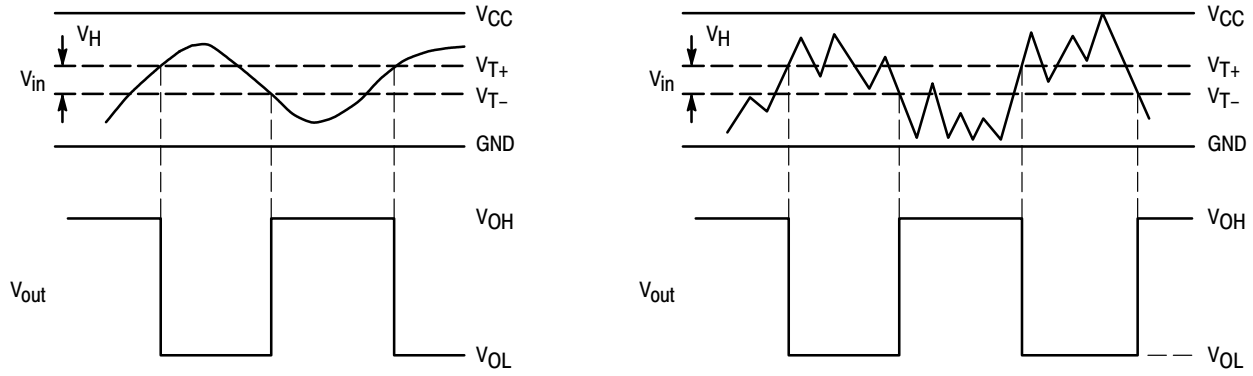


Figure 5. Typical Input Threshold, V_{T+}, V_{T-} versus Power Supply Voltage



(a) A Schmitt−Trigger Squares Up Inputs With Slow Rise and Fall Times

(b) A Schmitt−Trigger Offers Maximum Noise Immunity

Figure 6. Typical Schmitt−Trigger Applications

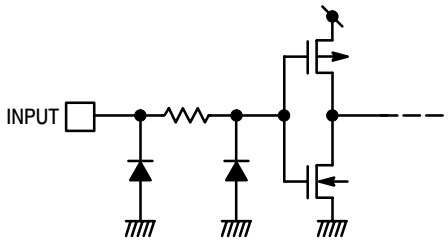
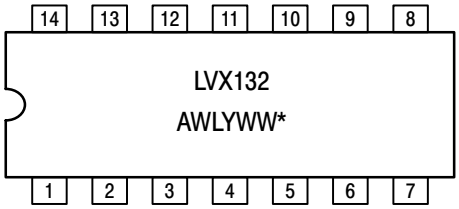


Figure 7. Input Equivalent Circuit



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D SUFFIX
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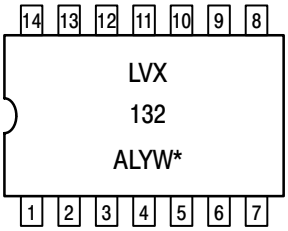
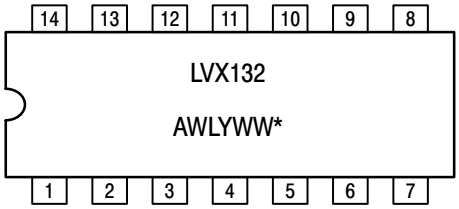


14–LEAD TSSOP
DT SUFFIX
CASE 948G



14–LEAD SOIC EIAJ
M SUFFIX
CASE 965

*See Applications Note #AND8004/D for date code and traceability information.

Figure 8. Marking Diagrams
(Top View)