February 2008

MM74HC08
Quad 2-Input AND Gate

Features

- Typical propagation delay: 7ns (t_{PHL}), 12ns (t_{PLH})
- Fanout of 10 LS-TTL loads
- Quiescent power consumption: 2μA maximum at room temperature
- Low input current: 1μA maximum

General Description

The MM74HC08 AND gates utilize advanced silicon-gate CMOS technology to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. The HC08 has buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads. The 74HC logic family is functionally as well as pin-out compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

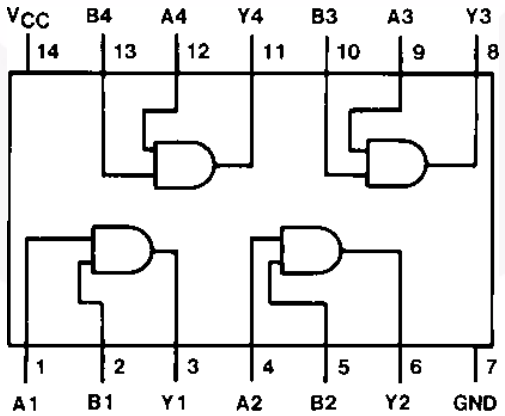
Ordering Information

Order Number	Package Number	Package Description
MM74HC08M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HC08SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC08MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC08N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel except for N14A. Specify by appending suffix letter “X” to the ordering number.

All packages are lead free per JEDEC: J-STD-020B standard.

Connection Diagram



Top View

Absolute Maximum Ratings(1)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	–0.5 to +7.0V
V_{IN}	DC Input Voltage	–1.5 to V_{CC}+1.5V
V_{OUT}	DC Output Voltage	–0.5 to V_{CC}+0.5V
I_{IK}, I_{OK}	Clamp Diode Current	±20mA
I_{OUT}	DC Output Current, per pin	±25mA
I_{CC}	DC V_{CC} or GND Current, per pin	±50mA
T_{STG}	Storage Temperature Range	–65°C to +150°C
P_D	Power Dissipation Note 2	600mW
	S.O. Package only	500mW
T_L	Lead Temperature (Soldering 10 seconds)	260°C

Notes:

1. Unless otherwise specified all voltages are referenced to ground.
2. Power Dissipation temperature derating — plastic “N” package: –12mW/°C from 65°C to 85°C.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Supply Voltage	2	6	V
V_{IN}, V_{OUT}	DC Input or Output Voltage	0	V_{CC}	V
T_A	Operating Temperature Range	–40	+85	°C
t_r, t_f	Input Rise or Fall Times V_{CC} = 2.0V		1000	ns
	V_{CC} = 4.5V		500	ns
	V_{CC} = 6.0V		400	ns

DC Electrical Characteristics[3]

Symbol	Parameter	V_{CC} (V)	Conditions	$T_A = 25°C$	$T_A = -40°C$ to 85°C	$T_A = -55°C$ to 125°C	Units
				Typ.	Guaranteed Limits		
V_{IH}	Minimum HIGH Level Input Voltage	2.0			1.5	1.5	1.5	V
		4.5			3.15	3.15	3.15	
		6.0			4.2	4.2	4.2	
V_{IL}	Maximum LOW Level Input Voltage	2.0			0.5	0.5	0.5	V
		4.5			1.35	1.35	1.35	
		6.0			1.8	1.8	1.8	
V_{OH}	Minimum HIGH Level Output Voltage	2.0	$V_{IN} = V_{IH}$, $\|I_{OUT}\| \le 20\mu A$	2.0	1.9	1.9	1.9	V
		4.5		4.5	4.4	4.4	4.4	
		6.0		6.0	5.9	5.9	5.9	
		4.5	$V_{IN} = V_{IH}$, $\|I_{OUT}\| \le 4.0mA$	4.2	3.98	3.84	3.7	
		6.0	$V_{IN} = V_{IH}$, $\|I_{OUT}\| \le 5.2mA$	5.7	5.48	5.34	5.2	
V_{OL}	Maximum LOW Level Output Voltage	2.0	$V_{IN} = V_{IH}$ or V_{IL}, $\|I_{OUT}\| \le 20\mu A$	0	0.1	0.1	0.1	V
		4.5		0	0.1	0.1	0.1	
		6.0		0	0.1	0.1	0.1	
		4.5	$V_{IN} = V_{IH}$ or V_{IL}, $\|I_{OUT}\| \le 4.0mA$	0.2	0.26	0.33	0.4	
		6.0	$V_{IN} = V_{IH}$ or V_{IL}, $\|I_{OUT}\| \le 5.2mA$	0.2	0.26	0.33	0.4	
I_{IN}	Maximum Input Current	6.0	$V_{IN} = V_{CC}$ or GND		±0.1	±1.0	±1.0	µA
I_{CC}	Maximum Quiescent Supply Current	6.0	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0\mu A$		2.0	20	40	µA

Note:

3. For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at $V_{CC} = 5.5V$ and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

V_{CC} = 5V, T_A = 25°C, C_L = 15pF, $t_r = t_f$ = 6ns

Symbol	Parameter	Conditions	Typ.	Guaranteed Limit	Units
t_{PHL}	Maximum Propagation Delay, Output HIGH-to-LOW		12	20	ns
t_{PLH}	Maximum Propagation Delay, Output LOW-to-HIGH		7	15	ns

AC Electrical Characteristics

V_{CC} = 2.0V to 6.0V, C_L = 50pF, $t_r = t_f$ = 6ns (unless otherwise specified)

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = 25°C		T_A = –40°C to 125°C	Units
				Typ.	Guaranteed Limits		
t_{PHL}	Maximum Propagation Delay, Output HIGH-to-LOW	2.0		77	121	175	ns
		4.5		15	24	35	
		6.0		13	20	30	
t_{PLH}	Maximum Propagation Delay, Output LOW-to-HIGH	2.0		30	90	134	ns
		4.5		10	18	27	
		6.0		8	15	23	
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time	2.0		30	75	110	ns
		4.5		8	15	22	
		6.0		7	13	19	
C_{PD}	Power Dissipation Capacitance(4)		(per gate)	38			pF
C_{IN}	Maximum Input Capacitance			4	10	10	pF

Note:

4. C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Physical Dimensions

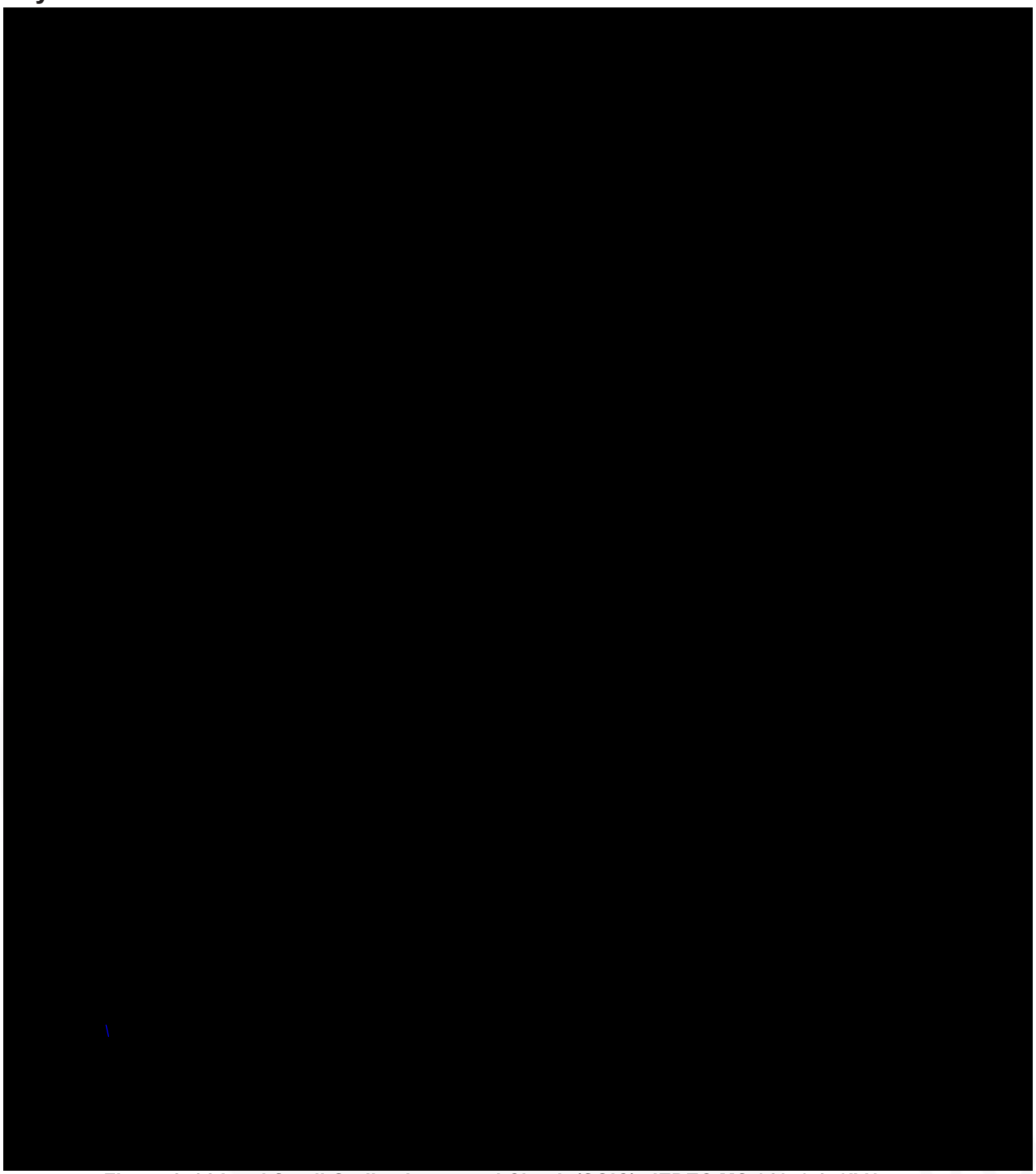


Figure 1. 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow

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Physical Dimensions (Continued)

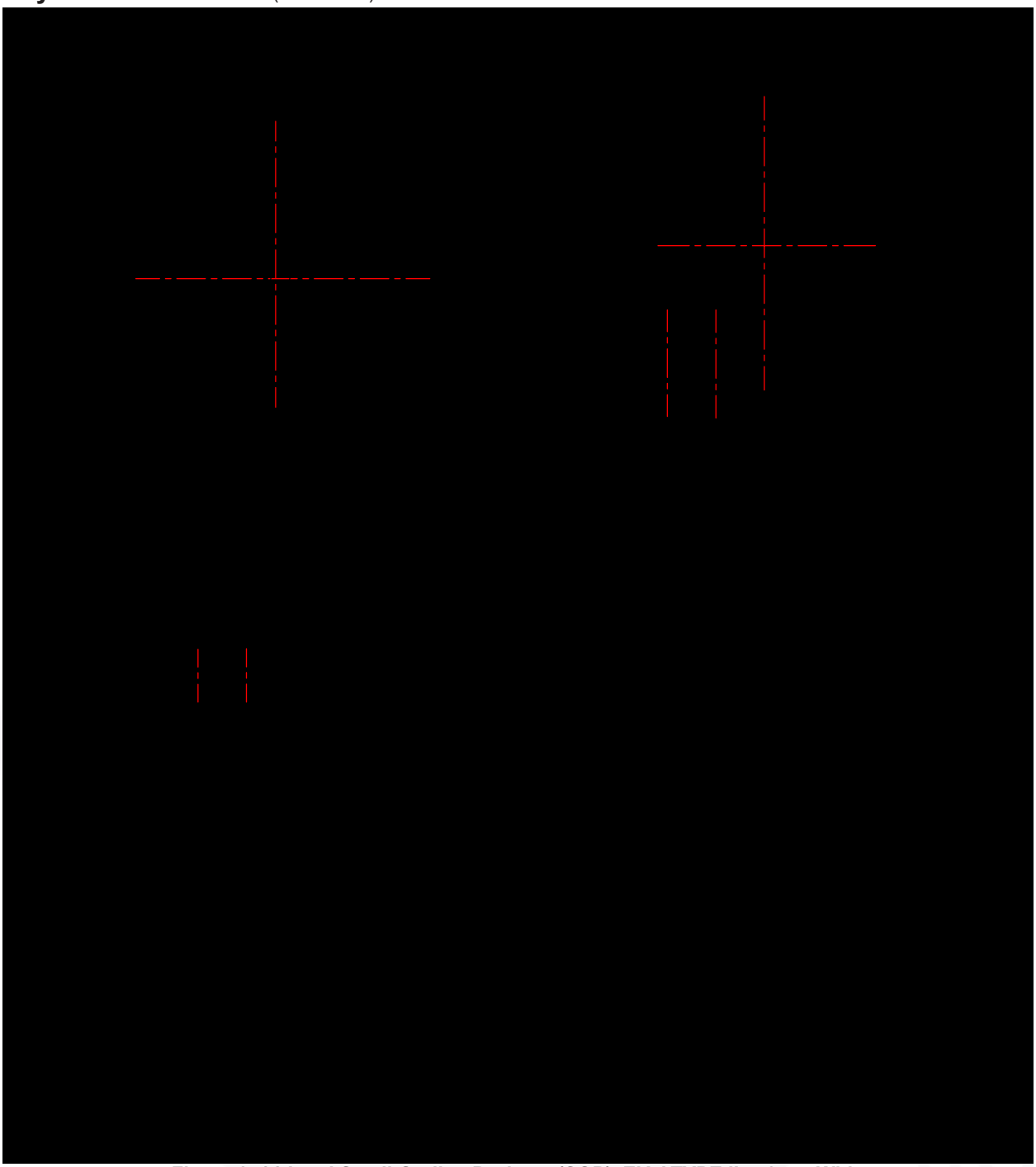

Figure 2. 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

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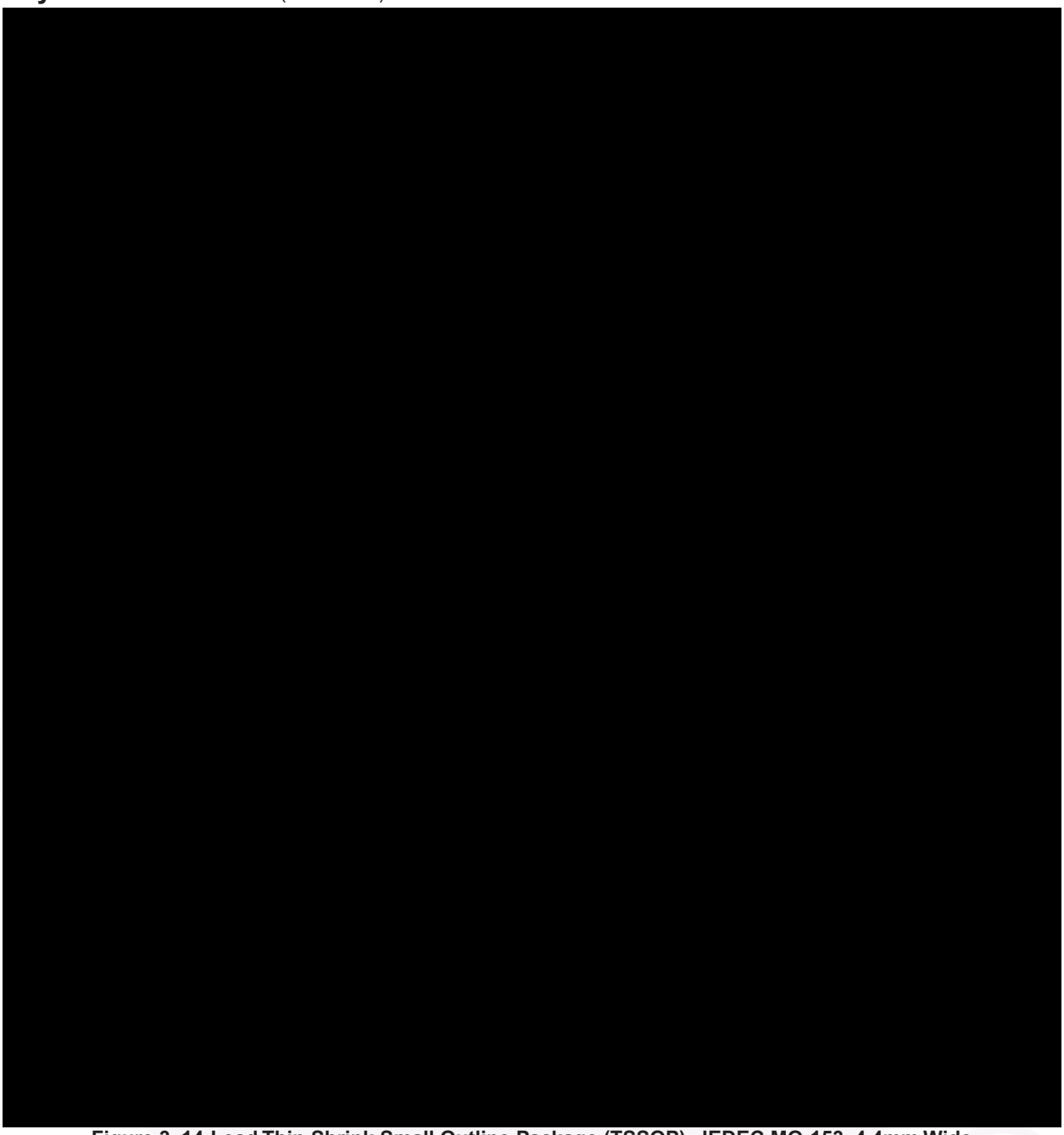

Figure 3. 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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Physical Dimensions (Continued)

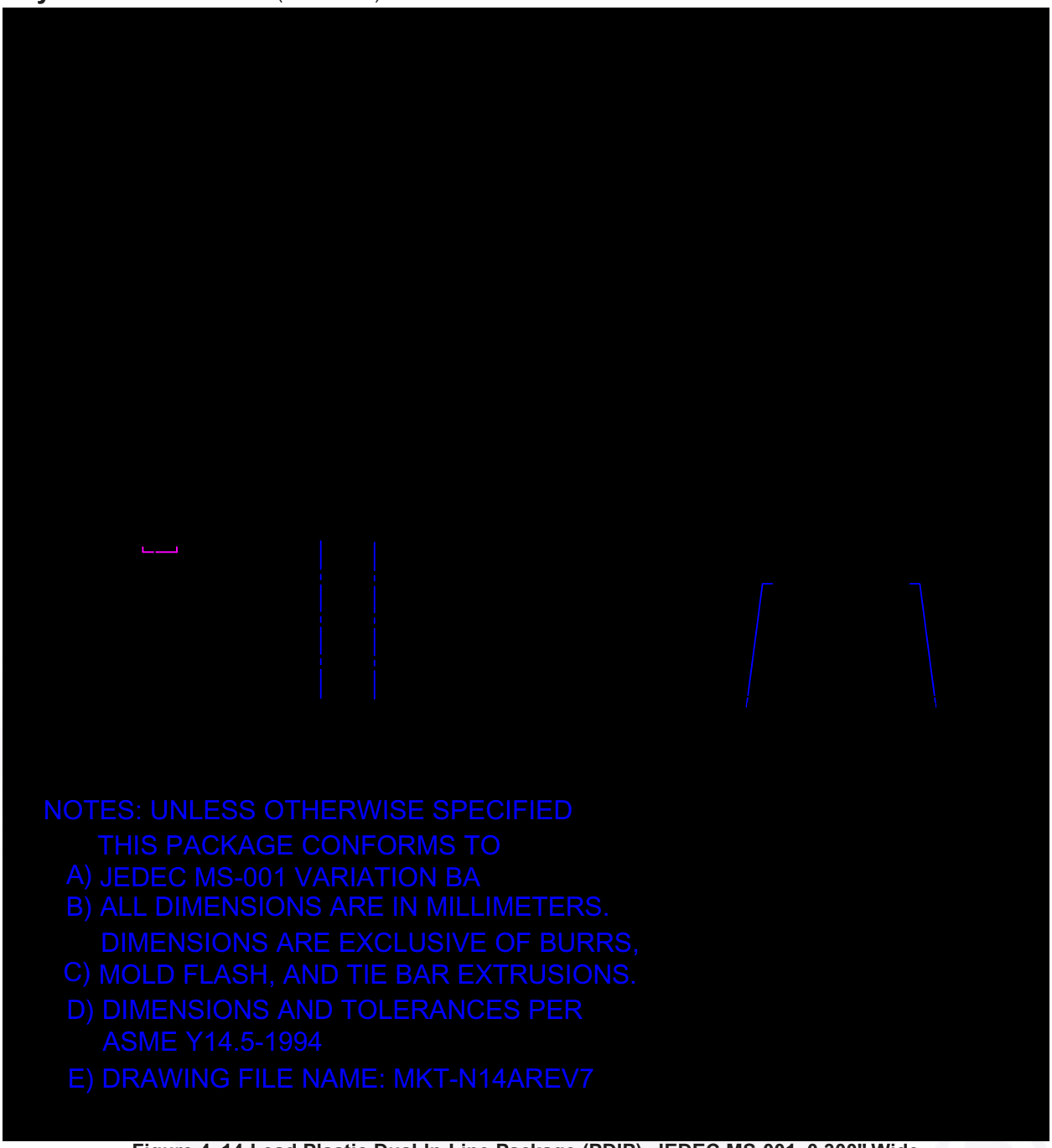

Figure 4. 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

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