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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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(5400 + 5400) PIXELS × 3 + COLOR CCD LINEAR IMAGE SENSOR

DESCRIPTION

The μPD8874 is a color CCD (Charge Coupled Device) linear image sensor that changes optical images to electrical signal and has the function of color separation.

The μPD8874 has 3 rows of (5400 + 5400) staggered pixels, and each row has dual-sided readout type of charge transfer register. This product is high speed and High response version of the existing product μPD8873.

And it has reset feed-through level clamp circuits and voltage amplifiers. Therefore, it is suitable for 1200 dpi/A4 color image scanners, color MFP and so on.

FEATURES

- Valid photocell : (5400 + 5400) staggered pixels × 3
- Photocell's size : 5.25 × 5.25 μm
- Line spacing : 63 μm (12 lines) Red line - Green line, Green line - Blue line
10.5 μm (2 lines) Odd line - Even line (for each color)
- Color filter : High transmittance new color filter
Primary colors (red, green and blue), pigment filter
Light resistance 10⁷ lx•hour with standard sunlight and ultraviolet cut filter (L40).
- Resolution : 48 dot/mm A4 (210 × 297 mm) size (shorter side) for color
1200 dpi US letter (8.5" × 11") size (shorter side) for color
- Drive clock level : CMOS output under 5 V operation
- Data rate : 20 MHz Max.
- Power supply : +12 V
- On-chip circuit : Reset feed-through level clamp circuits
Voltage amplifiers

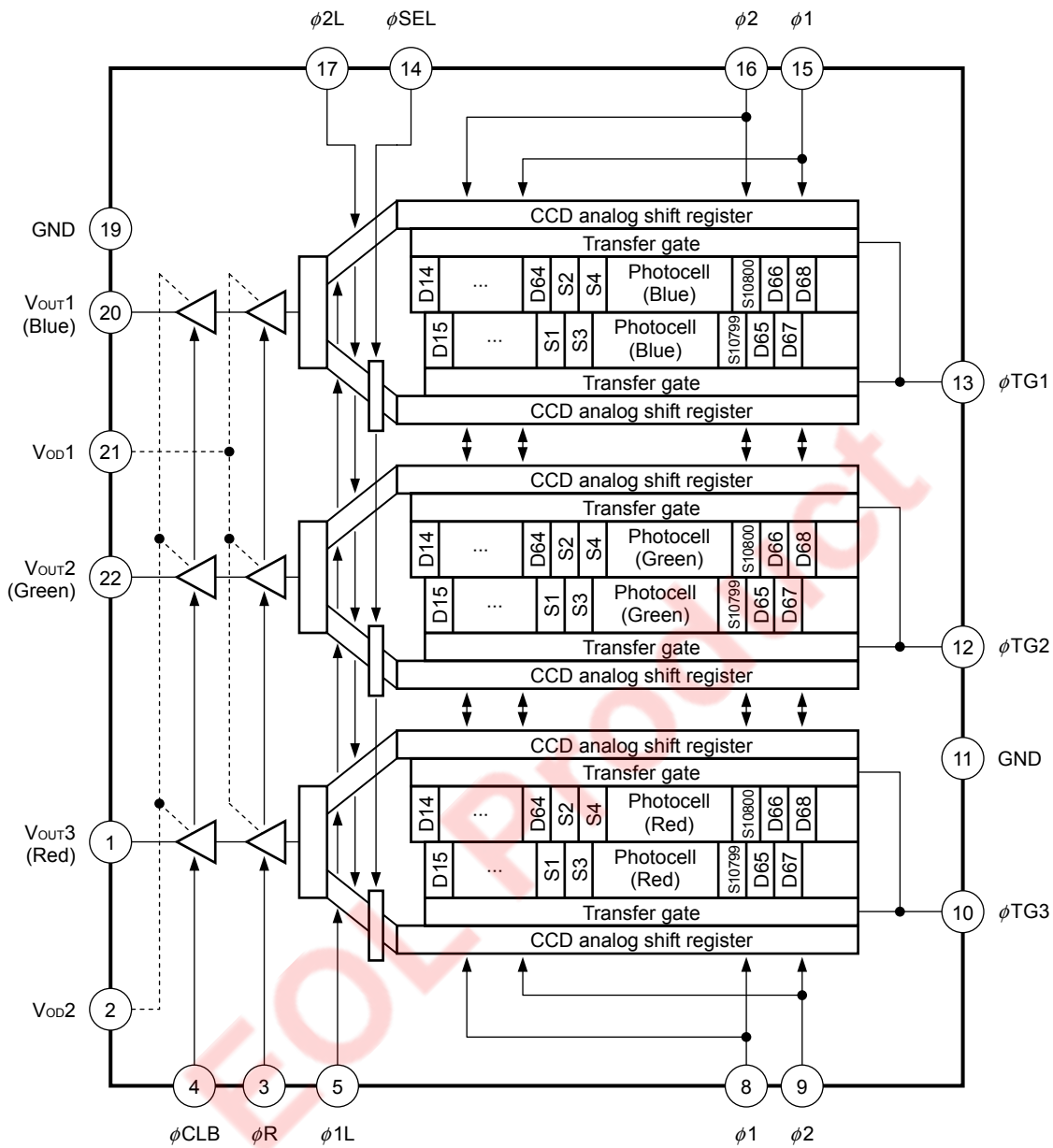
ORDERING INFORMATION

Part Number	Package
μPD8874CY-A	CCD linear image sensor 22-pin plastic DIP (10.16 mm (400))

Remark The μPD8874CY-A is a lead-free product.

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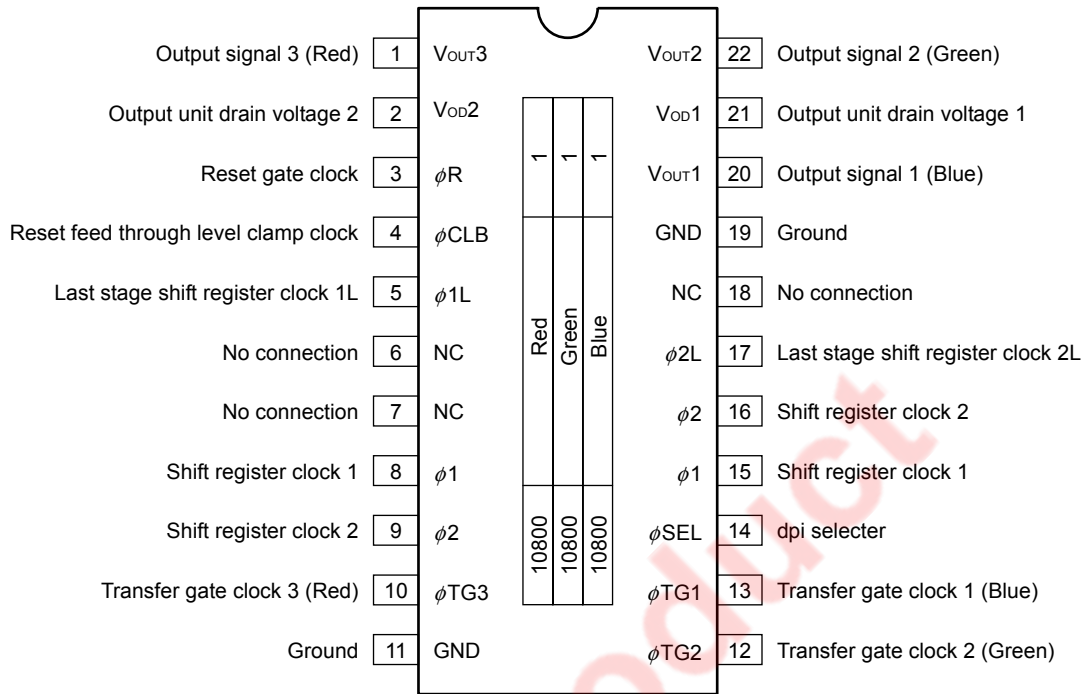
BLOCK DIAGRAM



PIN CONFIGURATION (Top View)

CCD linear image sensor 22-pin plastic DIP (10.16 mm (400))

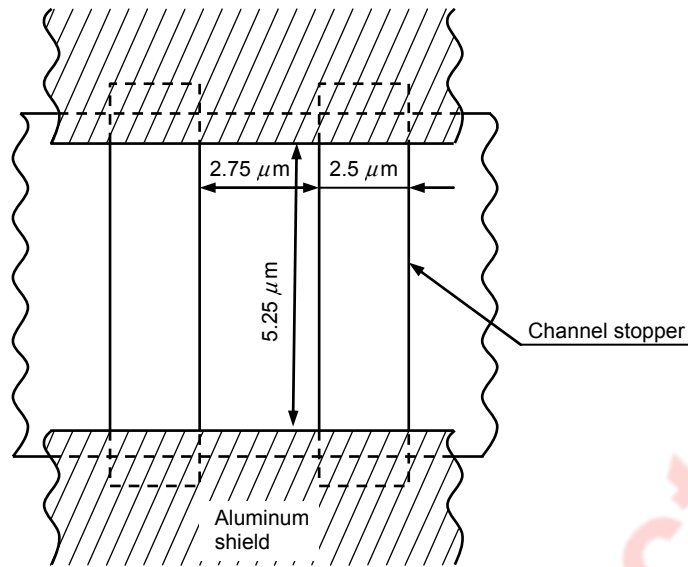
μPD8874CY-A



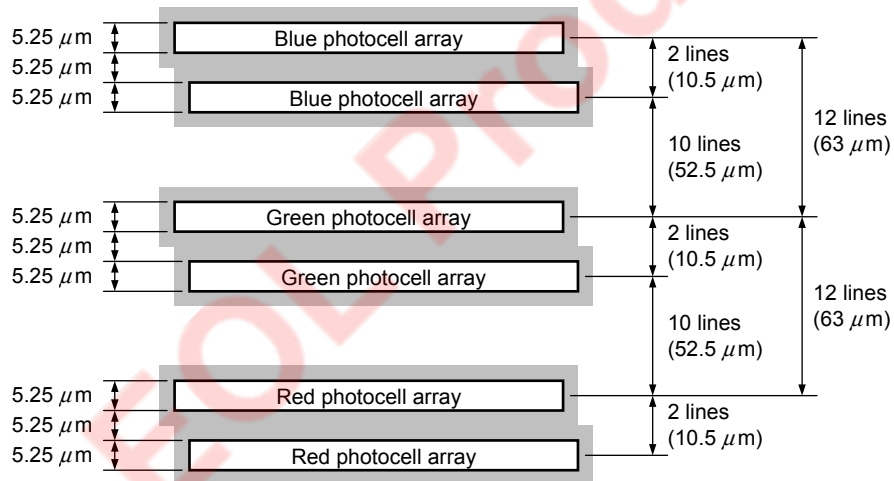
Caution Connect the no connection pins (NC) to GND.

EOL Product

PHOTOCELL STRUCTURE DIAGRAM



PHOTOCELL ARRAY STRUCTURE DIAGRAM (Line spacing)



ABSOLUTE MAXIMUM RATINGS (T_A = +25°C)

Parameter	Symbol	Ratings	Unit
Output drain voltage	V _{OD1} , V _{OD2}	-0.3 to +15	V
Shift register clock voltage	V _{φ1} , V _{φ2}	-0.3 to +8	V
Last stage shift register clock voltage	V _{φ1L} , V _{φ2L}	-0.3 to +8	V
Reset gate clock voltage	V _{φR}	-0.3 to +8	V
Reset feed-through level clamp clock voltage	V _{φCLB}	-0.3 to +8	V
Dpi select signal voltage	V _{φSEL}	-0.3 to +8	V
Transfer gate clock voltage	V _{φTG1} to V _{φTG3}	-0.3 to +8	V
Operating ambient temperature ^{Note}	T _A	0 to +55	°C
Storage temperature	T _{stg}	-40 to +70	°C

Note The operating ambient temperature T_A is defined as an atmosphere temperature in a point 10 mm away on the substrate, and 10 mm away from the short side of package (pin 1 side). Use at the condition without dewy condensation.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

RECOMMENDED OPERATING CONDITIONS (T_A = +25°C)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Output drain voltage	V _{OD1} , V _{OD2}	11.4	12.0	12.6	V
Shift register clock high level	V _{φ1H} , V _{φ2H}	4.75	5.0	5.5	V
Shift register clock low level	V _{φ1L} , V _{φ2L}	0	0	0.15	V
Last stage shift register clock high level	V _{φ1LH} , V _{φ2LH}	4.75	5.0	5.5	V
Last stage shift register clock low level	V _{φ1LL} , V _{φ2LL}	0	0	0.15	V
Reset gate clock high level	V _{φRH}	4.75	5.0	5.5	V
Reset gate clock low level	V _{φRL}	0	0	0.15	V
Reset feed-through level clamp clock high level	V _{φCLBH}	4.75	5.0	5.5	V
Reset feed-through level clamp clock low level	V _{φCLBL}	0	0	0.15	V
Dpi select signal high level	V _{φSELH}	4.75	5.0	5.5	V
Dpi select signal low level	V _{φSELL}	0	0	0.15	V
Transfer gate clock high level	V _{φTG1H} to V _{φTG3H}	4.75	V _{φ1H} ^{Note}	V _{φ1H} ^{Note}	V
Transfer gate clock low level	V _{φTG1L} to V _{φTG3L}	0	0	0.15	V
Data rate	f _{φR}	–	2	20	MHz
Clock pulse frequency	f _{φ1} , f _{φ2}	–	2	20	MHz

Note When Transfer gate clock high level (V_{φTG1H} to V_{φTG3H}) is higher than Shift register clock high level (V_{φ1H}), Image lag increases.

ELECTRICAL CHARACTERISTICS

($T_A = +25^{\circ}\text{C}$, $V_{OD} = 12\text{ V}$, data rate ($f_{\phi R}$) = 2 MHz, storage time = 5.5 ms, input signal clock = 5 V_{p-p}
light source: 3200 K halogen lamp + C-500S (infrared cut filter, t = 1 mm)+ HA-50 (heat absorbing filter, t = 3 mm)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Saturation voltage	V_{sat}		2.0	2.5	–	V
Saturation exposure	Red	SER	–	0.25	–	lx•s
	Green	SEG	–	0.27	–	lx•s
	Blue	SEB	–	0.5	–	lx•s
Photo response non-uniformity	PRNU	$V_{OUT} = 1.0\text{ V}$	–	6	20	%
Average dark signal	ADS	Light shielding	–	0.2	2.0	mV
Dark signal non-uniformity	DSNU	Light shielding	–	1.5	5.0	mV
Total power consumption	P_W	Light shielding	–	360	540	mW
Output impedance	Z_o		–	0.2	0.4	kΩ
Response	Red	R_R	7.0	10.0	13.0	V/lx•s
	Green	R_G	6.3	9.0	11.7	V/lx•s
	Blue	R_B	3.5	5.0	6.5	V/lx•s
Image lag	IL	$V_{OUT} = 1.0\text{ V}$	–	3.0	7.0	%
Offset level	V_{OS}		6.5	7.5	8.5	V
Output fall delay time ^{Note}	t_d	$V_{OUT} = 1.0\text{ V}$	–	15	–	ns
Total transfer efficiency ^{Note}	TTE	$V_{OUT} = 1.0\text{ V}$, data rate = 20 MHz	92	98	–	%
Register imbalance	RI	$V_{OUT} = 1.0\text{ V}$	–	1.0	4.0	%
Response peak	Red		–	610	–	nm
	Green		–	535	–	nm
	Blue		–	460	–	nm
Dynamic range	DR1	$V_{sat} / DSNU$	–	1666	–	times
	DR2	V_{sat} / σ_{dark}	–	1041	–	times
Reset feed-through noise	RFTN	Light shielding	–2000	–100	+500	mV
	PRFTN	Light shielding, t4 and t5 = 2 ns	–	500	800	mV
Random noise	σ_{dark}	Light shielding, Bit clamp (t11 > 10 ns)	–	2.4	–	mV

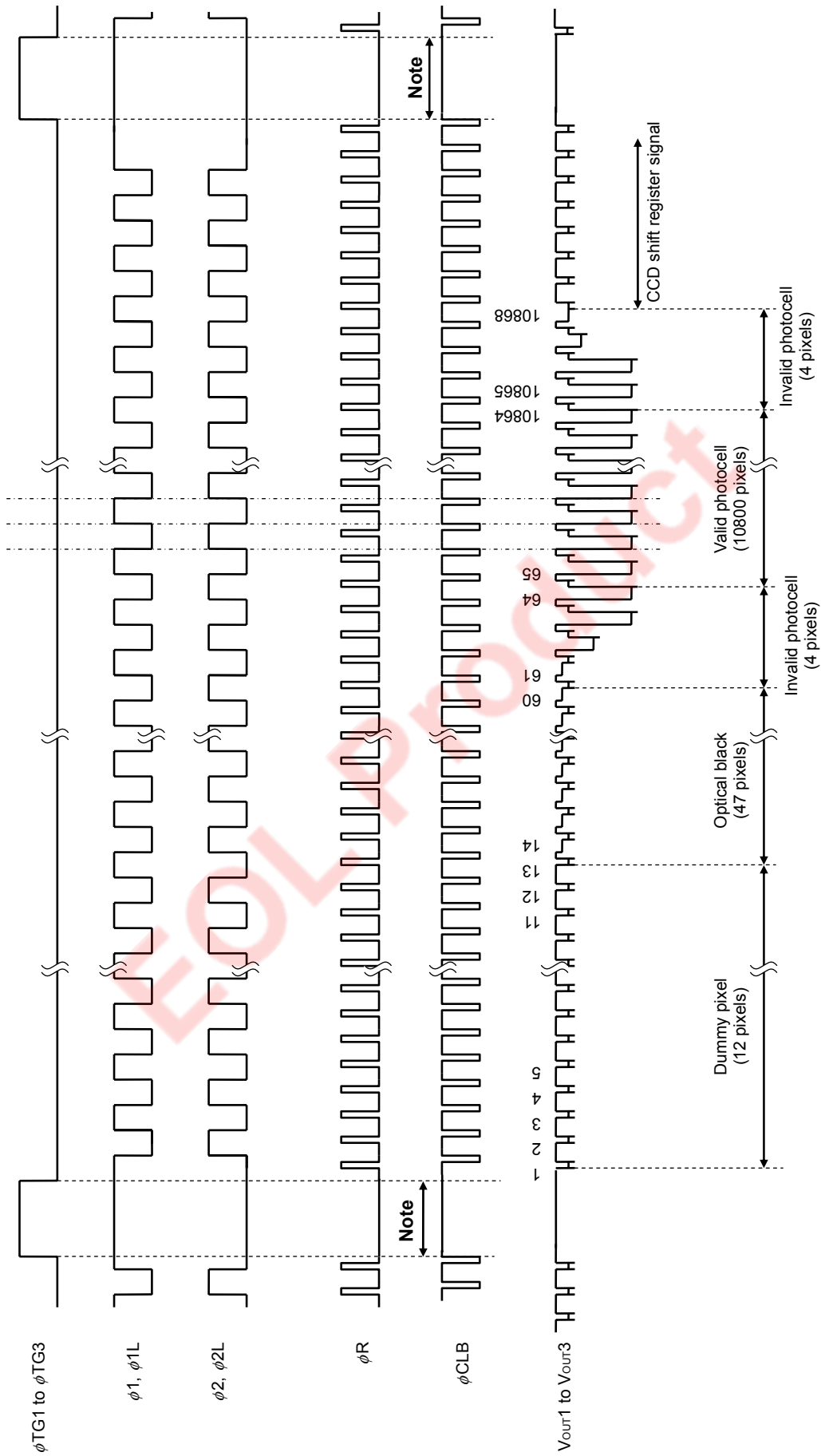
Note When the fall time of $\phi 1L$ and $\phi 2L$ (t1L and t2L) is the typical value (refer to **TIMING CHART 2-1 to 2-3**).

INPUT PIN CAPACITANCE (T_A = +25°C, V_{OD} = 12 V)

Parameter	Symbol	Pin name	Pin No.	MIN.	TYP.	MAX.	Unit
Shift register clock pin capacitance 1	C _{φ1}	φ1	8	–	550	–	pF
			15	–	550	–	pF
	C _{φ1} total capacitance			–	1100	–	pF
Shift register clock pin capacitance 2	C _{φ2}	φ2	9	–	550	–	pF
			16	–	550	–	pF
	C _{φ2} total capacitance			–	1100	–	pF
Last stage shift register clock pin capacitance 1	C _{φ1L}	φ1L	5	–	10	–	pF
Last stage shift register clock pin capacitance 2	C _{φ2L}	φ2L	17	–	10	–	pF
Reset gate clock pin capacitance	C _{φR}	φR	3	–	10	–	pF
Reset feed-through level clamp clock pin capacitance	C _{φCLB}	φCLB	4	–	10	–	pF
Dpi select signal pin capacitance	C _{φSEL}	φSEL	14	–	10	–	pF
Transfer gate clock pin capacitance	C _{φTG}	φTG1	13	–	100	–	pF
		φTG2	12	–	100	–	pF
		φTG3	10	–	100	–	pF

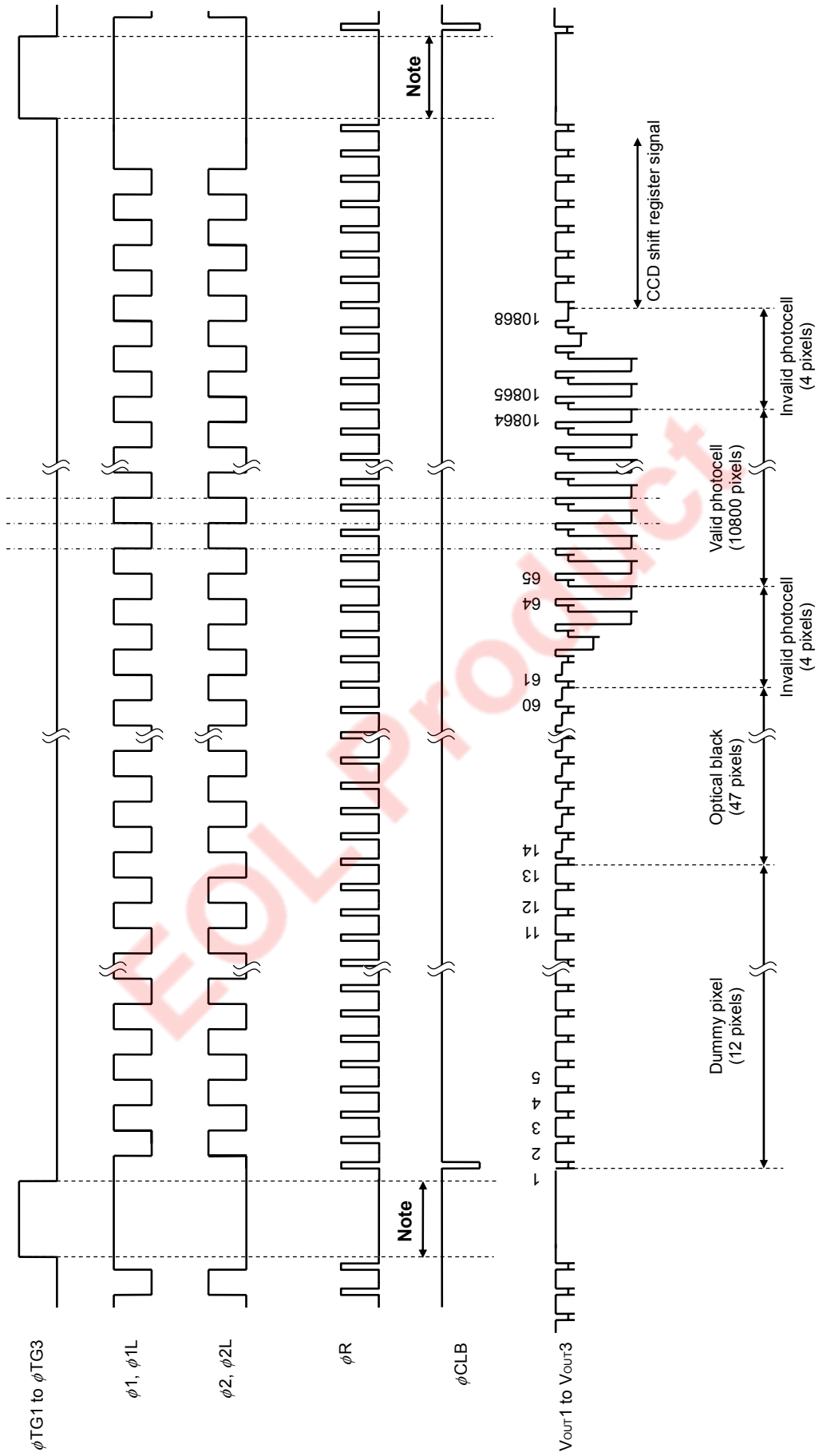
- Remarks**
- Pin 8, 15 (φ1) and pin 9, 16 (φ2) are each connected inside of the device.
 - C_{φ1} and C_{φ2} show the equivalent capacity of the real drive including the capacity of between φ1 and φ2.

TIMING CHART 1-1 (for each color, 1200 dpi, φSEL = high, bit clamp mode)



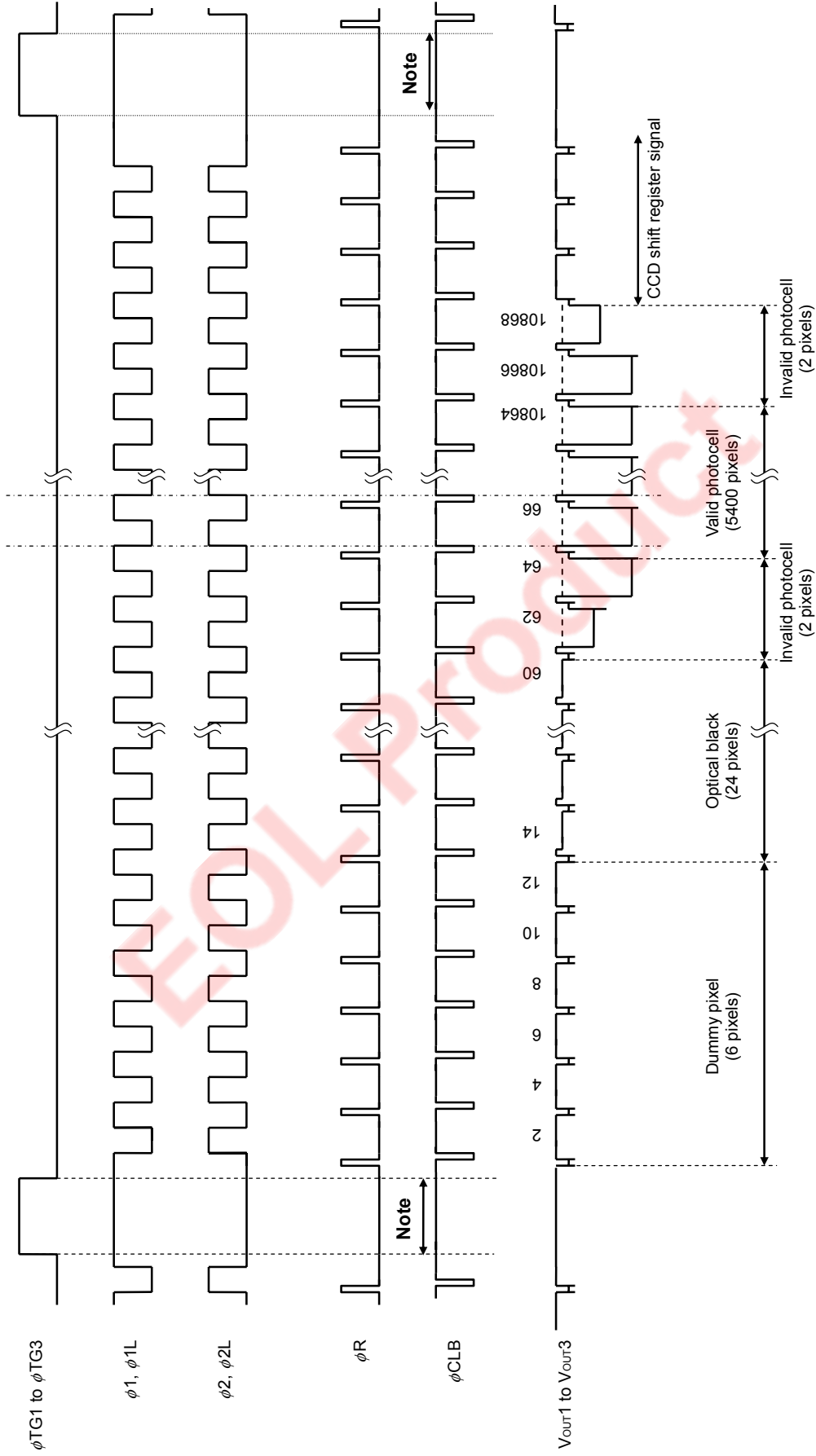
Note Set the ϕ_R to low level and ϕ_{CLB} to high level during this period.

TIMING CHART 1-2 (for each color, 1200 dpi, φSEL = high, line clamp mode)



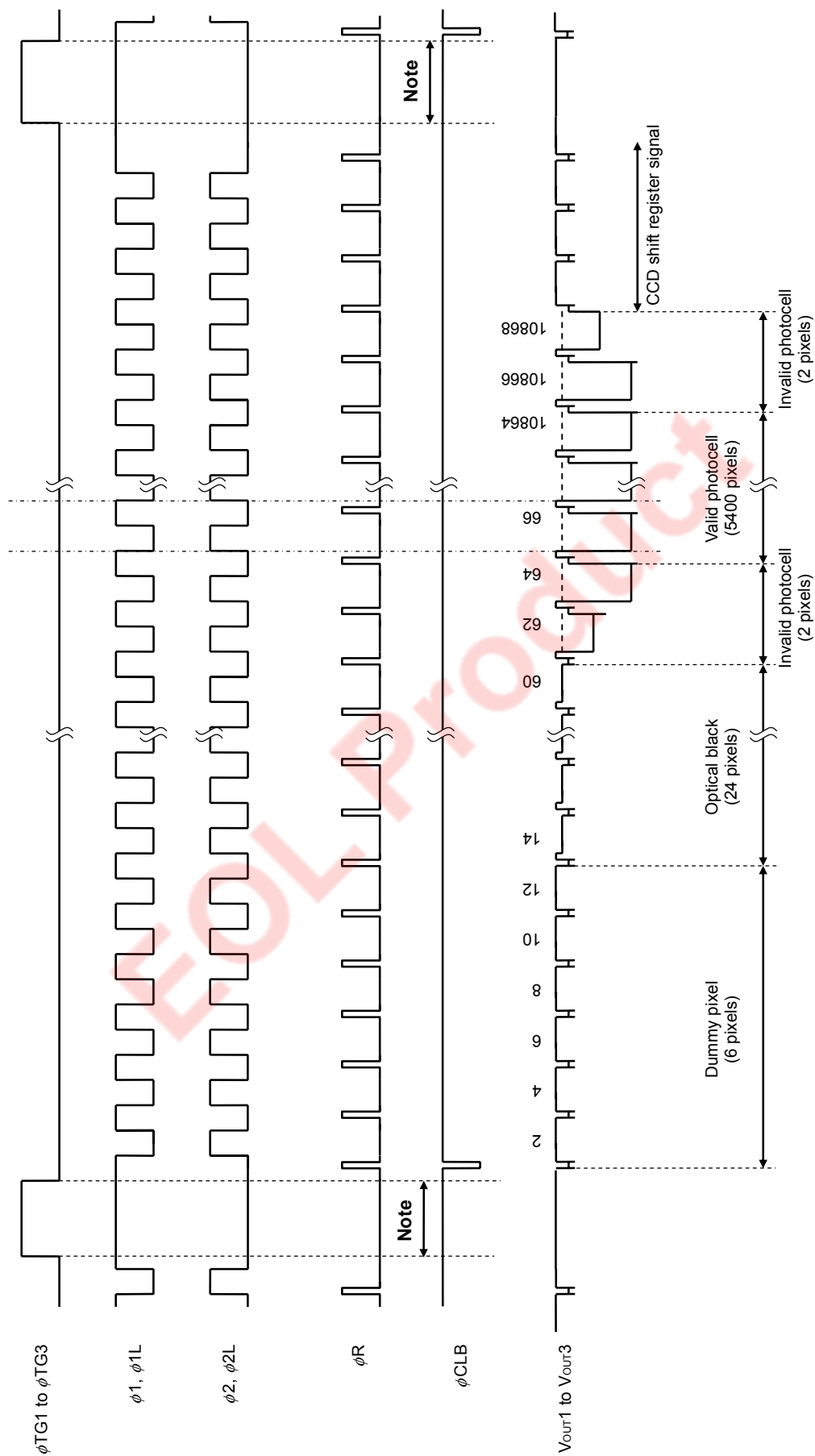
Note Set the ϕ_R to low level and ϕ_{CLB} to high level during this period.

TIMING CHART 1-3 (for each color, 600 dpi, φSEL = low, bit clamp mode)



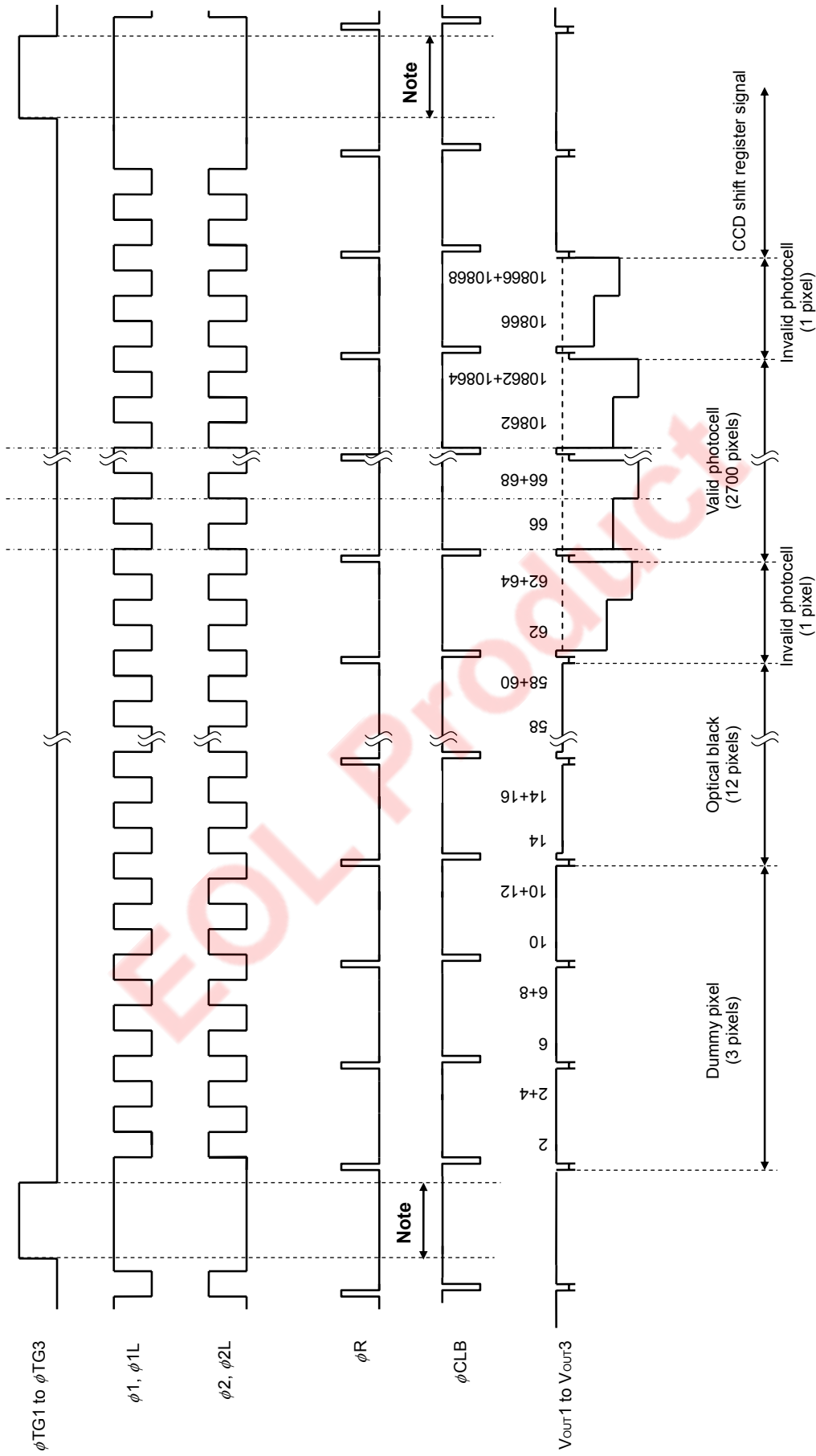
Note Set the ϕ_R to low level and ϕ_{CLB} to high level during this period.

TIMING CHART 1-4 (for each color, 600 dpi, φSEL = low, line clamp mode)



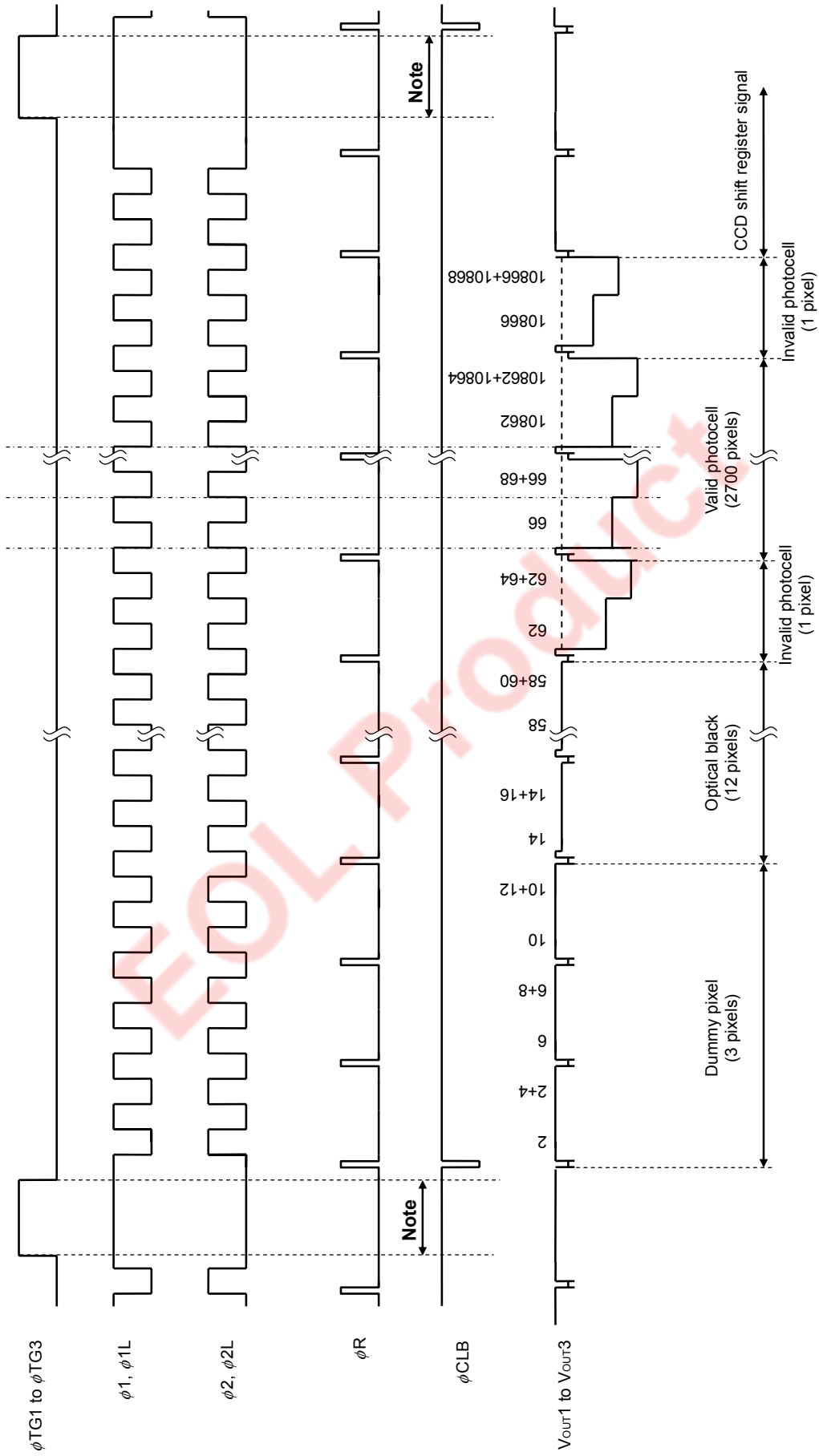
Note Set the ϕ_R to low level and ϕ_{CLB} to high level during this period.

TIMING CHART 1-5 (for each color, 300 dpi, φSEL = low, bit clamp mode)



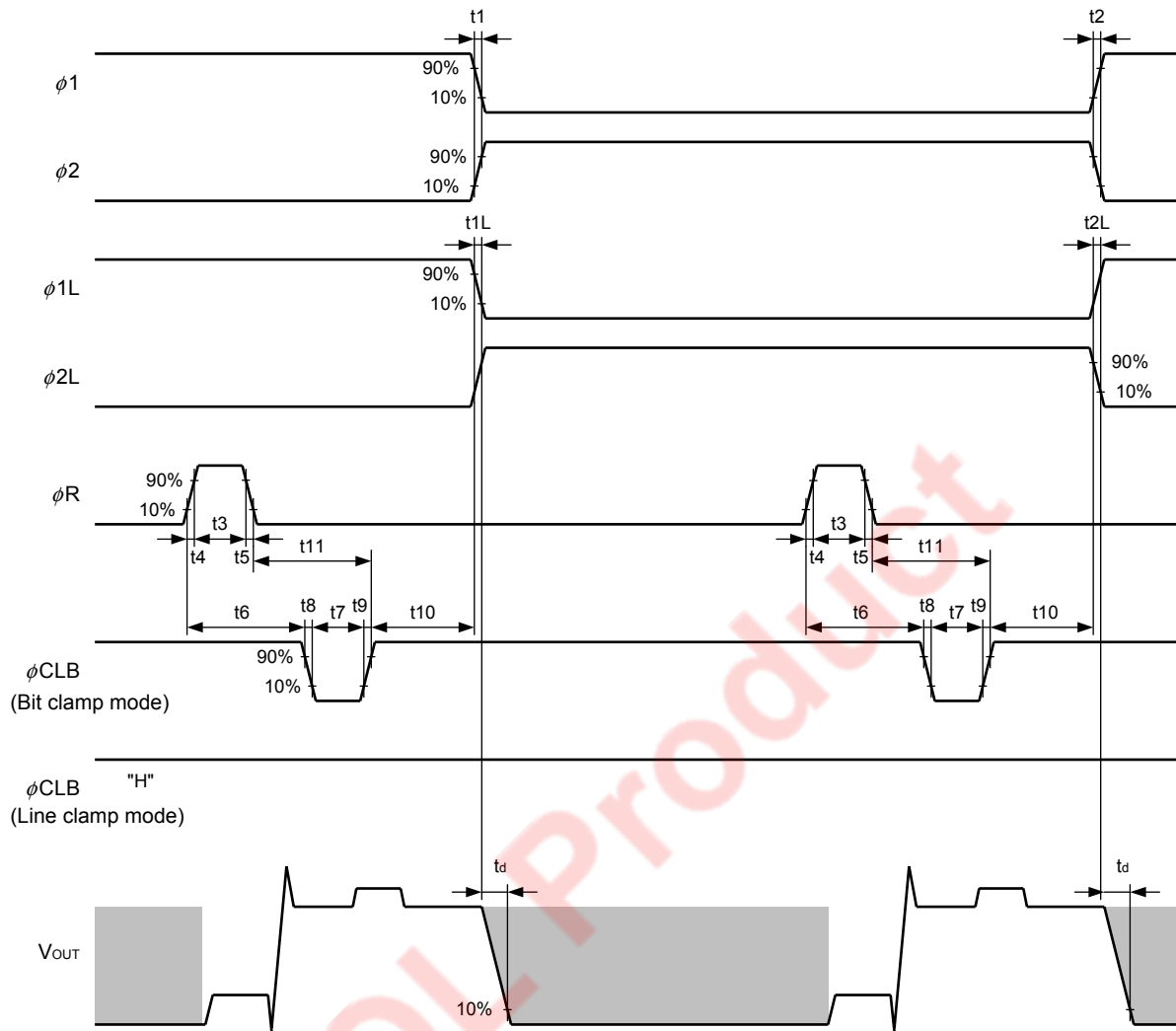
Note Set the ϕ_R to low level and ϕ_{CLB} to high level during this period.

TIMING CHART 1-6 (for each color, 300 dpi, φSEL = low, line clamp mode)



Note Set the ϕ_R to low level and ϕ_{CLB} to high level during this period.

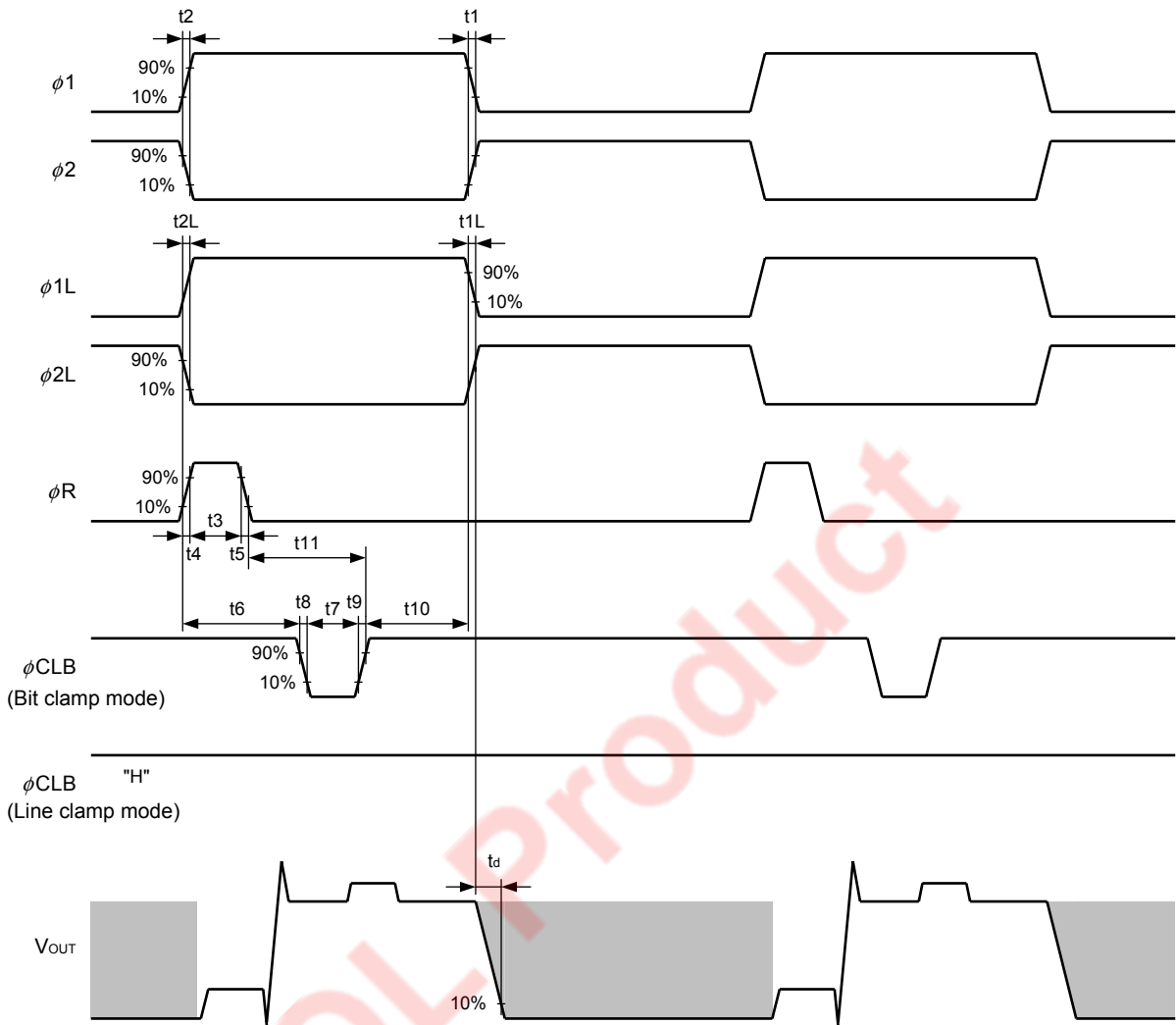
TIMING CHART 2-1 (1200 dpi, for each color)



Symbol	MIN.	TYP. ^{Note}	MAX.	Unit
t1, t2	0	15	–	ns
t1L, t2L	0	5	–	ns
t3	5	50	–	ns
t4, t5	0	5	–	ns
t6	0	70	–	ns
t7	10	50	–	ns
t8, t9	0	5	–	ns
t10	0	45	–	ns
t11	10	50	–	ns

Note TYP. is the case of $\phi R = 2$ MHz

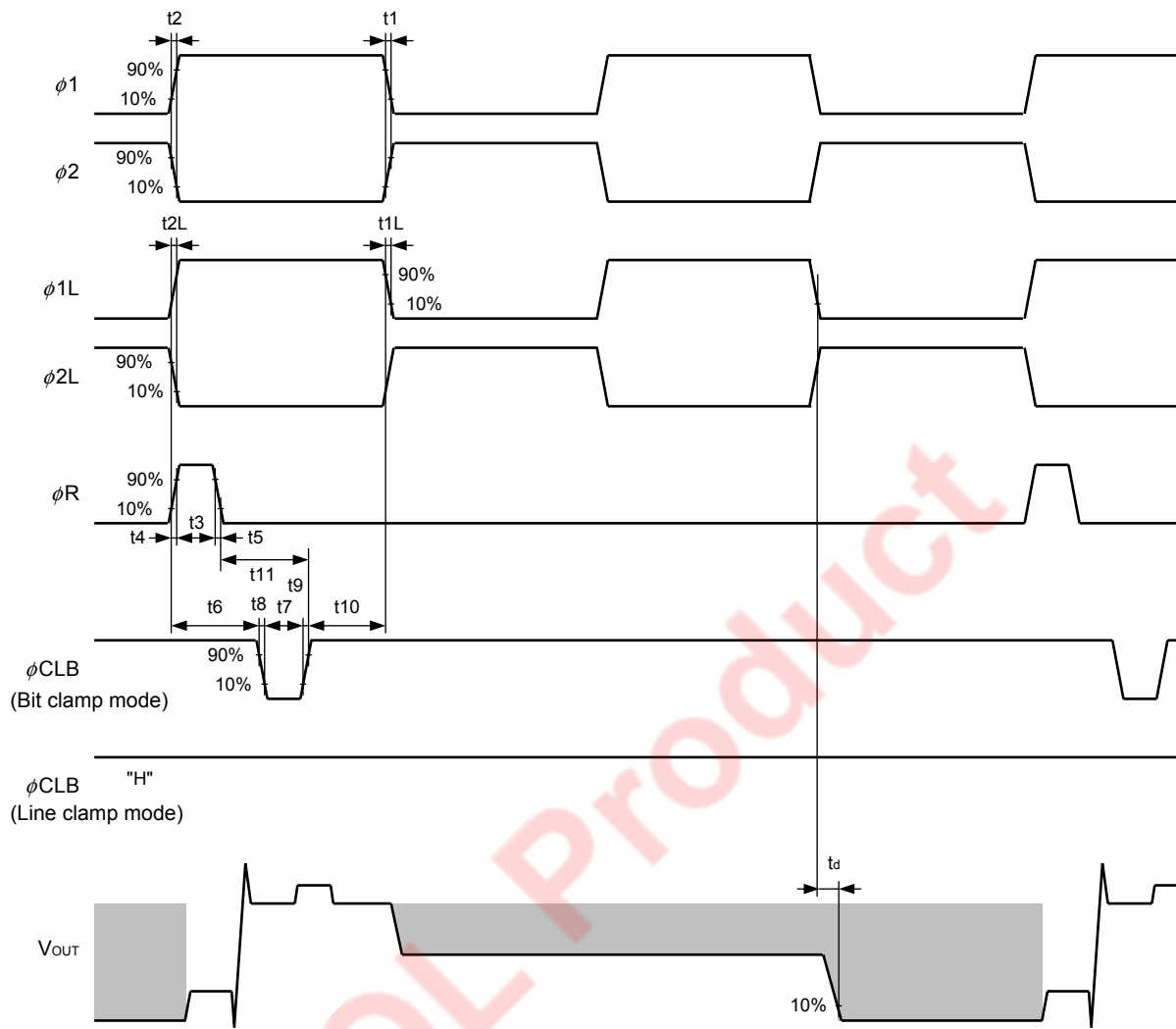
TIMING CHART 2-2 (600 dpi, for each color)



Symbol	MIN.	TYP. ^{Note}	MAX.	Unit
t1, t2	0	15	–	ns
t1L, t2L	0	5	–	ns
t3	5	50	–	ns
t4, t5	0	5	–	ns
t6	0	70	–	ns
t7	10	50	–	ns
t8, t9	0	5	–	ns
t10	0	45	–	ns
t11	10	50	–	ns

Note TYP. is the case of $\phi R = 2$ MHz

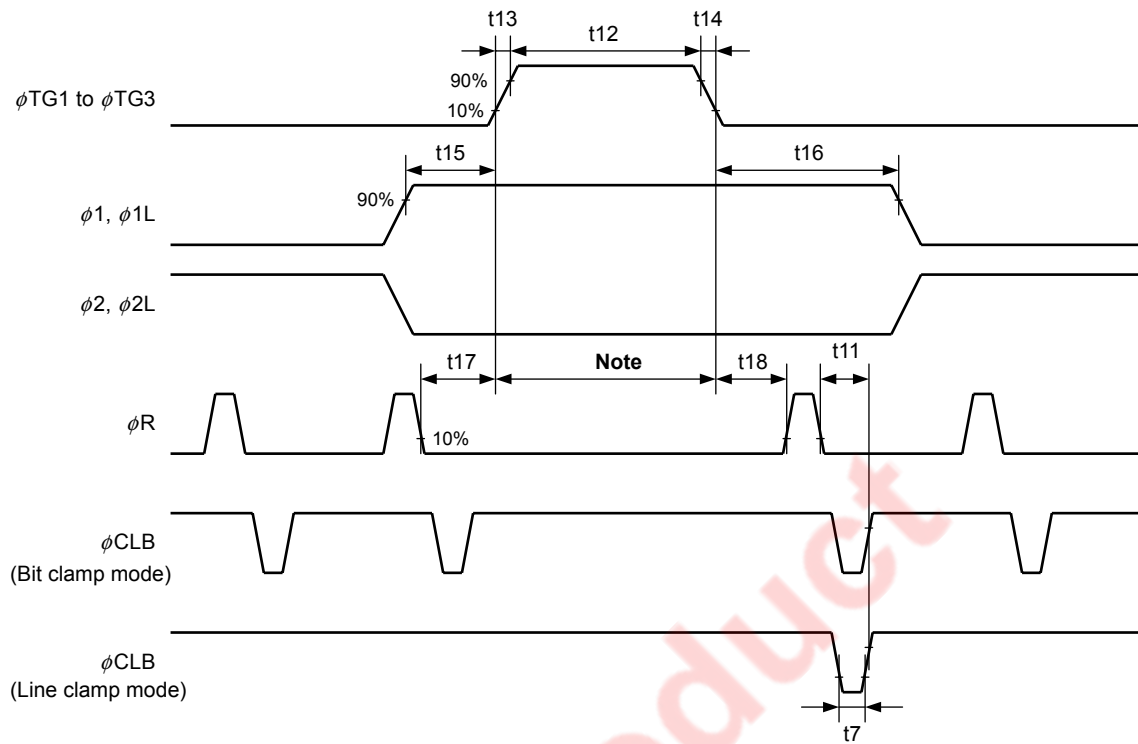
TIMING CHART 2-3 (300 dpi, for each color)



Symbol	MIN.	TYP. ^{Note}	MAX.	Unit
t1, t2	0	15	–	ns
t1L, t2L	0	5	–	ns
t3	5	50	–	ns
t4, t5	0	5	–	ns
t6	0	70	–	ns
t7	10	50	–	ns
t8, t9	0	5	–	ns
t10	0	45	–	ns
t11	10	50	–	ns

Note TYP. is the case of $\phi R = 1$ MHz

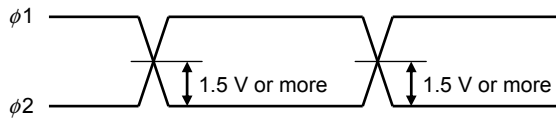
φTG1 to φTG3, φ1, φ2 TIMING CHART



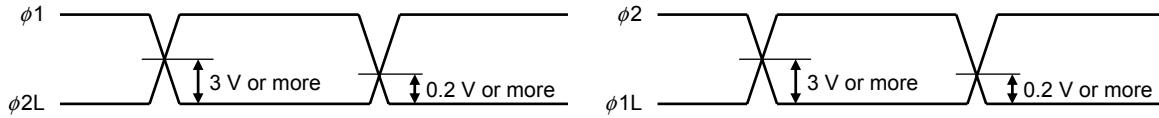
Symbol	MIN.	TYP.	MAX.	Unit
t7	10	50	-	ns
t11	10	50	-	ns
t12	5000	10000	50000	ns
t13, t14	0	50	-	ns
t15, t16	900	1000	-	ns
t17, t18	200	400	-	ns

Note Set the ϕR to low level and ϕCLB to high level during this period.

φ1, φ2 cross points

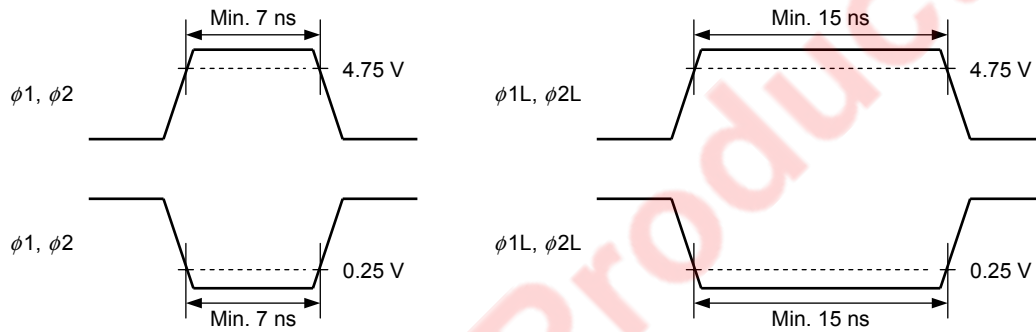


φ1, φ2L cross points, φ2, φ1L cross points

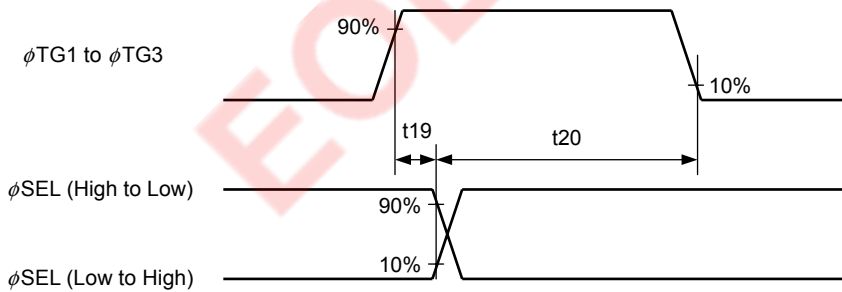


Remark Adjust cross points (φ1, φ2), (φ1L, φ2) and (φ1, φ2L) with input resistance of each pin.

φ1, φ2, φ1L, φ2L clock width



φTG, φSEL TIMING CHART



Symbol	MIN.	TYP.	MAX.	Unit
t19	0	0	–	ns
t20	4500	9500	–	ns

SELECTION OF RESOLUTION MODE

The μPD8874 has function of two readout modes, High Resolution Mode and Low Resolution Mode. These two modes can be selected by φSEL switch.

Read Mode	Description	φSEL
High Resolution Mode	1200 dpi (Max.)	High level
Low Resolution Mode	600 dpi (Max.) (even line readout mode)	Low level

(1) High Resolution Mode

In this mode, both signals in even lines and odd lines can be read out. This mode enables 1200 dpi (Max.) resolution with A4 size (210 × 297 mm, shorter side).

Please refer to **TIMING CHART 1-1, 1-2 and 2-1**.

(2) Low Resolution Mode

In this mode, only signal in even lines can be read out.

This mode enables 600 dpi (Max.) resolution with A4 size.

To use intermittent reset drive enable signal charges of adjacent pixels in even line to add at the charge to voltage conversion area. Then it can achieve low resolution with A4 size such as 300, 200 or 150 dpi.

Please refer to **TIMING CHART 1-3 to 1-6, 2-2 and 2-3**.

EOL Product

DEFINITIONS OF CHARACTERISTIC ITEMS

1. Saturation voltage : V_{sat}

Output signal voltage at which the response linearity is lost.

2. Saturation exposure : SE

Product of intensity of illumination (lx) and storage time (s) when saturation of output voltage occurs.

3. Photo response non-uniformity : PRNU

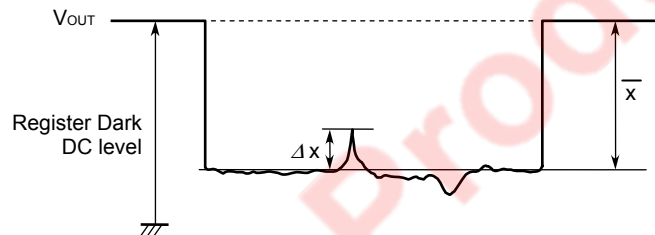
The output signal non-uniformity of all the valid pixels when the photosensitive surface is applied with the light of uniform illumination. This is calculated by the following formula.

$$PRNU (\%) = \frac{\Delta x}{\bar{x}} \times 100$$

Δx : maximum of $|x_j - \bar{x}|$

$$\bar{x} = \frac{\sum_{j=1}^{10800} x_j}{10800}$$

x_j : Output voltage of valid pixel number j



4. Average dark signal : ADS

Average output signal voltage of all the valid pixels at light shielding. This is calculated by the following formula.

$$ADS (mV) = \frac{\sum_{j=1}^{10800} d_j}{10800}$$

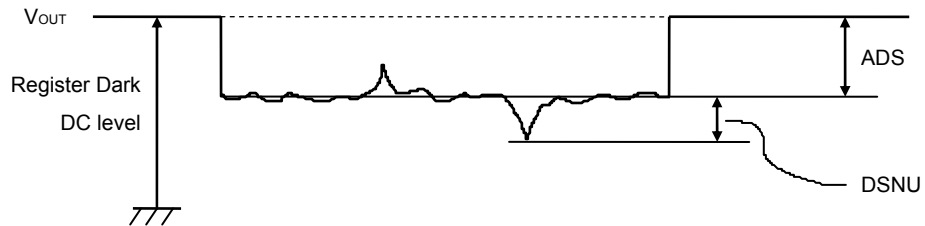
d_j : Dark signal of valid pixel number j

5. Dark signal non-uniformity : DSNU

Absolute maximum of the difference between ADS and voltage of the highest or lowest output pixel of all the valid pixels at light shielding. This is calculated by the following formula.

DSNU (mV) : maximum of $|d_j - ADS|$ $|j = 1 \text{ to } 10800$

d_j : Dark signal of valid pixel number j



6. Output impedance : Zo

Impedance of the output pins viewed from outside.

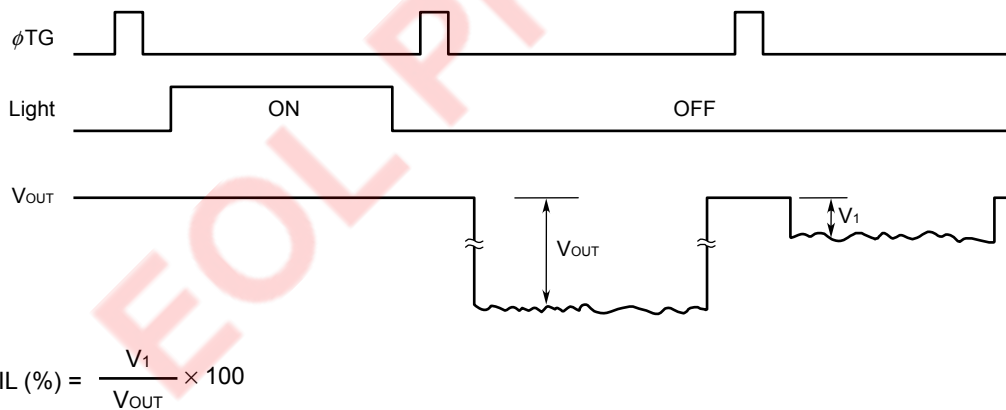
7. Response : R

Output voltage divided by exposure ($I \times s$).

Note that the response varies with a light source (spectral characteristic).

8. Image lag : IL

The rate between the last output voltage and the next one after read out the data of a line.



9. Register imbalance : RI

The rate of the difference between the averages of the output voltage of Odd and Even pixels, against the average output voltage of all the valid pixels.

$$RI (\%) = \frac{\frac{2}{n} \left| \sum_{j=1}^{\frac{n}{2}} (V_{2j-1} - V_{2j}) \right|}{\frac{1}{n} \sum_{j=1}^n V_j} \times 100$$

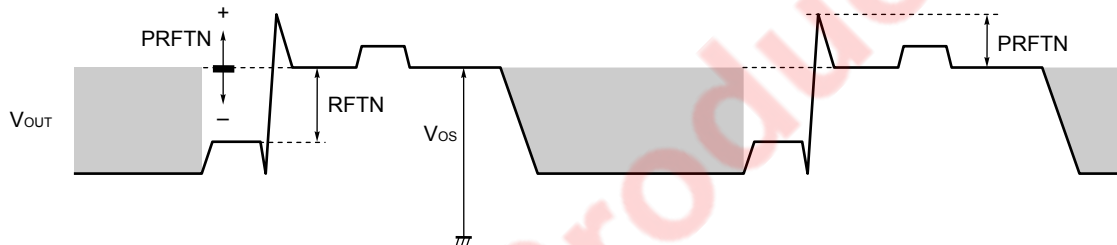
n : Number of valid pixels
 V_j : Output voltage of each pixel

10. Offset level : VOS

DC level of output signal is defined as follows.

11. Reset feed-through noise : RFTN, PRFTN

Reset feed-through noise (RFTN) and peak of RFTN (PRFTN) are defined as follows.

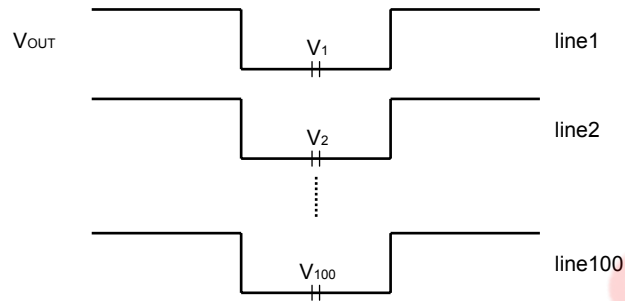


12. Light shielding random noise: σ dark

Light shielding random noise σ dark is defined as the standard deviation of a valid pixel output signal with 100 times (= 100 lines) data sampling at dark (light shielding).

$$\sigma \text{ (mV)} = \sqrt{\frac{\sum_{i=1}^{100} (V_i - \bar{V})^2}{100}}, \quad \bar{V} = \frac{1}{100} \sum_{i=1}^{100} V_i$$

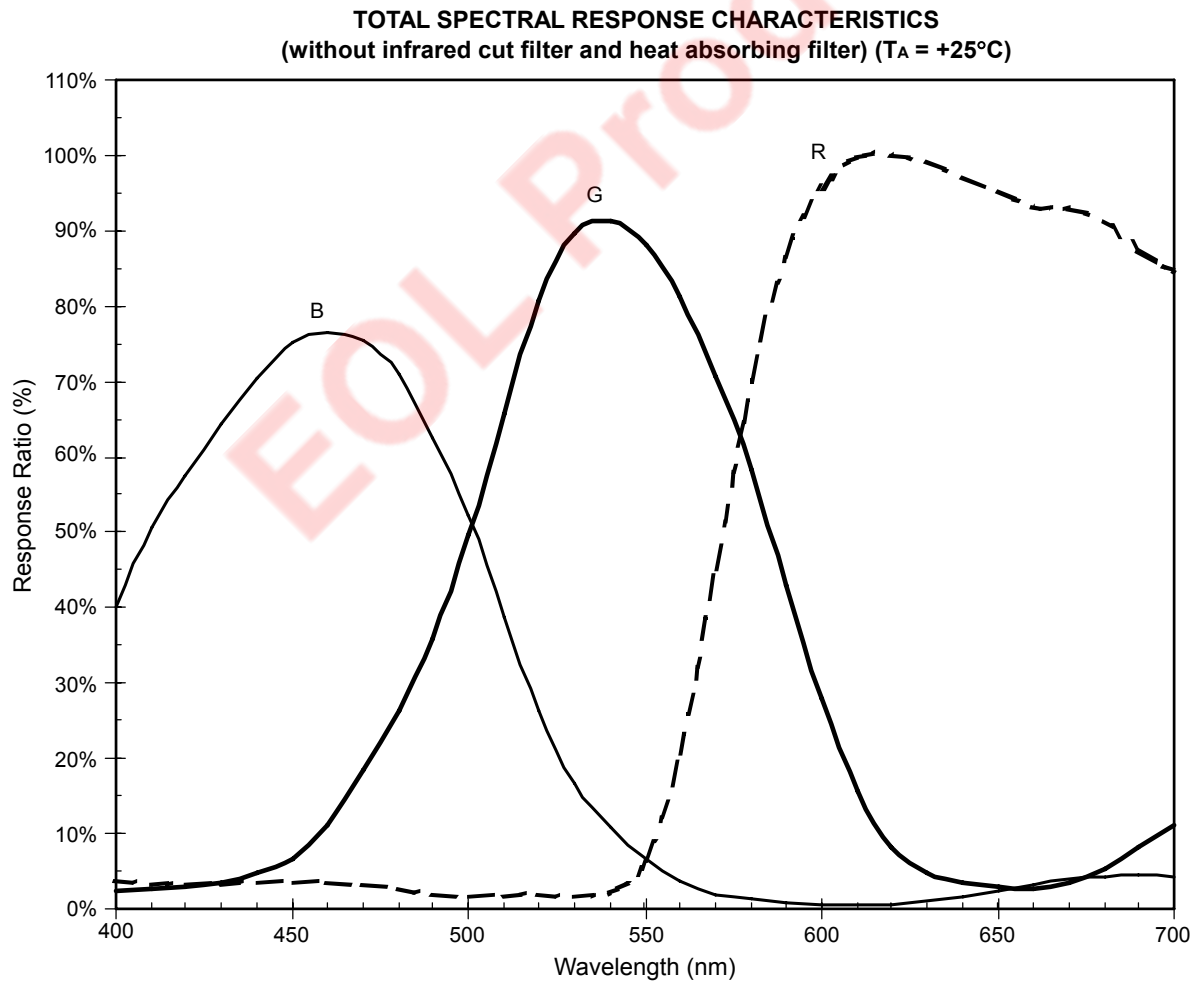
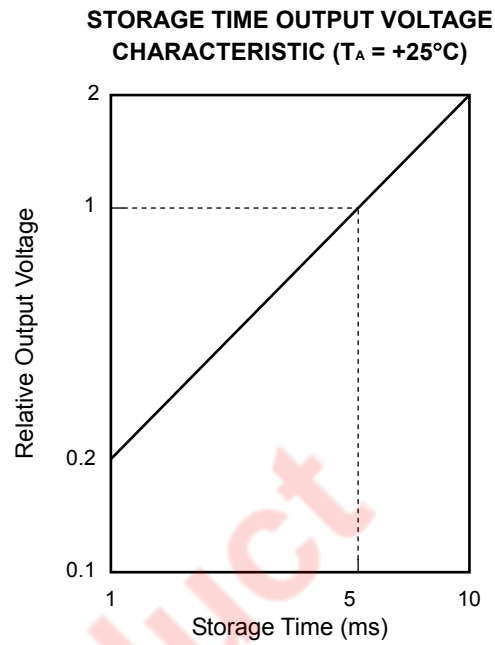
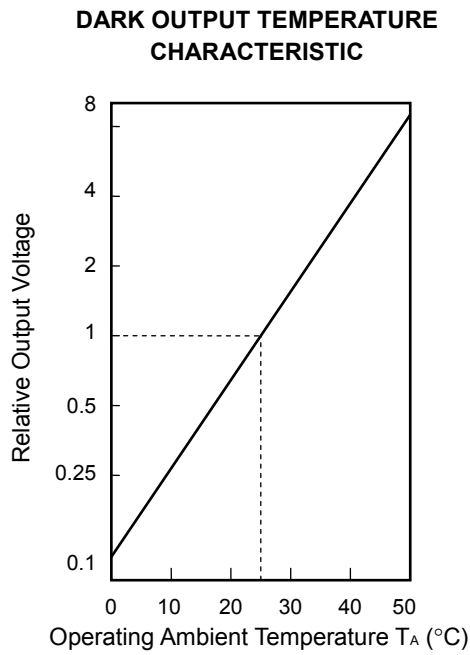
V_i : A valid pixel output signal among all of the valid pixels for each



Remark This is measured by the DC level sampling of only the signal level, not by CDS (Correlated Double Sampling)

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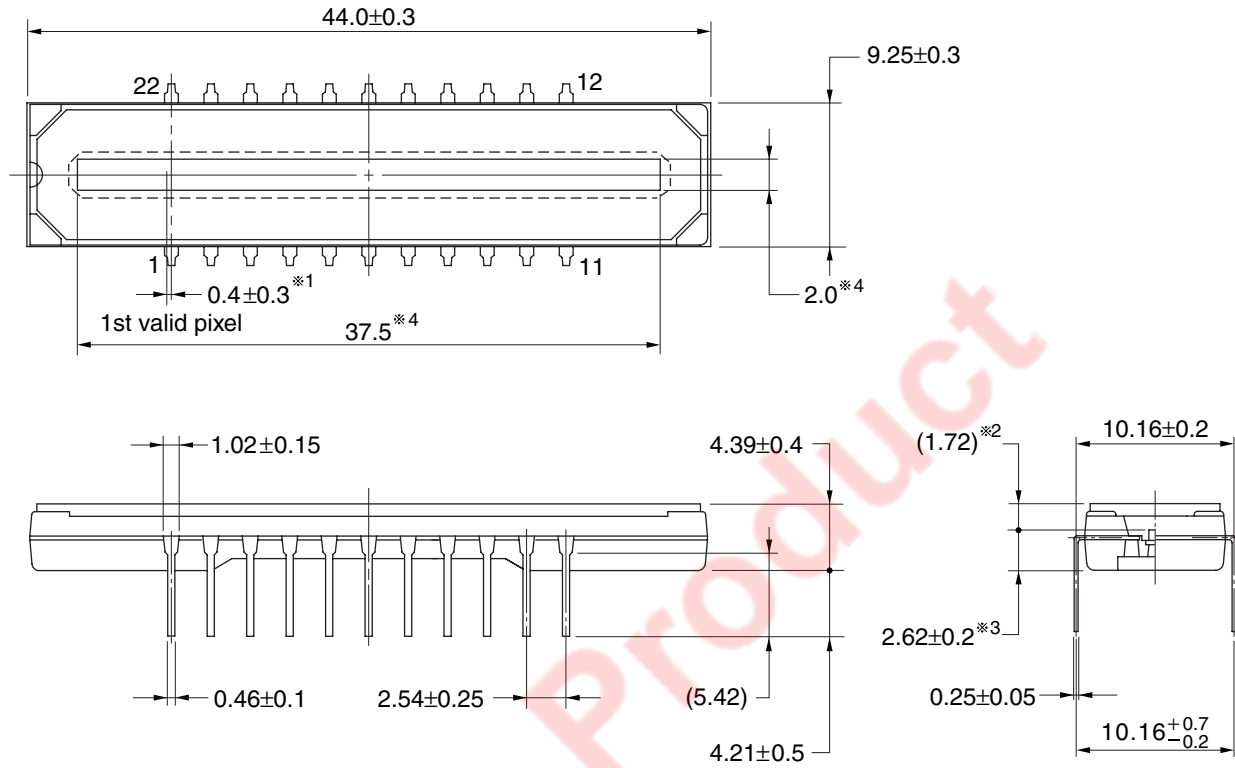
STANDARD CHARACTERISTIC CURVES (Reference Value)



PACKAGE DRAWING

μPD8874CY-A
 CCD LINEAR IMAGE SENSOR 22-PIN PLASTIC DIP (10.16 mm (400))

(Unit : mm)



Name	Dimensions	Refractive index
Plastic cap	42.7×8.35×0.8(0.7*5)	1.5

- ※1 Distance between the 1st valid pixel and the center of the pin1
- ※2 Distance between the top of the cap and the surface of the CCD chip
- ※3 Distance between the bottom of the package and the surface of the CCD chip
- ※4 Transparent window
- ※5 Thickness of the transparent window

22C-1CCD-PKG19

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RECOMMENDED SOLDERING CONDITIONS

When soldering this product, it is highly recommended to observe the conditions as shown below.

If other soldering processes are used, or if the soldering is performed under different conditions, please make sure to consult with our sales offices.

Type of Through-hole Device

μPD8874CY-A: CCD linear image sensor 22-pin plastic DIP (10.16 mm (400))

Process	Conditions
Partial heating method	Pin temperature: 380°C or below, Heat time: 3 seconds or less (per pin).

- Cautions**
1. **During assembly care should be taken to prevent solder or flux from contacting the plastic cap. The optical characteristics could be degraded by such contact.**
 2. **Soldering by the solder flow method may have deleterious effects on prevention of plastic cap soiling and heat resistance. So the method cannot be guaranteed.**

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NOTES ON HANDLING THE PACKAGES

① DUST AND DIRT PROTECTING

The optical characteristics of the CCD will be degraded if the cap is scratched during cleaning. Don't either touch plastic cap surface by hand or have any object come in contact with plastic cap surface. Should dirt stick to a plastic cap surface, blow it off with an air blower. For dirt stuck through electricity ionized air is recommended. And if the plastic cap surface is grease stained, clean with our recommended solvents.

○ CLEANING THE PLASTIC CAP

Care should be taken when cleaning the surface to prevent scratches.
We recommend cleaning the cap with a soft cloth moistened with one of the recommended solvents below. Excessive pressure should not be applied to the cap during cleaning. If the cap requires multiple cleanings it is recommended that a clean surface or cloth be used.

○ RECOMMENDED SOLVENTS

The following are the recommended solvents for cleaning the CCD plastic cap.
Use of solvents other than these could result in optical or physical degradation in the plastic cap. Please consult your sales office when considering an alternative solvent.

Solvents	Symbol
Ethyl Alcohol	EtOH
Methyl Alcohol	MeOH
Isopropyl Alcohol	IPA
N-methyl Pyrrolidone	NMP

② MOUNTING OF THE PACKAGE

The application of an excessive load to the package may cause the package to warp or break, or cause chips to come off internally. Particular care should be taken when mounting the package on the circuit board. Don't have any object come in contact with plastic cap. You should not reform the lead frame. We recommended to use a IC-inserter when you assemble to PCB.

Also, be care that the any of the following can cause the package to crack or dust to be generated.

1. Applying heat to the external leads for an extended period of time with soldering iron.
2. Applying repetitive bending stress to the external leads.
3. Rapid cooling or heating

③ OPERATE AND STORAGE ENVIRONMENTS

Operate in clean environments. CCD image sensors are precise optical equipment that should not be subject to mechanical shocks. Exposure to high temperatures or humidity will affect the characteristics. So avoid storage or usage in such conditions.

Keep in a case to protect from dust and dirt. Dew condensation may occur on CCD image sensors when the devices are transported from a low-temperature environment to a high-temperature environment. Avoid such rapid temperature changes.

For more details, refer to our document "Review of Quality and Reliability Handbook" (C12769E)

④ ELECTROSTATIC BREAKDOWN

CCD image sensor is protected against static electricity, but destruction due to static electricity is sometimes detected. Before handling be sure to take the following protective measures.

1. Ground the tools such as soldering iron, radio cutting pliers of or pincer.
2. Install a conductive mat or on the floor or working table to prevent the generation of static electricity.
3. Either handle bare handed or use non-chargeable gloves, clothes or material.
4. Ionized air is recommended for discharge when handling CCD image sensor.
5. For the shipment of mounted substrates, use box treated for prevention of static charges.
6. Anyone who is handling CCD image sensors, mounting them on PCBs or testing or inspecting PCBs on which CCD image sensors have been mounted must wear anti-static bands such as wrist straps and ankle straps which are grounded via a series resistance connection of about 1 MΩ.

[MEMO]

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[MEMO]

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NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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