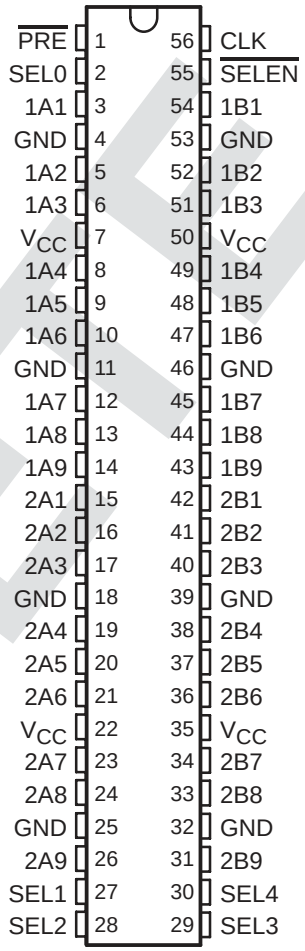
- ***EPIC*** ™ **(Enhanced-Performance Implanted CMOS) Submicron Process**
- **Member of the Texas Instruments *Widebus+*™ Family**
- ***UBE*** ™ **(Universal Bus Exchanger) Allows Synchronous Data Exchange**
- **Designed to Facilitate Incident-Wave Switching for Line Impedances of 50 Ω or Greater**
- **Typical $V_{OLP}$ (Output Ground Bounce) < 0.8 V at $V_{CC}$ = 3.3 V, $T_A$ = 25°C**
- **Typical $V_{OHV}$ (Output $V_{OH}$ Undershoot) > 2 V at $V_{CC}$ = 3.3 V, $T_A$ = 25°C**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

**DGG OR DL PACKAGE**
**(TOP VIEW)**




## description

The SN74ALVC16409 allows synchronous data exchange between four different buses.

Data flow is controlled by the select ($\overline{SEL0}$−$\overline{SEL4}$) inputs. A data-flow state is stored on the rising edge of the clock (CLK) input if the select-enable ($\overline{SELEN}$) input is low. Once a data-flow state has been established, data is stored in the flip-flop on the rising edge of CLK if $\overline{SELEN}$ is high.

The data-flow control logic is designed to allow glitch-free data transmission.

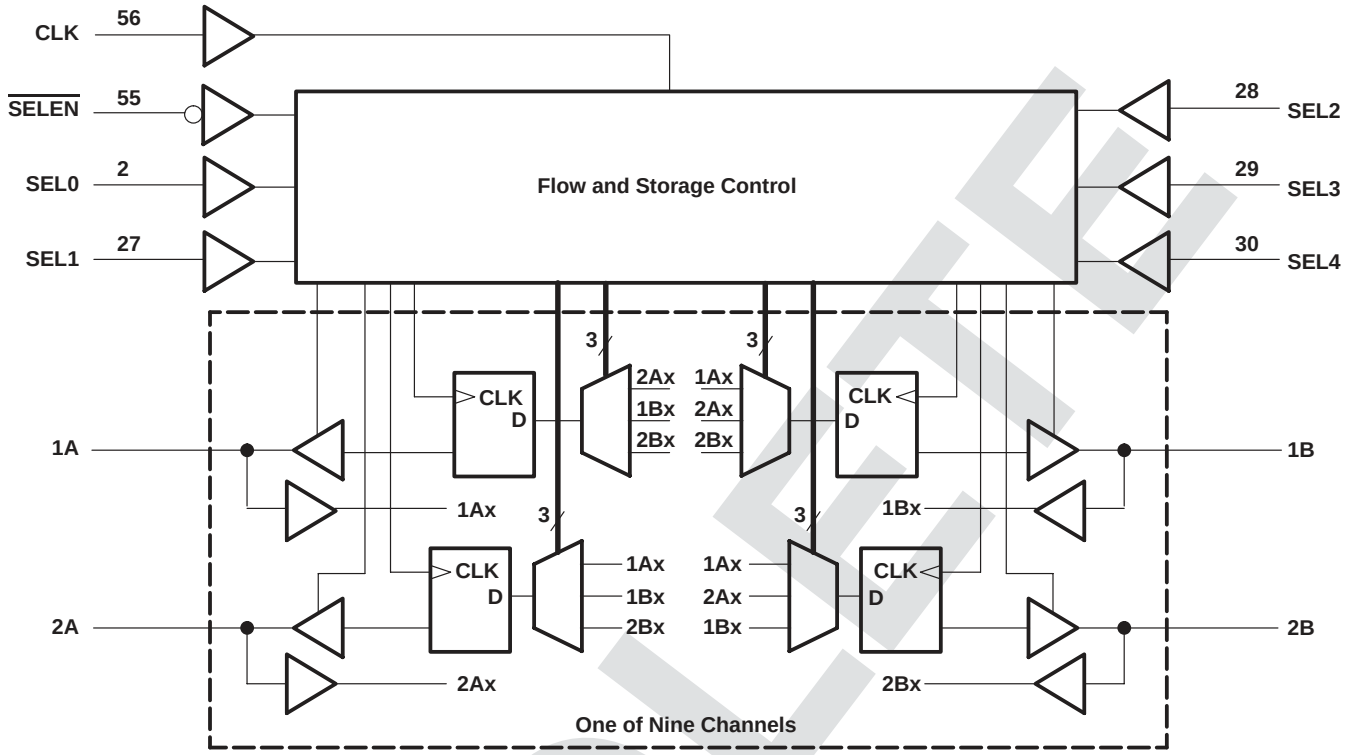
Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVC16409 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16409 is characterized for operation from −40°C to 85°C.



## logic diagram (positive logic)




**FUNCTION TABLE**

| INPUTS | | OUTPUT RECEIVE PORT |
|---|---|---|
| CLK | SEND PORT | |
| X | X | $B_0$† |
| X | L | L |
| X | H | H |
| ↑ | L | L |
| ↑ | H | H |
| H | X | $B_0$† |
| L | X | $B_0$† |

† Output level before the indicated steady-state input conditions were established

**DATA-FLOW CONTROL FUNCTION TABLE**

| INPUTS | | | | | | | DATA FLOW |
|---|---|---|---|---|---|---|---|
| $\overline{\text{SELEN}}$ | CLK | SEL0 | SEL1 | SEL2 | SEL3 | SEL4 | |
| H | ↑ | X | X | X | X | X | No change |
| L | ↑ | 0 | 0 | 0 | 0 | 0 | None, all I/Os off |
| L | ↑ | 0 | 0 | 0 | 0 | 1 | Not used |
| L | ↑ | 0 | 0 | 0 | 1 | 0 | Not used |
| L | ↑ | 0 | 0 | 0 | 1 | 1 | Not used |
| L | ↑ | 0 | 0 | 1 | 0 | 0 | Not used |
| L | ↑ | 0 | 0 | 1 | 0 | 1 | Not used |
| L | ↑ | 0 | 0 | 1 | 1 | 0 | Not used |
| L | ↑ | 0 | 0 | 1 | 1 | 1 | Not used |
| L | ↑ | 0 | 1 | 0 | 0 | 0 | 2A to 1A and 1B to 2B |
| L | ↑ | 0 | 1 | 0 | 0 | 1 | 2A to 1A |
| L | ↑ | 0 | 1 | 0 | 1 | 0 | 2B to 1B |
| L | ↑ | 0 | 1 | 0 | 1 | 1 | 2A to 1A and 2B to 1B |
| L | ↑ | 0 | 1 | 1 | 0 | 0 | 1A to 2A and 1B to 2B |
| L | ↑ | 0 | 1 | 1 | 0 | 1 | 1A to 2A |
| L | ↑ | 0 | 1 | 1 | 1 | 0 | 1B to 2B |
| L | ↑ | 0 | 1 | 1 | 1 | 1 | 1A to 2A and 2B to 1B |
| L | ↑ | 1 | 0 | 0 | 0 | 0 | 1A to 1B and 2B to 2A |
| L | ↑ | 1 | 0 | 0 | 0 | 1 | 1A to 1B |
| L | ↑ | 1 | 0 | 0 | 1 | 0 | 2A to 2B |
| L | ↑ | 1 | 0 | 0 | 1 | 1 | 1A to 1B and 2A to 2B |
| L | ↑ | 1 | 0 | 1 | 0 | 0 | 1B to 1A and 2A to 2B |
| L | ↑ | 1 | 0 | 1 | 0 | 1 | 1B to 1A |
| L | ↑ | 1 | 0 | 1 | 1 | 0 | 2B to 2A |
| L | ↑ | 1 | 0 | 1 | 1 | 1 | 1B to 1A and 2B to 2A |
| L | ↑ | 1 | 1 | 0 | 0 | 0 | 2B to 1A and 2A to 1B |
| L | ↑ | 1 | 1 | 0 | 0 | 1 | 1B to 2A |
| L | ↑ | 1 | 1 | 0 | 1 | 0 | 2B to 1A |
| L | ↑ | 1 | 1 | 0 | 1 | 1 | 2B to 1A and 1B to 2A |
| L | ↑ | 1 | 1 | 1 | 0 | 0 | 1A to 2B and 1B to 2A |
| L | ↑ | 1 | 1 | 1 | 0 | 1 | 1A to 2B |
| L | ↑ | 1 | 1 | 1 | 1 | 0 | 2A to 1B |
| L | ↑ | 1 | 1 | 1 | 1 | 1 | 1A to 2B and 2A to 1B |

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . −0.5 V to 4.6 V
Input voltage range, VI: Except I/O ports (see Note 1) . . . . . −0.5 V to $V_{CC}$ + 4.6 V
I/O ports (see Notes 1 and 2) . . . . . −0.5 V to $V_{CC}$ + 0.5 V
Output voltage range, $V_O$ (see Notes 1 and 2) . . . . . −0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) . . . . . −50 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) . . . . . ±50 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) . . . . . ±50 mA
Continuous current through $V_{CC}$ or GND pins . . . . . ±100 mA
Maximum power dissipation at $T_A$ = 55°C (in still air) (see Note 3): DGG package . . . . . 1 W
DL package . . . . . 1.4 W
Storage temperature range, $T_{stg}$ . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

### recommended operating conditions (see Note 4)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2.7 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2.7 V to 3.6 V | 2 | | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.7 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2.7 V to 3.6 V | | 0.8 | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | 0.7 | |
| $V_I$ | Input voltage | | 0 | $V_{CC}$ | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2.3 V | | −12 | mA |
| | | $V_{CC}$ = 2.7 V | | −12 | |
| | | $V_{CC}$ = 3 V | | −24 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2.3 V | | 12 | mA |
| | | $V_{CC}$ = 2.7 V | | 12 | |
| | | $V_{CC}$ = 3 V | | 24 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 0 | 10 | ns/V |
| $T_A$ | Operating free-air temperature | | −40 | 85 | °C |

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | $V_{CC}$† | $T_A$ = −40°C to 85°C | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP‡ | MAX | |
| $V_{OH}$ | $I_{OH}$ = −100 μA | | MIN to MAX | $V_{CC}$ − 0.2 | | | V |
| | $I_{OH}$ = −6 mA | $V_{IH}$ = 1.7 V | 2.3 V | 2 | | | |
| | $I_{OH}$ = −12 mA | $V_{IH}$ = 1.7 V | 2.3 V | 1.7 | | | |
| | | $V_{IH}$ = 2 V | 2.7 V | 2.2 | | | |
| | | $V_{IH}$ = 2 V | 3 V | 2.4 | | | |
| | $I_{OH}$ = −24 mA | $V_{IH}$ = 2 V | 3 V | 2 | | | |
| $V_{OL}$ | $I_{OL}$ = 100 μA | | MIN to MAX | | | 0.2 | V |
| | $I_{OL}$ = 6 mA | $V_{IL}$ = 0.7 V | 2.3 V | | | 0.4 | |
| | $I_{OL}$ = 12 mA | $V_{IL}$ = 0.7 V | 2.3 V | | | 0.7 | |
| | | $V_{IL}$ = 0.8 V | 2.7 V | | | 0.4 | |
| | $I_{OL}$ = 24 mA | $V_{IL}$ = 0.8 V | 3 V | | | 0.55 | |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | | 3.6 V | | | ±5 | μA |
| $I_{I(hold)}$ | $V_I$ = 0.7 V | | 2.3 V | 45 | | | μA |
| | $V_I$ = 1.7 V | | | −45 | | | |
| | $V_I$ = 0.8 V | | 3 V | 75 | | | |
| | $V_I$ = 2 V | | | −75 | | | |
| | $V_I$ = 0 to 3.6 V | | 3.6 V | | | ±500 | |
| $I_{OZ}$§ | $V_O$ = $V_{CC}$ or GND | | 3.6 V | | | ±10 | μA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, | $I_O$ = 0 | 3.6 V | | | 40 | μA |
| $\Delta I_{CC}$ | One input at $V_{CC}$ − 0.6 V, | Other inputs at $V_{CC}$ or GND | 3 V to 3.6 V | | | 500 | μA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | | 3.3 V | | 4 | | pF |
| $C_o$ | $V_O$ = $V_{CC}$ or GND | | 3.3 V | | 8 | | pF |

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.
‡ All typical values are measured at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.
§ For I/O ports, the parameter $I_{OZ}$ includes the input leakage current.

## timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| | | | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 2.7 V | $V_{CC}$ = 3.3 V ± 0.3 V | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MIN | MAX | |
| $f_{clock}$ | Clock frequency | | 0 | 120 | | 0 | 120 | MHz |
| $t_w$ | Pulse duration, CLK high or low | | 4.2 | | 4.2 | 3 | | ns |
| $t_{su}$ | Setup time | A or B before CLK↑ | 1.9 | | 1.9 | 1.4 | | ns |
| | | S before CLK↑ | 5.1 | | 4.2 | 3.5 | | |
| | | $\overline{\text{SELEN}}$ before CLK↑ | 2.5 | | 2.5 | 1.8 | | |
| | | $\overline{\text{PRE}}$ before CLK↑ | 1 | | 1 | 0.7 | | |
| $t_h$ | Hold time | A or B after CLK↑ | 0.8 | | 0.8 | 1 | | ns |
| | | S after CLK↑ | 0 | | 0 | 0 | | |
| | | $\overline{\text{SELEN}}$ after CLK↑ | 0.5 | | 0.5 | 0.8 | | |

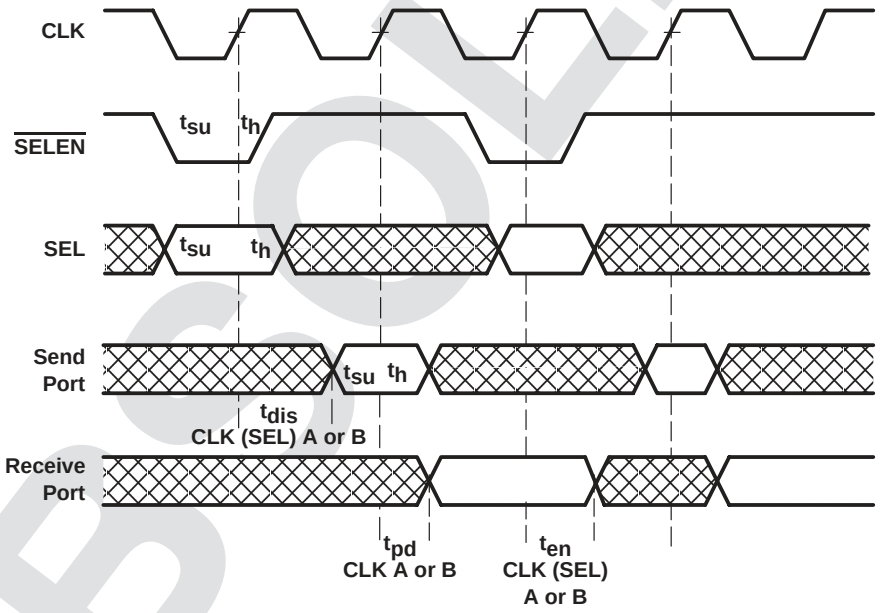
### switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (unless otherwise noted) (see Figures 1 and 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 2.5 V ± 0.2 V | | | $V_{CC}$ = 2.7 V | $V_{CC}$ = 3.3 V ± 0.3 V | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MAX | MIN | TYP | MAX | |
| $f_{max}$ | | | 120 | | | | 120 | | | MHz |
| $t_{pd}$ | CLK (A or B) | B or A | 2 | 4.2 | 6.6 | 5.7 | 1.5 | 3.3 | 5.1 | ns |
| $t_{en}$ | CLK (SEL) | A or B | 2.5 | 4.8 | 7.4 | 6.3 | 2 | 3.8 | 5.7 | ns |
| $t_{dis}$ | CLK (SEL) | A or B | 3 | 5.1 | 7.3 | 6 | 2 | 4 | 5.7 | ns |
| $t_{dis}$ | $\overline{PRE}$ | A or B | 3.5 | 5.5 | 7.7 | 6.5 | 2.5 | 4.2 | 6.1 | ns |

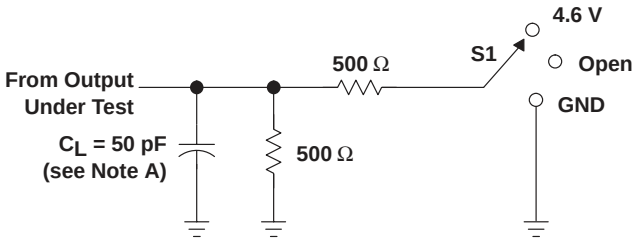
### operating characteristics, $T_A$ = 25°C

| PARAMETER | | | TEST CONDITIONS | $V_{CC}$ = 2.5 V ± 0.2 V | $V_{CC}$ = 3.3 V ± 0.3 V | UNIT |
|---|---|---|---|---|---|---|
| | | | | TYP | TYP | |
| $C_{pd}$ | Power dissipation capacitance | Outputs enabled | $C_L$ = 50 pF, f = 10 MHz | 60 | 60 | pF |
| | | Outputs disabled | | | | |

### timing diagram

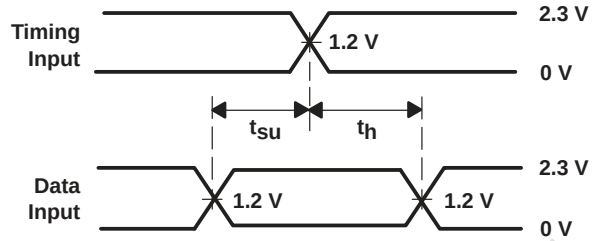


## PARAMETER MEASUREMENT INFORMATION
## $V_{CC}$ = 2.5 V ± 0.2 V

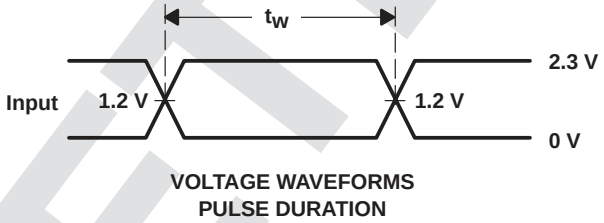



| TEST | S1 |
|---|---|
| $t_{pd}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 4.6 V |
| $t_{PHZ}/t_{PZH}$ | GND |

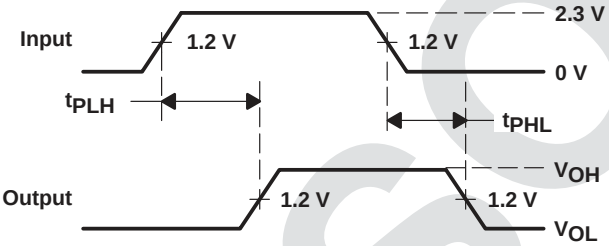
LOAD CIRCUIT



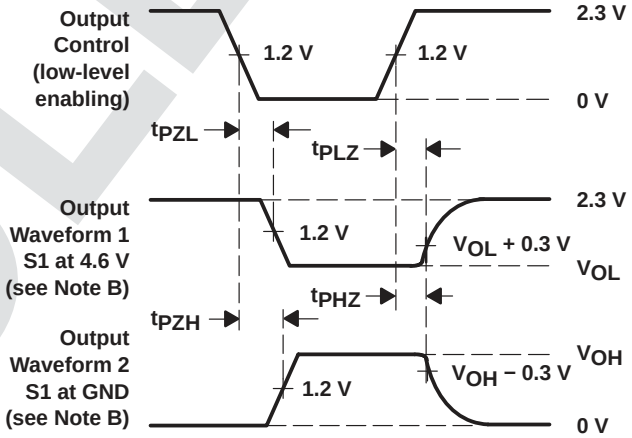

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

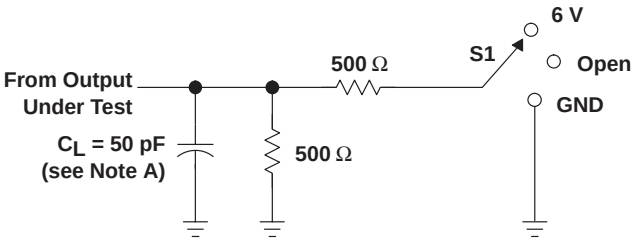



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

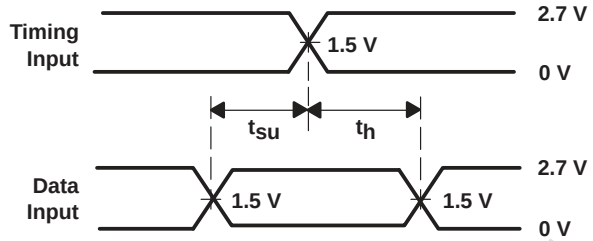
**Figure 1. Load Circuit and Voltage Waveforms**

## PARAMETER MEASUREMENT INFORMATION
## $V_{CC}$ = 2.7 V AND 3.3 V ± 0.3 V

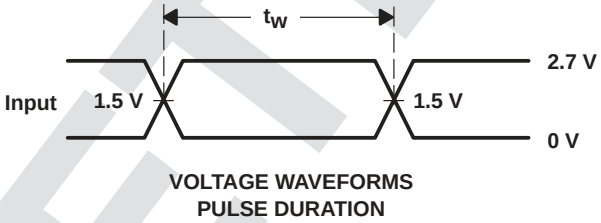



| TEST | S1 |
|---|---|
| $t_{pd}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 6 V |
| $t_{PHZ}/t_{PZH}$ | GND |

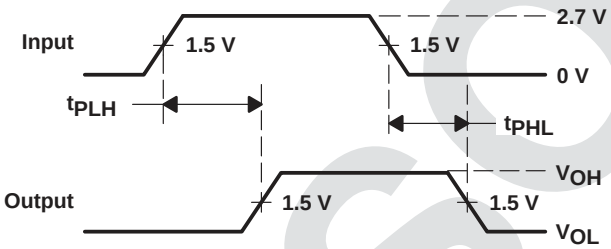
LOAD CIRCUIT



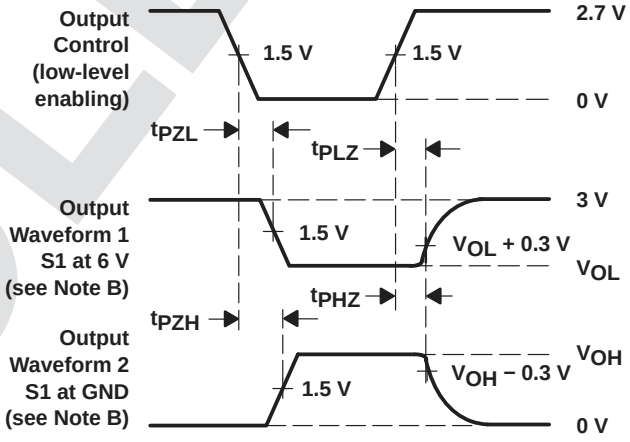

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

**Figure 2. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74ALVC16409DL | OBSOLETE | SSOP | DL | 56 | | TBD | Call TI | Call TI | -40 to 85 | | |
| SN74ALVC16409DLR | OBSOLETE | SSOP | DL | 56 | | TBD | Call TI | Call TI | -40 to 85 | | |

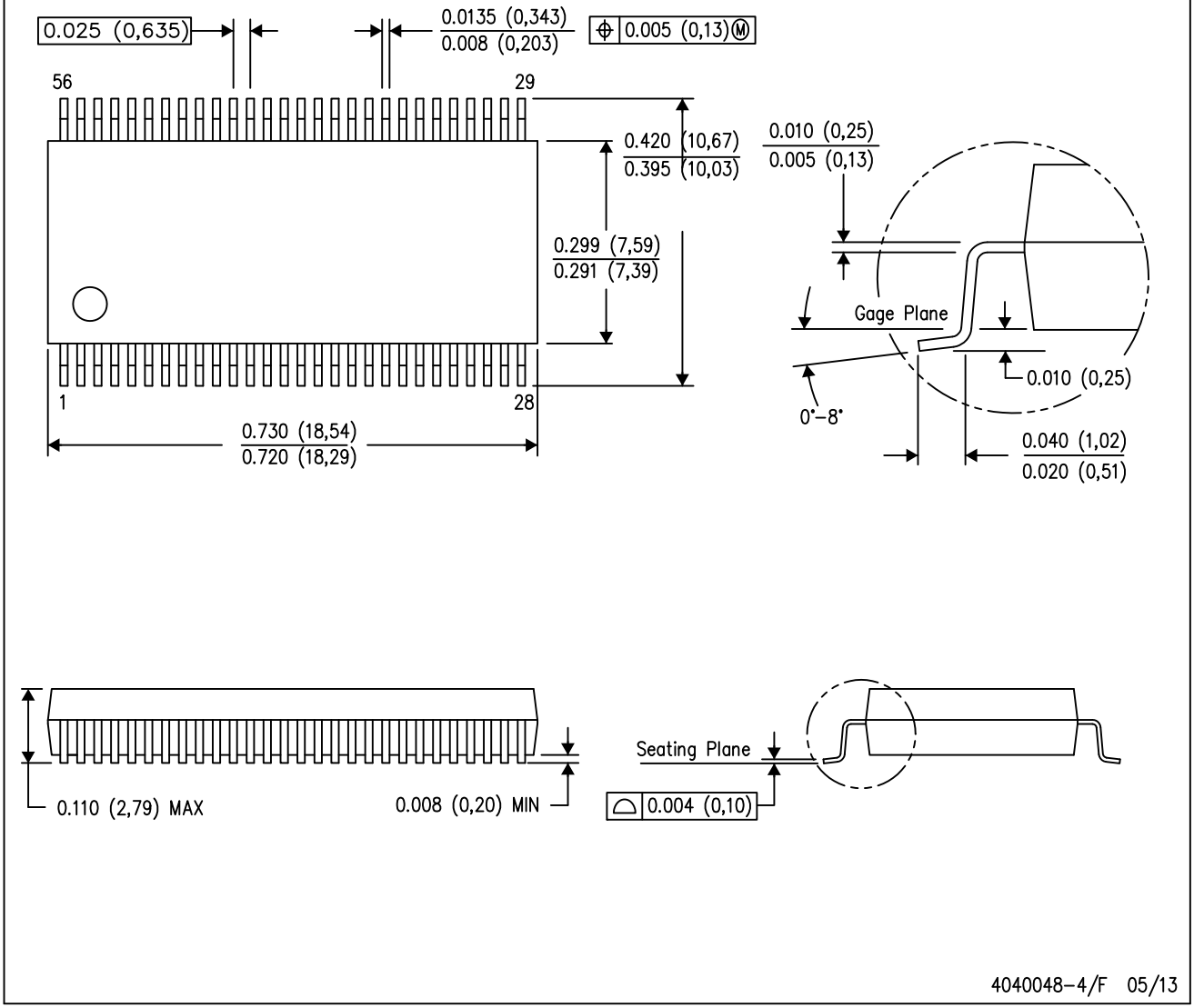
(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

DL (R–PDSO–G56) PLASTIC SMALL–OUTLINE PACKAGE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO–118

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