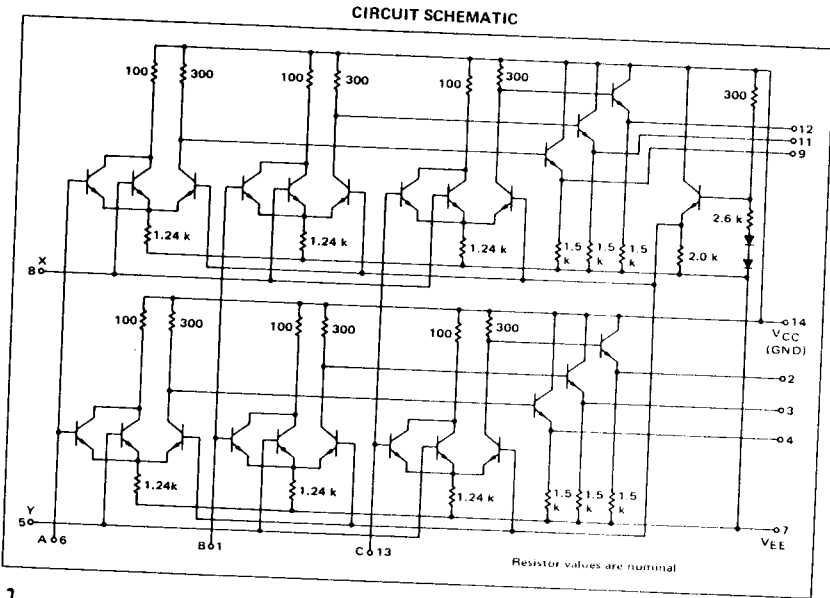
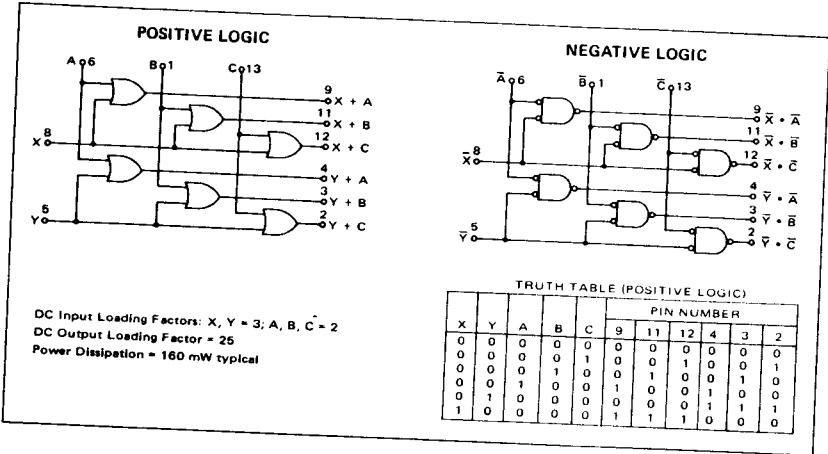
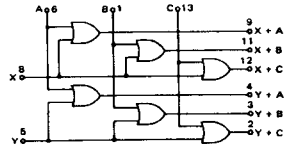


**MC1029
MC1229**

A 2 X 3 array of 2-input OR gates, designed primarily for the handling of data in a digital system.



MC1029, MC1229 (continued)

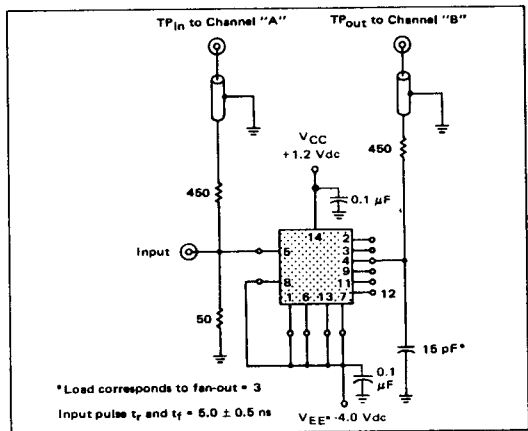


ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	MC1229 Test Limits						MC1029 Test Limits								
			-55°C		+25°C		+125°C		0°C		+25°C		+75°C		Unit		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
Power Supply Drain Current	I_E	7	-	-	-	36	-	-	mAdc	-	-	-	45	-	-	mAdc	
Input Current	I_{in}	5	-	-	-	300	-	-	μ Adc	-	-	-	300	-	-	μ Adc	
		8	-	-	-	300	-	-	-	-	-	-	300	-	-	-	
		1	-	-	-	200	-	-	-	-	-	-	200	-	-	-	
		6	-	-	-	200	-	-	-	-	-	-	200	-	-	-	
Input Leakage Current	I_R	5, 8*	-	-	-	0.6	-	3.0	μ Adc	-	-	-	0.6	-	3.0	μ Adc	
		1, 6, 13*	-	-	-	0.4	-	2.0	μ Adc	-	-	-	0.4	-	2.0	μ Adc	
Logical "1" Output Voltage	$V_{OH} \ddagger$	3, 11†	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc	
		4, 9†	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
Logical "0" Output Voltage	V_{OL}	2, 12†	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc	
		2, 3, 4†	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
Switching Times	Propagation Delay	t_{5+4+}	4	4.0	7.5	4.0	7.5	6.0	9.0	ns	4.0	7.5	4.0	7.5	5.0	8.0	ns
			↓	4.0	7.5	4.0	7.5	6.0	9.0	↓	4.0	7.5	4.0	7.5	5.0	8.0	↓
Rise Time	Fall Time	t_{4+}	↓	5.0	8.5	5.0	8.5	7.0	9.5	↓	5.0	8.5	5.0	8.5	6.0	9.0	↓
			↓	5.0	8.0	5.0	8.0	7.0	9.0	↓	5.0	8.0	5.0	8.0	6.0	8.5	↓
Propagation Delay	Rise Time	Fall Time	t_{1+3+}	3	4.0	7.5	4.0	7.5	6.0	↓	4.0	7.5	4.0	7.5	5.0	8.0	↓
				↓	4.0	7.5	4.0	7.5	6.0	↓	4.0	7.5	4.0	7.5	5.0	8.0	↓
Rise Time	Fall Time	t_{1-3-}	↓	5.0	8.5	5.0	8.5	7.0	9.5	↓	5.0	8.5	5.0	8.5	6.0	9.0	↓
			↓	5.0	8.0	5.0	8.0	7.0	8.0	↓	5.0	8.0	5.0	8.0	6.0	8.5	↓

* Individually test each input using the pin connections shown. † Individually test each output using the pin connections shown.

SWITCHING TIME TEST CIRCUIT
@ 25°C

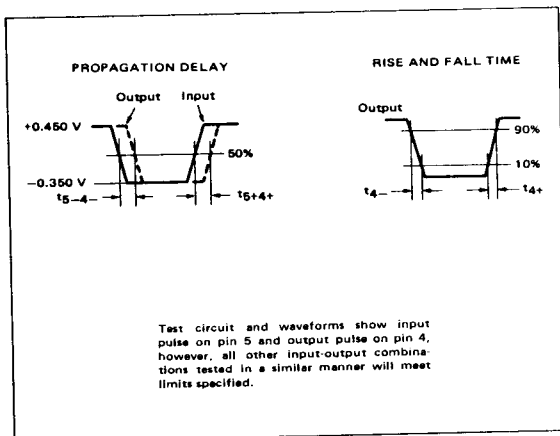


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		TEST VOLTAGE/CURRENT VALUES					
@ Test Temperature		V _{dc} ± 1.0%				mAdc	
		V _{IL min} to V _{IL max}	V _{IH min} to V _{IH max}	V _{IH max}	V _{EE}	I _L	
MC1229	-55°C	-5.2 to -1.405	-1.165 to -0.825	-	-5.2	-2.5	
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5	
	+125°C	-5.2 to -1.205	-0.875 to -0.530	-	-5.2	-2.5	
MC1029	0°C	-5.2 to -1.350	-1.070 to -0.740	-	-5.2	-2.5	
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5	
	+75°C	-5.2 to -1.260	-0.950 to -0.615	-	-5.2	-2.5	

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW:					V _{cc} (Gnd)
			V _{IL min} to V _{IL max}	V _{IH min} to V _{IH max}	V _{IH max}	V _{EE}	I _L	
Power Supply Drain Current	I _E	7	-	-	-	1, 5, 6, 7, 8, 13	-	14
Input Current	I _{in}	5	-	-	5	1, 6, 7, 8, 13	-	14
		8	-	-	8	1, 5, 6, 7, 13	-	14
		1	-	-	1	5, 6, 7, 8, 13	-	14
		6	-	-	6	1, 5, 7, 8, 13	-	14
Input Leakage Current	I _R	5, 8*	-	-	-	1, 5, 6, 7, 8, 13	-	14
		1, 6, 13*	-	-	-	1, 5, 6, 7, 8, 13	-	14
		3, 11†	-	1	-	5, 6, 7, 8, 13	↑	14
		4, 9†	-	6	-	1, 5, 7, 8, 13	↑	14
Logical "1" Output Voltage	V _{OH} †	2, 12†	-	13	-	1, 5, 6, 7, 8	-	14
		2, 3, 4†	-	5	-	1, 6, 7, 8, 13	-	14
		9, 11, 12†	-	8	-	1, 5, 6, 7, 13	-	14
		3, 11†	1	-	-	5, 6, 7, 8, 13	-	14
Logical "0" Output Voltage	V _{OL}	4, 9†	13	-	-	1, 5, 7, 8, 13	-	14
		2, 12†	5	-	-	1, 5, 6, 7, 8	-	14
		2, 3, 4†	8	-	-	1, 6, 7, 8, 13	-	14
		9, 11, 12†	8	-	-	1, 5, 6, 7, 13	-	14
Switching Times	Propagation Delay	t ₅₊₄	Pulse In	Pulse Out	-	V _{EE} = -4.0 Vdc	-	(+1.2 V)
			5	4				
Rise Time	t ₅₋₄	↓	↓	↓	1, 6, 7, 8, 13	-	14	
Fall Time	t ₄₋	↓	↓	↓	↓	↓	↓	↓
Propagation Delay	t ₁₊₃₊	1	3	-	5, 6, 7, 8, 13	-	14	
		↓	↓	↓	↓	↓	↓	↓
Rise Time	t ₁₋₃₋	↓	↓	↓	↓	↓	↓	↓
Fall Time	t ₃₋	↓	↓	↓	↓	↓	↓	↓

† V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA). I_L applied to output under test.



APPLICATIONS INFORMATION

The MC1029/MC1229 data distributor is a 2 X 3 array of 2-input OR gates, as shown in the logic diagram. Inputs X and Y may be used as control inputs to transfer the data on inputs A, B, and C, to the outputs on pins 9, 11, and 12, or to the outputs on pins 4, 3, and 2. Also, if it is desired to distribute data to three destinations, inputs X and Y may be used for data and A, B, and C as control inputs. The data distributor utilizes negative logic; i.e., the positive OR function becomes the negative AND. Data is transferred for a low level on the control inputs.

The data distributor is an example of the manner in which part of a logic system may be partitioned to reduce wiring and package count. Figure 1 illustrates the logic required for the transfer of data from "A" register to "B" register gating or to "C" register gating. Six stages per register are shown in the figure but arrays of any desired length may be built. The typical propagation delay of the data distributor in a system is 5.0 ns, permitting the rapid transfer of data through distribution gating. If data distribution is done on a double-rail basis instead of single-rail as shown, then twice the number of data distributors are required.

FIGURE 1 - REGISTER DATA TRANSFER

