dsPIC30F Family Overview

dsPIC® High-Performance 16-bit Digital Signal Controller

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dsPIC30F

dsPIC® High-Performance 16-bit Digital Signal Controller Family Overview

Operating Range:

- DC – 30 MIPS (30 MIPS @ 4.5-5.5V, -40 to 85°C)
- Wide VDD range: 2.5-5.5V
- Ind. (-40 to 85°C) and Ext. (-40 to 125°C)

High-Performance DSC CPU:

- Modified Harvard architecture
- C compiler optimized instruction set
- 16-bit wide data path
- 24-bit wide instructions
- Linear program memory addressing up to 4M instruction words
- Linear data memory addressing up to 64 Kbytes
- 84 base instructions: mostly 1 word/1 cycle
- 16 16-bit General Purpose Registers (GPR)
- 2 40-bit accumulators:
  - With rounding and saturation options
- Flexible and powerful addressing modes:
  - Indirect, Modulo and Bit-Reversed
- Software stack
- 16 x 16 fractional/integer multiply operations
- 32/16 and 16/16 divide operations
- Single cycle multiply-and-accumulate:
  - Accumulator write back for DSP operations
  - Dual data fetch
- 40-stage barrel shifter

Interrupt Controller:

- 5-cycle latency
- Up to 45 interrupt sources, up to 5 external
- 7 programmable priority levels
- 4 processor exceptions

Digital I/O:

- Up to 54 programmable digital I/O pins
- Wake-up/Interrupt-on-change on up to 24 pins
- 25 mA sink and source on all I/O pins

On-Chip Flash, Data EEPROM and SRAM:

- Flash program memory: up to 144 Kbytes:
  - 10,000 erase/write cycles, min. (-40 to 85°C)
  - 100,000 erase/write cycles, typical
- Data EEPROM: up to 4 Kbytes:
  - 100,000 erase/write cycles, min. (-40 to 85°C)
  - 1M erase/write cycles, typical
  - Data EEPROM retention > 20 years
- Data SRAM: up to 8 Kbytes

System Management:

- Flexible clock options:
  - External, crystal, resonator, internal RC
  - Fully integrated PLL (4X, 8X, 16X)
  - Extremely low jitter PLL
- Programmable Power-up Timer
- Oscillator start-up timer/stabilizer
- Watchdog Timer with its own RC oscillator
- Fail-Safe Clock Monitor
- Reset by multiple sources

Power Management:

- Switch between clock sources in real time
- Programmable low-voltage detect
- Programmable Brown-out Reset
- Idle and Sleep modes with fast wake-up

Timers/Capture/Compare/PWM:

- Timer/counters: up to 5 16-bit timers:
  - Can pair up to make 32-bit timers
  - 1 timer can run as real-time clock with external 32 KHz oscillator
  - Programmable prescaler
- Input capture: up to 8 channels:
  - Capture on up, down or both edges
  - 16-bit Capture input functions
  - 4-deep FIFO on each capture
- Output compare: up to 8 channels:
  - Single or dual 16-bit Compare mode
  - 16-bit glitchless PWM mode

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Communication Modules:

- 3-wire SPI™: up to 2 modules:
  - Framing supports I/O interface to simple codecs
  - Supports 8-bit and 16-bit data
  - Supports all serial clock formats and sampling modes
- I^2C™ full multi-master Slave mode support:
  - 7-bit and 10-bit addressing
  - Bus collision detection and arbitration
- UART: up to 2 modules:
  - Interrupt-on-address bit detect
  - Wake-up on Start bit from Sleep mode
  - 4-character TX and RX FIFO buffers
- Data Conversion Interface (DCI) module
  - Codec interface
  - Supports I^2S and AC'97 protocols
  - Up to 16-bit data words, up to 16 words per frame
  - 4-word deep TX and RX buffers
- CAN 2.0B active: up to 2 modules:
  - 3 transmit and 2 receive buffers
  - 6 receive filters and 2 masks
  - Loopback, Listen Only and Listen All Messages modes for diagnostics and bus monitoring
  - Wake-up on CAN message

Motor Control Peripherals:

- Motor Control PWM: up to 8 channels:
  - 4 duty cycle generators
  - Independent or Complementary mode
  - Programmable dead time and output polarity
  - Edge or center aligned
  - Manual output override control
  - Up to 2 Fault inputs
  - Trigger for A/D conversions
  - PWM Frequency for 16-bit resolution (@ 30 MIPS) = 915 Hz for Edge-Aligned mode, 457.5 Hz for Center-Aligned mode
  - PWM Frequency for 11-bit resolution (@ 30 MIPS) = 29.3 KHz for Edge-Aligned mode, 14.65 KHz for Center-Aligned mode
- Quadrature Encoder Interface module:
  - Phase A, Phase B and index pulse input
  - 16-bit up/down position counter
  - Count direction status
  - Position Measurement (x2 and x4) mode
  - Programmable digital noise filters on inputs
  - Alternate 16-bit Timer/Counter mode
  - Interrupt on position counter rollover/ underflow

Analog-to-Digital Converters:

- 10-bit 1 Msps A/D Converter module:
  - 2 or 4 simultaneous samples
  - Up to 16 input channels with auto scanning
  - 16 deep result buffer
  - Conversion start can be manual or synchronized with 1 of 4 trigger sources
  - Conversion possible in Sleep mode
  - ±1 LSB max. integral non-linearity
  - ±1 LSB max. differential non-linearity
- 12-bit 200 ksps A/D Converter module:
  - Up to 16 input channels with auto scanning
  - 16 deep result buffer
  - Conversion start can be manual or synchronized with 1 of 3 trigger sources
  - Conversion possible in Sleep mode
  - ±1 LSB max. integral non-linearity
  - ±1 LSB max. differential non-linearity

CMOS Flash Technology:

- Low-power, high-speed Flash technology
- Fully static design
- Wide operating voltage range (2.5V to 5.5V)
- Industrial and extended temperature ranges
- Low-power consumption

Packaging:

- 80-pin TQFP (12x12x1 mm, 14x14x1 mm)
- 64-pin TQFP (10x10x1 mm, 14x14x1 mm)
- 40-pin DIP, 44-pin TQFP
- 28-pin DIP (300 mil), 28-pin SOIC
- 28-pin QFN
- 18-pin DIP (300 mil), 18-pin SOIC

Note: See Table 1-1, Table 1-2 and Table 1-3 for exact peripheral features per device.

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1.0 dsPIC30F PRODUCT FAMILIES

1.1 General Purpose Family

The dsPIC30F General Purpose Family (Table 1-1) is ideal for a wide variety of 16-bit MCU embedded applications. The variants with codec interfaces are well suited for audio applications.

TABLE 1-1: dsPIC30F GENERAL PURPOSE FAMILY VARIANTS

Device	Pins	Program Memory		SRAM Bytes	EEPROM Bytes	Timer 16-bit	Input Capture	Output Compare Std. PWM	Codec Interface	A/D 12-bit 200 ksps	UART	SPI™	I²C™	CAN	I/O Pins (Max.)(1)	Packages (2)
		Bytes	Instructions													
dsPIC30F3014	40/44	24K	8K	2048	1024	3	2	2	—	13 ch	2	1	1	—	30	PG, PT
dsPIC30F4013	40/44	48K	16K	2048	1024	5	4	4	AC'97, I2S	13 ch	2	1	1	1	30	PG, PT
dsPIC30F5011	64	66K	22K	4096	1024	5	8	8	AC'97, I2S	16 ch	2	2	1	2	52	PT
dsPIC30F6011(3) dsPIC30F6011A	64	132K	44K	6144	2048	5	8	8	—	16 ch	2	2	1	2	52	PF, PT
dsPIC30F6012(3) dsPIC30F6012A	64	144K	48K	8192	4096	5	8	8	AC'97, I2S	16 ch	2	2	1	2	52	PF, PT
dsPIC30F5013	80	66K	22K	4096	1024	5	8	8	AC'97, I2S	16 ch	2	2	1	2	68	PT
dsPIC30F6013(3) dsPIC30F6013A	80	132K	44K	6144	2048	5	8	8	—	16 ch	2	2	1	2	68	PF, PT
dsPIC30F6014(3) dsPIC30F6014A	80	144K	48K	8192	4096	5	8	8	AC'97, I2S	16 ch	2	2	1	2	68	PF, PT

Note 1: Maximum I/O pin count includes pins shared by the peripheral functions.
2: All 28- and 40-pin devices may be offered in ML packages in the future, depending on die size.
3: This device is not recommended for new designs..

1.2 Motor Control and Power Conversion Family

These variants of dsPIC30F controllers (Table 1-2) support a variety of motor control applications such as brushless DC motors, single and 3-phase induction motors, and switched reluctance motors. They are also well suited for Uninterrupted Power Supply (UPS), inverters, switched mode power supplies and power factor correction, and also for controlling the Power Management module in servers, telecommunication equipment and other industrial equipment.

TABLE 1-2: dsPIC30F MOTOR CONTROL AND POWER CONVERSION FAMILY VARIANTS

Device	Pins	Program Memory		SRAM Bytes	EEPROM Bytes	Timer 16-bit	Input Capture	Output Compare/ Std. PWM	Motor Control PWM	A/D 10-bit 1 Msps	Quad Enc.	UART	SPI™	I²C™	CAN	I/O Pins (Max.)(1)	Packages (2)
		Bytes	Instructions														
dsPIC30F2010	28	12K	4K	512	1024	3	4	2	6 ch	6 ch	1	1	1	1	—	20	SOG, PG, ML
dsPIC30F3010	28	24K	8K	1024	1024	5	4	2	6 ch	6 ch	1	1	1	1	—	20	SOG, PG
dsPIC30F4012	28	48K	16K	2048	1024	5	4	2	6 ch	6 ch	1	1	1	1	1	20	SOG, PG
dsPIC30F3011	40/44	24K	8K	1024	1024	5	4	4	6 ch	9 ch	1	2	1	1	—	30	PG, PT
dsPIC30F4011	40/44	48K	16K	2048	1024	5	4	4	6 ch	9 ch	1	2	1	1	1	30	PG, PT
dsPIC30F5015	64	66K	22K	2048	1024	5	4	4	8 ch	16 ch	1	1	2	1	1	52	PT
dsPIC30F6015	64	144K	48K	8192	4096	5	8	8	8 ch	16 ch	1	2	2	1	2	52	PT
dsPIC30F6010(3) dsPIC30F6010A	80	144K	48K	8192	4096	5	8	8	8 ch	16 ch	1	2	2	1	2	68	PF, PT

Note 1: Maximum I/O pin count includes pins shared by the peripheral functions.
2: All 28- and 40-pin devices may be offered in ML packages in the future, depending on die size.
3: This device is not recommended for new designs.

1.3 Sensor Family

The dsPIC30F Sensor Family products (Table 1-3) have features that support high-performance, low-cost embedded control applications. The 18- and 28-pin packages are designed to fit space-critical applications.

TABLE 1-3: dsPIC30F SENSOR PROCESSOR FAMILY VARIANTS

Device	Pins	Program Memory		SRAM Bytes	EEPROM Bytes	Timer 16-bit	Input Capture	Output Compare Std. PWM	A/D 12-bit 200 Ksps	UART	SPI™	I^2C™	I/O Pins (<Max.)(1)	Packages(2)
		Bytes	Instructions											
dsPIC30F2011	18	12K	4K	1024	0	3	2	2	8 ch	1	1	1	12	SOG, PG
dsPIC30F3012	18	24K	8K	2048	1024	3	2	2	8 ch	1	1	1	12	SOG, PG
dsPIC30F2012	28	12K	4K	1024	0	3	2	2	10 ch	1	1	1	20	SOG, PG
dsPIC30F3013	28	24K	8K	2048	1024	3	2	2	10 ch	2	1	1	20	SOG, PG

Note 1: Maximum I/O pin count includes pins shared by the peripheral functions.

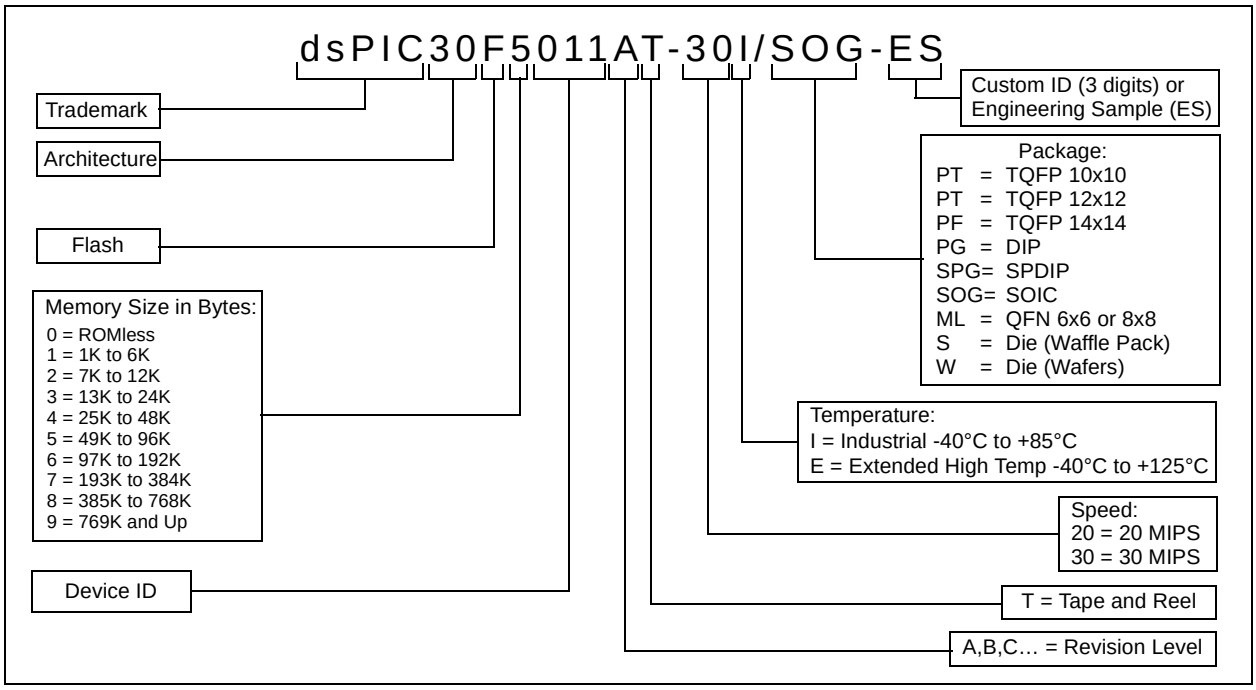
2: All 28- and 40-pin devices may be offered in ML packages in the future, depending on die size.

1.4 Product Identification System

Figure 1-1 illustrates the part number structure.

To order or obtain information (e.g., on pricing or delivery), refer to the factory or a listed sales office (sales offices and locations are listed in the back of this document).

FIGURE 1-1: PART NUMBER STRUCTURE



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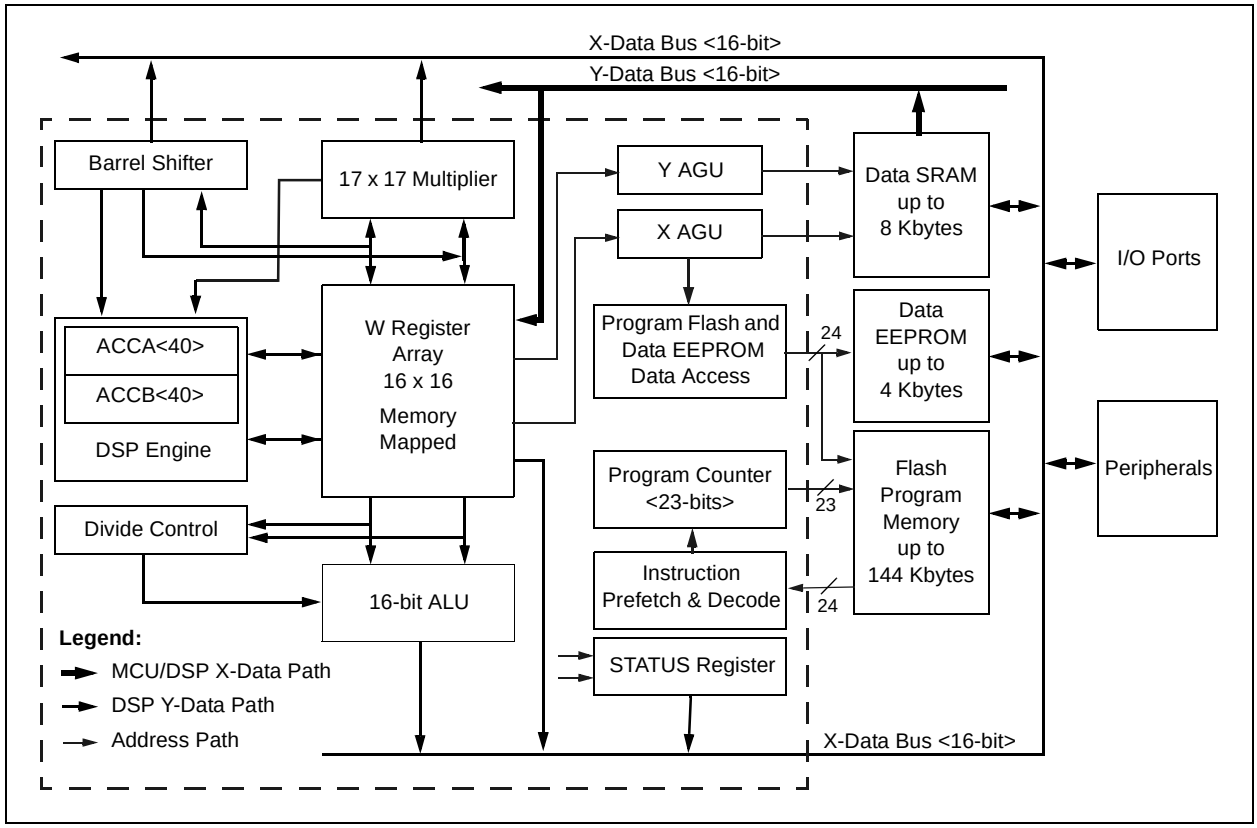
2.0 dsPIC30F DEVICE FAMILY OVERVIEW

The dsPIC30F device family employs a powerful 16-bit architecture that seamlessly integrates the control features of a microprocessor (MCU) with the computational capabilities of a digital signal processor (DSP). The resulting functionality is ideal for applications that rely on high-speed, repetitive computations as well as control.

The DSP engine, dual 40-bit accumulators, hardware support for division operations, barrel shifter, 17 x 17 multiplier, a large array of 16-bit working registers and a wide variety of data addressing modes, together provide the dsPIC30F CPU with extensive mathematical processing capability. Flexible and deterministic interrupt handling, coupled with a powerful array of peripherals, renders the dsPIC30F devices suitable for control applications. Reliable, field programmable Flash program memory and data EEPROM ensure scalability of applications that use dsPIC30F devices.

Figure 2-1 shows a sample device block diagram typical of the dsPIC30F product family.

FIGURE 2-1: dsPIC30F FAMILY BLOCK DIAGRAM

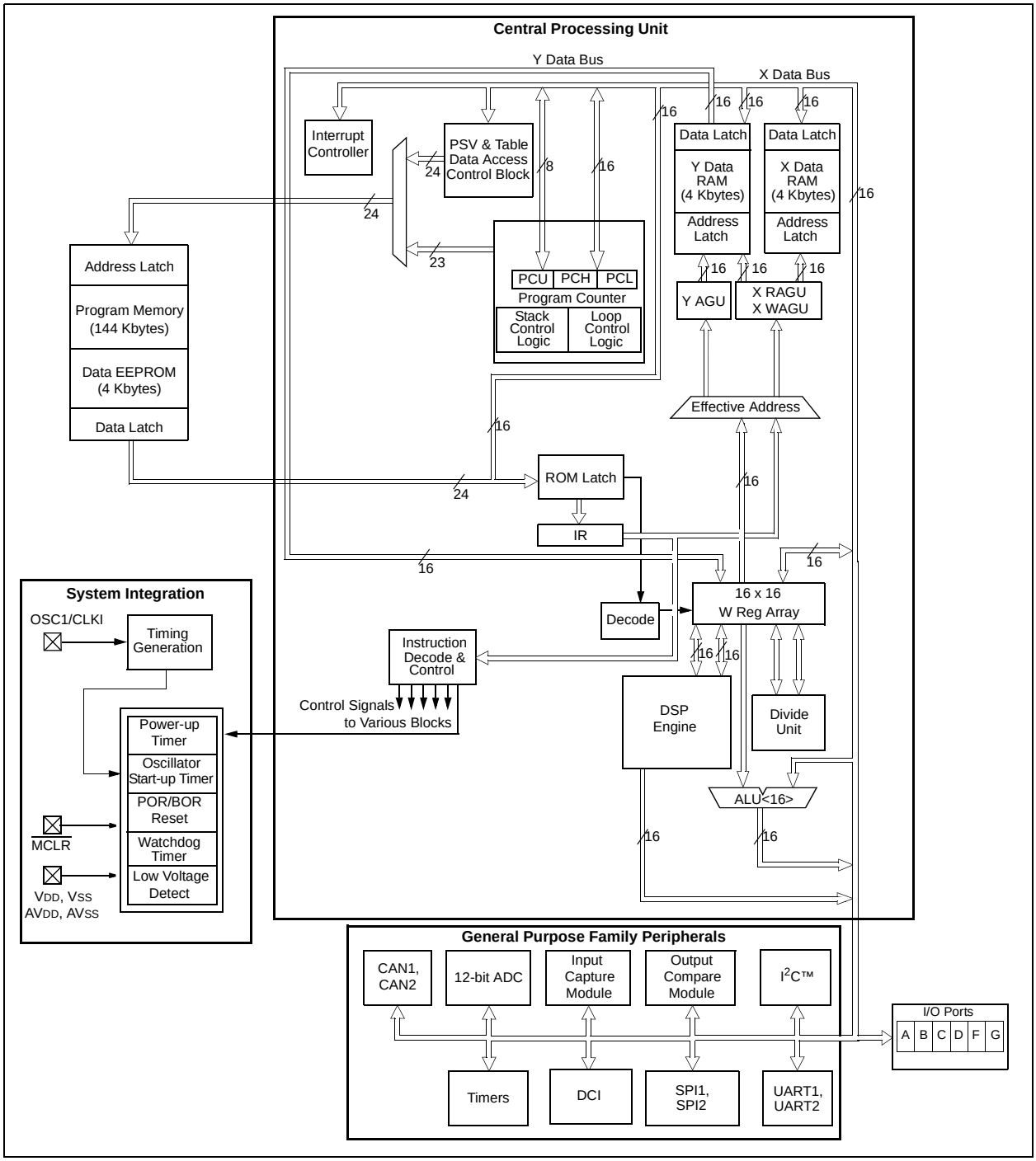


3.0 DEVICE OVERVIEW FOR GENERAL PURPOSE AND SENSOR FAMILIES

Figure 3-1 shows a sample device block diagram typical of the dsPIC30F General Purpose Product Family. Pin functionality and pinouts for this family are shown in Appendix A.

Note:	The device depicted in Figure 3-1 is representative of this family. Other devices of the same family may vary in terms of number of pins and multiplexing of pin functions. Typically, smaller devices in the family contain a subset of the peripherals present in the device(s) shown here.

FIGURE 3-1: dsPIC30F5013/6013A/6014A BLOCK DIAGRAM



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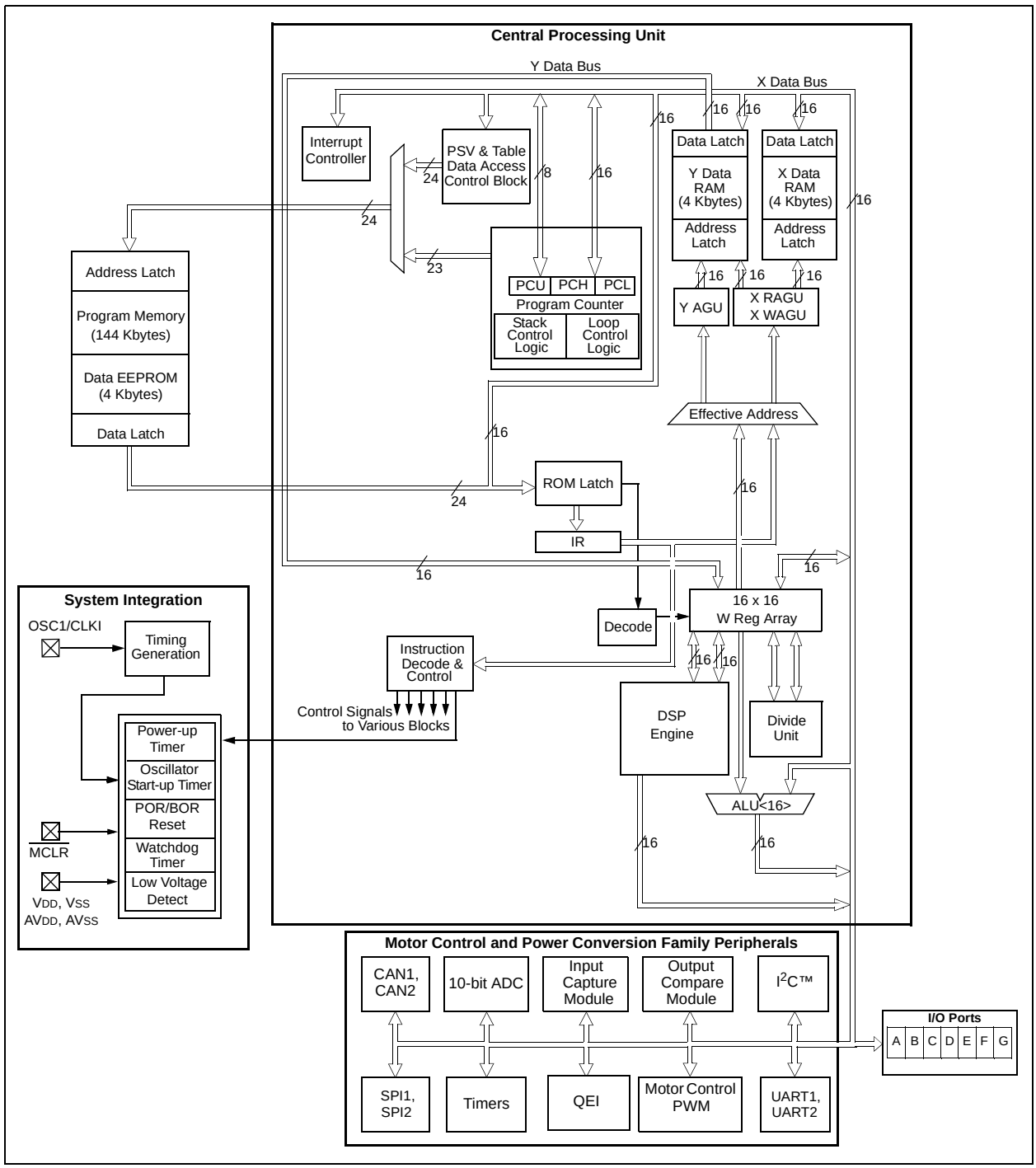
4.0 DEVICE OVERVIEW FOR MOTOR CONTROL AND POWER CONVERSION FAMILY

Figure 4-1 shows a sample device block diagram typical of the dsPIC30F Motor Control Product Family. Pin functionality and pinouts for this family are shown in Appendix B.

Note: The device depicted in Figure 4-1 is representative of this family. Other devices of the same family may vary in terms of number of pins and multiplexing of pin functions. Typically, smaller devices in the family contain a subset of the peripherals present in the device(s) shown here.

FIGURE 4-1: dsPIC30F6010A BLOCK DIAGRAM



5.0 CPU ARCHITECTURE

5.1 Overview

The dsPIC30F CPU module has a 16-bit (data) modified Harvard architecture with an enhanced instruction set, including significant support for DSP. The CPU has a 24-bit instruction word, with a variable length opcode field. The Program Counter (PC) is 23 bits wide and addresses up to 4M x 24 bits of user program memory space. The actual amount of program memory implemented, as illustrated in Figure 5-1, varies from one device to another. A single-cycle instruction pre-fetch mechanism is used to help maintain throughput and provides predictable execution. All instructions execute in a single cycle, with the exception of instructions that change the program flow, the double-word move (`MOV.D`) instruction and the table instructions. Overhead free program loop constructs are supported using the `DO` and `REPEAT` instructions, both of which are interruptible at any point.

The dsPIC30F devices have sixteen 16-bit working registers in the programmer's model. Each of the working registers can serve as a data, address or address offset register. The 16th working register (W15) operates as a software Stack Pointer for interrupts and calls.

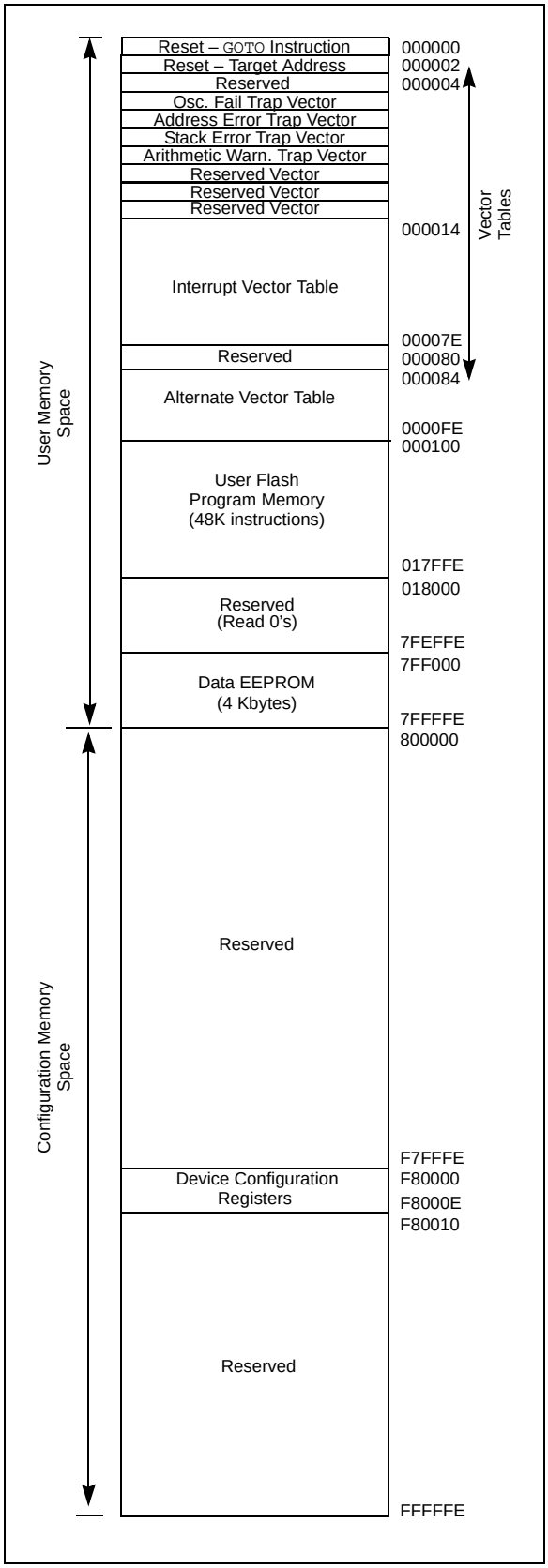
The dsPIC30F instruction set has two classes of instructions: the MCU class of instructions and the DSP class of instructions. These two instruction classes are seamlessly integrated into the architecture and execute from a single execution unit. The instruction set includes many addressing modes and is designed for optimum C compiler efficiency.

5.1.1 DATA MEMORY OVERVIEW

The data space can be addressed as 32 Kwords or 64 Kbytes and is split into two blocks, referred to as X and Y data memory. Each memory block has its own independent Address Generation Unit (AGU). The MCU class of instructions operate solely through the X memory AGU, which accesses the entire memory map as one linear data space. Certain DSP instructions operate through the X and Y AGUs to support dual operand reads, which splits the data address space into two parts. The X and Y data space boundary is device specific.

The upper 32 Kbytes of the data space memory map can optionally be mapped into program space at any 16K program word boundary defined by the 8-bit Program Space Visibility Page (PSVPAG) register. The program-to-data-space mapping feature lets any instruction access program space as if it were data space.

FIGURE 5-1: PROGRAM SPACE MEMORY MAP



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5.1.2 ADDRESSING MODES OVERVIEW

Overhead free circular buffers (modulo addressing) are supported in both X and Y address spaces. The modulo addressing removes the software boundary checking overhead for DSP algorithms. Furthermore, the X AGU circular addressing can be used with any of the MCU class of instructions. The X AGU also supports bit-reversed addressing to greatly simplify input or output data reordering for radix-2 FFT algorithms.

The CPU supports Inherent (no operand), Relative, Literal, Memory Direct, Register Direct and Register Indirect Addressing modes. Each instruction is associated with a predefined addressing mode group depending upon its functional requirements. As many as 6 addressing modes are supported for each instruction.

For most instructions, the dsPIC30F is capable of executing a data (or program data) memory read, a working register (data) read, a data memory write and a program (instruction) memory read per instruction cycle. As a result, three parameter instructions can be supported, allowing A + B = C operations to be executed in a single cycle.

5.1.3 DSP ENGINE OVERVIEW

The DSP engine features a high speed, 17-bit by 17-bit multiplier, a 40-bit ALU, two 40-bit saturating accumulators and a 40-bit bidirectional barrel shifter. The barrel shifter is capable of shifting a 40-bit value up to 16 bits right or left, in a single cycle. The DSP instructions operate seamlessly with all other instructions and have been designed for optimal real-time performance. The MAC instruction and other associated instructions can concurrently fetch two data operands from memory while multiplying two W registers and accumulating and optionally saturating the result in the same cycle. This instruction functionality requires that the RAM memory data space be split for these instructions and linear for all others. Data space partitioning is achieved in a transparent and flexible manner through dedicating certain working registers to each address space.

5.1.4 SPECIAL MCU FEATURES

The dsPIC30F features a 17-bit by 17-bit single-cycle multiplier that is shared by both the MCU ALU and DSP engine. The multiplier can perform signed, unsigned and mixed-sign multiplication. Using a 17-bit by 17-bit multiplier for 16-bit by 16-bit multiplication not only allows you to perform mixed-sign multiplication, it also achieves accurate results for special operations such as (-1.0) x (-1.0).

The dsPIC30F supports 16/16 and 32/16 divide operations, both fractional and integer. All divide instructions are iterative operations. They must be executed within a REPEAT loop, resulting in a total execution time of 19 instruction cycles. The divide operation can be interrupted during any of those 19 cycles without loss of data.

A 40-bit barrel shifter is used to perform up to a 16-bit left or right shift, in a single cycle. The barrel shifter can be used by both MCU and DSP instructions.

5.1.5 INTERRUPT OVERVIEW

The dsPIC30F has a vectored exception scheme with up to 8 sources of non-maskable traps and 54 interrupt sources. Each interrupt source can be assigned to one of seven priority levels.

5.1.6 FEATURES TO ENHANCE COMPILER EFFICIENCY

In addition to extensive DSP capability, the CPU architecture possesses several features that lead to a more efficient (code size and speed) C compiler.

1. For most instructions, three-parameter instructions can be supported, allowing A + B = C operations to be executed in a single cycle.
2. Instruction addressing modes are extremely flexible to meet compiler needs.
3. The working register array consists of 16 x 16-bit registers, each of which can act as data, address or offset registers. One working register (W15) operates as the software Stack Pointer for interrupts and calls.
4. Linear indirect access of all data space is possible, plus the memory direct address range is up to 8 Kbytes. This capability, together with the addition of 16-bit direct address `MOV` based instructions, has provided a contiguous linear addressing space.
5. Linear indirect access of 32 Kword (64 Kbyte) pages within program space is possible, using any working register via new table read and write instructions.
6. Part of data space can be mapped into program space, allowing constant data to be accessed as if it were in data space.

5.2 Programmer's Model

The programmer's model, shown in Figure 5-2, consists of 16 x 16-bit working registers (W0 through W15), 2 x 40-bit accumulators (ACCA and ACCB), STATUS Register (SR), Data Table Page register (TBLPAG), Program Space Visibility Page register (PSVPAG), DO and REPEAT registers (DOSTART, DOEND, DCOUNT and RCOUNT) and Program Counter (PC). The working registers can act as data, address or offset registers. All registers are memory mapped. W0 is the W register for all instructions that perform file register addressing.

Some of these registers have a shadow register associated with them (see the legend in Figure 5-2). The shadow register is used as a temporary holding register and can transfer its contents to or from its host register upon some event occurring in a single cycle. None of the shadow registers are accessible directly.

When a byte operation is performed on a working register, only the Least Significant Byte of the target register is affected. However, a benefit of memory mapped working registers is that both the Least and Most Significant Bytes can be manipulated through byte wide data memory space accesses.

W15 is the dedicated software Stack Pointer (SP). It is automatically modified by exception processing and subroutine calls and returns. However, W15 can be referenced by any instruction in the same manner as all other W registers. This simplifies the reading, writing and manipulation of the Stack Pointer (e.g., creating stack frames).

W14 has been dedicated as a Stack Frame Pointer, as defined by the `LNK` and `ULNK` instructions. However, W14 can be referenced by any instruction in the same manner as all other W registers.

The Stack Pointer always points to the first available free word and grows from lower addresses towards higher addresses. It pre-decrements for stack pops (reads) and post-increments for stack pushes (writes).

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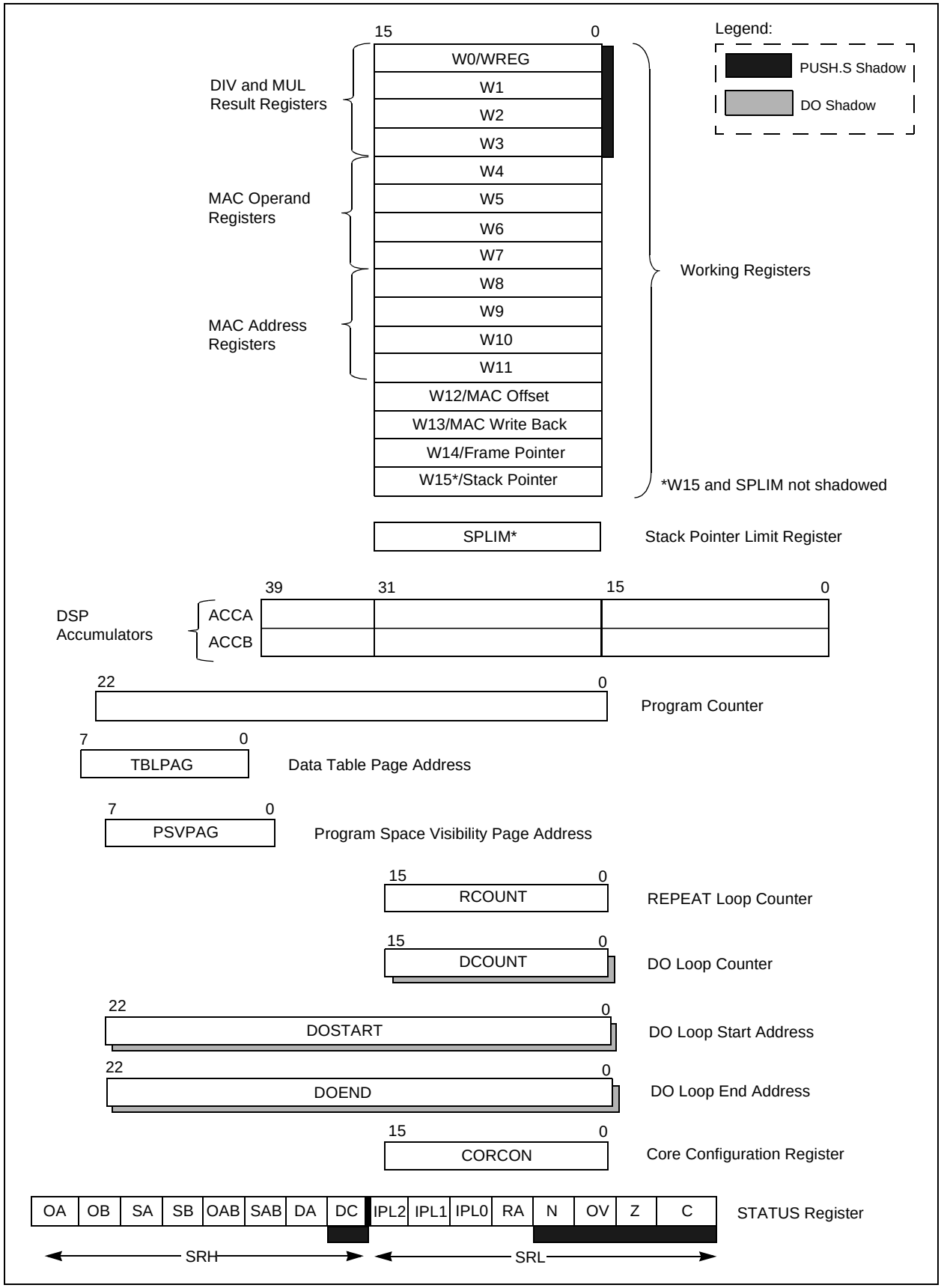
FIGURE 5-2: PROGRAMMER'S MODEL



5.3 Data Address Space

The core has two data spaces, X and Y. These data spaces can be considered either separate (for some DSP instructions), or as one unified linear address range (for MCU instructions). The data spaces are accessed using two Address Generation Units (AGUs) and separate data paths. This feature allows certain instructions to concurrently fetch two words from RAM, thereby enabling efficient execution of DSP algorithms such as Finite Impulse Response (FIR) filtering and Fast Fourier Transform (FFT).

5.3.1 X AND Y DATA SPACES

The X data space is used by all instructions and supports all addressing modes. There are separate read and write data buses for X data space. The X read data bus is the read data path for all instructions that view data space as combined X and Y address space. It is also the X data prefetch path for the dual operand DSP instructions (`MAC` class).

The Y data space is used in concert with the X data space by the `MAC` class of instructions (`CLR`, `ED`, `EDAC`, `MAC`, `MOVSAC`, `MPY`, `MPY.N` and `MSC`) to provide two concurrent data read paths.

Both the X and Y data spaces support modulo addressing for all instructions, subject to addressing mode restrictions. Bit-reversed addressing is only supported for writes to X data space.

All data memory writes, including in DSP instructions, view data space as combined X and Y address space. The boundary between the X and Y data spaces is device-dependent (an example is shown in Figure 5-3) and is not user programmable.

All effective addresses are 16 bits wide and point to bytes within the data space. Therefore, the data space address range is 64 Kbytes or 32 Kwords, though the implemented memory locations vary from one device to another.

5.3.2 DATA SPACE WIDTH

The core data width is 16-bits. All internal registers are organized as 16-bit wide words. Data space memory is organized in byte addressable, 16-bit wide blocks. Figure 5-3 depicts a sample data space memory map for the dsPIC30F.

5.3.3 DATA ALIGNMENT

To help maintain backward compatibility with PICmicro® devices and improve data space memory usage efficiency, the dsPIC30F instruction set supports both word and byte operations. Data is aligned in data memory and registers as words, but all data space EAs resolve to bytes. Data byte reads will read the complete word which contains the byte, using the Least Significant bit (LSb) of any EA to determine which byte to select.

As a consequence of this byte accessibility, all effective address calculations are internally scaled. For example, the core would recognize that Post-Modified Register Indirect Addressing mode, [Ws++], will result in a value of Ws+1 for byte operations and Ws+2 for word operations.

All word accesses must be aligned to an even address. Misaligned word data fetches are not supported. Should a misaligned read or write be attempted, a trap will then be executed, allowing the system and/or user to examine the machine state prior to execution of the address fault.

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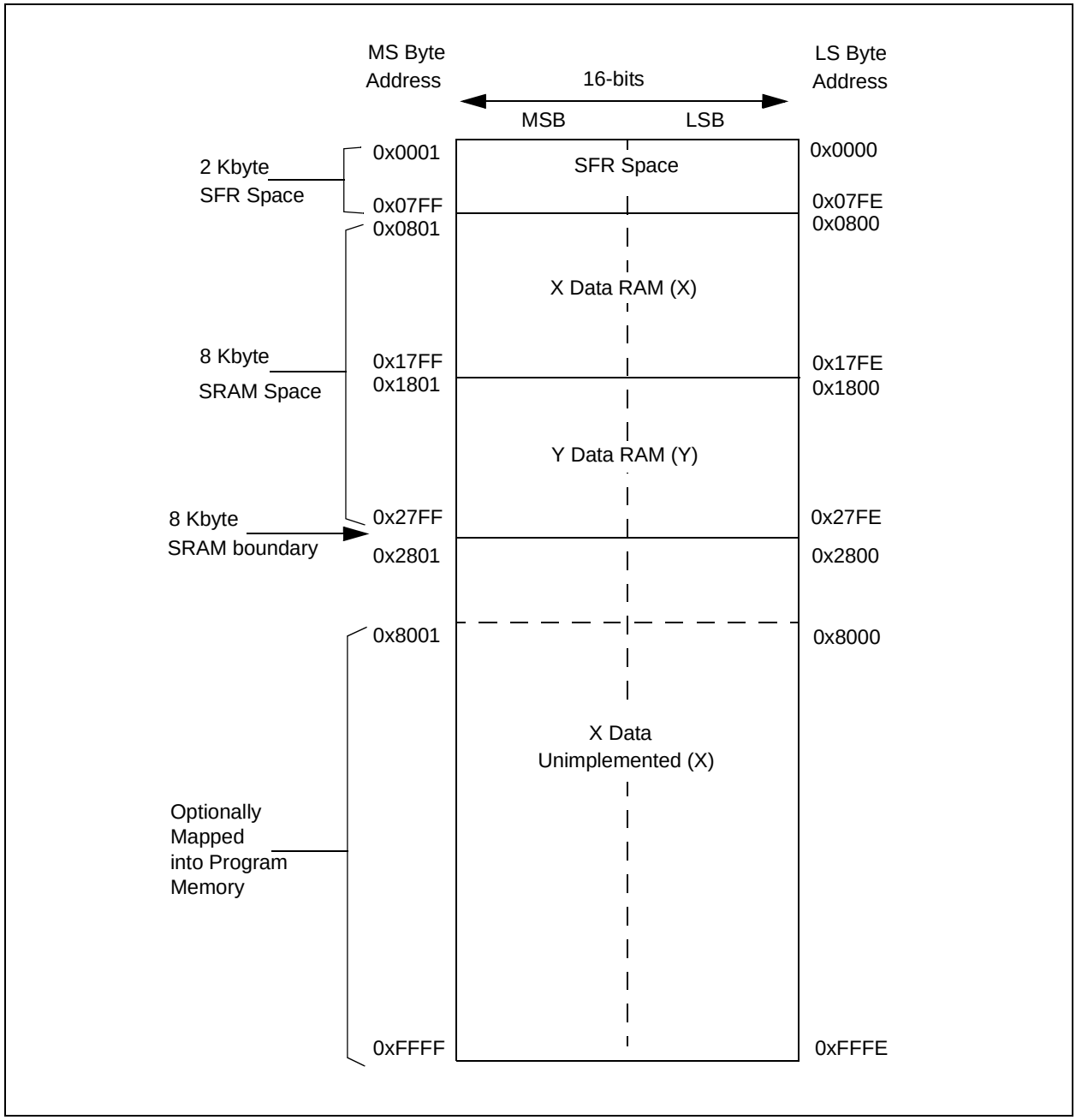
FIGURE 5-3: SAMPLE DATA SPACE MEMORY MAP



5.4 DSP Engine

The DSP engine consists of a high-speed, single-cycle, 17-bit x 17-bit multiplier, a barrel shifter and a 40-bit adder/subtractor with two target accumulators, round and saturation logic, all of which enable efficient execution of computationally intensive DSP algorithms. The 17-bit x 17-bit multiplier is also utilized for MCU-based multiply instructions.

The DSP engine also has the capability to perform inherent accumulator-to-accumulator operations, which require no additional data. These instructions are ADD, SUB and NEG. This feature greatly simplifies basic arithmetic operations on 32-bit or 40-bit data.

A block diagram of the DSP engine is shown in Figure 5-4.

5.4.1 17X17-BIT MULTIPLIER

The 17 x 17-bit multiplier is capable of signed or unsigned operation. It can suitably scale its output to support either 1.31 fractional (Q31) or 32-bit integer results, thereby diminishing the need to manually post-process multiplication results for fractional data.

5.4.2 40-BIT ACCUMULATORS

The data accumulators have a 40-bit adder/subtractor with automatic sign-extension logic. It can select one of two accumulators (A or B) as its pre-accumulation source and post-accumulation destination. For the ADD and LAC instructions, the data to be accumulated or loaded can be optionally scaled via the barrel shifter prior to accumulation.

The adder/subtractor generates overflow Status bits SA/SB and OA/OB, which are latched and reflected in the STATUS Register and can also optionally generate an Arithmetic Error Trap:

- Overflow from bit 39. This is a catastrophic overflow in which the sign of the accumulator is destroyed.
- Overflow into guard bits 32 through 39. This is a recoverable overflow. This bit (OA/OB) is set whenever all the guard bits are not identical to each other.

5.4.3 SATURATION AND OVERFLOW

The adder has an additional saturation block that controls accumulator data saturation, if selected. It uses the result of the adder, the overflow Status bits described above, and the user-configured control bits to determine when to saturate and to what value to saturate (a 40-bit or a 32-bit value).

In addition to adder/subtractor saturation, writes to data space can also be saturated, but without affecting the contents of the source accumulator.

The rounding logic performs a conventional (biased) or convergent (unbiased) data rounding function during an accumulator write (store). The Round mode is user-selectable. Rounding generates a 16-bit, 1.15 data value, which is passed to the data space write saturation logic. Data space write saturation ensures that the data in the accumulator is written back accurately even when rounding is performed. If rounding is not indicated by the instruction, a truncated 1.15 data value is stored and the least significant word (lsb) is simply discarded.

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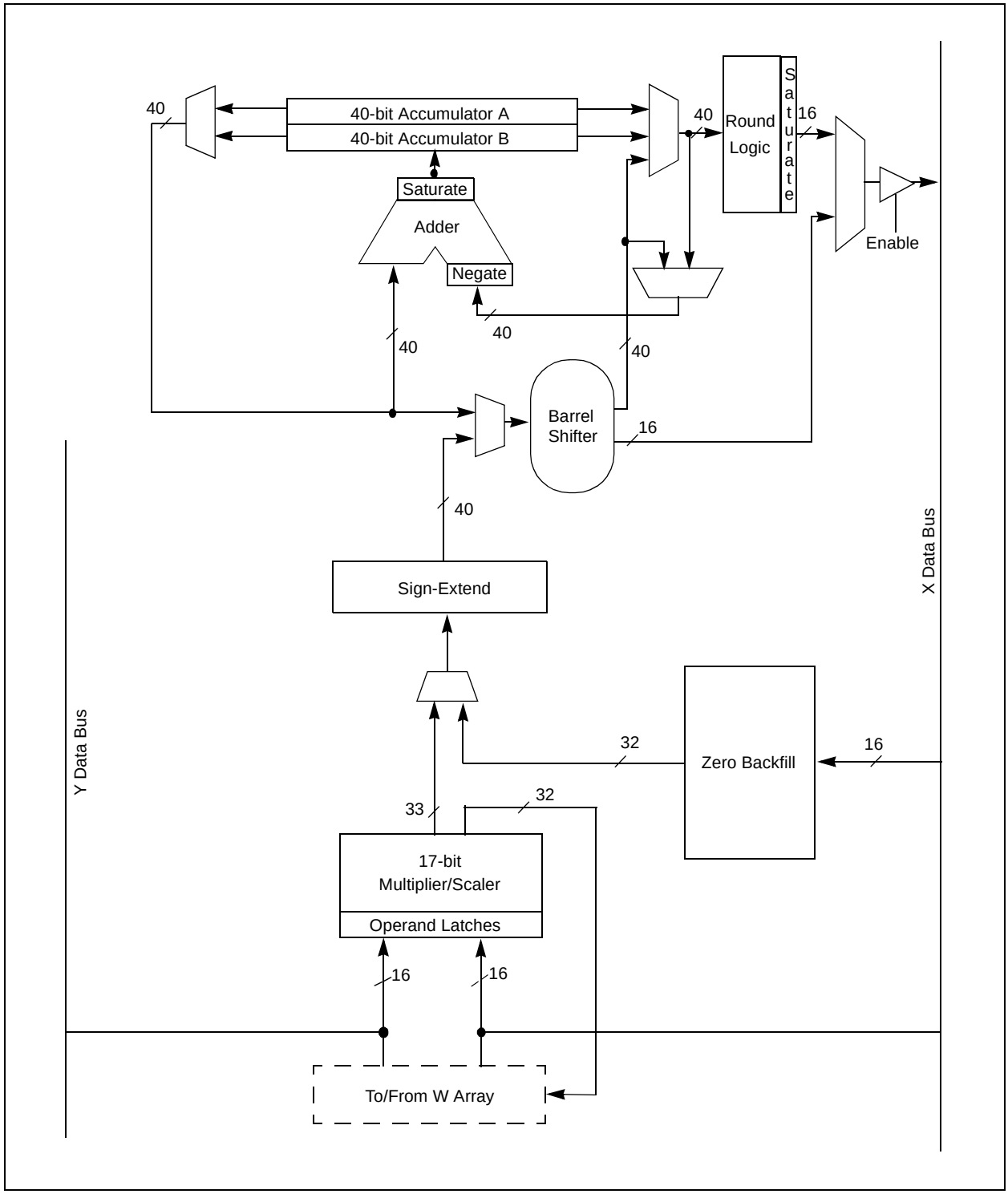
FIGURE 5-4: DSP ENGINE BLOCK DIAGRAM



6.0 EXCEPTION PROCESSING

The dsPIC30F has four processor exceptions (traps) and up to 45 sources of interrupts, which must be arbitrated based on a priority scheme.

The processor core is responsible for reading the Interrupt Vector Table (IVT) and transferring the address contained in the interrupt vector to the program counter.

The Interrupt Vector Table (IVT) and Alternate Interrupt Vector Table (AIVT) are placed near the beginning of program memory (0x000004) for ease of debugging.

The interrupt controller hardware pre-processes the interrupts before they are presented to the CPU. The interrupts and traps are enabled, prioritized and controlled using centralized Special Function Registers.

Each individual interrupt source has its own vector address and can be individually enabled and prioritized in user software. Each interrupt source also has its own status flag. This independent control and monitoring of the interrupt eliminates the need to poll various status flags to determine the interrupt source

Table 6-1 contains information about the interrupt vector.

Certain interrupts have specialized control bits for features like edge or level triggered interrupts, interrupt-on-change, etc. Control of these features remains within the Peripheral module, which generates the interrupt.

The special `DISI` instruction can be used to disable the processing of interrupts of priorities 6 and lower for a certain number of instruction cycles, during which the DISI bit remains set.

TABLE 6-1: INTERRUPT VECTORS

Vector Number	IVT Address	AIVT Address	Interrupt Source
8	0x000014	0x000094	INT0 – External Interrupt 0
9	0x000016	0x000096	IC1 – Input Compare 1
10	0x000018	0x000098	OC1 – Output Compare 1
11	0x00001A	0x00009A	T1 – Timer1
12	0x00001C	0x00009C	IC2 – Input Capture 2
13	0x00001E	0x00009E	OC2 – Output Compare 2
14	0x000020	0x0000A0	T2 – Timer2
15	0x000022	0x0000A2	T3 – Timer3
16	0x000024	0x0000A4	SPI1
17	0x000026	0x0000A6	U1RX – UART1 Receiver
18	0x000028	0x0000A8	U1TX – UART1 Transmitter
19	0x00002A	0x0000AA	ADC – ADC Convert Done
20	0x00002C	0x0000AC	NVM – NVM Write Complete
21	0x00002E	0x0000AE	I2C Slave Operation – Message Detect
22	0x000030	0x0000B0	I2C Master Operation – Message Event Complete
23	0x000032	0x0000B2	Change Notice Interrupt
24	0x000034	0x0000B4	INT1 – External Interrupt 1
25	0x000036	0x0000B6	IC7 – Input Capture 7
26	0x000038	0x0000B8	IC8 – Input Capture 8
27	0x00003A	0x0000BA	OC3 – Output Compare 3
28	0x00003C	0x0000BC	OC4 – Output Compare 4
29	0x00003E	0x0000BE	T4 – Timer4
30	0x000040	0x0000C0	T5 – Timer5
31	0x000042	0x0000C2	INT2 – External Interrupt 2
32	0x000044	0x0000C4	U2RX – UART2 Receiver
33	0x000046	0x0000C6	U2TX – UART2 Transmitter
34	0x000048	0x0000C8	SPI2
35	0x00004A	0x0000CA	CAN1

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TABLE 6-1: INTERRUPT VECTORS (CONTINUED)

Vector Number	IVT Address	AIVT Address	Interrupt Source
36	0x00004C	0x0000CC	IC3 – Input Capture 3
37	0x00004E	0x0000CE	IC4 – Input Capture 4
38	0x000050	0x0000D0	IC5 – Input Capture 5
39	0x000052	0x0000D2	IC6 – Input Capture 6
40	0x000054	0x0000D4	OC5 – Output Compare 5
41	0x000056	0x0000D6	OC6 – Output Compare 6
42	0x000058	0x0000D8	OC7 – Output Compare 7
43	0x00005A	0x0000DA	OC8 – Output Compare 8
44	0x00005C	0x0000DC	INT3 – External Interrupt 3
45	0x00005E	0x0000DE	INT4 – External Interrupt 4
46	0x000060	0x0000E0	CAN2
47	0x000062	0x0000E2	PWM – PWM Period Match
48	0x000064	0x0000E4	QEI – Position Counter Compare
49	0x000066	0x0000E6	DCI – Codec Transfer Done
50	0x000068	0x0000E8	LVD – Low Voltage Detect
51	0x00006A	0x0000EA	FLTA – MCPWM FAULT A
52	0x00006C	0x0000EC	FLTB – MCPWM FAULT B
53-61	0x00006E-0x00007E	0x00006E-0x00007E	Reserved

6.1 Interrupt Priority

Each interrupt source can be user assigned to one of 8 priority levels, 1 through 7. Levels 7 and 1 represent the highest and lowest maskable priorities, respectively. A priority level of 0 disables the interrupt.

Since more than one interrupt request source may be assigned to a user specified priority level, a means is provided to assign priority within a given level. This method is called “Natural Order Priority.”

The Natural Order Priority of an interrupt is numerically identical to its vector number. The natural order priority scheme has 0 as the highest priority and 53 as the lowest priority.

The ability for the user to assign every interrupt to one of eight priority levels implies that the user can assign a very high overall priority level to an interrupt with a low natural order priority, thereby providing much flexibility in designing applications that use a large number of peripherals.

6.2 Interrupt Nesting

Interrupts, by default, are nestable. Any ISR that is in progress may be interrupted by another source of interrupt with a higher user assigned priority level. Interrupt nesting may be optionally disabled by setting the NSTDIS control bit (INTCON1<15>). When the NSTDIS control bit is set, all interrupts in progress will force the CPU priority to level 7 by setting IPL<2:0> = `111`. This action will effectively mask all other sources of interrupt until a `RETFIE` instruction is executed. When interrupt nesting is disabled, the user assigned interrupt priority levels will have no effect, except to resolve conflicts between simultaneous pending interrupts.

The IPL<2:0> bits become read-only when interrupt nesting is disabled. This prevents the user software from setting IPL<2:0> to a lower value, which would effectively re-enable interrupt nesting.

6.3 Traps

Traps can be considered as non-maskable, nestable interrupts that adhere to a fixed priority structure. Traps are intended to provide the user a means to correct erroneous operation during debug and when operating within the application. If the user does not intend to take corrective action in the event of a trap error condition, these vectors must be loaded with the address of a software routine that will reset the device. Otherwise, the trap vector is programmed with the address of a service routine that will correct the trap condition.

The dsPIC30F has four implemented sources of non-maskable traps:

- Oscillator Failure Trap
- Address Error Trap
- Stack Error Trap
- Arithmetic Error Trap

Many of these trap conditions can only be detected when they happen. Consequently, the instruction that caused the trap is allowed to complete before exception processing begins. Therefore, the user may have to correct the action of the instruction that caused the trap.

Each trap source has a fixed priority as defined by its position in the IVT. An oscillator failure trap has the highest priority, while an arithmetic error trap has the lowest priority.

Table 6-2 contains information about the trap vector.

6.4 Generating a Software Interrupt

Any available interrupt can be manually generated by user software (even if the corresponding peripheral is disabled), simply by enabling the interrupt and then setting the interrupt flag bit when required.

TABLE 6-2: TRAP VECTORS

Vector Number	IVT Address	AIVT Address	Trap Source
0	0x000004	0x000084	Reserved
1	0x000006	0x000086	Oscillator Failure
2	0x000008	0x000088	Address Error
3	0x00000A	0x00008A	Stack Error
4	0x00000C	0x00008C	Arithmetic Error
5	0x00000E	0x00008E	Reserved
6	0x000010	0x000090	Reserved
7	0x000012	0x000092	Reserved

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7.0 SYSTEM INTEGRATION

System management services provided by the dsPIC30F device family include:

- Control of clock options and oscillators
- Power-on Reset
- Programmable Brown-out Reset
- Program control of Power-up Timer
- Oscillator start-up timer/stabilizer
- Watchdog Timer with RC oscillator
- Fail-Safe Clock Monitor
- Reset by multiple sources

7.1 Clock Options and Oscillators

There are three primary clock oscillators: XTL, XT and HS. The XTL oscillator is designed for crystals or ceramic resonators in the range of 200 kHz to 4 MHz. The XT oscillator is designed for crystals and ceramic resonators in the range of 4 to 10 MHz. The HS (High-Speed) oscillator is for crystals in the 10 to 25 MHz range. These oscillators use the OSC1 and OSC2 pins.

The secondary (LP) oscillator is designed for low power and uses a 32 kHz crystal or ceramic resonator. The LP oscillator uses the SOSC1 and SOSC2 pins.

The FRC (Fast RC) internal oscillator runs at a nominal 7.37 MHz ±2%. The user software can tune the FRC frequency. The LPRC (Low Power RC) internal oscIllator is connected to the Watchdog Timer, and it runs at a nominal 512 kHz. The External RC (ERC) oscillator uses an external resistor and capacitor connected to the OSC1 pin. Frequency of operation is up to 4 MHz.

The OSC1 pin can also be used as an input from an external clock source; this mode is called “EC”.

The dsPIC30F oscillator system provides:

- Various external and internal oscillator options as clock sources
- An on-chip PLL to boost internal operating frequency 4, 8 or 16 times
- In some devices, the FRC oscillator can also be used with the PLL
- Clock switching between various clock sources
- Programmable clock postscaler for system power savings
- A Fail-Safe Clock Monitor (FSCM) that detects clock failure and takes fail-safe measures
- A Clock Control register (OSCCON)
- Nonvolatile Configuration bits for main oscillator selection.

A simplified block diagram of the oscillator system is shown in Figure 7-1.

7.2 Power-On Reset

When a supply voltage is applied to the device, a Power-on Reset is generated. A new Power-on Reset event is generated if the supply voltage falls below the device threshold voltage (V_{POR}). An internal POR pulse is generated when the rising supply voltage crosses the POR circuit threshold voltage.

7.3 Programmable Brown-out Reset

The BOR (Brown-out Reset) module is based on an internal voltage reference circuit. The main purpose of the BOR module is to generate a device Reset when a brown-out condition occurs. Brown-out conditions are generally caused by glitches on the AC mains (i.e., missing portions of the AC cycle waveform due to bad power transmission lines or voltage sags due to excessive current draw when a large inductive load is turned on).

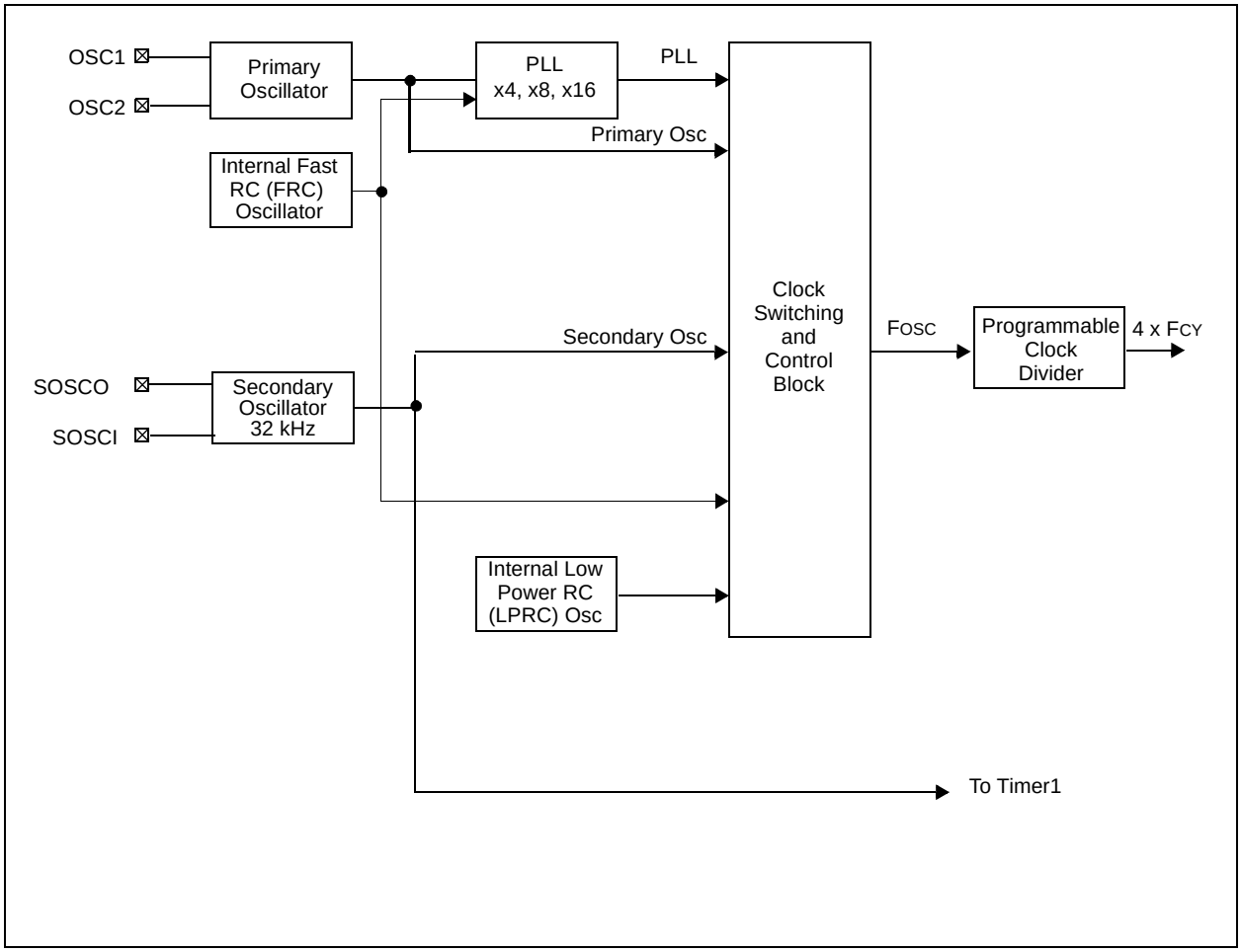
The BOR module allows selection of one of the following voltage trip points:

- 2.0V
- 2.7V
- 4.2V
- 4.5V

Note:	The BOR voltage trip points indicated here are nominal values provided for design guidance only. Refer to the Electrical Specifications in the specific device data sheet for BOR voltage limit specifications.

A BOR generates a Reset pulse, which resets the device.

FIGURE 7-1: OSCILLATOR SYSTEM BLOCK DIAGRAM



7.4 Programmable Power-up Timer (PWRT)

There are two internal timers that offer necessary delays on power-up. One is the Power-up Timer (PWRT), which provides a delay on power-up only. The PWRT keeps the part in Reset while the power supply stabilizes. The other is the Oscillator Start-up Timer (OST), intended to keep the chip in Reset until the crystal oscillator is stable. With these two timers on-chip, most applications need no external Reset circuitry.

7.5 Oscillator Start-up Timer/Stabilizer (OST)

An Oscillator Start-up Timer (OST) is included to ensure that a crystal oscillator (or ceramic resonator) has started and stabilized. The OST is a simple 10-bit counter that counts 1024 TOSC cycles before releasing the oscillator clock to the rest of the system. The time-out period is designated as TOST. The TOST time is involved every time the oscillator has to restart (i.e., on Power-On Reset (POR), Brown-Out Reset (BOR) and wake-up from Sleep). The oscillator start-up timer is applied to the LP oscillator, XT, XTL and HS modes (upon wake-up from Sleep, POR and BOR) for the primary oscillator.

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7.6 Watchdog Timer (WDT)

The primary function of the Watchdog Timer (WDT) is to reset the processor in the event of a software malfunction. The WDT is a free running timer that runs off an on-chip RC oscillator, requiring no external component. The WDT Timer continues to operate even if the main processor clock (e.g., the crystal oscillator) fails.

The Watchdog Timer can be “Enabled” or “Disabled” either through a Configuration bit (FWDTEN) in the Configuration register or through an SFR bit (SWDTEN).

Any device programmer capable of programming dsPIC devices (such as Microchip’s PRO MATE® II programmer) allows programming of this and other Configuration bits to the desired state. If enabled, the WDT increments until it overflows or “times out”. A WDT time-out forces a device Reset (except during Sleep).

7.7 Fail-Safe Clock Monitor (FSCM)

The Fail-Safe Clock Monitor (FSCM) allows the device to continue to operate even in the event of an oscillator failure. The FSCM function is enabled by programming. If the FSCM function is enabled, the LPRC internal oscillator runs at all times (except during Sleep mode) and is not subject to control by the watchdog timer.

In the event of an oscillator failure, the FSCM generates a Clock Failure Trap event and switches the system clock over to the FRC oscillator. The application program then can either attempt to restart the oscillator, or execute a controlled shutdown. The Trap can be treated as a warm Reset by simply loading the Reset address into the oscillator fail trap vector.

7.8 Reset System

The Reset system combines all Reset sources and controls the device Master Reset signal.

Device Reset sources include:

- POR: Power-on Reset
- SWR: `RESET` instruction
- EXTR: $\overline{\text{MCLR}}$ Reset
- WDTR: Watchdog Timer Time-out Reset
- BOR: Brown-out Reset
- TRAPR: Trap Conflict Reset
- IOPUWR: Attempted execution of an Illegal Opcode, or Indirect Addressing using an Uninitialized W Register

8.0 DEVICE POWER MANAGEMENT

Power management services provided by the dsPIC30F device include:

- Real-time Clock Source Switching
- Programmable low-voltage detection
- Idle and Sleep modes with fast wake-up

8.1 Real-Time Clock Source Switching

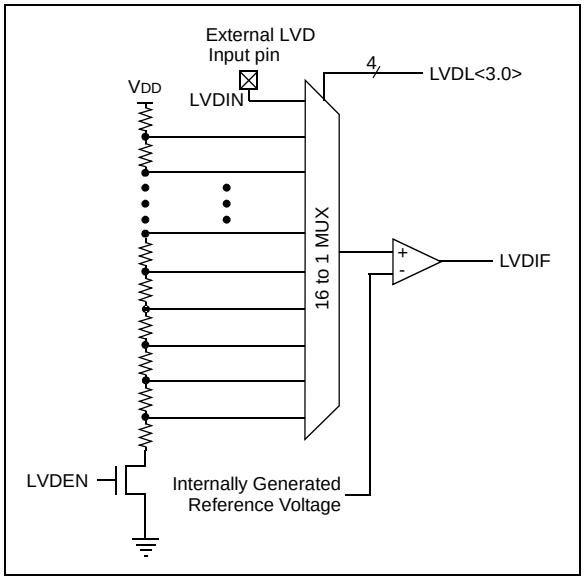
Configuration bits determine the clock source upon Power-on Reset (POR) and Brown-out Reset (BOR). Thereafter, the clock source can be changed between permissible clock sources. The OSCCON register controls the clock switching and reflects system clock related Status bits. To reduce power consumption, the user can switch to a slower clock source.

8.2 Low Voltage Detect (LVD)

The LVD module is used with battery operated applications to detect when the battery voltage (the VDD of the device) drops below a threshold, which is near the end of the battery life for the application. The LVD allows the application to gracefully shut down its operation.

This feature is only available on some devices. Figure 8-1 is a block diagram of the LVD module. A comparator uses an internally generated reference voltage as the set point. When the selected tap output of the device voltage is lower than the reference voltage, the LVD interrupt flag is set. Each node of the resistor divider represents a “trip point” voltage. The voltage is software programmable to any of 16 values, or can be obtained from an external pin (LVDIN).

FIGURE 8-1: LVD MODULE BLOCK DIAGRAM



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8.3 Power-Saving Modes

The dsPIC30F devices have two reduced power modes that can be entered through execution of the PWRSAV instruction.

- Sleep mode: The CPU, system clock source and any peripherals that operate on the system clock source are disabled. This is the lowest power mode of the device.
- Idle mode: The CPU is disabled, but the system clock source continues to operate. Peripherals continue to operate, but can optionally be disabled.

These modes provide an effective way to reduce power consumption during periods when the CPU is not is use.

8.3.1 SLEEP MODE

When the device enters Sleep mode:

- System clock source is shut down. If an on-chip oscillator is used, it is turned off.
- Device current consumption is at minimum, provided that no I/O pin is sourcing current.
- Fail-Safe Clock Monitor (FSCM) does not operate during Sleep mode because the system clock source is disabled.
- LPRC clock continues to run in Sleep mode if the WDT is enabled.
- Low Voltage Detect circuit, if enabled, remains operative during Sleep mode.
- BOR circuit, if enabled, remains operative during Sleep mode.
- WDT, if enabled, is automatically cleared prior to entering Sleep mode.
- Some peripherals may continue to operate in Sleep mode. These peripherals include I/O pins that detect a change in the input signal, or peripherals that use an external clock input. Any peripheral that is operating on the system clock source is disabled in Sleep mode.

The processor exits (wakes up) from Sleep on one of these events:

- Any interrupt source that is individually enabled.
- Any form of device Reset.
- A WDT time-out.

8.3.2 IDLE MODE

When the device enters Idle mode:

- CPU stops executing instructions.
- WDT is automatically cleared.
- System clock source remains active.
- Peripheral modules, by default, continue to operate normally from the system clock source.
- Peripherals, optionally, can be shut down in Idle mode using their ‘stop-in-idle’ control bit.
- If the WDT or FSCM is enabled, the LPRC also remains active.

The processor wakes from Idle mode on these events:

- Any interrupt that is individually enabled.
- Any source of device Reset.
- A WDT Time-out.

Upon wake up from Idle, the clock is re-applied to the CPU and instruction execution begins immediately starting with the instruction following the PWRSAV instruction, or the first instruction in the Interrupt Service Routine (ISR).

9.0 dsPIC30F PERIPHERALS

The Digital Signal Controller (DSC) family of 16-bit MCU devices provides the integrated functionality of many peripherals. Specific peripheral functions include:

- Analog-to-Digital Converters:
  - 10-bit high-speed A/D Converter
  - 12-bit high-resolution A/D Converter
- General Purpose 16-bit timers
- Motor Control PWM module
- Quadrature Encoder module
- Input Capture module
- Output Compare/PWM module
- Data Converter Interface
- Serial Peripheral Interface (SPI™) module
- UART module
- I^2C™ module
- Controller Area Network (CAN) module
- I/O pins

9.1 Analog-to-Digital Converters

The Analog-to-Digital (A/D) Converters provide up to 16 analog inputs with both single-ended and differential inputs. These modules offer on-board sample and hold circuitry.

To minimize control loop errors due to finite update times (conversion plus computations), a high-speed low-latency ADC is required.

In addition, several hardware features have been included in the peripheral interface to improve real-time performance in a typical DSP-based application.

- Result alignment options
- Automated sampling
- Automated channel scanning
- Dual Port data buffer
- External conversion start control

There are two versions of A/D converters available for the dsPIC30F family of devices:

- 10-bit high-speed A/D module
- 12-bit high-resolution A/D module

9.1.1 10-BIT HIGH-SPEED A/D MODULE

- 10-bit resolution
- Unipolar differential sample/hold amplifiers
- Up to 16 input channels
- Selectable reference inputs:
  - External VREF+ and VREF- pins available
- ±1 LSB max. Differential Non-Linearity (DNL) (5V ±10%)
- ±1 LSB max. Integral Non-Linearity (INL) (5V ±10%)
- Four on-chip sample and hold amplifiers:
  - Enables simultaneous sampling of 2 or 4 analog inputs
- Automated channel scanning
- Single supply operation: 2.7-5.5V
- 1 Msps sampling rate at 5V
- Ability to convert during CPU Sleep and Idle modes
- Conversion start can be manual or synchronized with 1 of 4 trigger sources (Automatic, Timer3, External Interrupt, PWM period match)
- 16-word deep memory-mapped result buffer:
  - Lower and upper half of buffer can be filled on alternate conversions

9.1.2 12-BIT HIGH RESOLUTION A/D MODULE

- 12-bit resolution
- Unipolar differential sample/hold amplifiers
- Up to 16 input channels:
  - External VREF+ and VREF- pins available
- Selectable reference inputs
- ±1 LSB max. DNL (5V ±10%)
- ±1 LSB max. INL (5V ±10%)
- One on-chip sample and hold amplifier
- Automated channel scanning
- Single supply operation: 2.7-5.5V
- 200 ksps sampling rate at 5V
- Ability to convert during CPU Sleep and Idle modes
- Conversion start can be manual or synchronized with 1 of 3 trigger sources (Automatic, Timer3, External Interrupt)
- 16-word deep memory-mapped result buffer:
  - Lower and upper half of buffer can be filled on alternate conversions

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9.2 General Purpose Timer Modules

The General Purpose (GP) Timer modules provide the time base elements for Input Capture and Output Compare/PWM. They can be configured for real-time clock operation as well as various timer/counter modes. The timer modes count pulses of the internal time base, whereas counter modes count external pulses that appear on the Timer Clock pin.

The dsPIC30F device supports up to five 16-bit timers (Timer1 through Timer5). Four of the 16-bit timers can be configured as two 32-bit timers (Timer2/3 and 4/5). Each timer has several selectable operating modes.

9.2.1 TIMER1

The Timer1 module (Figure 9-1) is a 16-bit timer that can serve as the time counter for an asynchronous real-time clock, or operate as a free-running interval timer/counter. The 16-bit timer has the following modes:

- 16-bit Timer
- 16-bit Synchronous Counter
- 16-bit Asynchronous Counter

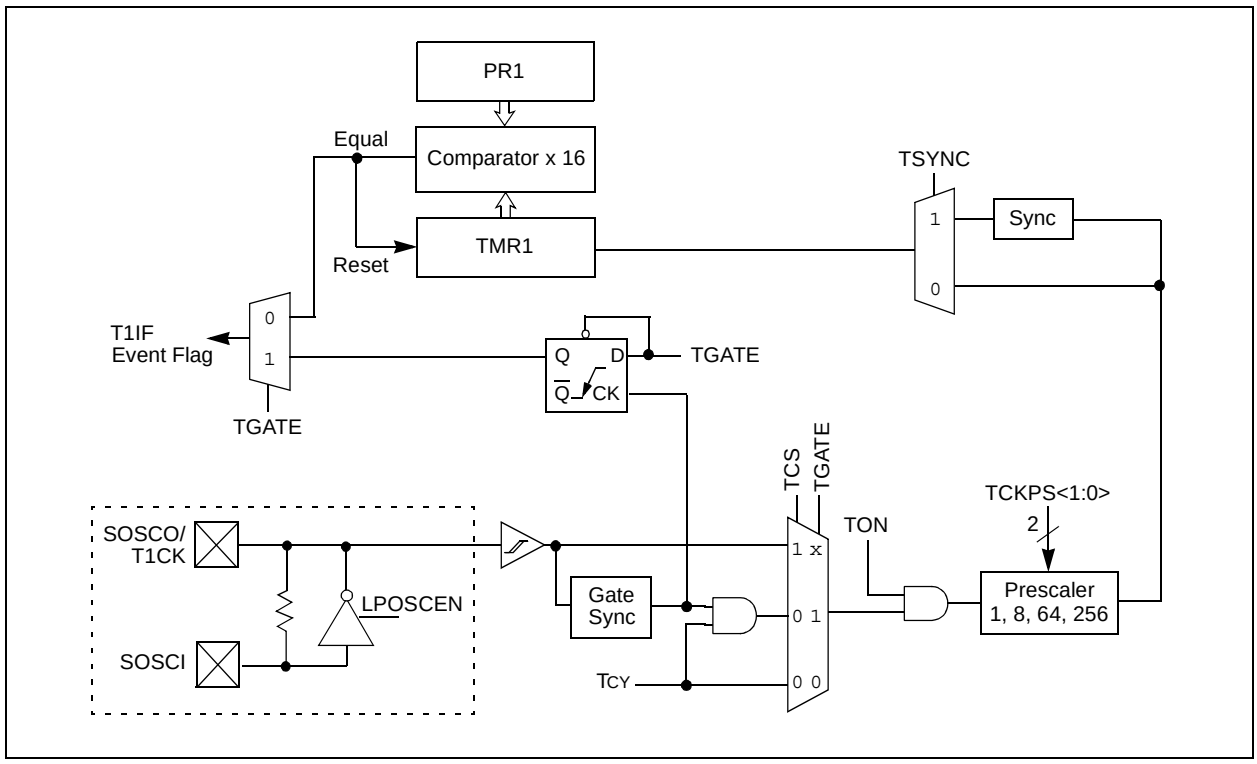
Further, the following operational characteristics are supported:

- Timer gated by external pulse
- Selectable prescaler settings
- Timer operation during CPU Idle and Sleep modes
- Interrupt on 16-bit Period register match or falling edge of external gate signal

Timer1, when operating in Real-Time Clock (RTC) mode, provides time of day and event time-stamping capabilities. Key operational features of the RTC are:

- Operation from 32 kHz LP oscillator
- 8-bit prescaler
- Low power
- Real-Time Clock interrupts

FIGURE 9-1: 16-BIT TIMER1 MODULE BLOCK DIAGRAM



9.2.2 TIMER 2/3

The Timer2/3 module is a 32-bit timer (which can be configured as two 16-bit timers) with selectable operating modes. These timers are used by other peripheral modules, such as:

- Input Capture
- Output Compare/Simple PWM

Timer2/3 has the following modes:

- Two independent 16-bit timers (Timer2 and Timer3) with Timer and Synchronous Counter modes
- Single 32-bit timer operation
- Single 32-bit synchronous counter

Further, the following operational characteristics are supported:

- ADC conversion start trigger
- 32-bit Timer gated by external pulse
- Selectable prescaler settings
- Timer counter operation during Idle and Sleep modes
- Interrupt on a 32-bit period register match

9.2.3 TIMER 4/5

The Timer4/5 module is similar in operation to the Timer2/3 module. Differences include:

- The Timer4/5 module does not support the ADC event trigger feature
- Timer 4/5 can not be used by other peripheral modules, such as Input Capture and Output Compare

9.3 Motor Control PWM Module

The Motor Control PWM (MCPWM) module simplifies the task of generating multiple, synchronized pulse width modulated outputs. In particular, the following power and motion control applications are supported:

- Three-Phase AC Induction Motor
- Switched Reluctance (SR) Motor
- Brushless DC (BLDC) Motor
- Uninterrupted Power Supply (UPS)

The PWM module has the following features:

- Dedicated time base supports $T_{CY}/2$ PWM edge resolution
- Two output pins (pair) for each PWM generator
- Complementary or independent operation for each output pin pair
- Hardware dead-time generators for Complementary mode
- Output pin polarity defined by nonvolatile device Configuration bits
- Multiple output modes:
  - Edge-Aligned mode
  - Center-Aligned mode
  - Center-Aligned mode with double updates
  - Single Event mode
- Manual override register for PWM output pins
- Hardware Fault input pins with programmable function
- Trigger for synchronizing A/D samples and conversions to PWM timing
- Each output pin associated with the PWM can be individually enabled

9.3.1 MCPWM MODULE VARIANTS

There are two versions of the MCPWM module depending on the dsPIC30F device that is selected. There is an 8-output module that is typically found on devices that have 64 or more pins. A 6-output MCPWM module is also available and is typically found on smaller devices that have fewer than 64 pins.

The 6-output MCPWM module is useful for single or 3-phase power application, while the 8 MCPWM can support 4-phase motor applications. The 8-output MCPWM (Figure 9-2) also provides increased flexibility in an application because it supports two fault pins and two programmable dead times.

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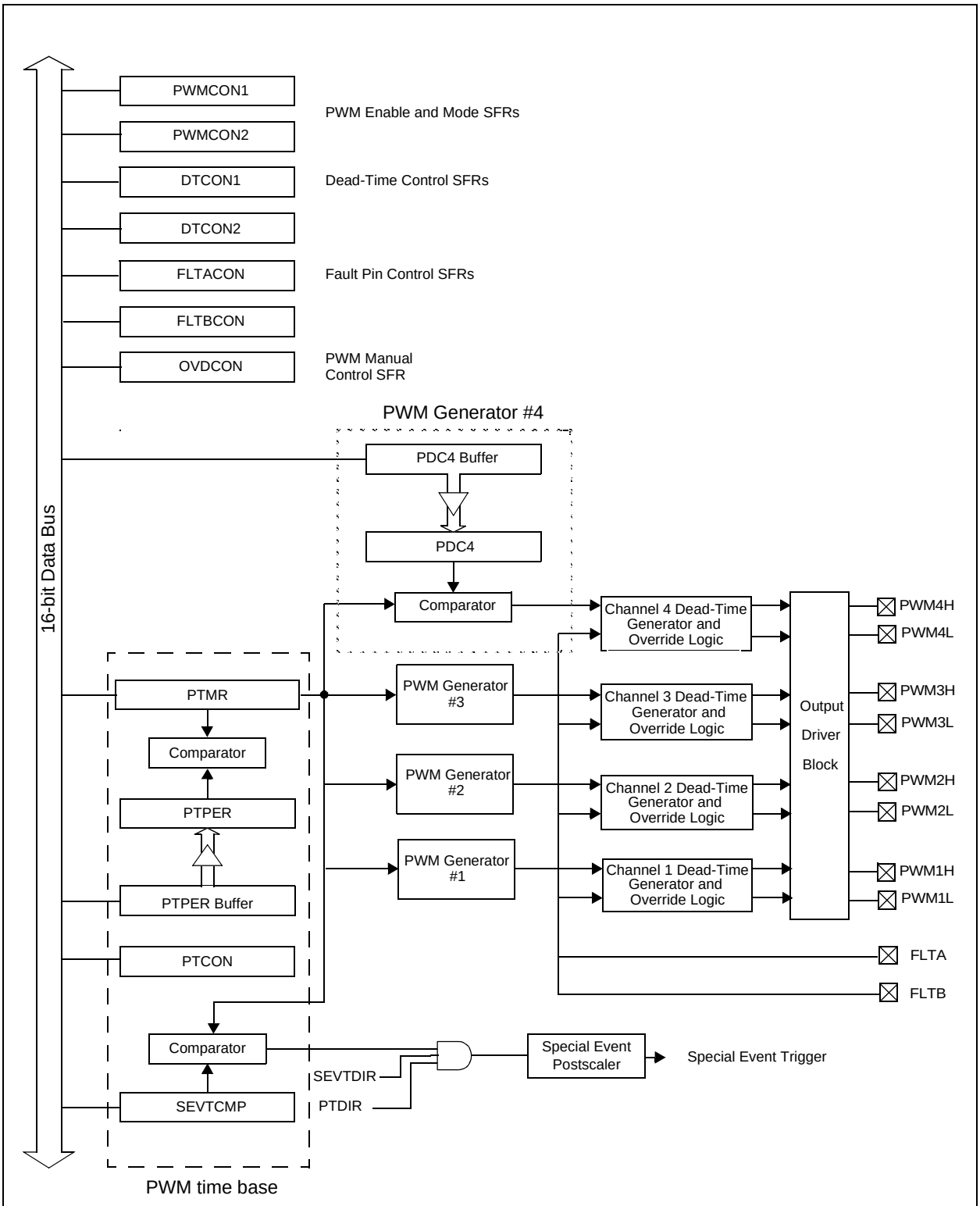
FIGURE 9-2: 8-OUTPUT PWM MODULE BLOCK DIAGRAM



Note: Details of PWM Generator #1, #2 and #3 not shown for clarity.

9.3.2 PWM TIME BASE

The PWM time base is provided by a 15-bit timer with a prescaler and postscaler. The PWM time base can be configured for four different modes of operation:

- Free Running mode
- Single-Shot mode
- Continuous Up/Down Count mode
- Continuous Up/Down Count mode with interrupts for double-updates

The Up/Down Counting modes support center aligned PWM generation. The Single-Shot mode allows the PWM module to support pulse control of certain Electronically Commutated Motors (ECMs).

Table 9-1 lists the frequencies and resolutions that can be attained as a function of the dsPIC30F device instruction cycle frequency.

TABLE 9-1: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS, 1:1 PRESCALER

TCY (FCY)	PTPER Value	PWM Resolution	PWM Frequency*
33 ns (30 MHz)	0x7FFF	16 bits	915 Hz
33 ns (30 MHz)	0x03FF	11 bits	29.3 KHz
50 ns (20 MHz)	0x7FFF	16 bits	610 Hz
50 ns (20 MHz)	0x01FF	10 bits	39.1 KHz
100 ns (10 MHz)	0x7FFF	16 bits	305 Hz
100 ns (10 MHz)	0x00FF	9 bits	39.1 KHz
200 ns (5 MHz)	0x7FFF	16 bits	153 Hz
200 ns (5 MHz)	0x007F	8 bits	39.1 KHz

* PWM frequencies will be 1/2 the value indicated for center aligned operation.

9.4 QEI Module

Quadrature encoders (also referred to as Incremental encoders or Optical encoders) are used in position and speed detection of rotating motion systems. Quadrature encoders enable closed loop control of many motor control applications, such as Switched Reluctance (SR) motor and AC Induction Motor (ACIM).

Typically, three outputs, termed: Phase A, Phase B and INDEX, provide information that can be decoded to provide information on the movement of the motor shaft including distance and direction.

A Quadrature Decoder captures the phase signals and index pulse and converts the information into a numeric count of the position pulses. Generally, the count will increment when the shaft is rotating one direction and decrement when the shaft is rotating in the other direction.

The QEI module (Figure 9-3) includes:

- Three input pins for two-phase signals and index pulse
- Programmable digital noise filters on inputs
- Quadrature decoder providing counter pulses and count direction
- 16-bit up/down position counter
- Count direction status
- X2 and X4 count resolution
- Two modes of position counter reset
- General Purpose16-bit Timer/Counter mode
- Interrupts generated by QEI or counter events

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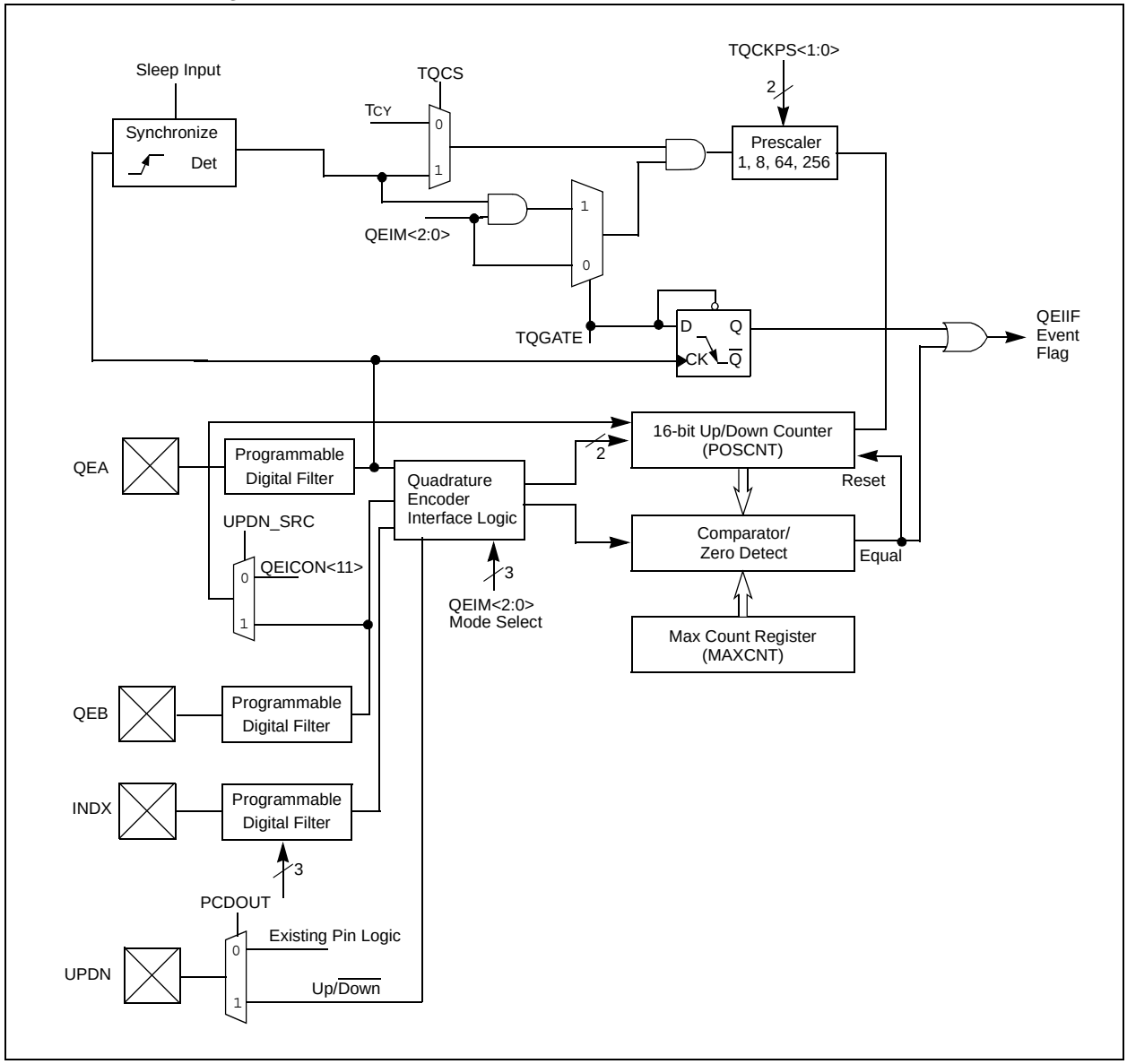
FIGURE 9-3: QUADRATURE ENCODER INTERFACE BLOCK DIAGRAM



9.5 Input Capture Module

The Input Capture module is useful in applications requiring Frequency (Period) and Pulse measurement. The dsPIC30F devices support up to eight input capture channels.

The Input Capture module captures the 16-bit value of the selected time base register when an event occurs at the ICx pin. The events that cause a capture event are listed below in three categories:

1. Simple Capture Event modes:
   - Capture timer value on every falling edge of input at ICx pin
   - Capture timer value on every rising edge of input at ICx pin
2. Capture timer value on every edge (rising and falling)
3. Prescaler Capture Event modes:
   - Capture timer value on every 4th rising edge of input at ICx pin
   - Capture timer value on every 16th rising edge of input at ICx pin

Each input capture channel can select between one of two 16-bit timers (Timer2 or Timer3) for the time base. The selected timer can use either an internal or an external clock.

Other operational features include:

- Device wake-up from capture pin during CPU Sleep and Idle modes
- Interrupt on input capture event
- 4-word FIFO buffer for capture values:
  - Interrupt optionally generated after 1, 2, 3 or 4 buffer locations are filled

Input capture can also be used to provide additional sources of external interrupts.

9.6 Output Compare/PWM Module

The Output Compare module features are quite useful in applications that require controlled timing pulses or PWM modulated pulse streams.

The Output Compare module has the ability to compare the value of a selected time base with the value of one or two compare registers (depending on the Operation mode selected). Furthermore, it has the ability to generate a single output pulse, or a repetitive sequence of output pulses, on a compare match event. Like most dsPIC30F peripherals, it also has the ability to generate interrupts-on-compare match events.

The dsPIC30F device may have up to eight output compare channels, designated OC1 through OC8. Refer to the specific device data sheet for the number of channels available in a particular device. All output compare channels are functionally identical.

Each output compare channel can use one of two selectable time bases. The time base is selected using the OCTSEL bit (OCxCON<3>). An ‘x’ in the pin, register or bit name denotes the specific output compare channel. Refer to the device data sheet for the specific timers that can be used with each output compare channel number.

Each Output Compare module has the following modes of operation:

- Single Compare Match mode
- Dual Compare Match mode generating:
  - Single Output Pulse
  - Continuous Output Pulses
- Simple Pulse Width Modulation mode:
  - With Fault Protection Input
  - Without Fault Protection Input

9.7 Data Converter Interface Module

The dsPIC30F Data Converter Interface (DCI) module allows simple interfacing to devices such as audio coder/decoders (codecs), A/D converters and D/A converters.

The following interfaces are supported:

- Framed Synchronous Serial Transfer (Single or Multi-Channel)
- Inter-IC Sound (I^2S) Interface
- AC-Link (AC’97) Compliant mode

Many codecs intended for use in audio applications support sampling rates between 8 kHz and 48 kHz and use one of the interface protocols listed above. The DCI automatically handles the interface timing associated with these codecs. No overhead from the CPU is required until the requested amount of data has been transmitted and/or received by the DCI. Up to four data words can be transferred between CPU interrupts.

The data word length for the DCI is programmable up to 16 bits to match the data size of the dsPIC30F CPU. However, many codecs have data word sizes greater than 16 bits. Long data word lengths can be supported by the DCI. The DCI is configured to transmit/receive the long word in multiple 16-bit time slots. This operation is transparent to the user, and the long data word is stored in consecutive register locations.

Figure 9-4 is a block diagram of the DCI Module. The DCI can support up to 16 time slots in a data frame, for a maximum frame size of 256 bits. There are control bits for each time slot in the data frame that determine whether the DCI will transmit/receive during the time slot.

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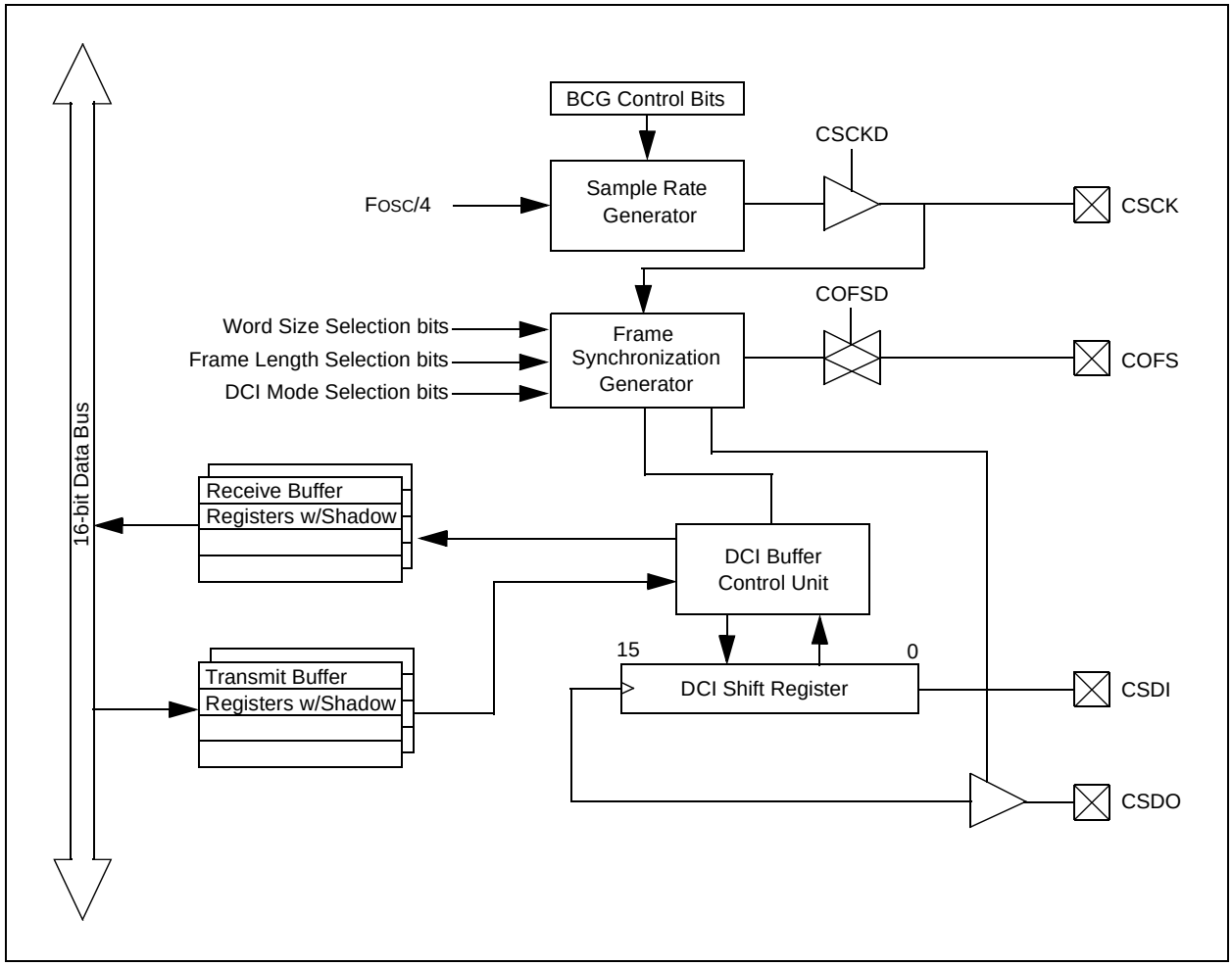
FIGURE 9-4: DCI MODULE BLOCK DIAGRAM



9.8 SPI™ Module

The Serial Peripheral Interface (SPI) module is a synchronous serial interface for communicating with other peripheral or microcontroller devices such as Serial EEPROMs, shift registers, display drivers, A/D converters, etc. It is compatible with Motorola's SPI™ and SIOP interfaces.

This SPI module includes all SPI modes. A Frame Synchronization mode is also included for support of voice band codecs.

Four pins make up the serial interface: SDI, serial data input; SDO, serial data output; SCK, shift clock input or output; $\overline{SS}$, active low slave select, which also serves as the FSYNC, frame synchronization pulse. A device set up as an SPI Master provides the serial communication clock signal on its SCK pin.

A series of 8 or 16 clock pulses (depending on mode) shift out the 8 or 16 bits (depending on whether a byte or word is being transferred) and simultaneously shift in 8 or 16 bits of data from the SDI pin. An interrupt is generated when the transfer is complete.

Transmits and receives are double-buffered, which allows the buffer to be used while the shift register is still shifting data in or out. Slave Select synchronization allows selective enabling of SPI Slave devices, which is particularly useful when a single Master is connected to multiple slaves.

9.9 UART Module

The UART is a full-duplex asynchronous system that can communicate with peripheral devices, such as personal computers, RS-232, and RS-485 interfaces.

The dsPIC30F devices have one or more UART's.

The key features of the UART module are:

- Full-duplex operation with 8- or 9-bit data
- Even, Odd or No Parity options (for 8-bit data)
- One or two Stop bits
- Fully integrated Baud Rate Generator with 16-bit prescaler
- Baud rates range from up to 2.5 Mbps and down to 38 Hz at 30 MIPs
- 4-character deep transmit data buffer
- 4-character deep receive data buffer
- Parity, Framing and Buffer Overrun error detection
- 16x Baud Clock output for IrDA® support
- Support for interrupt on Address Detect (9th bit = 1)
- Separate Transmit and Receive interrupts:
  - On transmission of 1 or 4 characters
  - On reception of 1, 3 and 4 characters
- Loopback mode for diagnostics
- Alternate TX/RX pins on smaller pin count devices, for efficient pin utilization.

9.10 I^2C^{TM} Module

The I^2C module is a synchronous serial interface, useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be Serial EEPROMs, shift registers, display drivers, A/D converters, etc.

The Inter-Integrated Circuit (I^2C) module offers full hardware support for both Slave and Multi-Master operations.

The key features of the I^2C module are:

- I^2C Slave operation supports 7- and 10-bit address.
- I^2C Master operation supports 7- and 10-bit address.
- I^2C port allows bidirectional transfers between master and slaves.
- Serial clock synchronization for I^2C port can be used as a handshake mechanism to suspend and resume serial transfer (serial clock stretching).
- I^2C supports Multi-Master operation. Detects bus collision and will arbitrate accordingly.
- Slew Rate Control for 100 kHz and 400 kHz bus speeds.

In I^2C mode, pin SCL is clock and pin SDA is data. The module will override the data direction bits for these pins.

9.11 Controller Area Network (CAN) Module

The Controller Area Network (CAN) module is a serial interface useful for communicating with other CAN modules or microcontroller devices. This interface/ protocol was designed to allow communications within noisy environments.

The CAN module is a communication controller implementing the CAN 2.0 A/B protocol, as defined in the BOSCH specification. The module supports CAN 1.2, CAN 2.0A, CAN2.0B Passive and CAN 2.0B Active versions of the protocol. Details of these protocols can be found in the BOSCH CAN specification.

The CAN module features:

- Implementation of the CAN protocol CAN 1.2, CAN 2.0A and CAN 2.0B
- Standard and extended data frames
- Data lengths of 0-8 bytes
- Programmable bit rate up to 1 Mbit/sec
- Support for remote frames
- Double buffered receiver with two prioritized received message storage buffers (each buffer may contain up to 8 bytes of data)
- Six full (standard/extended identifier) acceptance filters, two associated with the high priority receive buffer, and four associated with the low priority receive buffer
- Two full acceptance filter masks, one each associated with the high and low priority receive buffers
- Three transmit buffers with application specified prioritization and abort capability (each buffer may contain up to 8 bytes of data)
- Programmable wake-up functionality with integrated low pass filter
- Programmable Loopback mode supports self-test operation
- Signaling via interrupt capabilities for all CAN receiver and transmitter error states
- Programmable clock source
- Programmable link to Timer module for time-stamping and network synchronization
- Low-power Sleep and Idle mode

The CAN Bus module consists of a protocol engine and message buffering/control. The CAN protocol engine handles all functions for receiving and transmitting messages on the CAN bus. Messages are transmitted by first loading the appropriate data registers. Status and errors can be checked by reading the appropriate registers. Any message detected on the CAN bus is checked for errors and then matched against filters to see if it should be received and stored in one of the receive registers.

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9.12 I/O Pins

Some pins for the I/O pin functions are multiplexed with an alternate function for the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

All I/O port pins have three registers directly associated with the operation of the port pin. The Data Direction register determines whether the pin is an input or an output. The Port Data Latch register provides latched output data for the I/O pins. The Port register provides visibility of the logic state of the I/O pins. Reading the Port register provides the I/O pin logic state, while writes to the Port register write the data to the port Data Latch register.

I/O port pins have latch bits (Port Latch register). This register, when read, yields the contents of the I/O latch, and when written, modifies the contents of the I/O latch, thus modifying the value driven out on a pin if the corresponding Data Direction register bit is configured for output. This can be used in read-modify-write instructions that allow the user to modify the contents of the latch register, regardless of the status of the corresponding pins.

The I/O pins have the following features:

- Schmitt Trigger input
- CMOS output drivers
- Weak internal pull-up

The Input Change Notification module gives dsPIC30F devices the ability to generate interrupt requests to the processor in response to a change of state on selected input pins. This module is capable of detecting input changes of state even in Sleep mode, when the clocks are disabled. There are up to 24 external signals (CN0 through CN23) that can be selected (enabled) for generating an interrupt request on a change of state. Each of the CN pins also has an optional weak pull-up feature.

10.0 dsPIC30F INSTRUCTION SET

10.1 Introduction

The dsPIC30F instruction set provides a broad suite of instructions, which supports traditional microcontroller applications, and a class of instructions, which supports math intensive applications. Since almost all of the functionality of the PICmicro instruction set has been maintained, this hybrid instruction set allows a friendly DSP migration path for users already familiar with the PICmicro® microcontroller.

10.2 Instruction Set Overview

The dsPIC30F instruction set contains 84 instructions, which can be grouped into the ten functional categories shown in Table 10-1. Table 10-2 defines the symbols used in the instruction summary tables, Table 10-3 through Table 10-12. These tables define the syntax, description, storage and execution requirements for each instruction. Storage requirements are represented in 24-bit instruction words, and execution requirements are represented in instruction cycles. Most instructions have several different addressing modes and execution flows, which require different instruction variants. For instance, there are six unique ADD instructions and each instruction variant has its own instruction encoding.

TABLE 10-1: dsPIC30F INSTRUCTION GROUPS

Functional Group	Summary Table
Move Instructions	Table 10-3
Math Instructions	Table 10-4
Logic Instructions	Table 10-5
Rotate/Shift Instructions	Table 10-6
Bit Instructions	Table 10-7
Compare/Skip Instructions	Table 10-8
Program Flow Instructions	Table 10-9
Shadow/Stack Instructions	Table 10-10
Control Instructions	Table 10-11
DSP Instructions	Table 10-12

10.2.1 MULTI-CYCLE INSTRUCTIONS

As the instruction summary tables show, most instructions execute in a single cycle, with the following exceptions:

- Instructions `DO, MOV.D, POP.D, PUSH.D, TBLRDH, TBLRDL, TBLWTH` and `TBLWTL` require 2 cycles to execute.
- Instructions `DIVF, DIV.S, DIV.U` are single-cycle instructions, which should be executed 18 consecutive times as the target `REPEAT` instruction.
- Instructions that change the program counter also require 2 cycles to execute, with the extra cycle executed as a `NOP`. SKIP instructions, which skip over a 2-word instruction, require 3 instruction cycles to execute, with 2 cycles executed as a `NOP`.
- The `RETFIE, RETLW` and `RETURN` are a special case of an instruction that changes the program counter. These execute in 3 cycles, unless an exception is pending, and then they execute in 2 cycles.

Note:	Instructions that access program memory as data, using Program Space Visibility, incur some cycle count overhead. See the *dsPIC30F Family Reference Manual* (DS70046) for details.

10.2.2 MULTI-WORD INSTRUCTIONS

As the instruction summary tables show, almost all instructions consume one instruction word (24 bits), with the exception of the `CALL, DO` and `GOTO` instructions, which are flow instructions listed in Table 10-9. These instructions require two words of memory because their opcodes embed large literal operands.

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TABLE 10-2: SYMBOLS USED IN SUMMARY TABLES

Symbol	Description
#	Literal operand designation
Acc	Accumulator A or Accumulator B
AWB	Accumulator Write Back
bit4	4-bit wide bit position (0:15)
Expr	Absolute address, label or expression (resolved by the linker)
f	File register address
lit1	1-bit literal (0:1)
lit4	4-bit literal (0:15)
lit5	5-bit literal (0:31)
lit8	8-bit literal (0:255)
lit10	10-bit literal (0:255 for Byte mode, 0:1023 for Word mode)
lit14	14-bit literal (0:16383)
lit16	16-bit literal (0:65535)
lit23	23-bit literal (0:8388607)
Slit4	Signed 4-bit literal (-8:7)
Slit6	Signed 6-bit literal (-16:16)
Slit10	Signed 10-bit literal (-512:511)
Slit16	Signed 16-bit literal (-32768:32767)
TOS	Top-of-Stack
Wb	Base working register
Wd	Destination working register (direct and indirect addressing)
Wm, Wn	Working register divide pair (dividend, divisor)
Wm*Wm	Working register multiplier pair (same source register)
Wm*Wn	Working register multiplier pair (different source registers)
Wn	Both source and destination working register (direct addressing)
Wnd	Destination working register (direct addressing)
Wns	Source working register (direct addressing)
WREG	Default working register
Ws	Source working register (direct and indirect addressing)
Wx	Source Addressing mode and working register for X data bus pre-fetch
Wxd	Destination working register for X data bus pre-fetch
Wy	Source Addressing mode and working register for Y data bus pre-fetch
Wyd	Destination working register for Y data bus pre-fetch

TABLE 10-3: MOVE INSTRUCTIONS

Assembly	Syntax	Description	Words	Cycles
EXCH	Wns,Wnd	Swap Wns and Wnd	1	1
MOV	f {,WREG}	Move f to destination	1	1
MOV	WREG,f	Move WREG to f	1	1
MOV	f,Wnd	Move f to Wnd	1	1
MOV	Wns,f	Move Wns to f	1	1
MOV.b	#lit8,Wnd	Move 8-bit literal to Wnd	1	1
MOV	#lit16,Wnd	Move 16-bit literal to Wnd	1	1
MOV	[Ws+Slit10],Wnd	Move [Ws + signed 10-bit offset] to Wnd	1	1
MOV	Wns,[Wd+Slit10]	Move Wns to [Wd + signed 10-bit offset]	1	1
MOV	Ws,Wd	Move Ws to Wd	1	1
MOV.D	Ws,Wnd	Move double Ws to Wnd:Wnd + 1	1	2
MOV.D	Wns,Wd	Move double Wns:Wns + 1 to Wd	1	2
SWAP	Wn	Wn = byte or nibble swap Wn	1	1
TBLRDH	Ws,Wd	Read high program word to Wd	1	2
TBLRDL	Ws,Wd	Read low program word to Wd	1	2
TBLWTH	Ws,Wd	Write Ws to high program word	1	2
TBLWTL	Ws,Wd	Write Ws to low program word	1	2

Note: When the optional {,WREG} operand is specified, the destination of the instruction is WREG. When {,WREG} is not specified, the destination of the instruction is the file register f.

Note: Table 10-3 through Table 10-12 present the base instruction syntax for the dsPIC30F. These instructions do not include all the available addressing modes. For example, some instructions show the Byte Addressing mode and others do not. Please refer to the *dsPIC30F Programmer's Reference Manual* (DS70030) for details on each instruction.

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TABLE 10-4: MATH INSTRUCTIONS

Assembly	Syntax	Description	Words	Cycles
ADD	f {,WREG}	Destination = f + WREG	1	1
ADD	#lit10,Wn	Wn = lit10 + Wn	1	1
ADD	Wb,#lit5,Wd	Wd = Wb + lit5	1	1
ADD	Wb,Ws,Wd	Wd = Wb + Ws	1	1
ADDC	f {,WREG}	Destination = f + WREG + (C)	1	1
ADDC	#lit10,Wn	Wn = lit10 + Wn + (C)	1	1
ADDC	Wb,#lit5,Wd	Wd = Wb + lit5 + (C)	1	1
ADDC	Wb,Ws,Wd	Wd = Wb + Ws + (C)	1	1
DAW.B	Wn	Wn = decimal adjust Wn	1	1
DEC	f {,WREG}	Destination = f – 1	1	1
DEC	Ws,Wd	Wd = Ws – 1	1	1
DEC2	f {,WREG}	Destination = f – 2	1	1
DEC2	Ws,Wd	Wd = Ws – 2	1	1
DIV.S	Wm,Wn	Signed 16/16-bit integer divide*	1	18
DIV.SD	Wm,Wn	Signed 32/16-bit integer divide*	1	18
DIV.U	Wm,Wn	Unsigned 16/16-bit integer divide*	1	18
DIV.UD	Wm,Wn	Unsigned 32/16-bit integer divide*	1	18
DIVF	Wm,Wn	Signed 16/16-bit fractional divide*	1	18
INC	f {,WREG}	Destination = f + 1	1	1
INC	Ws,Wd	Wd = Ws + 1	1	1
INC2	f {,WREG}	Destination = f + 2	1	1
INC2	Ws,Wd	Wd = Ws + 2	1	1
MUL	f	W3:W2 = f * WREG	1	1
MUL.SS	Wb,Ws,Wnd	{Wnd+1,Wnd} = sign(Wb) * sign(Ws)	1	1
MUL.SU	Wb,#lit5,Wnd	{Wnd+1,Wnd} = sign(Wb) * unsign(lit5)	1	1
MUL.SU	Wb,Ws,Wnd	{Wnd+1,Wnd} = sign(Wb) * unsign(Ws)	1	1
MUL.US	Wb,Ws,Wnd	{Wnd+1,Wnd} = unsign(Wb) * sign(Ws)	1	1
MUL.UU	Wb,#lit5,Wnd	{Wnd+1,Wnd} = unsign(Wb) * unsign(lit5)	1	1
MUL.UU	Wb,Ws,Wnd	{Wnd+1,Wnd} = unsign(Wb) * unsign(Ws)	1	1
SE	Ws,Wnd	Wnd = sign-extended Ws	1	1
SUB	f {,WREG}	Destination = f – WREG	1	1
SUB	#lit10, Wn	Wn = Wn – lit10	1	1
SUB	Wb,#lit5,Wd	Wd = Wb – lit5	1	1
SUB	Wb,Ws,Wd	Wd = Wb – Ws	1	1
SUBB	f {,WREG}	Destination = f – WREG – (C)	1	1
SUBB	#lit10, Wn	Wn = Wn – lit10 – (C)	1	1
SUBB	Wb,#lit5,Wd	Wd = Wb – lit5 – ($\overline{C}$)	1	1
SUBB	Wb,Ws,Wd	Wd = Wb – Ws – ($\overline{C}$)	1	1
SUBBR	f {,WREG}	Destination = WREG – f – ($\overline{C}$)	1	1
SUBBR	Wb,#lit5,Wd	Wd = lit5 – Wb – ($\overline{C}$)	1	1
SUBBR	Wb,Ws,Wd	Wd = Ws – Wb – ($\overline{C}$)	1	1
SUBR	f {,WREG}	Destination = WREG – f	1	1
SUBR	Wb,#lit5,Wd	Wd = lit5 – Wb	1	1
SUBR	Wb,Ws,Wd	Wd = Ws – Wb	1	1
ZE	Ws,Wnd	Wnd = zero-extended Ws	1	1

* Divide instructions are interruptible on a cycle-by-cycle basis. Also, divide instructions must be accompanied by a REPEAT instruction, which adds 1 extra cycle.

TABLE 10-5: LOGIC INSTRUCTIONS

Assembly	Syntax	Description	Words	Cycles
AND	f {,WREG}	Destination = f .AND. WREG	1	1
AND	#lit10,Wn	Wn = lit10 .AND. Wn	1	1
AND	Wb,#lit5,Wd	Wd = Wb .AND. lit5	1	1
AND	Wb,Ws,Wd	Wd = Wb .AND. Ws	1	1
CLR	f	f = 0x0000	1	1
CLR	WREG	WREG = 0x0000	1	1
CLR	Wd	Wd = 0x0000	1	1
COM	f {,WREG}	Destination = $\overline{f}$	1	1
COM	Ws,Wd	Wd = $\overline{Ws}$	1	1
IOR	f {,WREG}	Destination = f .IOR. WREG	1	1
IOR	#lit10,Wn	Wn = lit10 .IOR. Wn	1	1
IOR	Wb,#lit5,Wd	Wd = Wb .IOR. lit5	1	1
IOR	Wb,Ws,Wd	Wd = Wb .IOR. Ws	1	1
NEG	f {,WREG}	Destination = $\overline{f}$ + 1	1	1
NEG	Ws,Wd	Wd = $\overline{Ws}$ + 1	1	1
SETM	f	f = 0xFFFF	1	1
SETM	WREG	WREG = 0xFFFF	1	1
SETM	Wd	Wd = 0xFFFF	1	1
XOR	f {,WREG}	Destination = f .XOR. WREG	1	1
XOR	#lit10,Wn	Wn = lit10 .XOR. Wn	1	1
XOR	Wb,#lit5,Wd	Wd = Wb .XOR. lit5	1	1
XOR	Wb,Ws,Wd	Wd = Wb .XOR. Ws	1	1

Note: When the optional {,WREG} operand is specified, the destination of the instruction is WREG. When {,WREG} is not specified, the destination of the instruction is the file register f.

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TABLE 10-6: ROTATE/SHIFT INSTRUCTIONS

Assembly	Syntax	Description	Words	Cycles
ASR	f {,WREG}	Destination = arithmetic right shift f	1	1
ASR	Ws,Wd	Wd = arithmetic right shift Ws	1	1
ASR	Wb,#lit4,Wnd	Wnd = arithmetic right shift Wb by lit4	1	1
ASR	Wb,Wns,Wnd	Wnd = arithmetic right shift Wb by Wns	1	1
LSR	f {,WREG}	Destination = logical right shift f	1	1
LSR	Ws,Wd	Wd = logical right shift Ws	1	1
LSR	Wb,#lit4,Wnd	Wnd = logical right shift Wb by lit4	1	1
LSR	Wb,Wns,Wnd	Wnd = logical right shift Wb by Wns	1	1
RLC	f {,WREG}	Destination = rotate left through Carry f	1	1
RLC	Ws,Wd	Wd = rotate left through Carry Ws	1	1
RLNC	f {,WREG}	Destination = rotate left (no Carry) f	1	1
RLNC	Ws,Wd	Wd = rotate left (no Carry) Ws	1	1
RRC	f {,WREG}	Destination = rotate right through Carry f	1	1
RRC	Ws,Wd	Wd = rotate right through Carry Ws	1	1
RRNC	f {,WREG}	Destination = rotate right (no Carry) f	1	1
RRNC	Ws,Wd	Wd = rotate right (no Carry) Ws	1	1
SL	f {,WREG}	Destination = left shift f	1	1
SL	Ws,Wd	Wd = left shift Ws	1	1
SL	Wb,#lit4,Wnd	Wnd = left shift Wb by lit4	1	1
SL	Wb,Wns,Wnd	Wnd = left shift Wb by Wns	1	1

Note: When the optional {,WREG} operand is specified, the destination of the instruction is WREG. When {,WREG} is not specified, the destination of the instruction is the file register f.

TABLE 10-7: BIT INSTRUCTIONS

Assembly	Syntax	Description	Words	Cycles
BCLR	f,#bit4	Bit clear f	1	1
BCLR	Ws,#bit4	Bit clear Ws	1	1
BSET	f,#bit4	Bit set f	1	1
BSET	Ws,#bit4	Bit set Ws	1	1
BSW.C	Ws,Wb	Write C bit to Ws<Wb>	1	1
BSW.Z	Ws,Wb	Write $\overline{SZ}$ bit to Ws<Wb>	1	1
BTG	f,#bit4	Bit toggle f	1	1
BTG	Ws,#bit4	Bit toggle Ws	1	1
BTST	f,#bit4	Bit test f	1	1
BTST.C	Ws,#bit4	Bit test Ws to C	1	1
BTST.Z	Ws,#bit4	Bit test Ws to SZ	1	1
BTST.C	Ws,Wb	Bit test Ws<Wb> to C	1	1
BTST.Z	Ws,Wb	Bit test Ws<Wb> to SZ	1	1
BTSTS	f,#bit4	Bit test f then set f	1	1
BTSTS.C	Ws,#bit4	Bit test Ws to C then set Ws	1	1
BTSTS.Z	Ws,#bit4	Bit test Ws to SZ then set Ws	1	1
FBCL	Ws,Wnd	Find bit change from left (MSb) side	1	1
FF1L	Ws,Wnd	Find first one from left (MSb) side	1	1
FF1R	Ws,Wnd	Find first one from right (LSb) side	1	1

Note: Bit positions are specified by bit4 (0:15) for word operations.

TABLE 10-8: COMPARE/SKIP INSTRUCTIONS

Assembly	Syntax	Description	Words	Cycles
BTSC	f,#bit4	Bit test f, skip if clear	1	1 (2 or 3)
BTSC	Ws,#bit4	Bit test Ws, skip if clear	1	1 (2 or 3)
BTSS	f,#bit4	Bit test f, skip if set	1	1 (2 or 3)
BTSS	Ws,#bit4	Bit test Ws, skip if set	1	1 (2 or 3)
CP	f	Compare (f – WREG)	1	1
CP	Wb,#lit5	Compare (Wb – lit5)	1	1
CP	Wb,Ws	Compare (Wb – Ws)	1	1
CP0	f	Compare (f – 0x0000)	1	1
CP0	Ws	Compare (Ws – 0x0000)	1	1
CPB	f	Compare with Borrow (f – WREG – $\overline{C}$)	1	1
CPB	Wb,#lit5	Compare with Borrow (Wb – lit5 – $\overline{C}$)	1	1
CPB	Wb,Ws	Compare with Borrow (Wb – Ws – $\overline{C}$)	1	1
CPSEQ	Wb,Wn	Compare Wb with Wn, Skip if Equal (Wb = Wn)	1	1 (2 or 3)
CPSGT	Wb,Wn	Signed Compare Wb with Wn, Skip if Greater Than (Wb > Wn)	1	1 (2 or 3)
CPSLT	Wb,Wn	Signed Compare Wb with Wn, Skip if Less Than (Wb < Wn)	1	1 (2 or 3)
CPSNE	Wb,Wn	Signed Compare Wb with Wn, Skip if Not Equal (Wb ≠ Wn)	1	1 (2 or 3)

Note 1: Bit positions are specified by bit4 (0:15) for word operations.

2: Conditional skip instructions execute in 1 cycle if the skip is not taken, 2 cycles if the skip is taken over a one-word instruction and 3 cycles if the skip is taken over a two-word instruction.

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TABLE 10-9: PROGRAM FLOW INSTRUCTIONS

Assembly	Syntax	Description	Words	Cycles
BRA	Expr	Branch unconditionally	1	2
BRA	Wn	Computed branch	1	2
BRA	C,Expr	Branch if Carry (no Borrow)	1	1 (2)
BRA	GE,Expr	Branch if greater than or equal	1	1 (2)
BRA	GEU,Expr	Branch if unsigned greater than or equal	1	1 (2)
BRA	GT,Expr	Branch if greater than	1	1 (2)
BRA	GTU,Expr	Branch if unsigned greater than	1	1 (2)
BRA	LE,Expr	Branch if less than or equal	1	1 (2)
BRA	LEU,Expr	Branch if unsigned less than or equal	1	1 (2)
BRA	LT,Expr	Branch if less than	1	1 (2)
BRA	LTU,Expr	Branch if unsigned less than	1	1 (2)
BRA	N,Expr	Branch if Negative	1	1 (2)
BRA	NC,Expr	Branch if not Carry (Borrow)	1	1 (2)
BRA	NN,Expr	Branch if not Negative	1	1 (2)
BRA	NOV,Expr	Branch if not Overflow	1	1 (2)
BRA	NZ,Expr	Branch if not Zero	1	1 (2)
BRA	OA,Expr	Branch if Accumulator A Overflow	1	1 (2)
BRA	OB,Expr	Branch if Accumulator B Overflow	1	1 (2)
BRA	OV,Expr	Branch if Overflow	1	1 (2)
BRA	SA,Expr	Branch if Accumulator A Saturate	1	1 (2)
BRA	SB,Expr	Branch if Accumulator B Saturate	1	1 (2)
BRA	Z,Expr	Branch if Zero	1	1 (2)
CALL	Expr	Call subroutine	2	2
CALL	Wn	Call indirect subroutine	1	2
DO	#lit14,Expr	Do code through PC + Expr, (lit14 + 1) times	2	2
DO	Wn,Expr	Do code through PC + Expr, (Wn + 1) times	2	2
GOTO	Expr	Go to address	2	2
GOTO	Wn	Go to address indirectly	1	2
RCALL	Expr	Relative call	1	2
RCALL	Wn	Computed call	1	2
REPEAT	#lit14	Repeat next instruction (lit14 + 1) times	1	1
REPEAT	Wn	Repeat next instruction (Wn + 1) times	1	1
RETFIE		Return from interrupt enable	1	3 (2)
RETLW	#lit10,Wn	Return with lit10 in Wn	1	3 (2)
RETURN		Return from subroutine	1	3 (2)

Note 1: Conditional branch instructions execute in 1 cycle if the branch is not taken, or 2 cycles if the branch is taken.

2: RETURN normally executes in 3 cycles. However, it executes in 2 cycles if an interrupt is pending.

TABLE 10-10: SHADOW/STACK INSTRUCTIONS

Assembly	Syntax	Description	Words	Cycles
LNK	#lit14	Link Frame Pointer	1	1
POP	f	Pop TOS to f	1	1
POP	Wd	Pop TOS to Wd	1	1
POP.D	Wnd	Double pop from TOS to Wnd:Wnd + 1	1	2
POP.S		Pop shadow registers	1	1
PUSH	f	Push f to TOS	1	1
PUSH	Ws	Push Ws to TOS	1	1
PUSH.D	Wns	Push double Wns:Wns + 1 to TOS	1	2
PUSH.S		Push shadow registers	1	1
ULNK		Unlink Frame Pointer	1	1

TABLE 10-11: CONTROL INSTRUCTIONS

Assembly	Syntax	Description	Words	Cycles
CLRWDT		Clear Watchdog Timer	1	1
DISI	#lit14	Disable interrupts for (lit14 + 1) instruction cycles	1	1
NOP		No operation	1	1
NOPR		No operation	1	1
PWRSAV	#lit1	Enter Power-Saving mode lit1	1	1
RESET		Software device Reset	1	1

TABLE 10-12: DSP INSTRUCTIONS

Assembly	Syntax	Description	Words	Cycles
ADD	Acc	Add accumulators	1	1
ADD	Ws,#Slit4,Acc	16-bit signed add to Acc	1	1
CLR	Acc,Wx,Wxd,Wy,Wyd,AWB	Clear Acc	1	1
ED	Wm*Wm,Acc,Wx,Wy,Wxd	Euclidean distance (no accumulate)	1	1
EDAC	Wm*Wm,Acc,Wx,Wy,Wxd	Euclidean distance	1	1
LAC	Ws,#Slit4,Acc	Load Acc	1	1
MAC	Wm*Wn,Acc,Wx,Wxd,Wy,Wyd,AWB	Multiply and accumulate	1	1
MAC	Wm*Wm,Acc,Wx,Wxd,Wy,Wyd	Square and accumulate	1	1
MOVSAC	Acc,Wx,Wxd,Wy,Wyd,AWB	Move Wx to Wxd and Wy to Wyd	1	1
MPY	Wm*Wn,Acc,Wx,Wxd,Wy,Wyd	Multiply Wn by Wm to Acc	1	1
MPY	Wm*Wm,Acc,Wx,Wxd,Wy,Wyd	Square to Acc	1	1
MPY.N	Wm*Wn,Acc,Wx,Wxd,Wy,Wyd	-(Multiply Wn by Wm) to Acc	1	1
MSC	Wm*Wn,Acc,Wx,Wxd,Wy,Wyd,AWB	Multiply and subtract from Acc	1	1
NEG	Acc	Negate Acc	1	1
SAC	Acc,#Slit4,Wd	Store Acc	1	1
SAC.R	Acc,#Slit4,Wd	Store rounded Acc	1	1
SFTAC	Acc,#Slit6	Arithmetic shift Acc by Slit6	1	1
SFTAC	Acc,Wn	Arithmetic shift Acc by (Wn)	1	1
SUB	Acc	Subtract accumulators	1	1

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11.0 MICROCHIP DEVELOPMENT TOOL SUPPORT

Microchip offers comprehensive development tools and libraries to support the dsPIC30F architecture. In addition, the company is partnering with many third party tools manufacturers for additional dsPIC30F device support. Table 11-1 lists development tools that support the dsPIC30F family. The paragraphs that follow describe each of the tools in more detail.

TABLE 11-1: dsPIC30F DEVELOPMENT TOOLS

	Development Tool	Description	Part #	From	List Price*
Essential Software Tools	**MPLAB® IDE 6.xx** (see 11.1)	Integrated Development Environment	—	Microchip	Free
	MPLAB ASM30 (see 11.2)	Assembler (included in MPLAB IDE)	—	Microchip	Free
	MPLAB SIM30 (see 11.3)	Software Simulator (Included in MPLAB IDE)	—	Microchip	Free
	MPLAB VDI (see 11.4)	Visual Device Initializer for dsPIC30F (included in MPLAB IDE)	—	Microchip	Free
	MPLAB C30 (see 11.5)	ANSI C Compiler, Assembler, Linker and Librarian	SW006012	Microchip	$895
Essential Hardware Tools	**MPLAB ICD 2** (see 11.6)	In-Circuit Debugger and Device Programmer	DV164005	Microchip	$159
		In-Circuit Debugger and Device Programmer With dsPIC30F “Getting Started” Development Board	DV164030	Microchip	$209
	MPLAB ICE 4000 (see 11.7)	In-Circuit Emulator Pod	ICE4000	Microchip	$2560
		Processor Module for dsPIC30F	PMF30XA1	Microchip	$595
		Device Adapter for 80L TQFP Devices	DAF30-2	Microchip	$295
		Device Adapter for 64L TQFP Devices	DAF30-2	Microchip	$295
		Device Adapter for 44L TQFP Devices	DAF30-3	Microchip	$295
		Device Adapter for 18L/28L/40L DIP Devices	DAF30-4	Microchip	$295
	MPLAB PRO MATE® II (see 11.8)	Full Featured Device Programmer, Base Unit	DV007003	Microchip	$695
		ICSP Socket Module	AC004004	Microchip	$349
		Socket Module for 18L DIP/SOIC Devices	AC30F005	Microchip	$189
		Socket Module for 28L DIP/SOIC Devices	AC30F004	Microchip	$189
		Socket Module for 40L DIP Devices	AC30F003	Microchip	$159
		Socket Module for 44L TQFP Devices	AC30F006	Microchip	$159
		Socket Module for 64L TQFP Devices (14 mm x 14 mm)	AC30F002	Microchip	$159
		Socket Module for 80L TQFP Devices (14 mm x 14 mm)	AC30F001	Microchip	$159
	MPLAB PM3 (see 11.9)	Full Featured Device Programmer, Base Unit	DV007004	Microchip	$895
		Socket Module for 18/28/40L DIP Devices	AC164301	Microchip	$189
		Socket Module for 18L SOIC Devices	AC164302	Microchip	$189
		Socket Module for 28L SOIC Devices	AC164302	Microchip	$189
		Socket Module for 44L TQFP Devices	AC164305	Microchip	$189
		Socket Module for 64L TQFP Devices (14 mm x 14 mm)	AC164313	Microchip	$189
		Socket Module for 80L TQFP Devices (14 mm x 14 mm)	AC164314	Microchip	$189

* List Prices are subject to change without notice. Visit www.microchip.com for the latest information.

11.1 MPLAB® Integrated Development Environment V6.XX Software

The MPLAB Integrated Development Environment (IDE) is available at no cost. The MPLAB IDE lets you edit, compile and emulate from a single user interface, as depicted in Figure 11-1. You can design and develop code for the dsPIC devices in the same design environment as PICmicro microcontrollers. The MPLAB IDE is a 32-bit Windows® based application that provides many advanced features for the demanding engineer in a modern, easy-to-use interface. MPLAB IDE integrates:

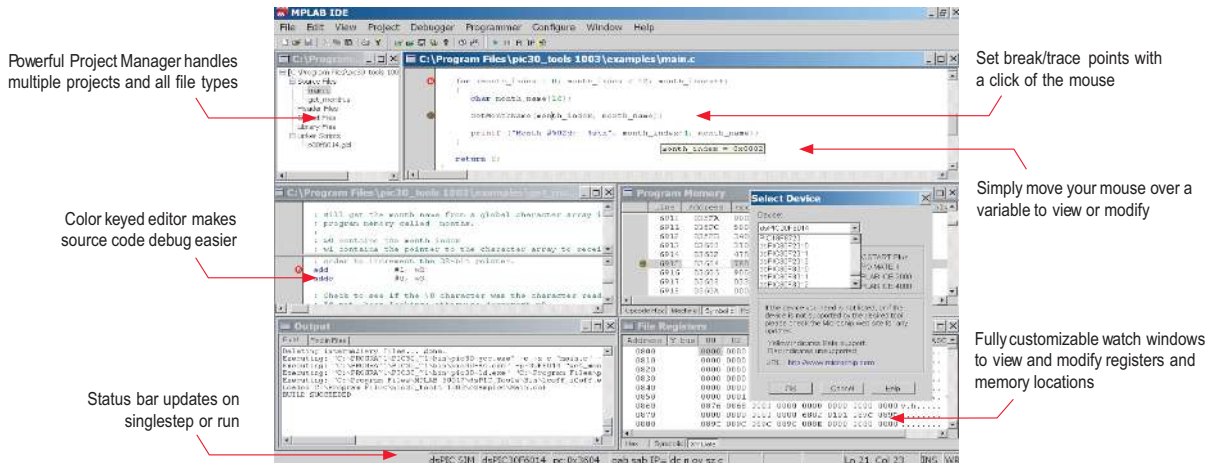
- Full featured, color coded text editor
- Easy-to-use project manager with visual display
- Source level debugging
- Enhanced source level debugging for 'C' (structures, automatic variables, etc.)
- Customizable toolbar and key mapping
- Dynamic status bar displays processor condition
- Context sensitive, interactive on-line help
- Integrated MPLAB SIM30 instruction simulator
- User interface for PRO MATE II and PICSTART Plus device programmers (sold separately)
- User interface for MPLAB ICE 4000 In-Circuit Emulator (sold separately)
- User interface for MPLAB ICD 2 In-Circuit Debugger (sold separately)

The MPLAB IDE allows:

- Editing of source files in either assembly or 'C'
- One-touch compiling and downloading to dsPIC emulator or simulator
- Debugging using:
  - Source files
  - Machine code
  - Mixed mode source and machine code

The ability to use the MPLAB IDE with multiple development and debugging targets provides easy transition from the cost effective simulator to MPLAB ICD 2 or to a full featured emulator with minimal retraining.

FIGURE 11-1: MPLAB IDE DESKTOP



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11.2 MPLAB ASM30 Assembler/Linker/ Librarian

MPLAB ASM30 is a full-featured Macro Assembler. User-defined macros, conditional assembly and a variety of assembler directives make the MPLAB ASM30 a powerful code generation tool.

The accompanying MPLAB LINK30 Linker and MPLAB LIB30 Librarian modules allow efficient linking, library creation and maintenance.

Notable features of the assembler include:

- Support for the entire dsPIC instruction set
- Support for fixed-point and floating-point data
- Available for Windows
- Command Line Interface
- Rich Directive Set
- Flexible Macro Language
- MPLAB IDE compatibility

Notable features of the linker include:

- Automatic or user-defined stack allocation
- Supports dsPIC Program Space Visibility (PSV) window
- Available for Windows
- Command Line Interface
- Linker scripts for all dsPIC devices
- MPLAB IDE compatibility

11.3 MPLAB SIM30 Software Simulator

The MPLAB SIM30 software simulator provides code development for the dsPIC30F family in a PC-hosted environment by simulating the dsPIC30F device on an instruction level. On any instruction you can examine or modify the data areas and apply stimuli to any of the pins from a file or by pressing a user-defined key

The execution can be performed in Single Step, Execute Until Break or Trace mode. The MPLAB SIM30 software simulator fully supports symbolic debugging using the MPLAB C30 compiler and assembler. The software simulator gives you the flexibility to develop and debug code outside of the laboratory environment, making it an excellent multi-project software development tool. Complex stimuli can be injected from files, synchronous clocks or user-defined keys. Output files log register activity for sophisticated post analysis.

Besides modeling the behavior of the CPU, MPLAB SIM 30 also supports the following peripherals:

- Timers
- Input Capture
- 12-bit ADC
- 10-bit ADC
- Motor Control PWM
- UART
- I/O Ports
- Program Flash and Data EEPROM

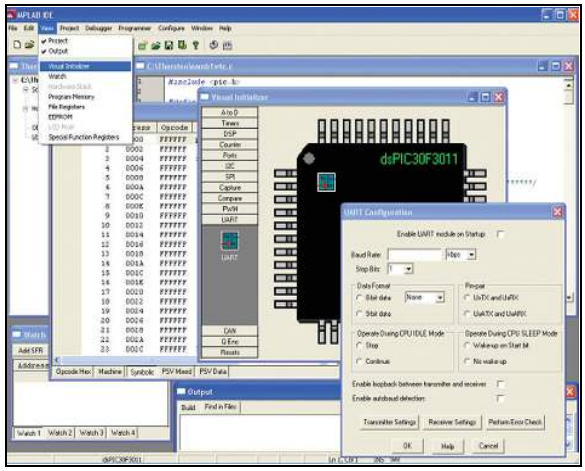
11.4 MPLAB Visual Device Initializer

The MPLAB Visual Device Initializer (VDI) simplifies the task of configuring the dsPIC30F. MPLAB VDI software allows you to configure the entire processor graphically (see Figure 11-2). And when you're done, a mouse click generates your code in Assembly or C code. MPLAB VDI performs extensive error checking on assignments and conflicts on pins, memories and interrupts as well as selection of operating conditions. Generated code files are integrated seamlessly with the rest of our application code through MPLAB Project.

Detailed resource assignment and configuration reports simplify project documentation. Key features of MPLAB VDI include:

- Drag-and-drop feature selection
- One click configuration
- Extensive error checking
- Generates initialization code in the form of a C-callable assembly function
- Integrates seamlessly in MPLAB Project
- Printed reports ease project documentation requirements
- MPLAB Visual Device Initializer is an MPLAB plug-in and can be installed independently of MPLAB

FIGURE 11-2: MPLAB VDI DISPLAY



11.5 MPLAB C30 Compiler/Linker/ Librarian

The Microchip Technology MPLAB C30 provides C language support for the dsPIC30F family. This C compiler is a fully ANSI compliant product with standard libraries. It is highly optimizing for the dsPIC30F family and takes advantage of many dsPIC30F architecture specific features to help you generate very efficient software code. Figure 11-3 illustrates the code size efficiency relative to several competitors.

MPLAB C30 also provides extensions that allow for excellent support of the hardware, such as interrupts and peripherals. It is fully integrated with the MPLAB IDE for high level, source debugging.

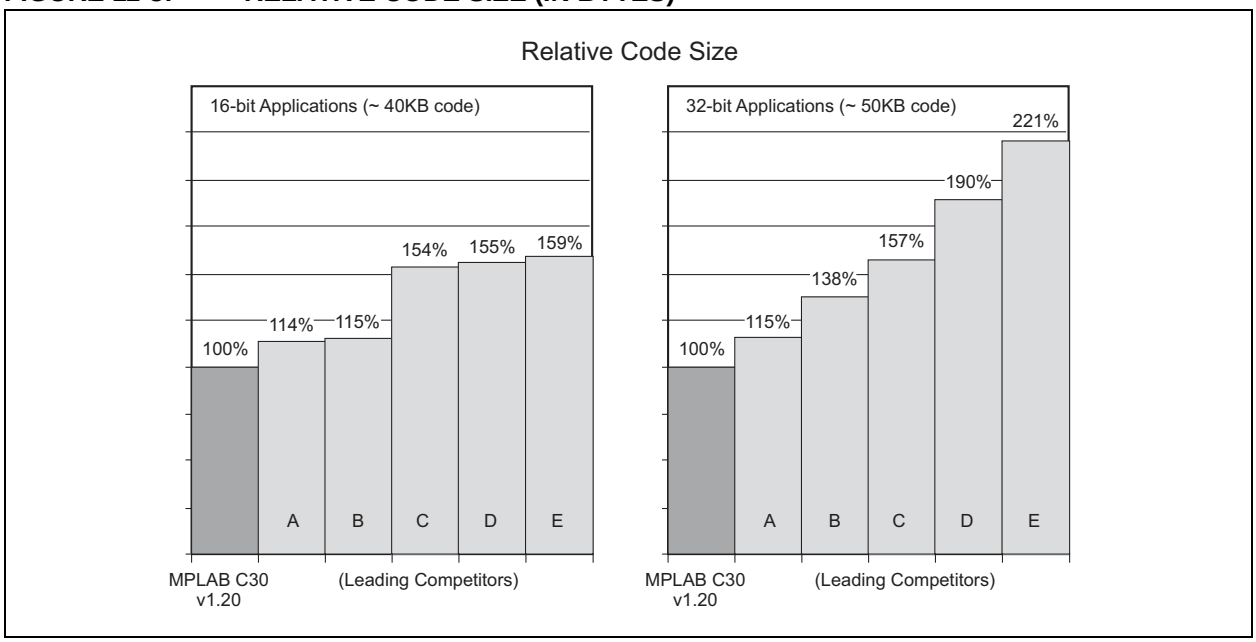
The MPLAB C30 has these characteristics:

- 16-bit native data types
- Efficient use of register based, 3-operand instructions
- Complex addressing modes
- Efficient multi-bit shift operations
- Efficient signed/unsigned comparisons

MPLAB C30 comes complete with its own assembler, linker and librarian. These allow mixed-mode C and assembly programs and link the resulting object files into a single executable file. The compiler is sold separately. The assembler, linker and librarian are available for free with MPLAB C30.

MPLAB C30 also includes the Math Library, Peripheral Library, DSP Library and standard C libraries.

FIGURE 11-3: RELATIVE CODE SIZE (IN BYTES)



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11.6 MPLAB ICD 2 In-Circuit Debugger

The MPLAB ICD 2 In-Circuit Debugger is a powerful, low cost, run-time development tool that uses in-circuit debugging capability built into the dsPIC30F Flash devices. This feature, along with Microchip's In-Circuit Serial Programming™ protocol, gives you cost effective, in-circuit debugging from the graphical user interface of MPLAB. It lets you develop and debug source code by watching variables, single-stepping and setting breakpoints as well as run at full speed to test hardware in real time.

The MPLAB ICD 2 has these features:

- Full speed operation to the range of the device
- Serial or USB PC connector
- USB powered from PC interface
- Low noise power (V_{PP} and V_{DD}) for use with analog and other noise sensitive applications
- Operation down to 2.0V
- Can be used as debugger and inexpensive serial programmer
- Some device resources required (RAM and 2 pins)

FIGURE 11-4: MPLAB ICD 2 IN-CIRCUIT DEBUGGER

11.7 MPLAB ICE 4000 In-Circuit Emulator

The MPLAB ICE 4000 In-Circuit Emulator gives you a complete hardware design tool for dsPIC30F devices. Software control of the emulator by MPLAB IDE lets you edit, build, download and source debug from a single environment. The MPLAB ICE 4000 is a full featured emulator system with enhanced trace, trigger and data monitoring features. Interchangeable processor modules allow you to easily reconfigure the system to emulate different processors. In addition to the dsPIC30F family of digital signal controllers, the MPLAB ICE 4000 supports the extended, high-end PICmicro microcontrollers, the PIC18CXXX and PIC18FXXX devices. The modular architecture of the MPLAB ICE in-circuit emulator allows expansion to support new devices.

The MPLAB ICE in-circuit emulator system has been designed as a real-time emulation system, with advanced features that are generally found on more expensive development tools.

- Full speed emulation, up to 50 MHz bus speed, or 200 MHz external clock speed
- Low voltage emulation down to 1.8 volts
- Configured with 2 Mb program emulation memory, additional modular memory up to 16 Mb
- 64K x 216-bit wide Trace Memory
- Unlimited software breakpoints
- Complex break, trace and trigger logic
- Multi-level trigger up to 4 levels
- Filter trigger functions to trace specific event
- 16-bit Pass counter for triggering on sequential events
- 16-bit Delay counter
- 48-bit time-stamp
- Stopwatch feature
- Time between events
- USB and parallel printer port PC connection

FIGURE 11-5: MPLAB ICE 4000 IN-CIRCUIT EMULATOR

11.8 PRO MATE® II Universal Device Programmer

The PRO MATE II universal device programmer is a full-featured, CE-compliant programming tool, capable of operating in both stand-alone and PC-hosted modes. The PRO MATE II universal device programmer has programmable VDD and VPP supplies, which allow it to verify programmed memory at VDDMIN and VDDMAX for maximum reliability. It has an LCD to display instructions and error messages, keys to enter commands and interchangeable socket modules for all package types. In Stand-Alone mode, the PRO MATE II universal device programmer can read, verify or program PICmicro and dsPIC30F devices. It can also set code protection in this mode. PRO MATE II features include:

- Runs under MPLAB IDE
- Field upgradable firmware
- Host, Safe and “Stand-Alone” operation
- Automatic downloading of object file
- SQTP^{SM} serialization adds unique serial number to each device programmed
- In-Circuit Serial Programming™ Kit (sold separately)
- Interchangeable socket modules supports all package options (sold separately)

If you already own a PRO MATE II universal device programmer, the dsPIC30F family is fully supported through a new set of socket modules.

11.9 MPLAB PM3 Universal Device Programmer

The MPLAB PM3 Universal Device Programmer is easy to use with a PC or as a stand-alone unit to program Microchip’s entire line of PICmicro devices as well as the latest dsPIC30F DSC devices. The MPLAB PM3 features a large and bright LCD unit (128x64 pixels) to display easy menus, programming statistics and status information.

The MPLAB PM3 programmer has exceptional programming speed to allow high production throughput, especially important for large memory devices. It also includes a Secure Digital/Multimedia Card slot for easy and secure data storage and transfer.

The MPLAB PM3 programmer is designed with 40 programmable socket pins, allowing each socket module to be configured to support many different devices. As a result, fewer socket modules are required to support the entire line of Microchip parts. The socket modules use multi-pin connectors for high reliability and quick interchange. An adapter allows current PROMATE® II socket modules to be used.

When connected to a PC-host system, the MPLAB PM3 programmer is seamlessly integrated with the MPLAB Integrated Development Environment (IDE), providing a user-friendly programming interface.

Key features of the MPLAB PM3 Programmer include:

- RS-232 or USB interface
- Integrated In-Circuit Serial Programming™ (ICSP™) interface
- Fast programming time
- Three operating modes:
  - PC Host mode for full control
  - Safe mode for secure data
  - Stand-Alone mode for programming without a PC
- Complete line of interchangeable socket modules to support all Microchip devices and package options (sold separately)
- SQTP^{sm} serialization for programming unique serial numbers while in PC Host mode.
- An alternate DOS command line interface for batch control
- Supports PROMATE II socket modules via adapter (sold separately)
- Large easy-to-read display
- Field upgradeable firmware allows quick new device support
- Secure Digital (SD) and Multimedia Card (MMC) external memory support
- Buzzer notification for noisy environments

FIGURE 11-6: MPLAB PM3 DEVICE PROGRAMMER

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12.0 dsPIC30F DEVELOPMENT TOOLS AND APPLICATION LIBRARIES

Microchip offers a comprehensive set of tools and libraries to help with rapid development of dsPIC30F based application(s). Also, Microchip partners with key third party tool manufacturers to develop quality hardware and software tools in support of the dsPIC30F product family.

Table 12-1 summarizes available and planned dsPIC30F software tools and libraries. Microchip also provides value added services such as skilled/certified technical application contacts, reference designs and hardware and software developers.

TABLE 12-1: SOFTWARE DEVELOPMENT TOOLS AND APPLICATION LIBRARIES

	Development Tool	Description	Part #	From	List Price*
Software Libraries and Application Development Tools	**dsPIC30F Math Library** (see 12.1)	Double Precision and Floating Point Library (ASM, C Wrapper)	SW300020	Microchip	Free
	dsPIC30F Peripheral Library (see 12.2)	Peripheral Initialization, Control and Utility Routines (C)	SW300021	Microchip	Free
	dsPIC30F DSP Library (see 12.3)	Essential DSP algorithm suite (Filters, FFT)	SW300022	Microchip	Free
	dsPICworks™ (see 12.4)	Graphical data analysis and conversion tool for DSP algorithms	SW300023	Microchip	Free
	Digital Filter Design (see 12.5)	Graphical IIR and FIR filter design package for dsPIC30F	SW300001	Microchip	$249
	CMX-RTX™ for dsPIC® (see12.6)	Fully preemptive Real-Time Operating System (RTOS) for dsPIC30F (from CMX)	CMX-RTX for dsPIC	CMX	$4000
		Fully preemptive Real-Time Operating System (RTOS) for dsPIC30F	SW300031	Microchip	$4000
	CMX-Tiny+™ for dsPIC (see 12.6)	Preemptive Real-Time Operating System (RTOS) for dsPIC30F (from CMX)	CMX-Tiny+ for dsPIC	CMX	$3000
		Preemptive Real-Time Operating System (RTOS) for dsPIC30F	SW300032	Microchip	$3000
	CMX Scheduler™ (see 12.6)	Multi-tasking, preemptive scheduler for dsPIC30F	SW300030	Microchip	Free
	TCP/IP Stack (see 12.7)	CMX-MicroNet™ for dsPIC30F TCP/IP connectivity and protocol support	CMX-MicroNet for dsPIC30F	CMX	Contact Vendor
	Soft Modem Library (see 12.8)	V.22bis/V.22 Soft Modem Library	SW300002	Microchip	Free
		V.32bis/V.32 Soft Modem Library	SW300003	Microchip	Contact Microchip
		V.32 (non-trellis) Soft Modem Library		VOCAL Technologies	Contact Vendor
	CANbedded for dsPIC (see12.9)	CAN Driver Library for dsPIC30F		Vector Informatik	Contact Vendor
	osCAN for dsPIC (see 12.10)	OSEK/VDX v2.2		Vector Informatik	Contact Vendor
C, C++ Compilers and IDE from Development Partners	Embedded Workbench for dsPIC30F	ISO/ANSI C and Embedded C++ Compiler in a professional, extensible IDE (Windows 98/ME/NT4/ 2000/XP) Special DSP support library	EWdsPIC 1	IAR	Contact Vendor
	C Compiler	ANSI C Compiler for dsPIC30F	dsPICC	HI-TECH	$950
	C Compiler	C Compiler for dsPIC30F	PCDSP	CCS	$200
	C Compiler with IDE	C Compiler for dsPIC30F with IDE	PCWHD	CCS	$550

* Prices are subject to change without notice

12.1 Math Library

The dsPIC30F Math Library is the compiled version of the math library that is distributed with the highly optimized, ANSI-compliant dsPIC30F MPLAB® C30 compiler (SW006012). It contains advanced single and double-precision floating-point arithmetic and trigonometric functions from the standard C header file <math.h>. The library delivers small program code size and data size, reduced cycles and high accuracy.

Features

- The Math library is callable from either MPLAB C30 or dsPIC30F assembly language.
- The functions are IEEE-754 compliant, with signed zero, signed infinity, NaN (Not a Number) and denormal support and operated in the “round to nearest” mode.
- Compatible with MPLAB ASM30 and MPLAB LINK30, which are available at no charge from Microchip’s web site.

Table 12-2 shows the memory usage and performance of the Math Library. Table 12-3 lists the math functions that are included.

TABLE 12-2: MEMORY USAGE AND PERFORMANCE

Memory Usage (bytes)(1)(2)	
Code size	5250
Data size	4
Performance (cycles)(1)(3)	
add	122
sub	124
mul	109
div	361
Rem	385
Sqrt	492

Note 1: Results are based on using dsPIC30F MPLAB C30 Compiler (SW006012) version 1.20.

2: Maximum “Memory Usage” when all functions in the library are loaded. Most applications will use less.

3: Average 32-bit floating-point performance results.

TABLE 12-3: MATH FUNCTIONS

Single and Double-Precision Floating-Point Functions	
Arithmetic functions	Add, subtract, multiply, divide, remainder
Root and Power Functions	pow, sqrt
Trigonometric and Hyperbolic Functions	acos, asin, atan, atan2, cos, cosh, sin, sinh, tan, tanh
Logarithmic and Exponential Functions	exp, log, log10, frexp, ldexp
Rounding Functions	ceil, floor
Absolute Value Functions	fabs
Modular Arithmetic Functions	fmod, modf
Comparison and Conversions	Comparison, integer and floating-point conversions

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12.2 Peripheral Driver Library

Microchip offers a free peripheral driver library that supports the setup and control of dsPIC30F hardware peripherals, including, but not limited to:

- Analog-to-Digital Converter
- Motor Control PWM
- Quadrature Encoder Interface
- UART
- SPI
- Data Converter Interface
- I^2C
- General Purpose Timers
- Input Capture
- Output Compare/Simple PWM
- CAN
- I/O Ports and External Interrupts
- Reset

In addition to the hardware peripherals, the library supports software generated peripherals, such as standard LCD drivers, which support a Hitachi style controller.

The peripheral library consist of more than 270 functions as well as several macros for simple tasks such as enabling and disabling interrupts. All peripheral driver routines are developed and optimized using the MPLAB C30 C Compiler. Electronic documentation accompanies the peripheral library to help you become familiar with and implement the library functions.

Key features of the dsPIC30F Peripheral Library include:

- A library file for each individual device from the dsPIC30F family, including functions corresponding to peripherals present in that particular device.
- C `include` files that let you take advantage of pre-defined constants for passing parameters to various library functions. There is an `include` file for each peripheral module.
- Since the functions are in the form of precompiled libraries, they can be called from a user application program written in either MPLAB C30 or dsPIC30F assembly language.
- Included C source code allows you to customize peripheral functions to suit your specific application requirements.
- Predefined constants in the C `include` files eliminate the need to refer to the details and structure of every Special Function Register while initializing peripherals or checking Status bits.

12.3 DSP Algorithm Library

The free DSP library supports multiple filtering, convolution, vector and matrix functions. Among the supported functions are:

- Cascaded Infinite Impulse Response (IIR) Filters
- Correlation
- Convolution
- Finite Impulse Response (FIR) Filters
- Windowing Functions
- FFTs
- LMS Filter
- Vector Addition and Subtraction
- Vector Dot Product
- Vector Power
- Matrix Addition and Subtraction
- Matrix Multiplication

Some DSP functions use double precision and floating point arithmetic. All DSP routines are developed and optimized in dsPIC30F assembly language and are callable from both assembly and C language. The Microchip MPLAB C30 and IAR C compilers are supported.

Key features of the DSP Algorithm Library include:

- 49 total functions
- Full compliance with the Microchip dsPIC30F C30 Compiler, Assembler and Linker
- Simple user interface – just one library file and one header file
- Functions are both C and assembly callable
- FIR filtering functions include support for Lattice, Decimating, Interpolating and LMS filters
- IIR filtering functions include support for Canonic, Transposed Canonic and Lattice filters
- FIR and IIR functions may be used with the filter files generated by the dsPIC30F Filter Design program
- Transform functions include support for in-place and out-of-place DCT, FFT and IFFT transforms
- Window functions include support for Bartlett, Blackman, Hamming, Hanning and Kaiser windows
- Support for Program Space Visibility
- Complete function profile information including register usage, cycle count and function size information
- Electronic documentation is included to help you comprehend and use the library functions

TABLE 12-4: FUNCTION EXECUTION TIMES

Function	Cycle Count Equation	Conditions(1)	Number of Cycles(2)	Execution Time @30 MIPS
Complex FFT(3)	-	N=64	3739	124.6 µs
Complex FFT(3)	-	N=128	8485	282.8 µs
Complex FFT(3)	-	N=256	19055	635.2 µs
Block FIR	53+N(4+M)	N=32, M=32	1205	40.2 µs
Block FIR Lattice	41+N(4+7M)	N=32, M=32	7337	244.6 µs
Block IIR Canonic	36+N(8+7S)	N=32, S=4	1188	39.6 µs
Block IIR Lattice	46+N(16+7M)	N=32, M=8	2350	78.3 µs
Matrix Add	20+3(C*R)	C=8, R=8	212	7.1 µs
Matrix Transpose	16+C(6+3(R-1))	C=8, R=8	232	7.7 µs
Vector Dot Product	17+3N	N=32	113	3.8 µs
Vector Max	19+7(N-2)	N=32	229	7.6 µs
Vector Multiply	17+4N	N=32	145	4.8 µs
Vector Power	16+2N	N=32	80	2.7 µs

Note 1: C = #columns, N = # samples, M = #taps, S = #sections, R = #rows

2: 1 cycle = 33 nanoseconds @30 MIPS

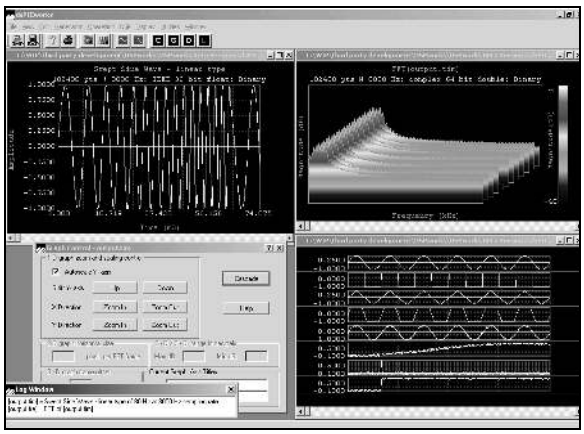
3: Complex FFT routine inherently prevents overflow

12.4 dsPICworks™ Data Analysis and DSP Software

dsPICworks is a free data analysis and signal processing package for use with Microsoft Windows 9x, NT, 2000 and XP platforms. It provides an extensive number of functions encompassing:

- Wide variety of signal generators – Sine, Square, Triangular, Window functions, Noise
- Extensive DSP functions – FFT, DCT, Filtering, Convolution, Interpolation
- Extensive arithmetic functions – Algebraic expressions, data-scaling, clipping etc.
- 1-D, 2-D and 3-D displays
- Multiple data quantization and saturation options
- Multi-channel data support
- Automatic “script file”-based execution options available for any user-defined sequence of dsPICworks functions
- File Import/Export interoperable with MPLAB IDE
- Digital filtering options support filters generated by dsPIC Filter Design
- ASM30 assembler file option to export data tables into dsPIC30F RAM.

FIGURE 12-1: dsPICworks Data Analysis and DSP Software



12.4.1 SIGNAL GENERATION:

dsPICworks™ Data Analysis and DSP Software supports an extensive set of signal generators including basic sine, square and triangle wave generators as well as advanced generators for window functions, unit step, unit sample, sine, exponential and noise functions. Noise, with specified distribution, can be added to any signal. Signals can be generated as 32 bit floating-point or as 16-bit fractional fixed point values for any desired sampling rate. The length of the generated signal is limited only by available disk space. Signals can be imported or exported from or to MPLAB file-register windows. Multi-channel data can be created by a set of multiplexing functions.

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12.4.2 DIGITAL SIGNAL PROCESSING (DSP) AND ARITHMETIC OPERATIONS:

dsPICworks Data Analysis and DSP Software has a wide range of DSP and arithmetic functions that can be applied to signals. Standard DSP functions include transform operations – FFT and DCT, convolution and correlation, signal decimation, signal interpolation sample rate conversion and digital filtering. Digital filtering is an important part of dsPICworks. It uses filters designed by the sister-application, dsPIC Filter Design, and applies them to synthesized or imported signals. dsPICworks also features special operations such as signal clipping, scaling, and quantization – all of which are vital in real practical analysis of DSP algorithms.

12.4.3 DISPLAY AND MEASUREMENT:

dsPICworks Data Analysis and DSP Software has a wide variety of display and measurement options. Frequency domain data may be plotted in the form of 2-dimensional 'spectrogram' and 3-dimensional 'waterfall' options. The signals can be measured accurately by a simple mouse-click. The log window shows current cursor coordinates as well as derived values such as difference from last position and signal frequency. Signal strength can be measured over a particular range of frequencies. Special support also exists for displaying multi-channel and multiplexed data. Graphs allow zoom options. The user can choose from a set of color scheme options to customize display settings.

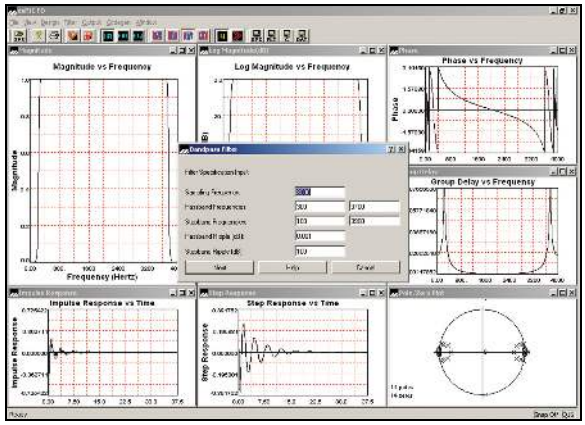
12.4.4 FILE IMPORT/EXPORT – MPLAB AND MPLAB ASM30 SUPPORT:

dsPICworks Data Analysis and DSP Software allows data to be imported from the external world in the form of ASCII-text or binary files. Conversely, it also allows data to be exported out in the form of files. dsPICworks supports all file formats supported by the MPLAB Import/Export Table. This feature allows the user to bring real-world data from MPLAB into dsPICworks for analysis. dsPICworks can also create ASM30 assembler files that can be included into the MPLAB workspace.

12.5 Digital Filter Design Software Utility

The Digital Filter Design tool for the dsPIC30F 16-bit Digital Signal Controllers makes designing, analyzing and implementing Finite Impulse Response (FIR) and Infinite Impulse Response (IIR) digital filters easy through a menu-driven, user-intuitive interface. This tool performs complex mathematical computations for filter design, provides superior graphical displays and generates comprehensive design reports. Desired filter frequency specifications are entered, and the tool automatically generates the filter code and coefficient files ready to use in the MPLAB® Integrated Development Environment (IDE). System analysis of the filter transfer function is supported with multiple generated graphs such as: magnitude, phase, group delay, log magnitude, impulse response and pole/zero locations.

FIGURE 12-2: DIGITAL FILTER DESIGN TOOL INTERFACE



Key features of the Digital Filter Design tool include:

Finite Impulse Response Filter Design

- Design Method Selection:
  - FIR Windows Design
  - FIR Equiripple Design (Parks-McClellan)
- Lowpass, Highpass, Bandpass and Bandstop filters
- FIR filters can have up to 513 taps

- The following window functions are supported:
  - Rectangular
  - Hanning (Hann)
  - Hamming
  - Triangular
  - Blackman
  - Exact Blackman
  - 3 Term Cosine
  - 3 Term Cosine with continuous 3rd Derivative
  - Minimum 3 Term Cosine
  - 4 Term Cosine
  - 4 Term Cosine with continuous 5th Derivative
  - Minimum 4 Term Cosine
  - Good 4 Term Blackman Harris
  - Harris Flat Top
  - Kaiser
  - Dolph-Tschebyscheff
  - Taylor
  - Gaussian
- Reports show design details such as window coefficients and Impulse Response prior to multiplying by the window function

Infinite Impulse Response Filter Design

- Lowpass, Highpass, Bandpass and Bandstop Filters
- Filter orders up to 10 for Lowpass and Highpass Filters
- Filter orders up to 20 for Bandpass and Bandstop Filters
- Five Analog Prototype Filters are available:
  - Butterworth
  - Tschebyscheff
  - Inverse Tschebyscheff
  - Elliptic
  - Bessel
- Digital Transformations are performed by Bilinear Transformation Method
- Reports show design details such as all transformations from normalized lowpass filter to desired filter

Code Generation Features

- Generated files are compliant with the Microchip dsPIC30F C30 Compiler, Assembler and Linker
- Choice of placement of coefficients in Program Space or Data Space
- C wrapper/header code generation

Graphs

- Magnitude Response vs. Frequency
- Log Magnitude vs. Frequency
- Phase Response vs. Frequency
- Group Delay vs. Frequency
- Impulse Response vs. Time (per sample)
- Step Response vs. Time (per sample)
- Pole and Zero Locations (IIR only)

12.6 Real-Time Operating Systems

Real-Time Operating System (RTOS) solutions for the dsPIC30F product family provide the necessary function calls and operating system routines to enable you to write efficient C and/or assembly code for multi-tasking applications. RTOS is especially suited for applications where program, and, more importantly, data memory resources, are limited. Configurable and optimized kernels support various RTOS application requirements.

The dsPIC30F RTOS solutions are three-tiered:

- CMX-RTX™ full-featured fully-preemptive multitasking RTOS
- CMX-Tiny+™ fully-preemptive scaled-down version of CMX-RTX
- CMX-Scheduler™ fully-preemptive, multitasking, mini RTOS (FREE)

12.6.1 CMX-RTX™

In some cases, well-structured linear programming is sufficient for a product. However, in most cases, programmers appreciate not having to worry about structuring their code to perform all necessary tasks in a timely manner. CMX-RTX helps by allowing tasks (pieces of code that do specific duties) to run quasi-concurrently. That is, tasks seem to run at the same time – doing many specific jobs simultaneously

CMX-RTX takes the headaches out of real-time programming. The software lets the programmer concentrate on the overall application while it takes care of the details. CMX-RTX lets you finish projects faster and more efficiently.

Some real-time operating systems offer only cooperative scheduling, which means that the running task is required to call the scheduler to perform a task switch. Others offer time slicing in which each task runs for a given period of time and then must switch tasks, regardless of conditions. Still others claim to be fully preemptive, yet they do not allow any interrupt to cause a preemption. All of these models will fail at one point or another.

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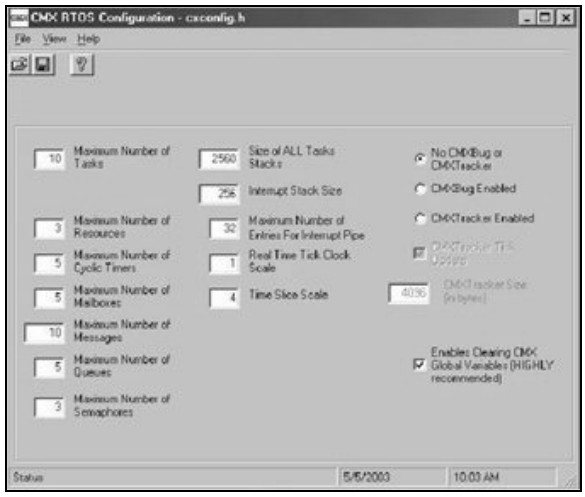
CMX-RTX allows a task of higher priority that is able to run (whether starting or resuming) to preempt the running task. The scheduler saves the context of the running (lower priority) task and restores the context of the higher priority task so that it is now running. A truly preemptive RTOS allows interrupts to cause an immediate task switch, which means that the interrupts now have the added ability of using the RTOS's functions.

FIGURE 12-3: CMX-RTX CONFIGURATION MANAGER



Key features of the CMX-RTX™ for dsPIC30F include:

- The smallest footprint
- The fastest context switch times
- The lowest interrupt latency times
- True preemption
- Scheduler and interrupt handler written in assembly for speed and code-size optimization
- Optional cooperative and time-slicing scheduling
- Nested interrupts
- All functions contained in a library
- Interrupt-callable functions
- Scalability
- Free source code provided
- Integrated with CMX-MicroNet™ for optional networking connectivity

FIGURE 12-4: CMX-TINY+ CONFIGURATION MANAGER

12.6.2 CMX-TINY+™

CMX-Tiny+ is a compact, real-time operating system that allows tasks to run quasi-concurrently, seeming to process multiple jobs simultaneously. CMX-Tiny+ has been especially designed to offer such a small Flash/RAM footprint that it can be used with only the on-board Flash/RAM of the dsPIC30F as a single-chip solution. Based upon a scaled-down version of the popular CMX-RTX, CMX-Tiny+ retains most of the power of CMX-RTX, including its more frequently used functions.

Like its larger counterpart, CMX-Tiny+ takes the headaches out of real-time programming. The software lets the programmer concentrate on the overall embedded application while taking care of the real-time program details. The result is projects that are finished faster and more efficiently.

CMX-Tiny+ allows a task of higher priority that is ready to run (whether starting or resuming) to preempt the running task. The scheduler saves the context of the running (lower priority) task and restores the context of the higher priority task so that it is now running. With CMX-Tiny+, an interrupt can immediately preempt the current task to ensure that a higher priority application condition is handled. In other words, CMX-Tiny+ gives interrupts the added capability of influencing the RTOS.

Key features of the CMX-Tiny+™ for dsPIC30F include:

- Extremely small Flash/RAM footprint
- Truly preemptive RTOS
- Low-Power mode supported
- Full source code with every purchase
- Free technical support and updates
- Low, economical pricing
- No royalties on shipped products
- Backward compatible with CMX-Scheduler™
- Integrated with CMX-MicroNet™ for optional networking connectivity

12.6.3 CMX-SCHEDULER™

CMX-Scheduler is the result of a special collaboration between CMX and Microchip. Available in object code only, CMX-Scheduler is available for FREE to embedded systems designers using the dsPIC microcontrollers. CMX-Scheduler is specially designed for developers whose designs do not require a full-blown RTOS and/or who are wondering if a kernel might help their application. The perfect entry-level kernel, CMX-Scheduler, is intuitive to use and easy to implement.

CMX-Scheduler offers many growth paths for future designs. User applications developed with the CMX-Scheduler kernel are upwardly compatible with the popular CMX-Tiny+™ or CMX-RTX™. CMX-Scheduler also is tightly integrated with the unique CMX-MicroNet™ TCP/IP stack for those applications that require networking connectivity.

CMX-Scheduler software and documentation is delivered in electronic format and is freely licensed for unlimited product usage on the dsPIC devices.

Key features of the CMX-Scheduler include:

- FREE for use on any dsPIC device
- Easy to learn and use
- Truly preemptive kernel
- Supports up to five tasks
- Fast performance
- Free bug fixes and updates
- No royalties on shipped products
- Compatible with CMX-Tiny+ and CMX-RTX
- Complete electronic documentation
- Integrated with CMX-MicroNet for optional networking connectivity

12.7 TCP/IP Stack (CMX-Micronet™)

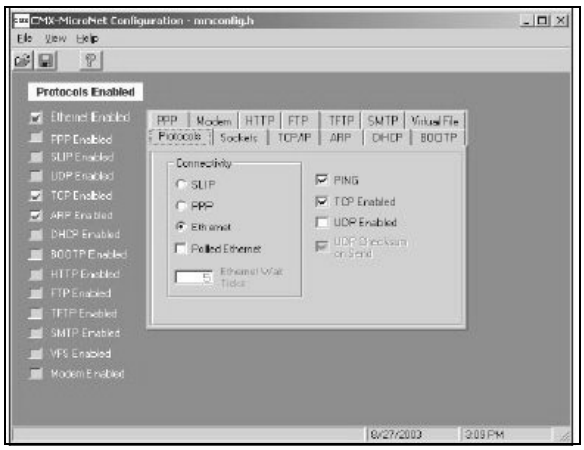
CMX-Micronet is an embedded TCP/IP stack that is specifically designed for optimized use of Flash and RAM resources on dsPIC30F devices. The software runs directly on the dsPIC30F with no gateways or PCs required. The stack can be run in Stand-Alone mode or work in conjunction with an RTOS. Using only industry standard protocols, CMX-MicroNet offers true TCP/IP networking via Direct, Dial Up or Ethernet connectivity and Wireless Ethernet (802.11b) as well.

Up to 127 sockets can be open at a time. They can be ethernet sockets and/or either PPP or SLIP sockets. PPP and SLIP cannot be used at the same time. An HTTP Web server, FTP server, SMTP client and DHCP client are also available. The RS-232 link, if used, can either be a direct cable link or through a modem.

Key features of CMX-MicroNet include:

- Tested and proven with hundreds of design wins around the world
- Extremely small Flash/RAM requirements
- Software solution does not require additional processor
- Web pages may contain CGI calls and Server Side Includes
- FTP files, including new firmware
- Send e-mail
- Can serve up Java applets
- No proprietary protocols
- Runs stand-alone or with any RTOS
- Economical one-time fee
- Full source code provided
- No royalties on shipped products
- Excellent documentation and support

FIGURE 12-5: CMX-MICRONET USER INTERFACE



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Supported Protocols

- TCP
- PPP
- UDP
- SLIP
- IP
- HTTP Web Server
- DHCP
- FTP
- TFTP
- SMTP

Connectivity

- Ethernet
- Wireless Ethernet
- Dial Up
- Direct

Memory Requirements

Flash	
UDP/IP + core	4470 bytes
TCP/IP + core	7827 bytes
UDP/TCP/IP + core	8685 bytes
PPP	6681 bytes
Modem	447 bytes
HTTP Server	3888 bytes
Virtual File	885 bytes
Ethernet	2652 bytes
DHCP Client	2202 bytes
FTP Server	3657 bytes
TFTP Client	723 bytes
BOOTP	684 bytes
SMTP	1918 bytes
Utility	1314 bytes
RAM (not including buffer sizes)	
UDP/SLIP	56 bytes
TCP/HTTP/PPP	304 bytes
Ethernet	38 bytes

12.8 Soft Modem Application Library

Microchip offers V.22/V.22bis (1200/2400 bps) and V.32/V.32bis (9600/14400 bps) ITU-T specifications to support a range of “connected” applications.

Applications that will benefit from these modem specifications include:

- Internet-enabled home security systems
- Internet-connected power, gas and water meters
- Internet-connected vending machines
- Smart Appliances
- Industrial Monitoring
- POS Terminals
- Set Top Boxes
- Drop Boxes
- Fire Panels

The ITU-T specification modules are written in C and Assembly language, yielding optimal performance. Some specific dsPIC30F hardware peripherals and key transmitter and receiver filtering routines use assembly language to optimize code size and execution time.

Electronic documentation accompanies the modem library to help you become familiar with and implement the library functions.

12.9 CAN Driver Library

Microchip offers a CAN driver library that supports the dsPIC30F CAN peripheral. Some of the CAN functions supported include:

- Initialize CAN Module
- Set CAN Operational Mode
- Set CAN Baud Rate
- Set CAN Mask
- Set CAN Filter
- Send CAN Message
- Receive CAN Message
- Abort CAN Sequence
- Provide error notification

All CAN driver routines are developed and optimized in dsPIC30F C language and are callable from C language. Support for the Microchip MPLAB C30 C Compiler is provided.

Electronic documentation accompanies the CAN library to help you become familiar with and implement the library functions.

Vector Informatik GmbH, a dsPIC30F development partner, has created a dsPIC30F architecture version of their CANbedded® tool, along with various support utilities.

12.10 OSEK Operating Systems

The dsPIC30F product family supports Operating Systems for the OSEK/VDX vehicle software standard. The functionality of OSEK “Offene Systeme und deren Schnittstellen für die Elektronik im Kraftfahrzeug” (open systems and the corresponding interfaces for automotive electronics) is harmonized with VDX “Vehicle Distributed eXecutive” yielding OSEK/VDX.

Structured and modular RTOS software implementations are provided based on standardized interfaces and protocols. Structured and modular implementations provide for portability and extendability for distributed control units for vehicles.

Microchip also provides Internal and External CAN driver support. The physical layer is integrated into the communication controller’s hardware and is not covered by the OSEK specifications.

Vector Informatik GmbH has created a dsPIC30F architecture version of their osCAN® operating system, along with various support utilities.

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13.0 dsPIC30F HARDWARE DEVELOPMENT BOARDS

Microchip provides several hardware development boards that help you quickly prototype and validate key design requirements. Each board features key dsPIC30F peripherals and supports Microchip's MPLAB In-Circuit Debugger (ICD 2) tool for cost effective debugging and programming of the dsPIC30F device. These boards are shown in Table 13-1.

TABLE 13-1: HARDWARE DEVELOPMENT BOARDS

	Development Tool	Description	Part #	From	List Price*
Development Boards and Reference Designs	**80-Pin Starter Demo Board** (see 13.1)	dsPICDEM 80-pin Starter Demonstration Board dsPIC30F6014A General Purpose device	DM300019	Microchip	$79.99
	28-Pin Starter Demo Board (see 13-2)	dsPICDEM Starter Demonstration Board with 28-pin dsPIC30F2010 Motor Control device	DM300017	Microchip	$79
	General Purpose Development (see 13.3)	dsPICDEM™ 1.1 Development Board for 80L TQFP devices	DM300014	Microchip	$299
	Motor Control and Power Conversion Development (see 13.4)	dsPICDEM MC1 Motor Control Development Board	DM300020	Microchip	$300
		dsPICDEM MC1H 3-Phase High-Voltage Power Module	DM300021	Microchip	$800
		3-Phase ACIM High-Voltage Motor (208/460V)	AC300021	Microchip	$120
		dsPICDEM MC1L 3-Phase Low-Voltage Power Module	DM300022	Microchip	$700
		3-Phase BLDC Low-Voltage Motor (24V)	AC300020	Microchip	$120
	Connectivity Development (see 13.5)	dsPICDEM.net™ 1 with FCC/JATE and Ethernet NIC support (Global compliant)	DM300004-1	Microchip	$389
		dsPICDEM.net 2 with PSTN and Ethernet NIC support (Global compliant)	DM300004-2	Microchip	$389
Plug-in Samples	**Plug-in Sample** (see 13.6)	Daughter PC board with 80-pin dsPIC30F6010 motor control MCU sample. Easy to plug in and remove from development board.	MA300013	Microchip	$25
		Daughter PC board with 80-pin dsPIC30F6014A general purpose MCU sample. Easy to plug in and remove from development board.	MA300014	Microchip	$25

* Prices are subject to change without notice.

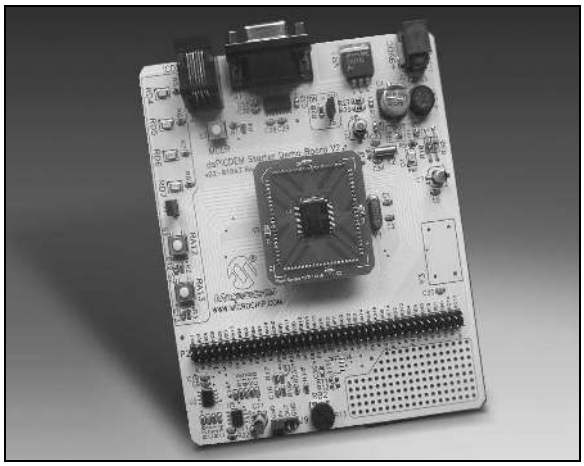
13.1 dsPICDEM™ 80-Pin Starter Development Board

This development board offers a very economical way to evaluate both the dsPIC30F and dsPIC33F General Purpose and Motor Control Family devices. This board is an ideal prototyping tool to help you quickly develop and validate key design requirements.

Some key features and attributes of the dsPICDEM 80-Pin Starter Development Board include:

- Includes an 80-pin dsPIC30F6014A plug-in module (MA300014)
- Power input from 9V supply
- Selectable voltage regulator outputs of 5V and 3.3V
- LEDs, switches, potentiometer, UART interface
- A/D input filter circuit for speech band signal input
- On-board DAC and filter for speech band signal output
- Circuit prototyping area
- Assembly language demonstration program and tutorial
- Can accommodate 80-pin dsPIC30F6010 plug-in module (MA300013)
- Can accommodate 100 to 80-pin adapter dsPIC33F plug-in module (MA330012)

FIGURE 13-1: dsPICDEM™ 80-PIN STARTER DEVELOPMENT BOARD



13.2 dsPICEM 28-Pin Starter Demo Board

The dsPICDEM 28-Pin Starter Demo Board is a development kit and evaluation tool for the dsPIC30F2010 High-Performance Digital Signal Controller. The following items comprise the dsPICDEM 28-Pin Starter Demo Board Development Kit:

- The dsPICDEM 28-Pin Starter Demo Board printed circuit board (see Figure 13-3)
- A preprogrammed dsPIC30F2010 device
- The dsPICDEM 28-Pin Starter Demo Board CD-ROM containing this manual, dsPIC30F documentation and demonstration program code

The dsPICDEM 28-Pin Starter Demo Board is a simple tool that allows you to begin development with dsPIC30F devices.

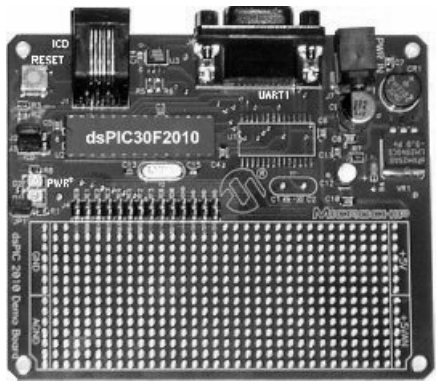
Development board power includes an on-board +5V regulator for V_{DD} and AV_{DD} with direct input from 9V AC or DC wall adapter, a 9V DC power source input jack for the development board and a LED power-on indicator.

MPLAB ICD 2 Connections include an MPLAB ICD 2 programming connector and pad locations for 28-pin SOIC or SDIP packages. Also included are a single RS-232 communication channel, 7.37 MHz crystal for dsPIC device clocking, and two crystal locations on the board to support either SDIP or SOIC packages.

Other features include:

- Reset push button for resetting the dsPIC device
- LED connected to pin RD0 for status indicator
- All device I/O pins are brought out to a header for test point and prototyping access
- Prototype area for user hardware

FIGURE 13-2: dsPICDEM 28-PIN STARTER DEMO BOARD



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13.3 dsPICDEM 1.1 Development Board

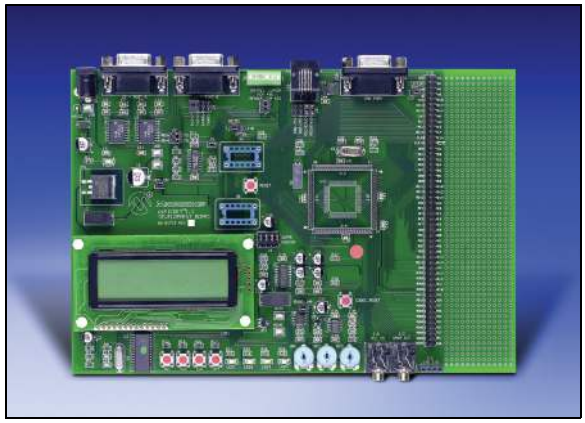
The dsPICDEM 1.1 Development Board is a low cost development tool that lets you familiarize yourself with the dsPIC30F 16-bit architecture, high performance peripherals and powerful instruction set. This development board is an ideal prototyping tool to help you quickly develop and validate key design requirements.

Some key features and attributes of the dsPICDEM 1.1 development board include:

- Supports dsPIC30F6014A device
- CAN communication channel
- RS-232 and RS-485 communication channels
- Voice band codec interface with line in/out jacks
- In-Circuit Debugger interface (MPLAB ICD 2)
- ICE 4000 Emulator interface
- Microchip temperature sensor
- Microchip Digital Potentiometer
- 122x32 Dot Addressable LCD
- General purpose prototyping area
- Various LEDS, switches and potentiometers

The general purpose development board is shipped with a 9V power supply, RS-232 I/O cable, preprogrammed dsPIC30F device, example software and appropriate documentation to enable you to exercise the development board demonstration programs.

FIGURE 13-3: dsPICDEM 1.1 DEVELOPMENT BOARD



13.4 Motor Control Development Board

The dsPIC30F Motor Control Development Board provides three main components for quick prototyping and validation of BLDC, PMAC and ACIM applications:

- dsPIC30F Motor Control Main Board
- 3-phase Low-Voltage Power module
- 3-phase High-Voltage Power module

The main control board supports the dsPIC30F6010 device, various peripheral interfaces and a custom interface header system, which allows different motor power modules to be connected to the PCB. The control board also has connectors for mechanical position sensors, such as incremental rotary encoders and Hall effect sensors, and a breadboard area for custom circuits. The main control board receives its power from a standard plug-in transformer.

The Low-Voltage Power module is optimized for 3-phase motor applications that require a DC bus voltage less than 50 volts and can deliver up to 400 watts power output. The 3-phase Low-Voltage Power module is intended to power BLDC and PMAC motors.

The High-Voltage Power module is optimized for 3-phase motor applications that require DC bus voltages up to 400 volts and can deliver up to 1 Kw power output. The high-voltage module has an active power factor correction circuit that is controlled by the dsPIC30F device. This power module is intended for AC induction motor and power inverter applications.

Both power modules have automatic Fault protection and the high-voltage module is electrically isolated from the control interface. Both power module boards provide pre-conditioned voltage and current signals to the main control board. All position feedback devices that are isolated from the motor control circuitry, such as incremental encoders, Hall effect sensors or tachometer sensors, can be directly connected to the main control board. Both modules are equipped with motor braking circuits.

Some key features and attributes of the motor control main development board are:

- dsPIC30F Motor Control Main Board supporting the dsPIC30F6010A
- RS-232 and RS-485 interface channels
- 2x16 LCD
- In-Circuit Debugger interface (MPLAB ICD 2)
- ICE 4000 Emulator interface
- General purpose prototyping area
- Custom interface header system
- Various LEDs, switches and potentiometers

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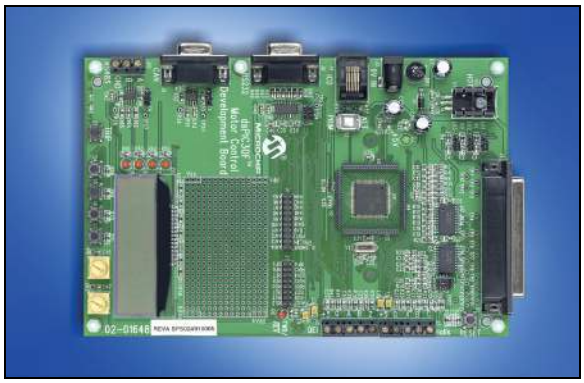
FIGURE 13-4: dsPIC30F MOTOR CONTROL DEVELOPMENT SYSTEM



The motor control development system is shipped with a 9V power supply for the control board, RS-232 I/O cable, pre-programmed dsPIC30F device, example software and documentation that allows you to exercise the development board demo programs. A list of motors that are compatible with the development system is also provided to facilitate rapid evaluation.

13.5 dsPICDEM.net™ Connectivity Development Board

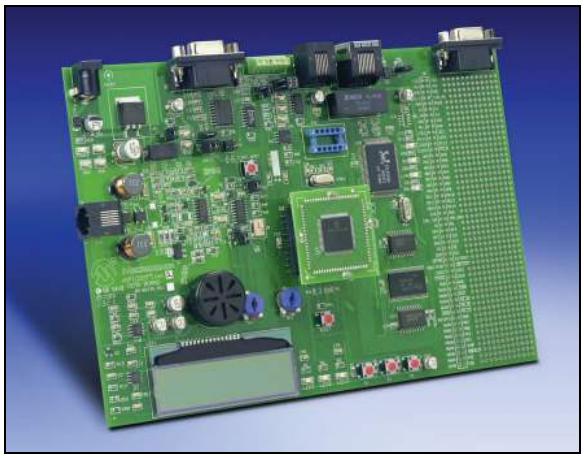
The dsPICDEM.net Connectivity Development Board provides you with a basic platform for developing and evaluating various connectivity solutions, implementing TCP/IP protocol layers, combined with V.32/V.32bis and V.22/V.22bis ITU-T specifications over PSTN or Ethernet communication channels.

Some key features and attributes of the dsPICDEM.net development board are:

- Supports dsPIC30F6014A device
- 10-Base T Ethernet support
- PSTN interface with DAA/AFE
- RS-232 and RS-485 communication channels
- In-Circuit Debugger interface (MPLAB ICD 2)
- ICE 4000 Emulator interface
- Microchip temperature sensor
- Microchip Dual Channel Digital Potentiometer
- 2x16 LCD
- General purpose prototyping area
- Various LEDs, switches and potentiometers
- External 64K x 16 SRAM
- External EE memory for storing HTML pages
- Expansion header for user applications

The connectivity development board is shipped with a 9V power supply, RS-232 I/O cable, pre-programmed dsPIC30F devices with example connectivity software and appropriate documentation to enable you to exercise the development board connectivity demo program.

FIGURE 13-5: dsPICDEM.net™ CONNECTIVITY DEVELOPMENT BOARD



13.6 Plug-in Modules

The various dsPIC30F development boards may use the plug-in modules for the dsPIC30F silicon devices. Since the boards support the ICE 4000 Emulator Device Adapter through the use of header pins on the PCB, they also are used to provide flexibility for the replacement of the dsPIC30F silicon. There are presently two different plug-in sample types that support the 80-pin TQFP package types, for general purpose (dsPIC30F6014A) and motor control dsPIC30F6010A samples. The use of plug-in samples is considered to be an interim development board mechanization.

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APPENDIX A: DEVICE I/O PINOUTS AND FUNCTIONS FOR GENERAL PURPOSE AND SENSOR FAMILY

Table A-1 provides a brief description of device I/O pinouts and functions that can be multiplexed to a port pin. Multiple functions may exist on one port pin. When multiplexing occurs, the peripheral module's functional requirements may force an override of the data direction of the port pin.

TABLE A-1: PINOUT I/O DESCRIPTIONS

Pin Name	Pin Type	Input Buffer Type	Description
AN0-AN15	I	Analog	Analog input channels. AN0 and AN1 are also used for device programming data and clock inputs, respectively.
AVDD	P	P	Positive supply for Analog module.
AVSS	P	P	Ground reference for Analog module.
CLKI	I	ST/CMOS	External clock source input. Always associated with OSC1 pin function.
CLKO	O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSC2 pin function.
CN0-CN23	I	ST	Input change notification inputs. Can be software programmed for internal weak pull-ups on all inputs.
COFS	I/O	ST	Data Converter Interface frame synchronization pin.
CSCK	I/O	ST	Data Converter Interface serial clock input/output pin.
CSDI	I	ST	Data Converter Interface serial data input pin.
CSDO	O	—	Data Converter Interface serial data output pin.
C1RX	I	ST	CAN1 bus receive pin.
C1TX	O	—	CAN1 bus transmit pin.
C2RX	I	ST	CAN2 bus receive pin.
C2TX	O	—	CAN2 bus transmit pin.
EMUD	I/O	ST	Primary data I/O pin for ICD Communication Channel.
EMUC	I	ST	Primary clock input pin for ICD Communication Channel.
EMUD1	I/O	ST	Alternate 1 data I/O pin for ICD Communication Channel.
EMUC1	I	ST	Alternate 1 clock input pin for ICD Communication Channel.
EMUD2	I/O	ST	Alternate 2 data I/O pin for ICD Communication Channel.
EMUC2	I	ST	Alternate 2 clock input pin for ICD Communication Channel.
EMUD3	I/O	ST	Alternate 3 data I/O pin for ICD Communication Channel.
EMUC3	I	ST	Alternate 3 clock input pin for ICD Communication Channel.
IC1-IC8	I	ST	Capture inputs 1 through 8.
INT0	I	ST	External interrupt 0.
INT1	I	ST	External interrupt 1.
INT2	I	ST	External interrupt 2.
INT3	I	ST	External interrupt 3.
INT4	I	ST	External interrupt 4.
LVDIN	I	Analog	Low Voltage Detect input.
$\overline{\text{MCLR}}$	I/P	ST	Master Clear (Reset) input or programming voltage input. This pin is an active low Reset to the device.
OCFA	I	ST	Compare Fault A input (for Compare channels 1, 2, 3 and 4).
OCFB	I	ST	Compare Fault B input (for Compare channels 5, 6, 7 and 8).
OC1-OC8	O	—	Compare outputs 1 through 8.
OSC1	I	ST/CMOS	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise.
OSC2	I/O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.

Legend: CMOS = CMOS compatible input or output Analog = Analog input
ST = Schmitt Trigger input with CMOS levels O = Output I = Input P = Power

TABLE A-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Type	Input Buffer Type	Description
PGD PGC	I/O I	ST ST	In-Circuit Serial Programming data input/output pin. In-Circuit Serial Programming clock input pin.
RA6-RA7 RA9-RA10 RA12-RA15	I/O I/O I/O	ST ST ST	PORTA is a bidirectional I/O port.
RB0-RB15	I/O	ST	PORTB is a bidirectional I/O port.
RC1-RC4 RC13-RC15	I/O I/O	ST ST	PORTC is a bidirectional I/O port.
RD0-RD15	I/O	ST	PORTD is a bidirectional I/O port.
RF0-RF8	I/O	ST	PORTF is a bidirectional I/O port.
RG0-RG3 RG6-RG9 RG12-RG15	I/O I/O I/O	ST ST ST	PORTG is a bidirectional I/O port.
SCK1 SDI1 SDO1 $\overline{SS1}$ SCK2 SDI2 SDO2 $\overline{SS2}$	I/O I O I I/O I O I	ST ST — ST ST ST — ST	Synchronous serial clock input/output for SPI1. SPI1 Data In. SPI1 Data Out. SPI1 Slave Synchronization. Synchronous serial clock input/output for SPI2. SPI2 Data In. SPI2 Data Out. SPI2 Slave Synchronization.
SCL SDA	I/O I/O	ST ST	Synchronous serial clock input/output for I^2C. Synchronous serial data input/output for I^2C.
SOSCI SOSCO	I O	ST/CMOS —	32 kHz low-power oscillator crystal input; CMOS otherwise. 32 kHz low-power oscillator crystal output.
T1CK T2CK T3CK T4CK T5CK	I I I I I	ST ST ST ST ST	Timer1 external clock input. Timer2 external clock input. Timer3 external clock input. Timer4 external clock input. Timer5 external clock input.
U1RX U1TX U1ARX U1ATX U2RX U2TX	I O I O I O	ST — ST — ST —	UART1 Receive. UART1 Transmit. UART1 Alternate Receive. UART1 Alternate Transmit. UART2 Receive. UART2 Transmit.
V_{DD}	P	—	Positive supply for logic and I/O pins.
V_{SS}	P	—	Ground reference for logic and I/O pins.
V_{REF+}	I	Analog	Analog Voltage Reference (High) input.
V_{REF-}	I	Analog	Analog Voltage Reference (Low) input.

Legend: CMOS = CMOS compatible input or output Analog = Analog input
ST = Schmitt Trigger input with CMOS levels O = Output I = Input P = Power

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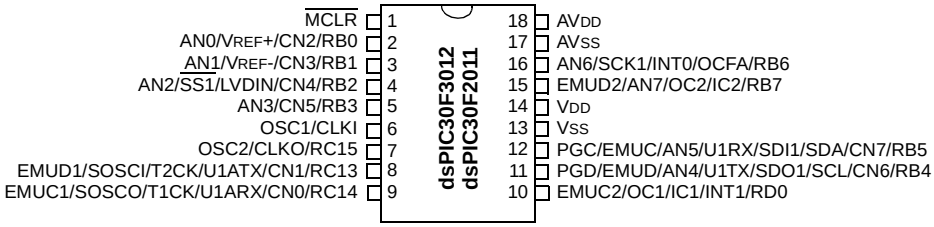
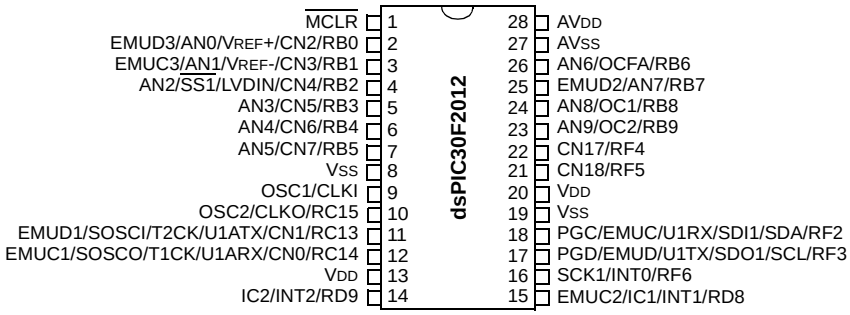
Pin Diagrams

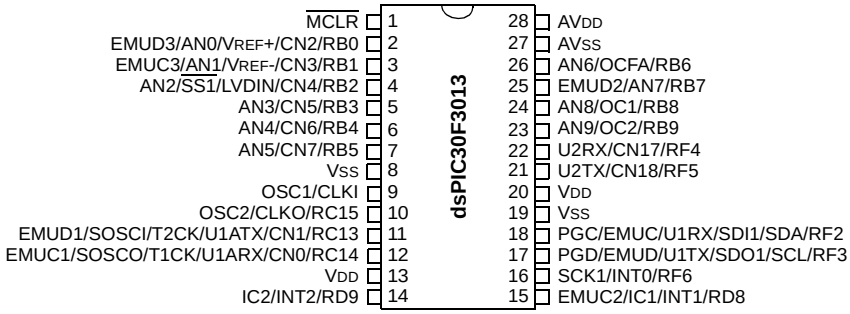
18-Pin PDIP and SOIC



28-Pin PDIP and SOIC

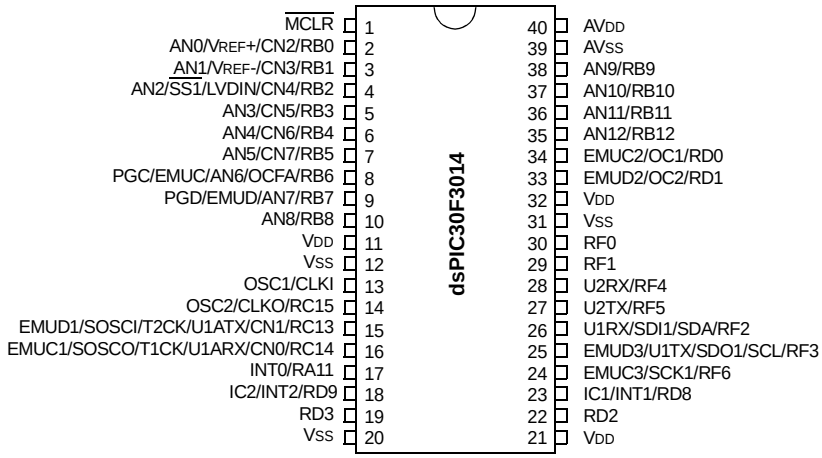


28-Pin SDIP and SOIC

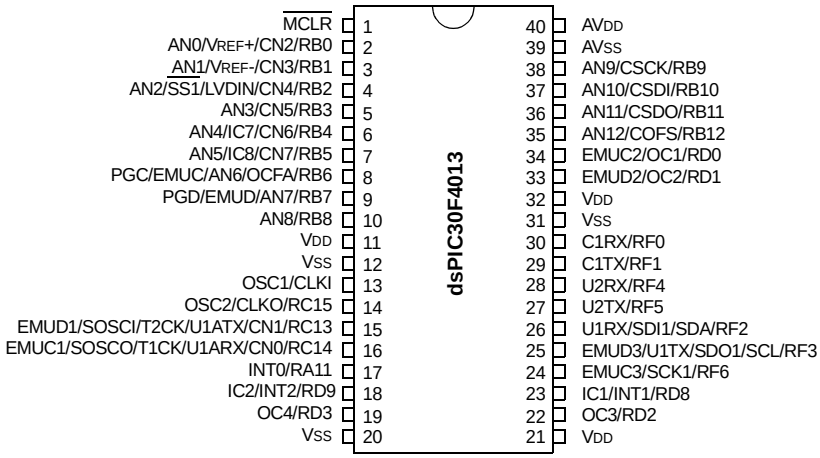


Pin Diagrams (Continued)

40-Pin PDIP



40-Pin PDIP



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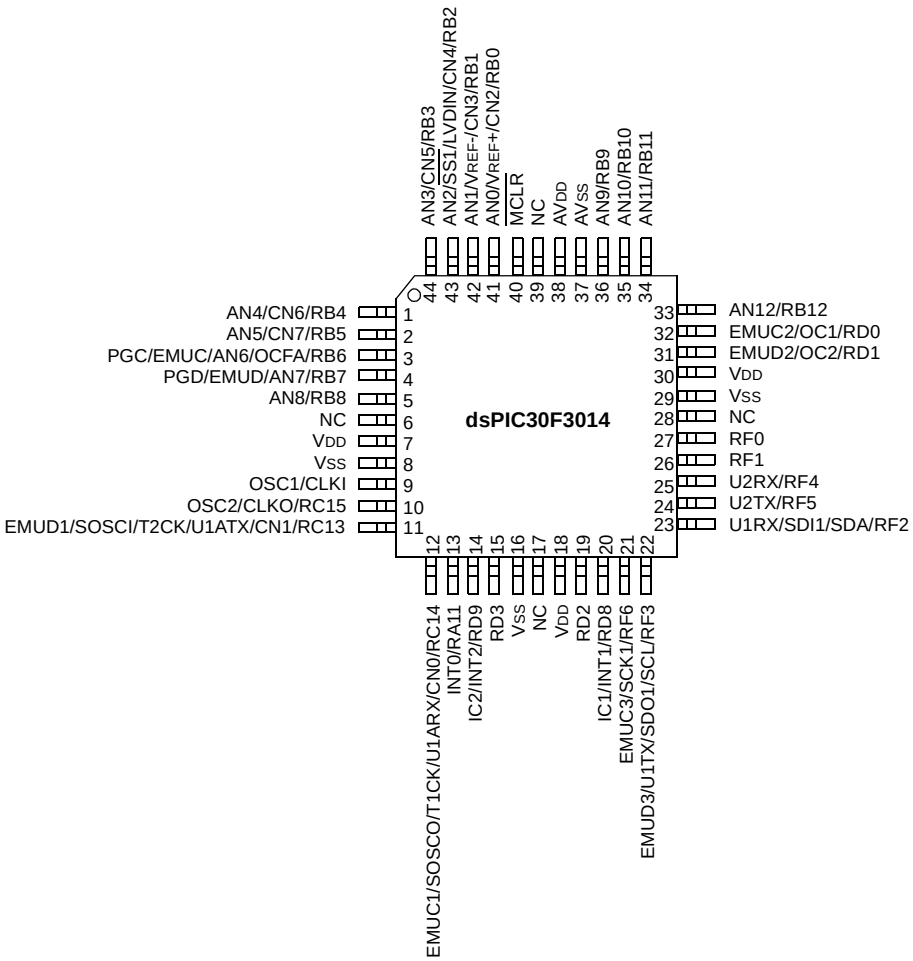
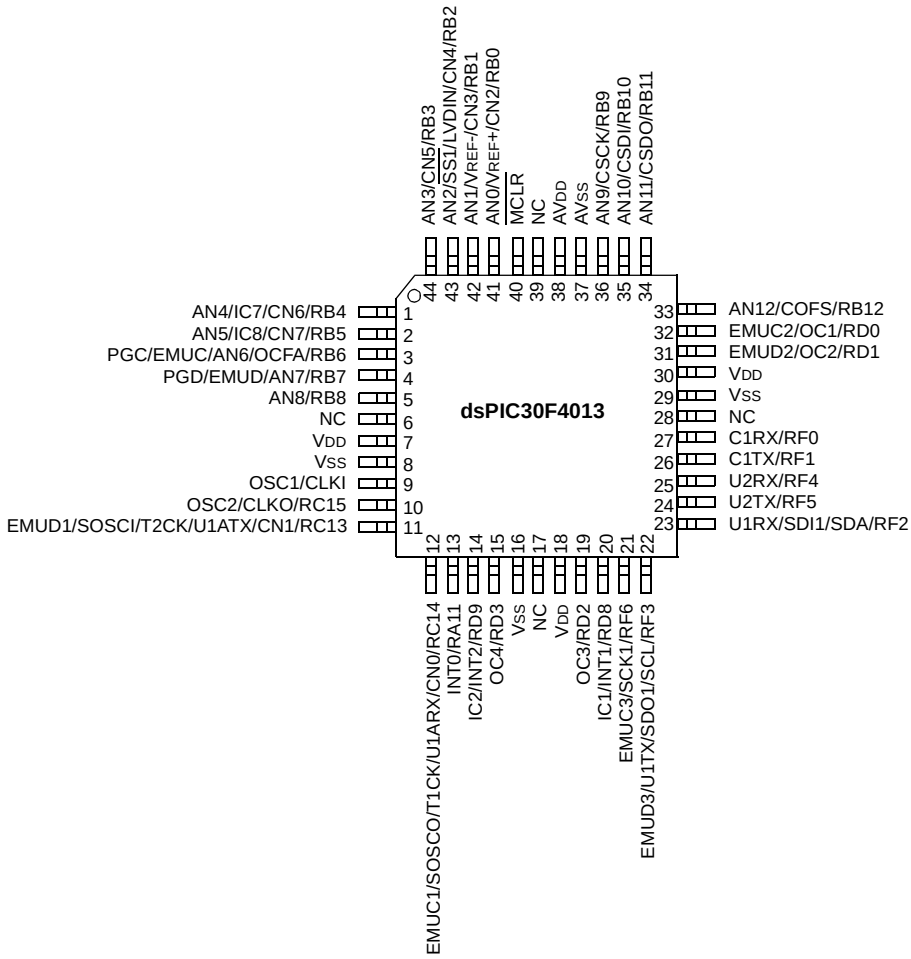
Pin Diagrams (Continued)

44-Pin TQFP



Pin Diagrams (Continued)

44-Pin TQFP



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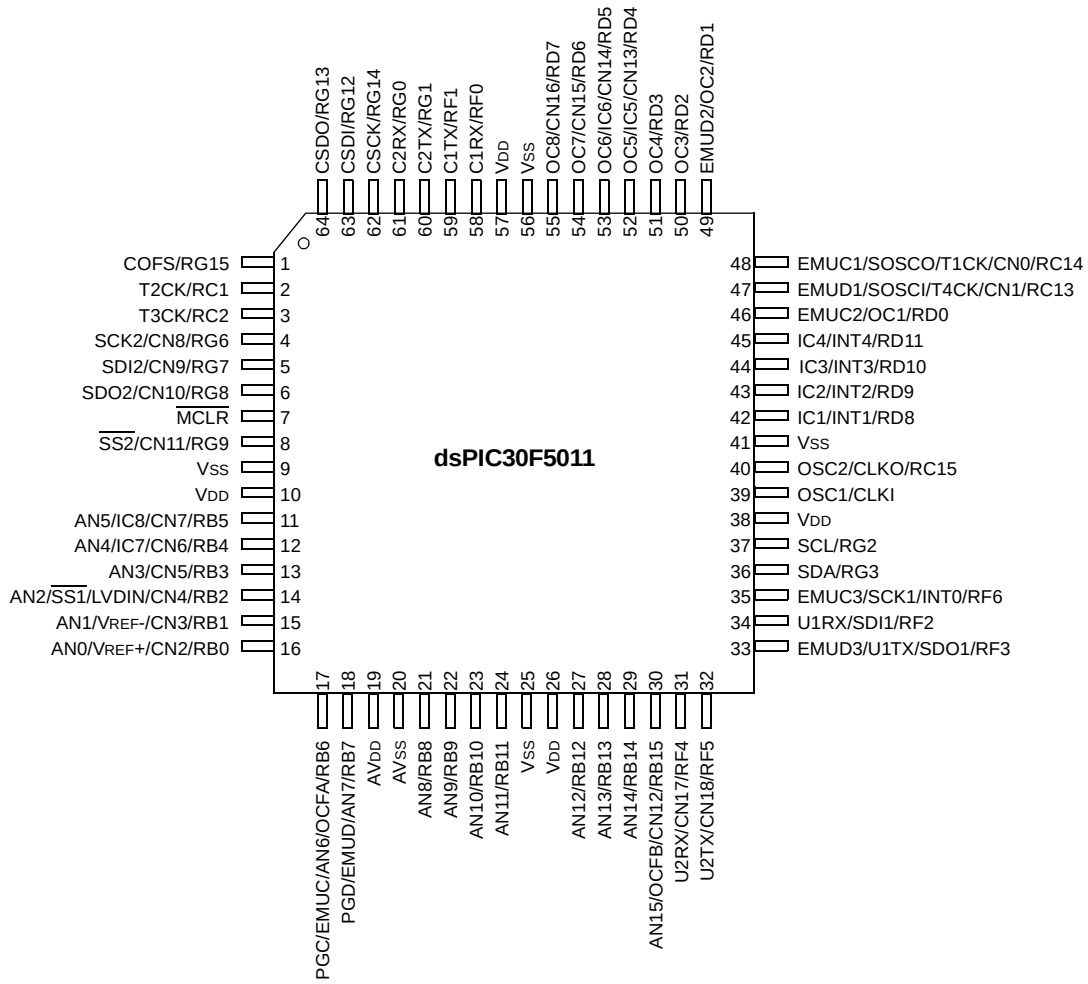
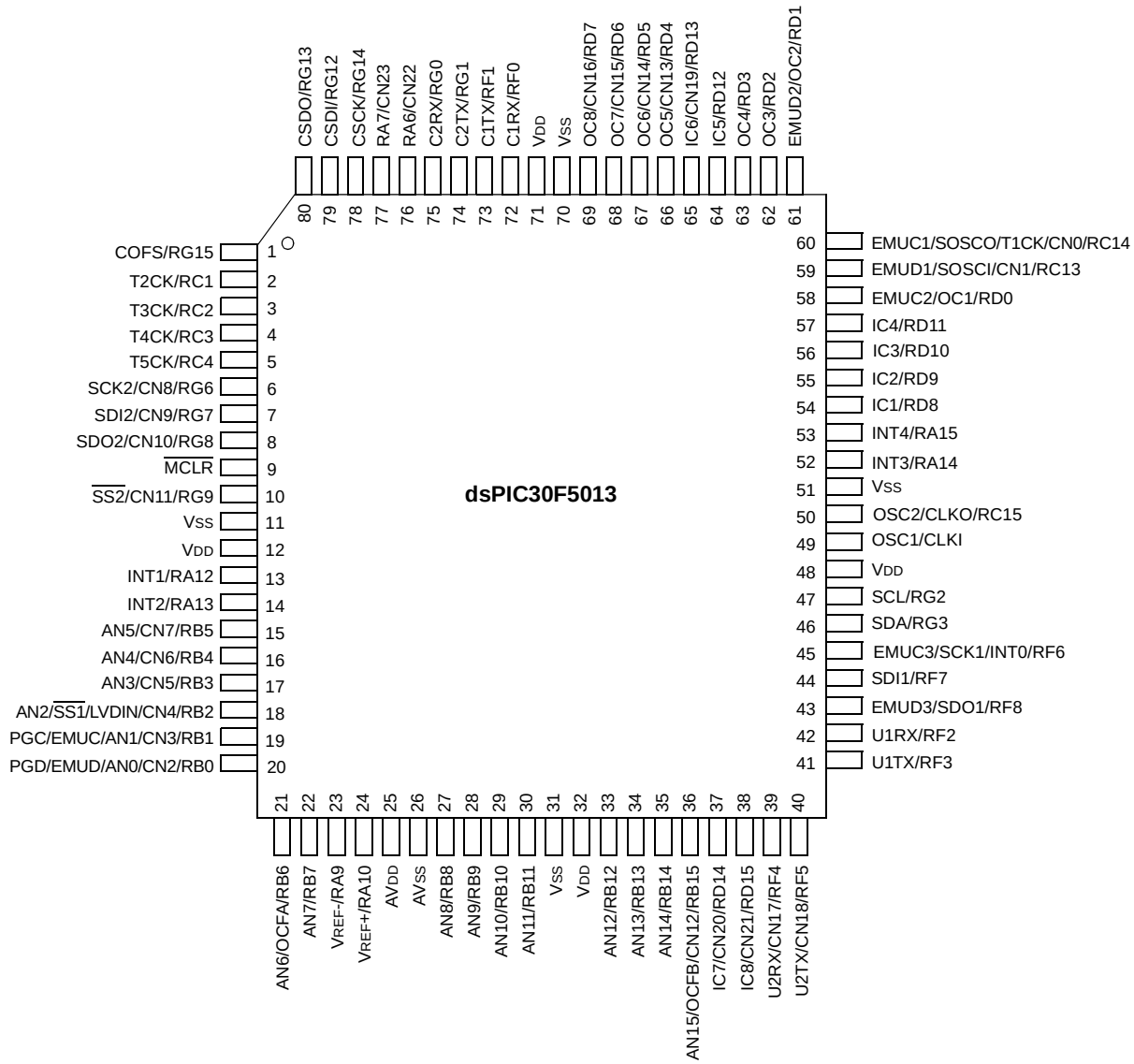
Pin Diagrams (Continued)

64-Pin TQFP



Pin Diagrams (Continued)

80-Pin TQFP



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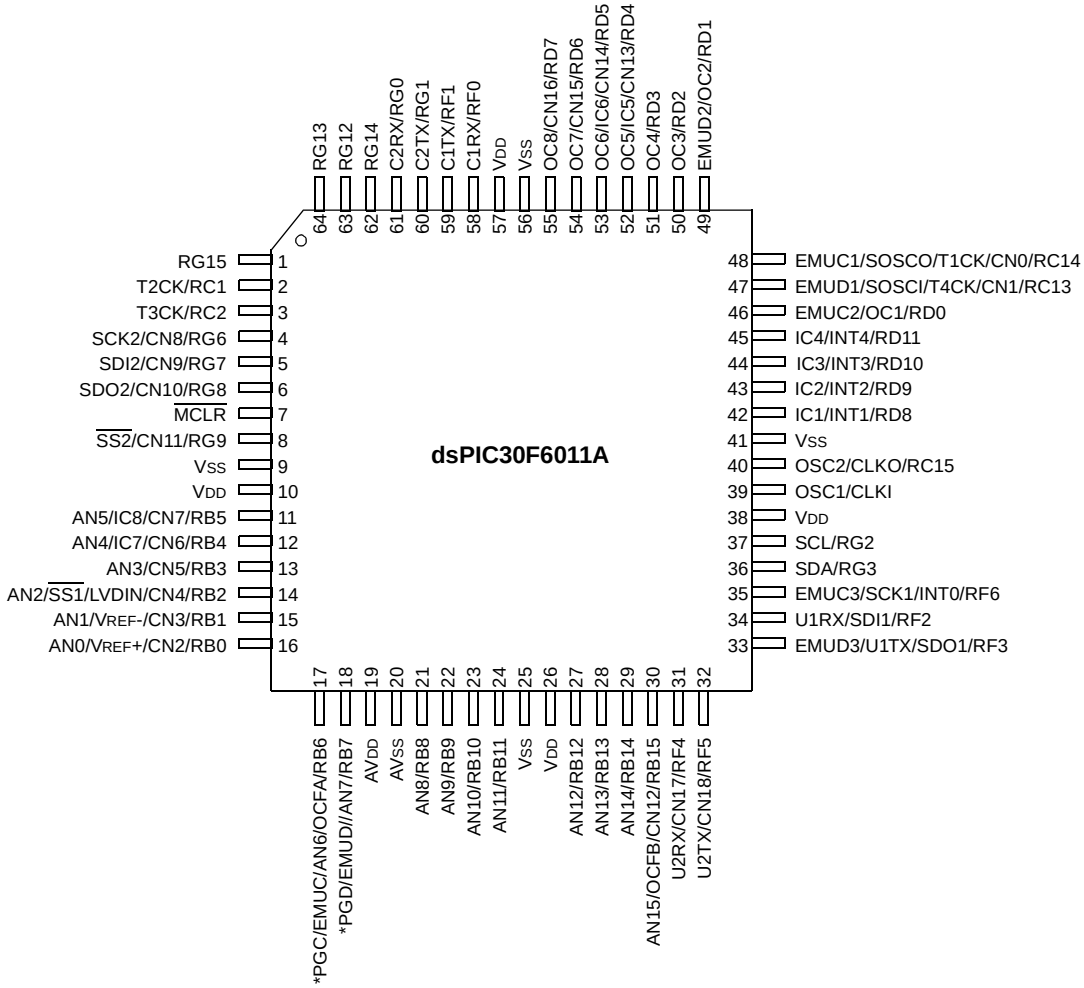
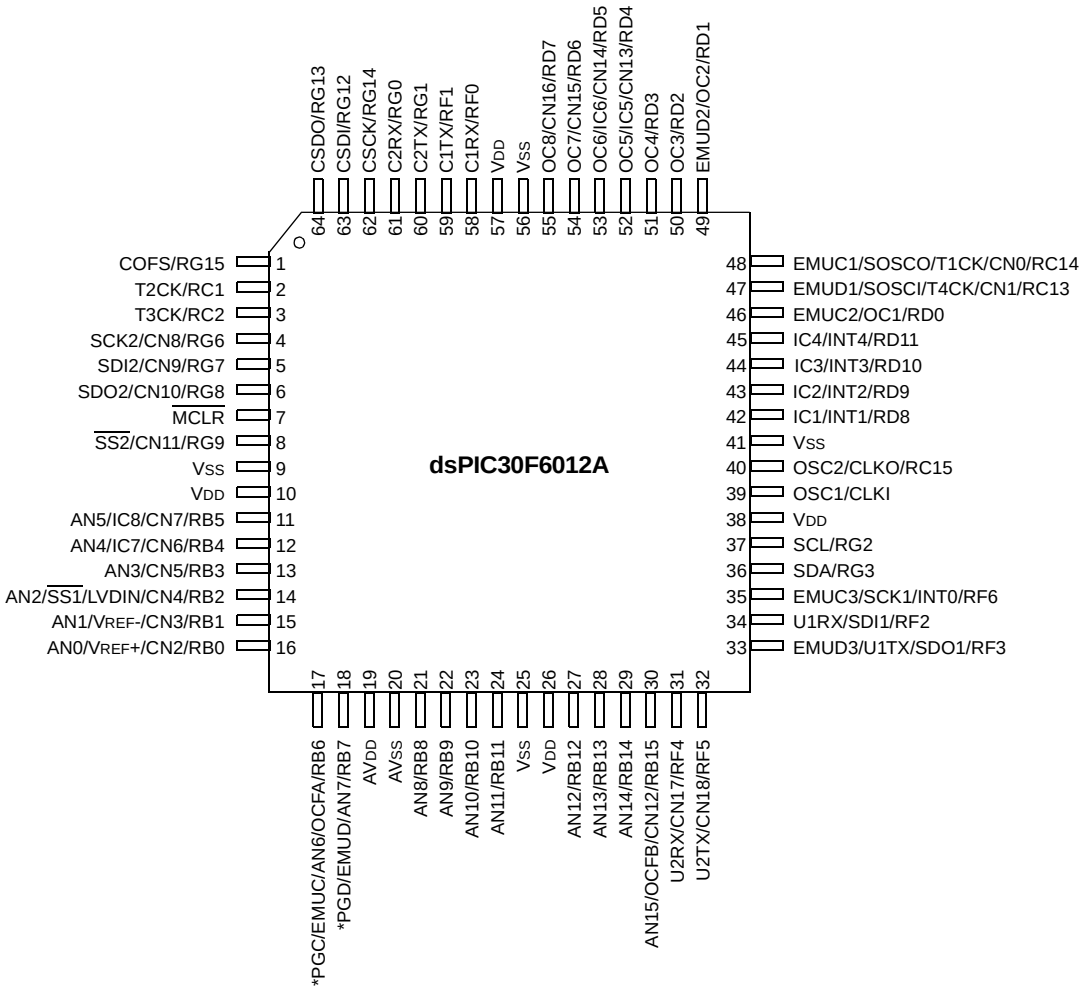
Pin Diagrams (Continued)

64-Pin TQFP



Pin Diagrams (Continued)

64-Pin TQFP



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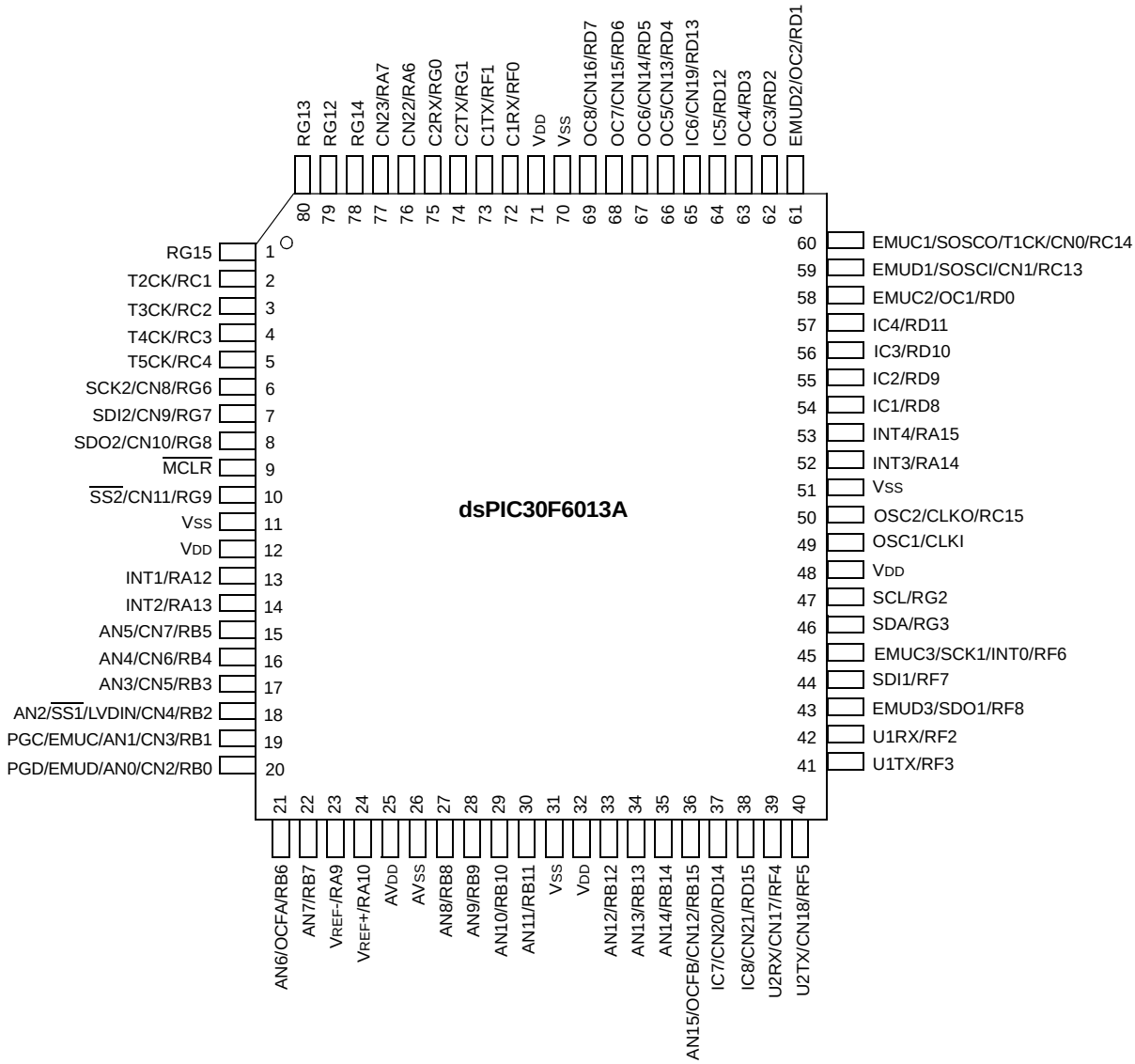
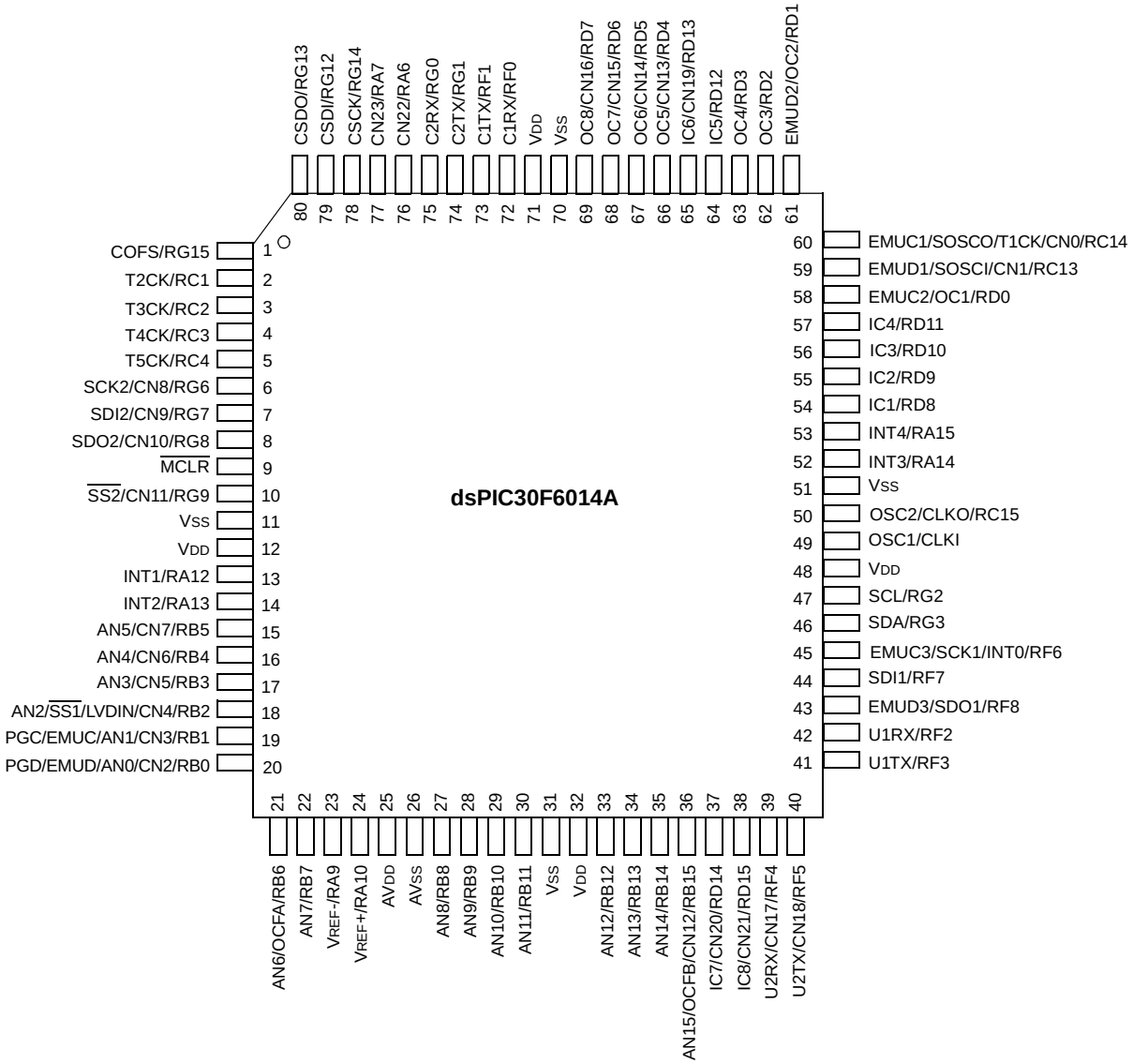
Pin Diagrams (Continued)

80-Pin TQFP



Pin Diagrams (Continued)

80-Pin TQFP



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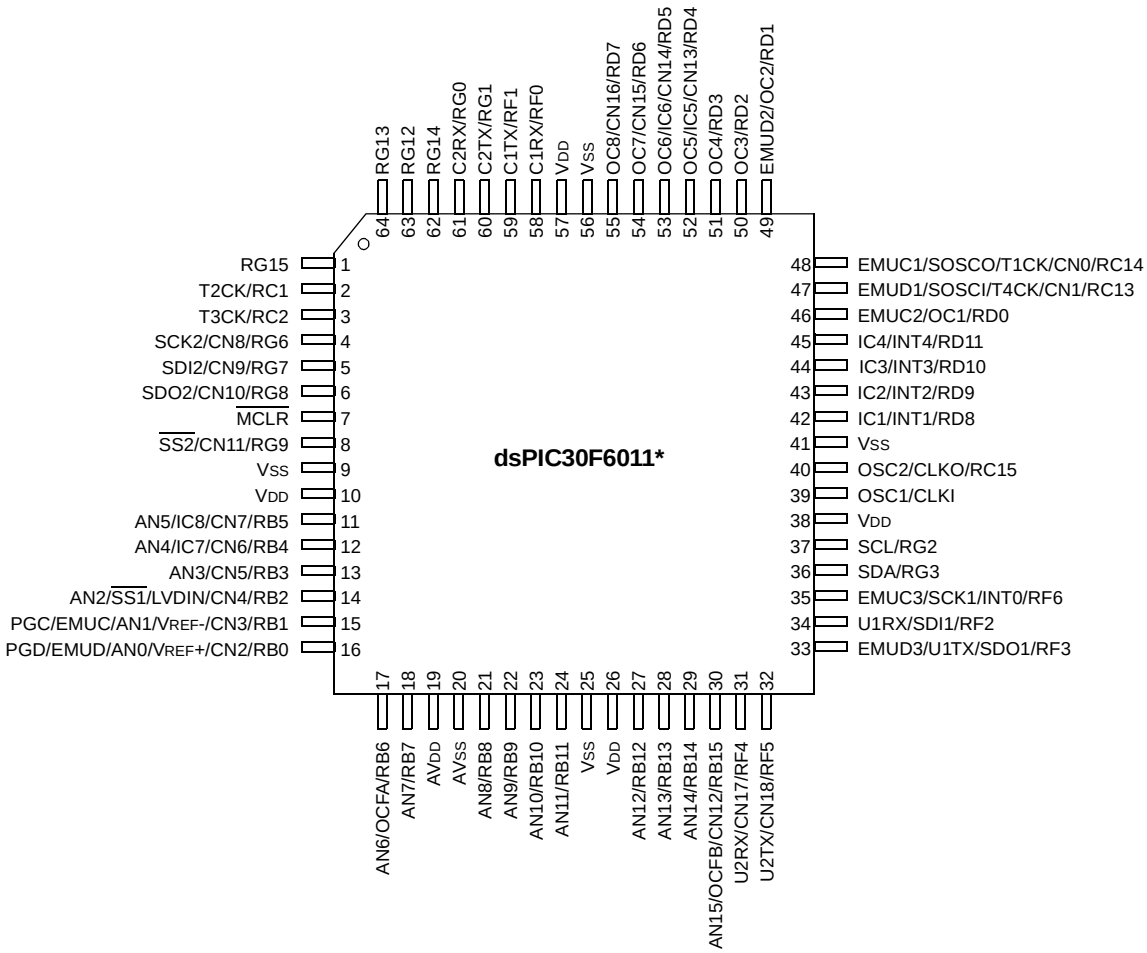
Pin Diagrams (Continued)

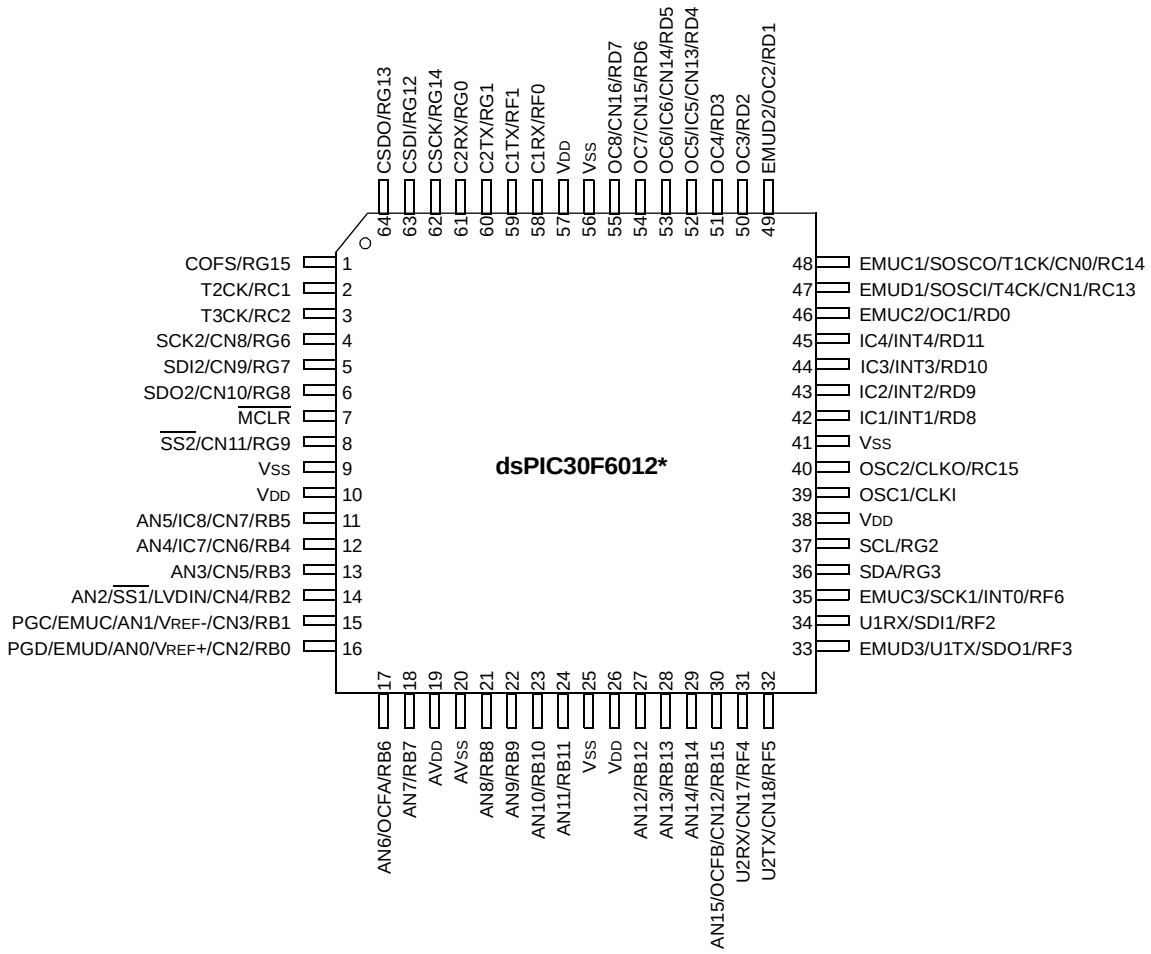
64-Pin TQFP



* This device is not recommened for new designs. See dsPIC30F6011A.

Pin Diagrams (Continued)

64-Pin TQFP



* This device is not recommened for new designs. See dsPIC30F6012A.

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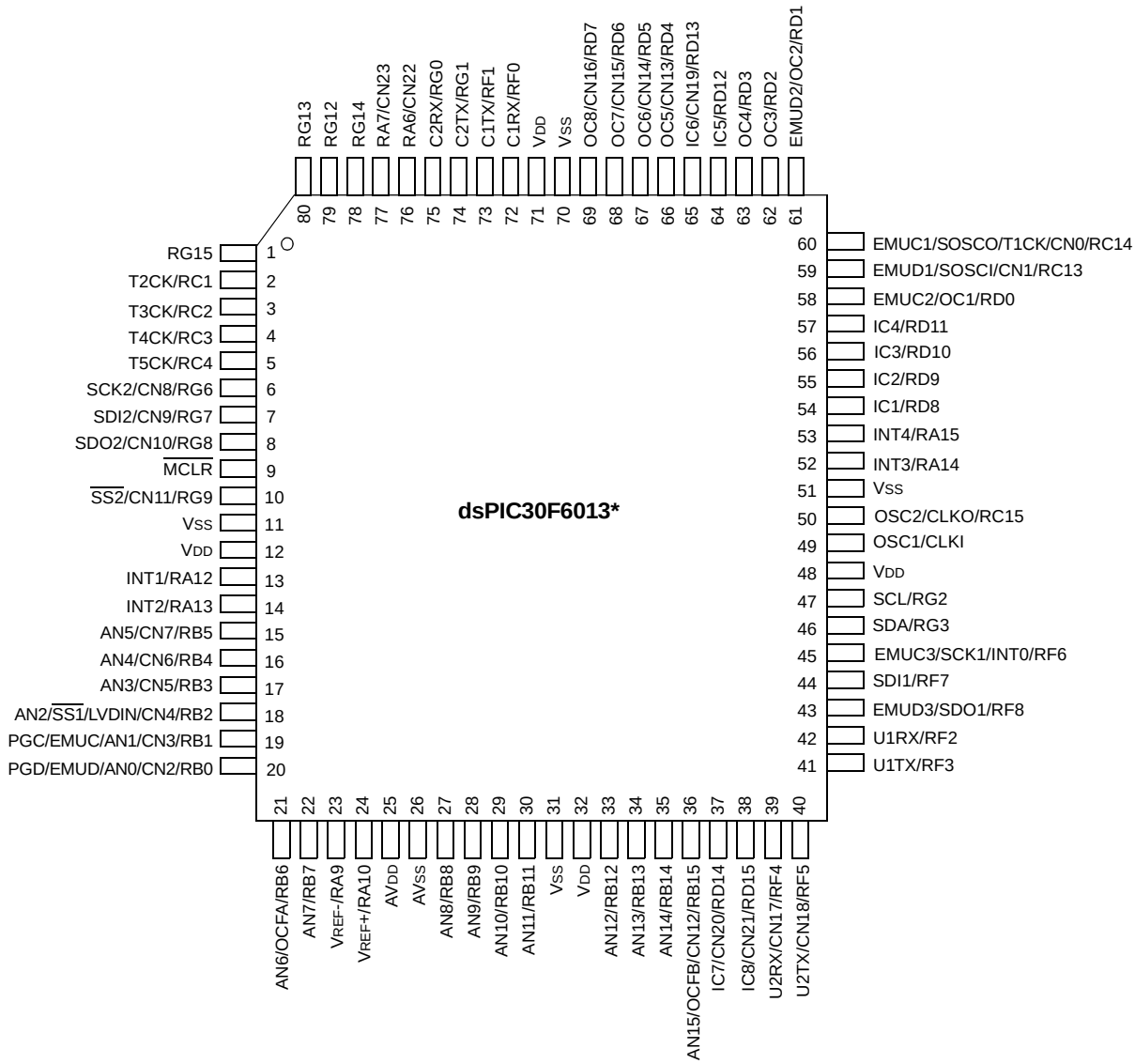
Pin Diagrams (Continued)

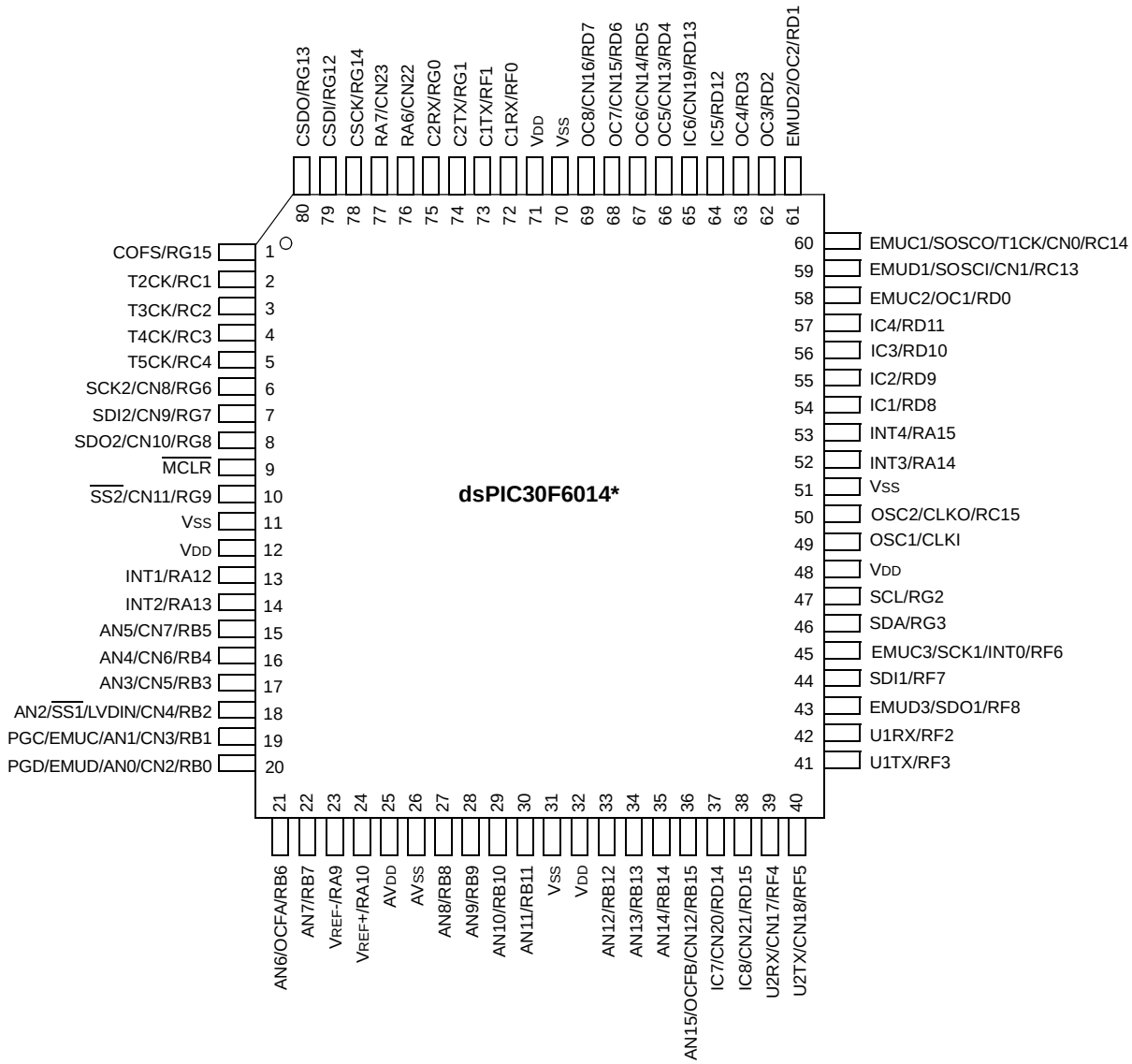
80-Pin TQFP



* This device is not recommened for new designs. See dsPIC30F6013A.

Pin Diagrams (Continued)

80-Pin TQFP



* This device is not recommened for new designs. See dsPIC30F6014A.

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APPENDIX B: DEVICE I/O PINOUTS AND FUNCTIONS FOR MOTOR CONTROL FAMILY

Table B-1 provides a brief description of device I/O pinouts and the functions that may be multiplexed to a port pin. Multiple functions may exist on one port pin. When multiplexing occurs, the peripheral module's functional requirements may force an override of the data direction of the port pin.

TABLE B-1: PINOUT I/O DESCRIPTIONS FOR MOTOR CONTROL FAMILY

Pin Name	Pin Type	Buffer Type	Description
AN0-AN15	I	Analog	Analog input channels. AN0 and AN1 are also used for device programming data and clock inputs, respectively.
AVDD	P	P	Positive supply for Analog module.
AVSS	P	P	Ground reference for Analog module.
CLKI CLKO	I O	ST/CMOS —	External clock source input. Always associated with OSC1 pin function. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSC2 pin function.
CN0-CN23	I	ST	Input change notification inputs. Can be software programmed for internal weak pull-ups on all inputs.
COFS CSCK CSDI CSDO	I/O I/O I O	ST ST ST —	Data Converter Interface frame synchronization pin. Data Converter Interface serial clock input/output pin. Data Converter Interface serial data input pin. Data Converter Interface serial data output pin.
C1RX C1TX C2RX C2TX	I O I O	ST — ST —	CAN1 bus receive pin. CAN1 bus transmit pin. CAN2 bus receive pin. CAN2 bus transmit pin.
EMUD EMUC EMUD1 EMUC1 EMUD2 EMUC2 EMUD3 EMUC3	I/O I I/O I I/O I I/O I	ST ST ST ST ST ST ST ST	Primary data I/O pin for ICD Communication Channel. Primary clock input pin for ICD Communication Channel. Alternate 1 data I/O pin for ICD Communication Channel. Alternate 1 clock input pin for ICD Communication Channel. Alternate 2 data I/O pin for ICD Communication Channel. Alternate 2 clock input pin for ICD Communication Channel. Alternate 3 data I/O pin for ICD Communication Channel. Alternate 3 clock input pin for ICD Communication Channel.
IC1-IC8	I	ST	Capture inputs 1 through 8.
INDX QEA QEB UPDN	I I I O	ST ST ST CMOS	Quadrature Encoder Index Pulse input. Quadrature Encoder Phase A input in QEI mode. Auxiliary Timer External Clock/Gate input in Timer mode. Quadrature Encoder Phase A input in QEI mode. Auxiliary Timer External Clock/Gate input in Timer mode. Position Up/Down Counter Direction State.
INT0 INT1 INT2 INT3 INT4	I I I I I	ST ST ST ST ST	External interrupt 0. External interrupt 1. External interrupt 2. External interrupt 3. External interrupt 4.
LVDIN	I	Analog	Low Voltage Detect Reference Voltage Input pin.

Legend: CMOS = CMOS compatible input or output Analog = Analog input
ST = Schmitt Trigger input with CMOS levels O = Output I = Input P = Power

TABLE B-1: PINOUT I/O DESCRIPTIONS FOR MOTOR CONTROL FAMILY (CONTINUED)

Pin Name	Pin Type	Buffer Type	Description
FLTA	I	ST	PWM Fault A input.
FLTB	I	ST	PWM Fault B input.
PWM1L	O	—	PWM 1 Low output.
PWM1H	O	—	PWM 1 High output.
PWM2L	O	—	PWM 2 Low output.
PWM2H	O	—	PWM 2 High output.
PWM3L	O	—	PWM 3 Low output.
PWM3H	O	—	PWM 3 High output.
PWM4L	O	—	PWM 4 Low output.
PWM4H	O	—	PWM 4 High output.
$\overline{MCLR}$	I/P	ST	Master Clear (Reset) input or programming voltage input. This pin is an active low Reset to the device.
OCFA	I	ST	Compare Fault A input (for Compare channels 1, 2, 3 and 4).
OCFB	I	ST	Compare Fault B input (for Compare channels 5, 6, 7 and 8).
OC1-OC8	O	—	Compare outputs 1 through 8.
OSC1	I	ST/CMOS	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise.
OSC2	I/O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.
PGD	I/O	ST	In-Circuit Serial Programming data input/output pin.
PGC	I	ST	In-Circuit Serial Programming clock input pin.
RA9-RA10	I/O	ST	PORTA is a bidirectional I/O port.
RA14-RA15	I/O	ST	
RB0-RB15	I/O	ST	PORTB is a bidirectional I/O port.
RC1	I/O	ST	PORTC is a bidirectional I/O port.
RC3	I/O	ST	
RC13-RC15	I/O	ST	
RD0-RD15	I/O	ST	PORTD is a bidirectional I/O port.
RE0-RE9	I/O	ST	PORTE is a bidirectional I/O port.
RF0-RF8	I/O	ST	PORTF is a bidirectional I/O port.
RG0-RG3	I/O	ST	PORTG is a bidirectional I/O port.
RG6-RG9	I/O	ST	
SCK1	I/O	ST	Synchronous serial clock input/output for SPI1.
SDI1	I	ST	SPI1 Data In.
SDO1	O	—	SPI1 Data Out.
$\overline{SS1}$	I	ST	SPI1 Slave Synchronization.
SCK2	I/O	ST	Synchronous serial clock input/output for SPI2.
SDI2	I	ST	SPI2 Data In.
SDO2	O	—	SPI2 Data Out.
$\overline{SS2}$	I	ST	SPI2 Slave Synchronization.
SCL	I/O	ST	Synchronous serial clock input/output for I^2C.
SDA	I/O	ST	Synchronous serial data input/output for I^2C.
SOSCI	I	ST/CMOS	32 kHz low-power oscillator crystal input; CMOS otherwise.
SOSCO	O	—	32 kHz low-power oscillator crystal output.
T1CK	I	ST	Timer1 external clock input.
T2CK	I	ST	Timer2 external clock input.
T3CK	I	ST	Timer3 external clock input.
T4CK	I	ST	Timer4 external clock input.
T5CK	I	ST	Timer5 external clock input.

Legend: CMOS = CMOS compatible input or output Analog = Analog input
ST = Schmitt Trigger input with CMOS levels O = Output I = Input P = Power

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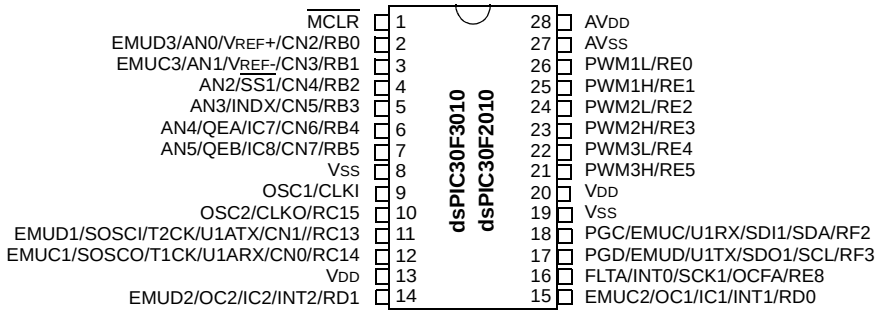
TABLE B-1: PINOUT I/O DESCRIPTIONS FOR MOTOR CONTROL FAMILY (CONTINUED)

Pin Name	Pin Type	Buffer Type	Description
U1RX	I	ST	UART1 Receive.
U1TX	O	—	UART1 Transmit.
U1ARX	I	ST	UART1 Alternate Receive.
U1ATX	O	—	UART1 Alternate Transmit.
U2RX	I	ST	UART2 Receive.
U2TX	O	—	UART2 Transmit.
VDD	P	—	Positive supply for logic and I/O pins.
VSS	P	—	Ground reference for logic and I/O pins.
VREF+	I	Analog	Analog Voltage Reference (High) input.
VREF-	I	Analog	Analog Voltage Reference (Low) input.

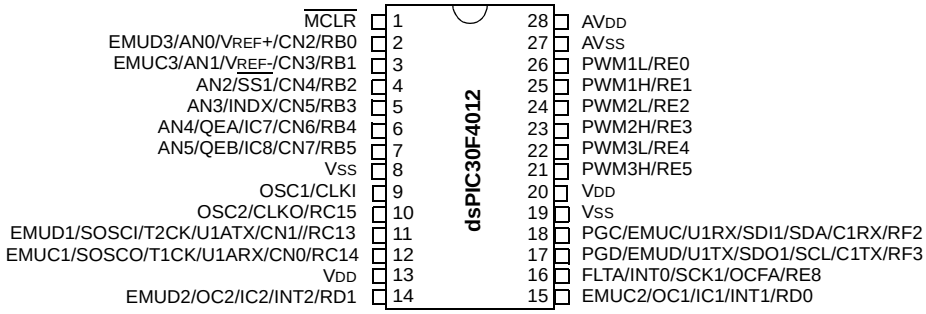
Legend: CMOS = CMOS compatible input or output Analog = Analog input
ST = Schmitt Trigger input with CMOS levels O = Output I = Input P = Power

Pin Diagrams

28-Pin PDIP and SOIC

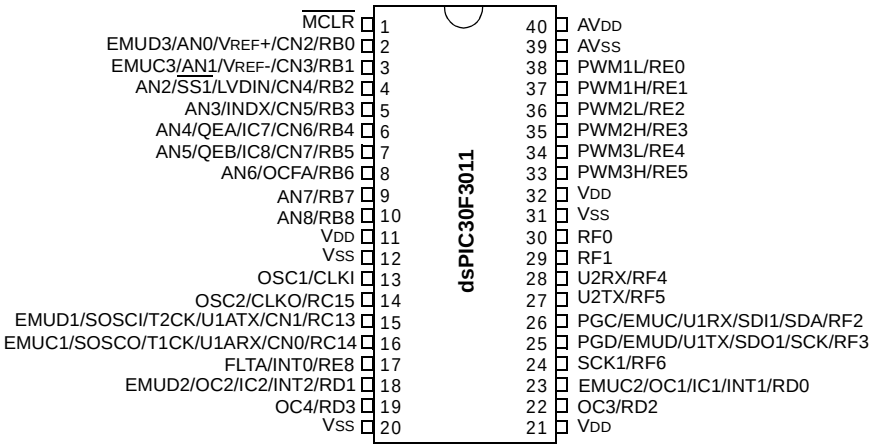


28-Pin PDIP and SOIC

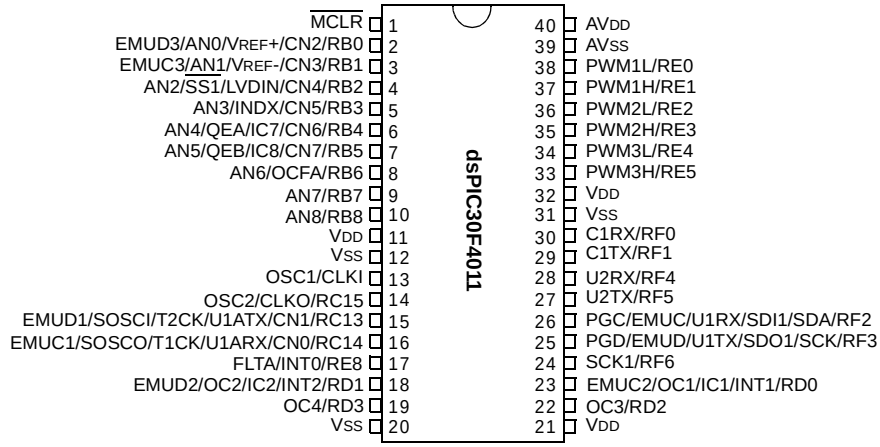


Pin Diagrams (Continued)

40-Pin PDIP



40-Pin PDIP



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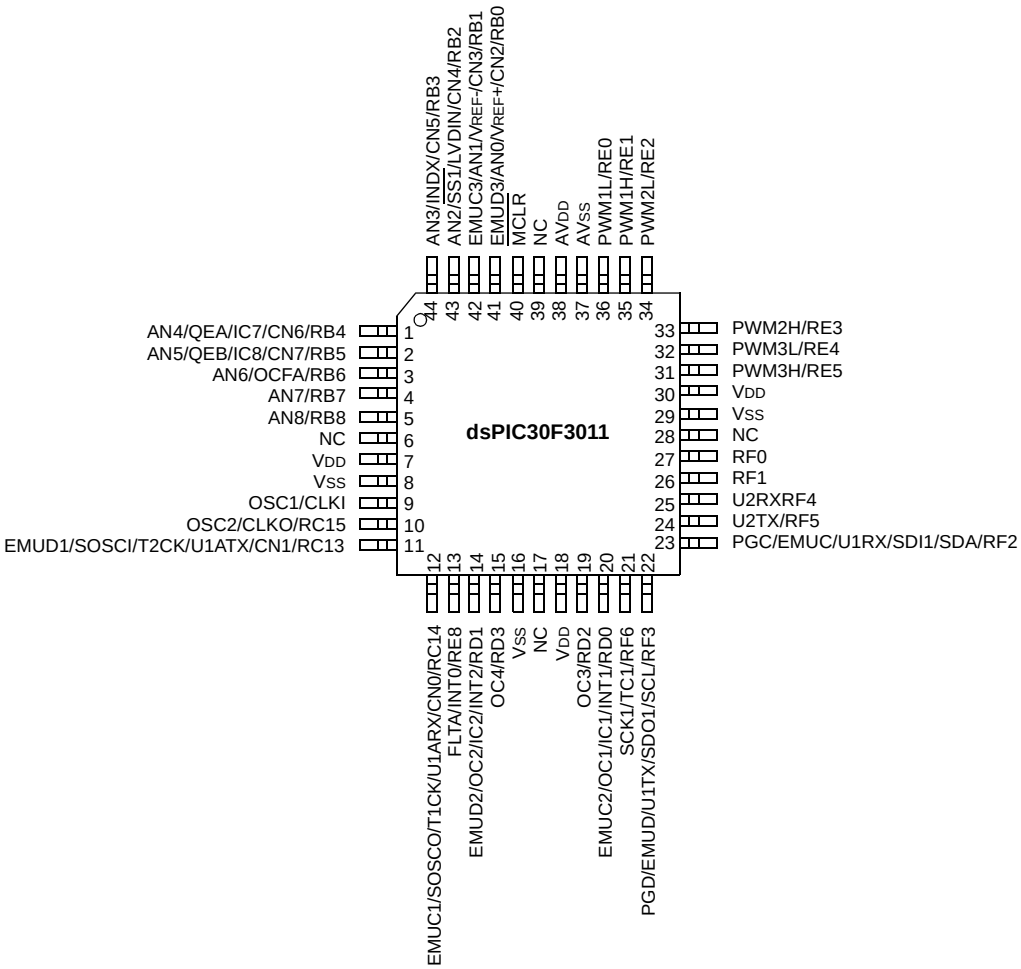
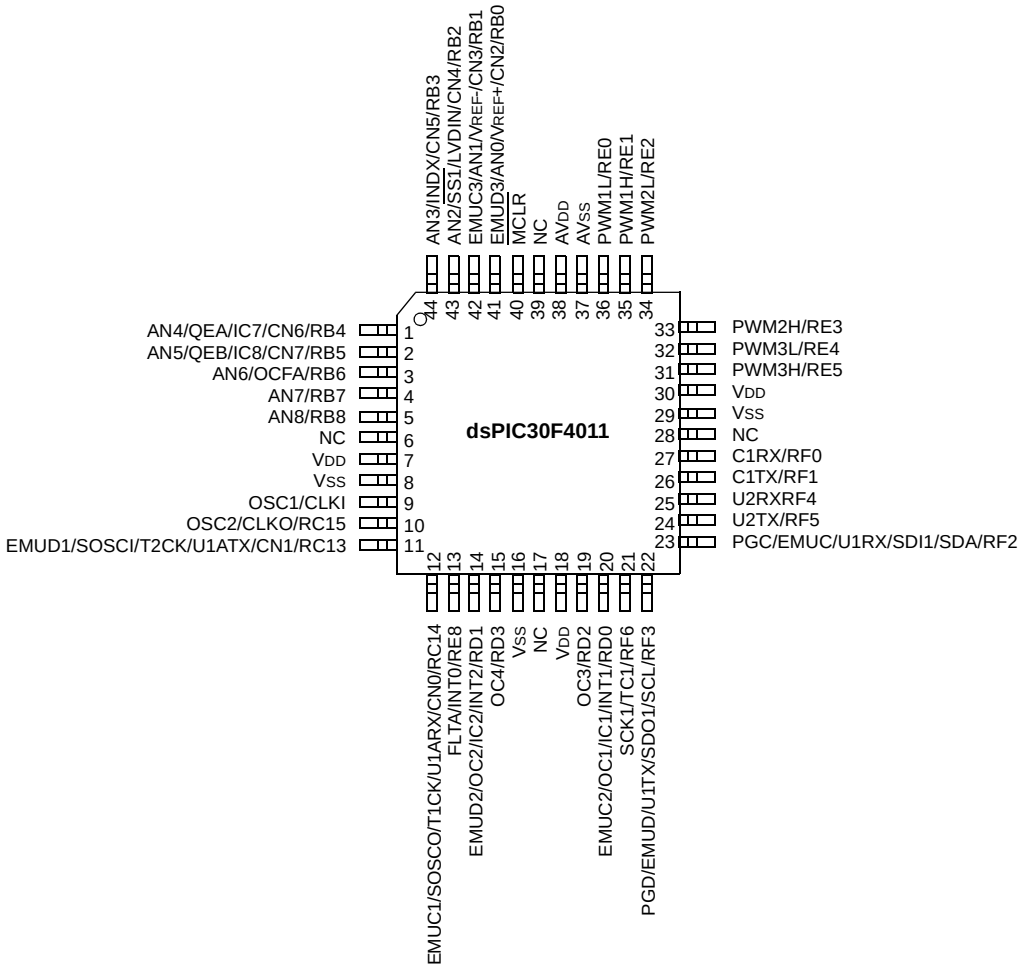
Pin Diagrams (Continued)

44-Pin TQFP



Pin Diagrams (Continued)

44-Pin TQFP



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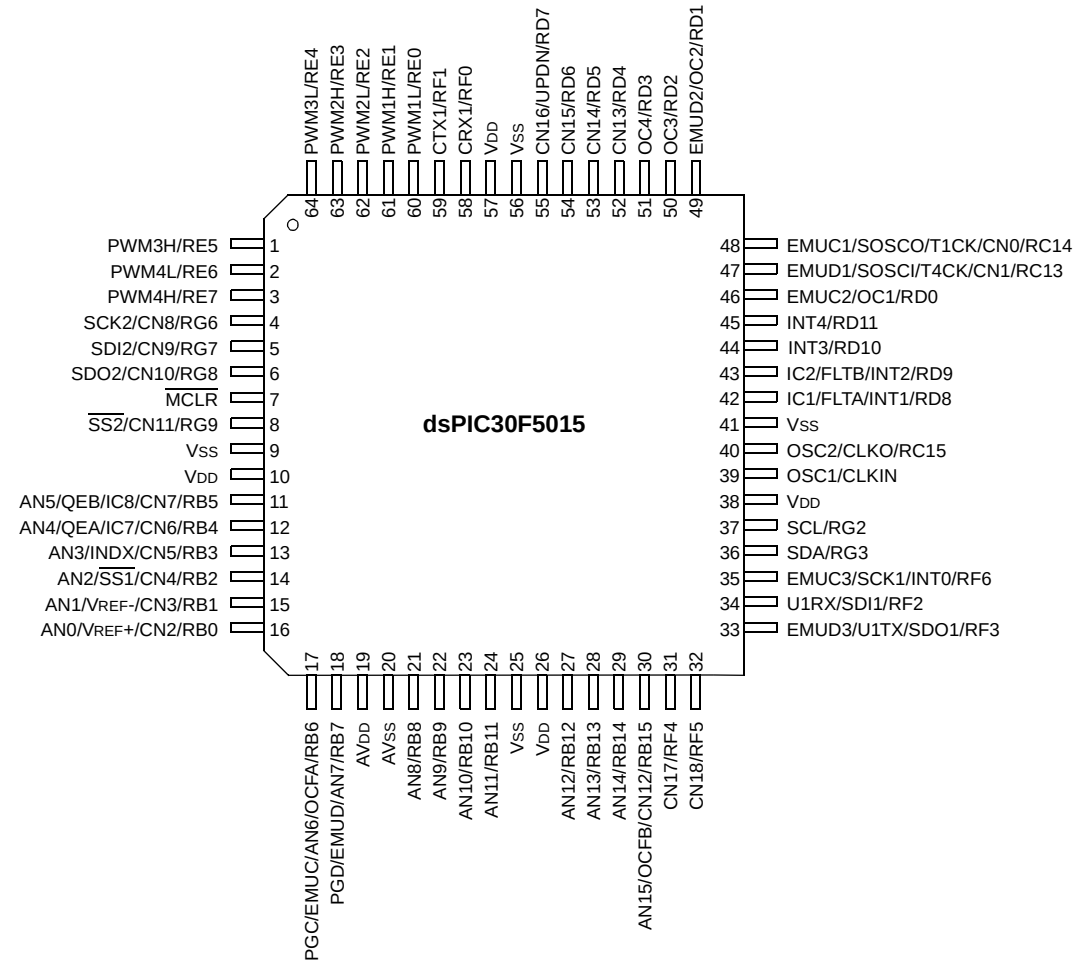
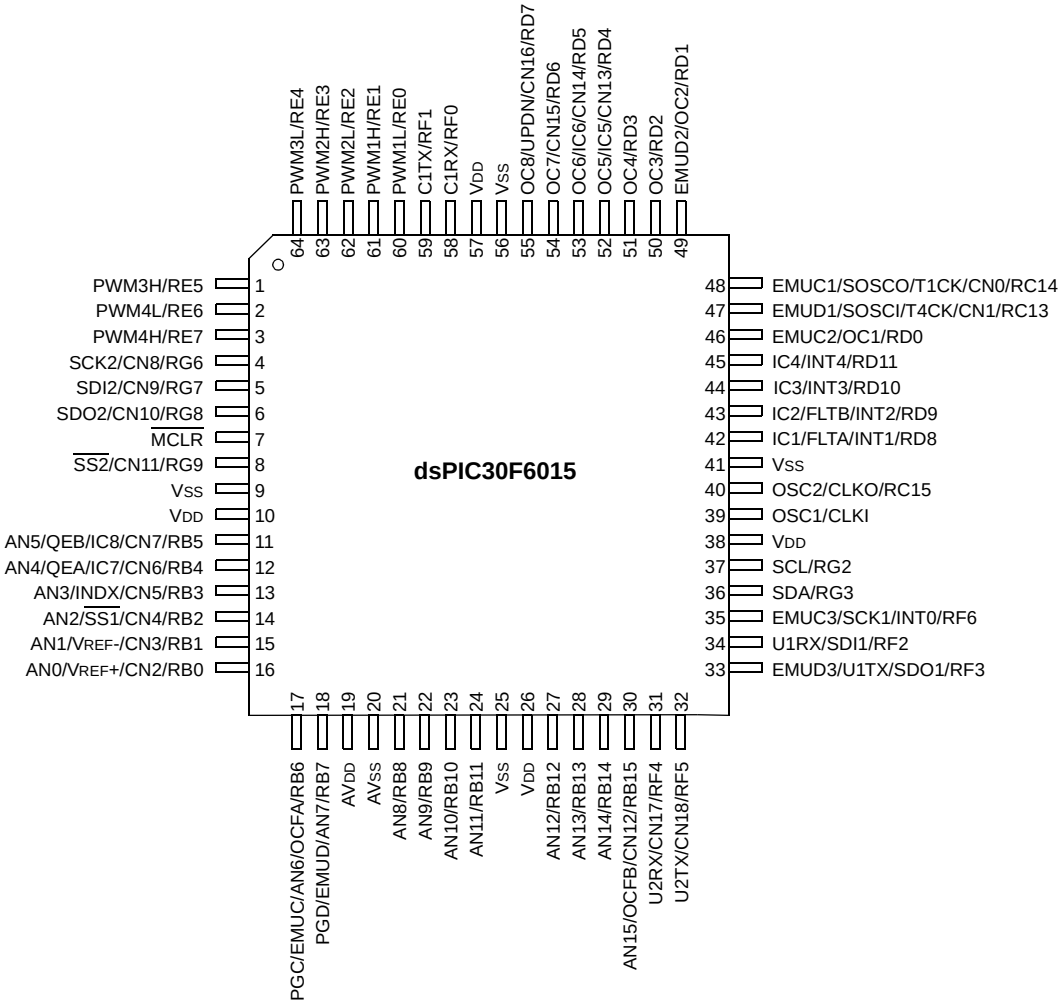
Pin Diagrams (Continued)

64-pin TQFP



Pin Diagrams (Continued)

64-pin TQFP



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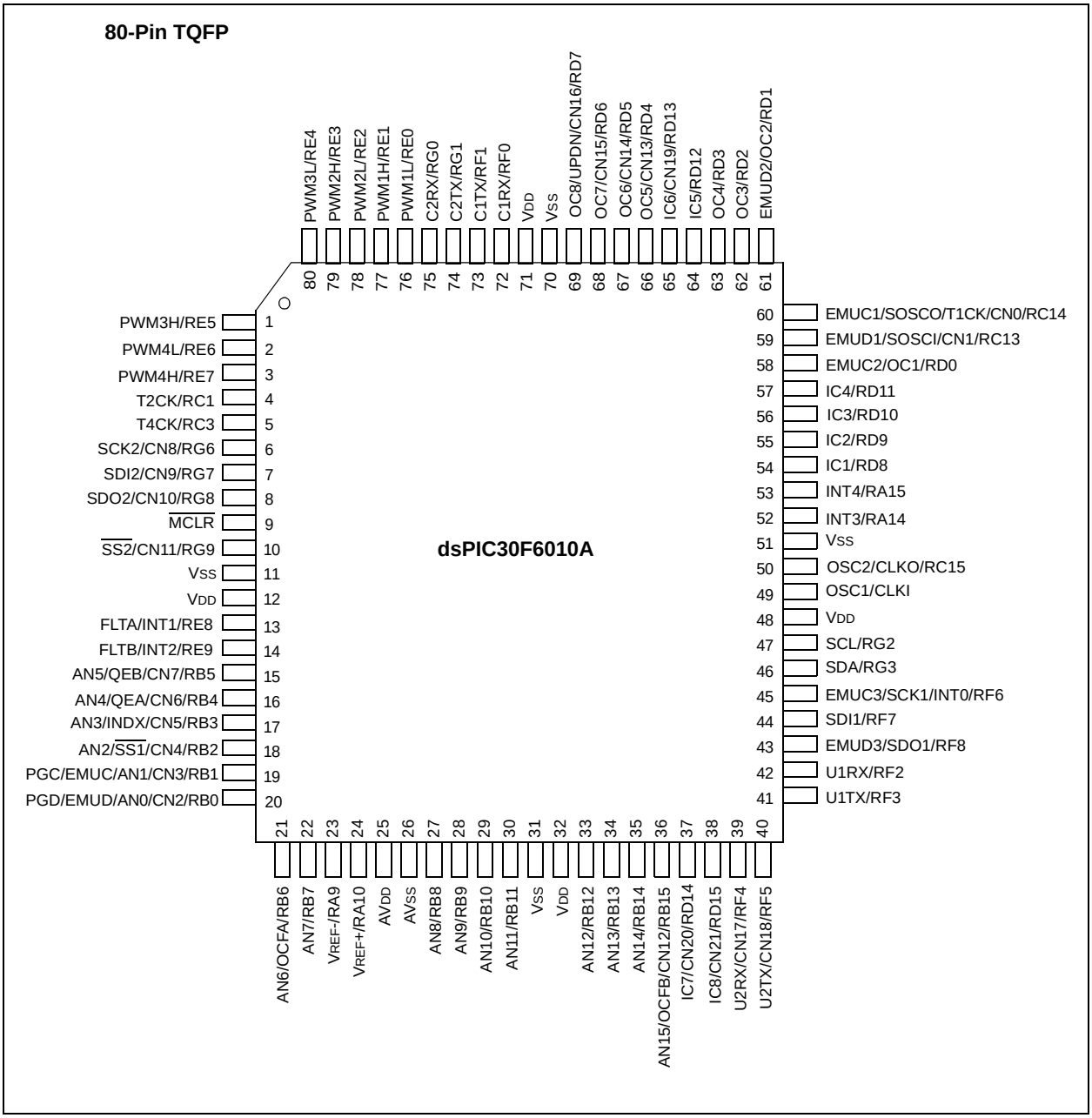
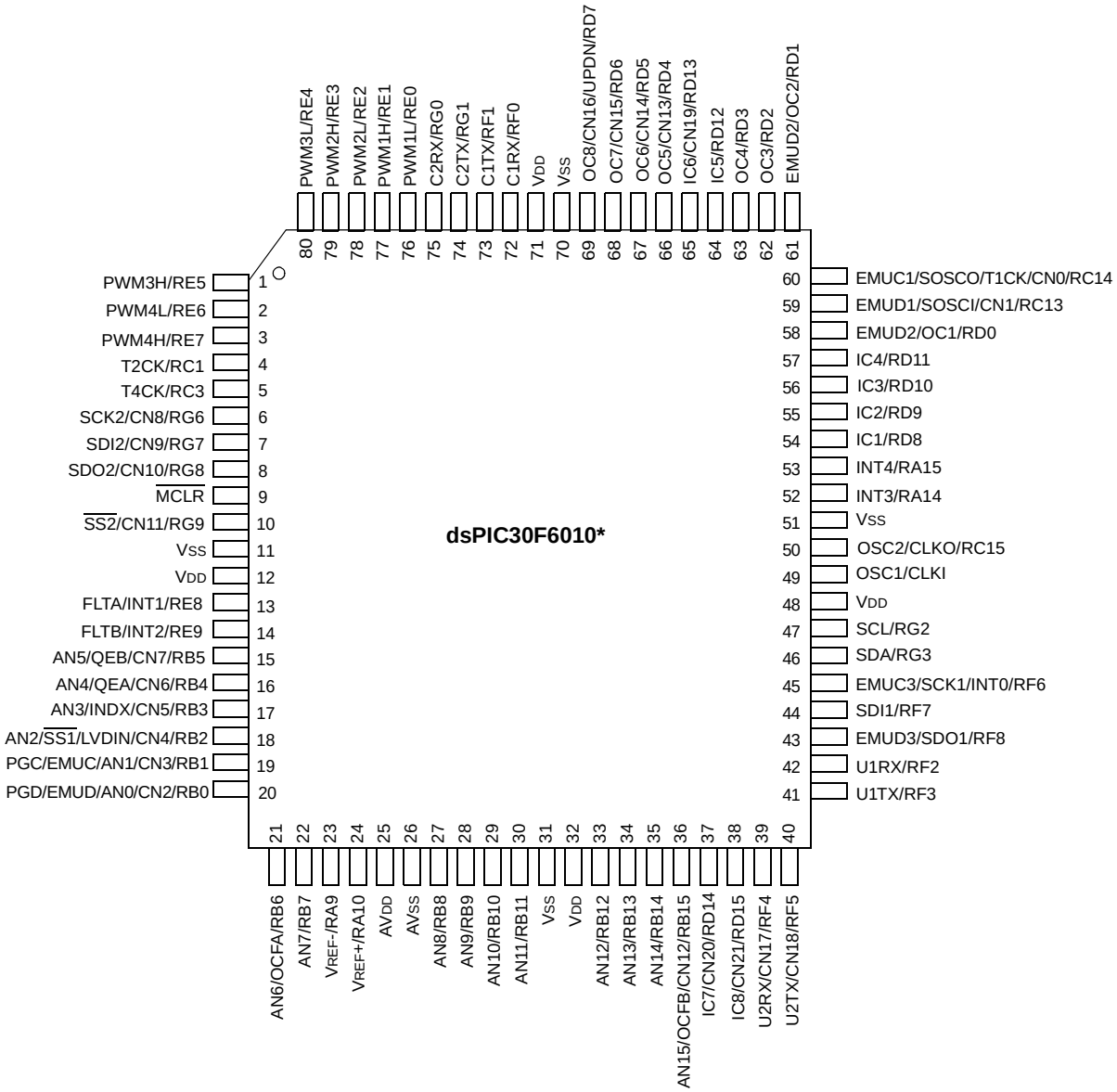
Pin Diagrams (Continued)

80-Pin TQFP



Pin Diagrams (Continued)

80-Pin TQFP



* This device is not recommened for new designs. See dsPIC30F6010A.

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