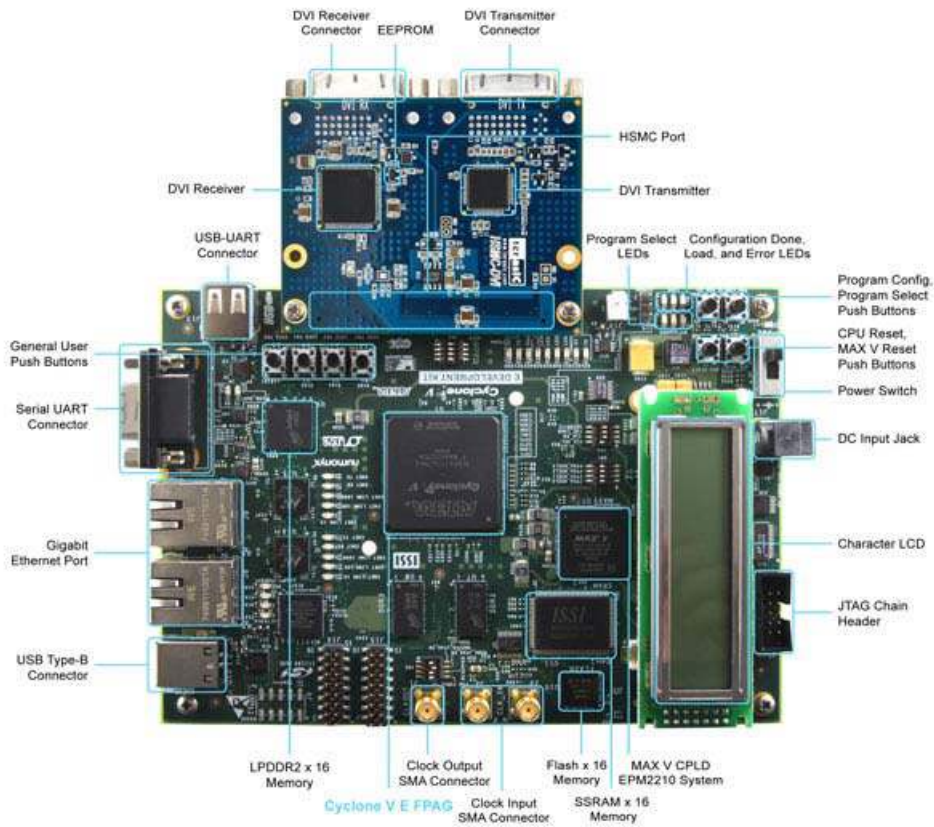




# Cyclone V E Video Development System

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## Altera Cyclone V E Video Development System

### Featured devices:

- Cyclone V E FPGA - 5CEFA7F31C7NES
- MAX V CPLD - 5M2210ZF256I5N (system controller)
- MAX II CPLD - EPM240M100I5N (embedded USB Blaster II)

### Configuration:

- On-board USB-Blaster™ II cable (USB, PHY, Max®V CPLD)
- JTAG direct via JTAG header

### Memory devices

- DDR3 x32 at 300 MHz (soft memory controller)
- LPDDR2 x16 (soft memory controller)
- Flash (512 Mb)
- SSRAM (18 Mb)
- EEPROM (64 Kb)

### General user input/output

- User control
- Four pushbuttons
- Five LEDs
- Four DIP switches
- 2x Resets (CPU reset, Dev Clear)
- LCD: Character LCD (16x2)

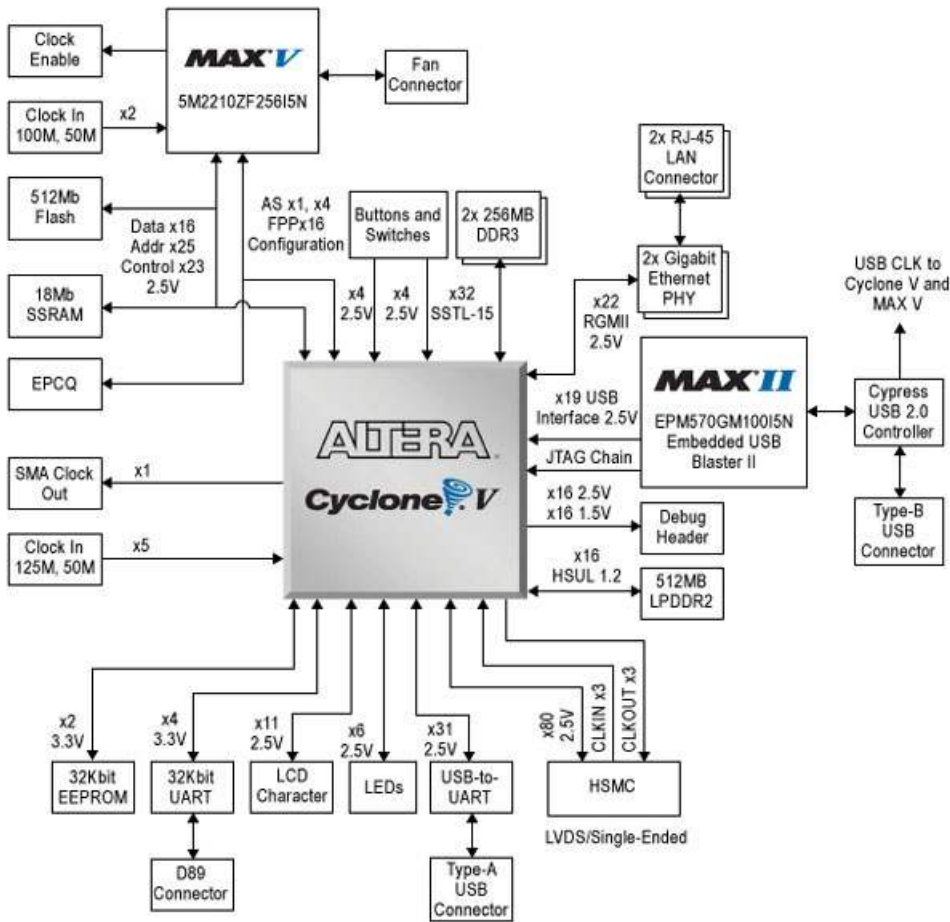
### Components and interfaces

- RJ45 for Ethernet
- UART interface

### Quartus®II design software information

- Quartus II Web Edition Software

### Altera Cyclone V E FPGA Development Board Block Diagram



## Terasic DVI-HSMC Card

### Digital Transmitter

- One DVI transmitter with single transmitting port
- Digital Visual Interface (DVI) Compliant
- Supports resolutions from VGA to UXGA (25 MHz – 165 MHz Pixel Rates)
- Universal Graphics Controller Interface
  - 12-Bit, Dual-Edge and 24-Bit, Single-Edge Input Modes
  - Adjustable 1.1 V to 1.8 V and Standard 3.3 V CMOS Input Signal Levels
  - Fully Differential and Single-Ended Input Clocking Modes
  - Standard Intel 12-Bit Digital Video Port Compatible as on Intel™ 81x Chipsets
- Enhanced PLL Noise Immunity
  - On-Chip Regulators and Bypass Capacitors for Reducing System Costs
- Enhanced Jitter Performance
  - No HSYNC Jitter Anomaly
  - Negligible Data-Dependent Jitter
    - Programmable Using I<sup>2</sup>C Serial Interface
    - Single 3.3-V Supply Operation

### Digital Receiver

- One DVI receiver with single receiving port

- Supports UXGA Resolution (Output Pixel Rates Up to 165 MHz)
- Digital Visual Interface (DVI) Specification Compliant
- True-Color, 24 Bit/Pixel, 16.7M Colors at 1 or 2-Pixels Per Clock
- Laser Trimmed Internal termination Resistors for Optimum Fixed Impedance Matching
- 4x Over-Sampling
- Reduced Ground Bounce Using Time Staggered Pixel Outputs
- Lowest Noise and Best Power Dissipation Using TI PowerPAD™ Packaging



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