STRUCTURE Silicon Monolithic Integrated Circuit

NAME OF PRODUCT DC-AC Inverter Control IC

TYPE **ＢＤ９８９２Ｋ**

FUNCTION
- 4ch control with Push-Pull
- Short circuit protection with Timer Latch
- Sequencing easily achieved with Soft Start Control
- Under Voltage Lock Out
- Short circuit protection with over voltage
- Mode-selectable the operating or stand-by mode by stand-by pin
- Synchronous operating the other BD9892FV IC's
- BURST mode controlled by PWN and DC input
- Output linear control by external DC voltage

○Absolute Maximum Ratings (Ta = 25℃)

Parameter	Symbol	Limits	Unit
Supply Voltage	V_{CC}	15	V
Operating Temperature Range	Topr	-40～+90	℃
Storage Temperature Range	Tstg	-55～+125	℃
Power Dissipation	Pd	1062*	mW
Maximum Junction Temperature	Tjmax	+150	℃

*Pd derated at 8.5mW/℃ for temperature above Ta = 25℃ (When mounted on a PCB 70.0mm×70.0mm×1.6mm)

○Operating condition

Parameter	Symbol	Limits	Unit
Supply voltage	V_{CC}	5.5～14.0	V
CT oscillation frequency	f_{CT}	20～150	kHz
BCT oscillation frequency	f_{BCT}	0.05～0.50	kHz

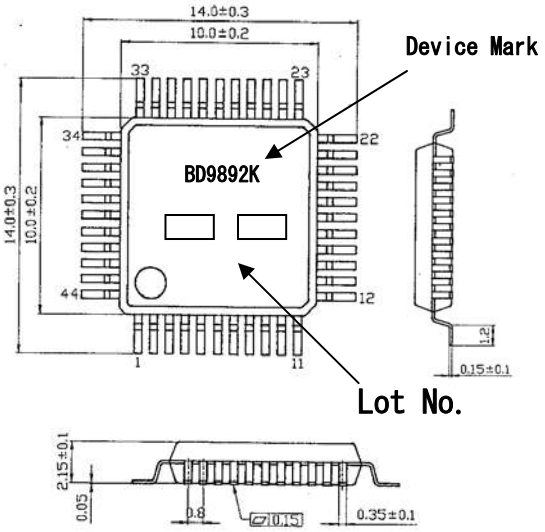
Status of this document
The Japanese version of this document is the official specification.
Please use the translation version of this document as a reference to expedite understanding of the official version.
If these are any uncertainty in translation version of this document, official version takes priority.

○Electric Characteristics (Ta=25℃, VCC=7V)

Parameter	Symbol	Limits			Unit	Conditions
		MIN.	TYP.	MAX.		
((WHOLE DEVICE))						
Operating current	Icc1	—	15.0	23.0	mA	CT=0.5V
Stand-by current	Icc2	—	2	10	μA	
((OVER VOLTAGE DETECT))						
FB over voltage detect voltage	Vovf	2.20	2.40	2.60	V	
((STAND BY CONTROL))						
Stand-by voltage H	VstH	2.0	—	VCC	V	System ＯＮ
Stand-by voltage L	VstL	-0.3	—	0.8	V	System ＯＦＦ
((TIMER LATCH))						
Timer Latch voltage	Vcp	1.9	2.0	2.1	V	
Timer Latch current	Icp	0.5	1.0	1.5	μA	
((BURST MODE))						
BOSC Max voltage	VburH	1.94	2.0	2.06	V	f_{BCT}=0.2kHz BCT(A,B)common spec
BOSC Min Voltage	VburL	0.4	0.5	0.6	V	f_{BCT}=0.2kHz BCT(A,B) common spec
BOSC constant current	IBCT	1.35/BRT	1.5/BRT	1.65/BRT	A	BCT(A,B) common spec
BOSC constant current	fBCT	292.5	300.0	307.5	Hz	BRT=36kΩ BCT=0.048μF BCT(A,B) common spec
((OSC BLOCK))						
OSC constant current	I_{CT}	1.35/RT	1.5/RT	1.65/RT	A	
OSC Max voltage	VoscH	1.8	2.0	2.2	V	f_{CT}=60kHz
OSC Min voltage	VoscL	0.3	0.5	0.7	V	f_{CT}=60kHz
MAX DUTY	MAXDUTY	44	46.5	49	%	f_{CT}=60kHz
Soft start current	Iss	1.0	2.0	3.0	μA	
IS COMP detect Voltage	Visc	0.45	0.50	0.55	V	
SS COMP detect voltage	Vss	2.0	2.2	2.4	V	SS(A,B) common spec
SRT ON resistance	RSRT	—	200	400	Ω	
((UVLO BLOCK))						
Operating voltage	V_A_uvloH	4.95	5.15	5.35	V	VCC(A,B) common spec
Hysteresis width	⊿V_A_uvlo	0.21	0.29	0.037	V	VCC(A,B) common spec
Operating voltage (External UVLO)	Vuvlo2	2.242	2.315	2.388	V	
Hysteresis width	⊿Vuvlo2	0.083	0.110	0.137	V	
FB OVP Mask Threshold voltage	Vuvlo_fb	2.222	2.315	2.407	V	
((REG BLOCK))						
REG output voltage	VREG	3.038	3.100	3.162	V	
REG source current	IREG	5.0	—	—	mA	
((FEED BACK BLOCK))						
IS threshold voltage	Vis	1.225	1.250	1.275	V	Connected REG When Vref pin is open IS(1,2,3,4) common spec
VS threshold voltage	Vvs	1.220	1.250	1.280	V	VS(1,2,3,4) common spec
IS source current 1	Iis1	—	—	1.5	μA	DUTY=2.0V IS(1,2,3,4) common spec
IS source current 2	Iis2	13.0	20.0	27.0	μA	DUTY=0V、IS=0.5V IS(1,2,3,4) common spec
VS source current	Ivs	—	—	1.0	μA	VS(1,2,3,4) common spec
((OUTPUT BLOCK))						
NAch output voltage H	VoutNAH	VCC-0.3	VCC-0.1	—	V	NA(1,2,3,4) common spec
NBch output voltage H	VoutNBH	VCC-0.3	VCC-0.1	—	V	NB(1,2,3,4) common spec
NAch output voltage L	VoutNAL	—	0.1	0.3	V	NA(1,2,3,4) common spec
NBch output voltage L	VoutNBL	—	0.1	0.3	V	NB(1,2,3,4) common spec
NAch output sink resistance	RsinkNA	—	5	10	Ω	Isink=10mA NA(1,2,3,4) common spec
NAch output source resistance	RsourceNA	—	8	16	Ω	Isource=10mA NA(1,2,3,4) common spec
NBch output sink resistance	RsinkNB	—	5	10	Ω	Isink=10mA NB(1,2,3,4) common spec
NBch output source resistance	RsourceNB	—	8	16	Ω	Isource=10mA NB(1,2,3,4) common spec
Drive output frequency	f_{OUT}	58.5	60.0	61.5	KHz	RT=20kΩ、CT=420pF NA,NB(1,2,3,4) common spec
((COMP BLOCK))						
Over voltage detect	VCOMP	3.033	3.100	3.167	V	COMP(A,B) common spec
Hysteresis width	⊿VCOMP	0.07	0.1	0.13	V	COMP(A,B) common spec
((PROTECT CLOCK))						
Normal output voltage	VPH	2.9	3.1	3.3	V	
Protect output voltage	VPL	—	—	0.5	V	

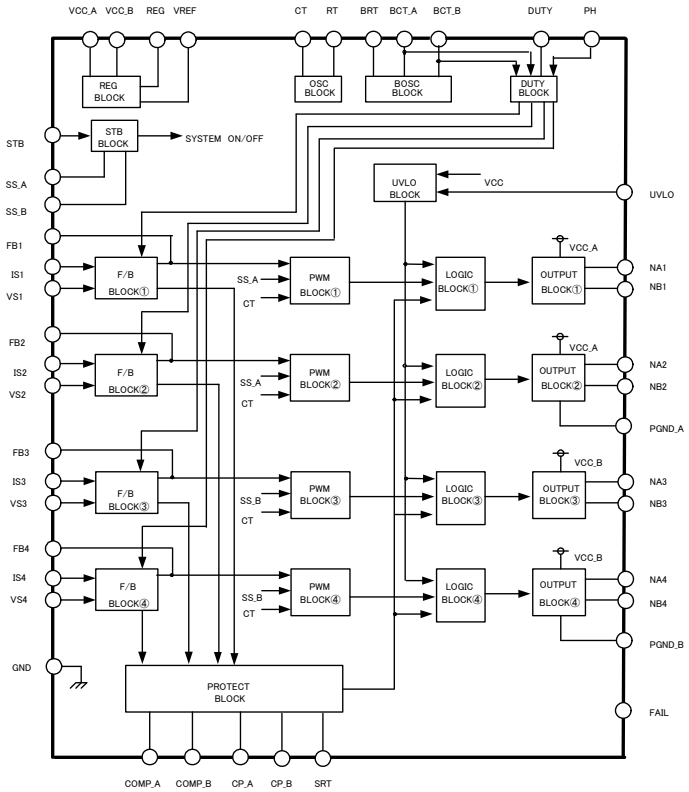
(This product is not designed for normal operation with in a radio active environment.)

○Package Dimensions



QFP44 (unit:mm)

○Block Diagram



○Pin Description

Pin No.	Pin Name	Function
1	COMP_A	Over voltage detect for 1ch,2ch
2	NA1	FET driver for 1ch
3	NB1	FET driver for 1ch
4	PGND_A	Ground for FET drivers
5	NB2	FET driver for 2ch
6	NA2	FET driver for 2ch
7	STB	Stand-by switch
8	VCC_A	Supply voltage input
9	VREF	Reference voltage input for IS error amplifier
10	FAIL	Protect clock output
11	PH	Shift control input
12	REG	Internal regulator output
13	DUTY	Control PWM mode and BURST mode
14	BRT	External resistor from BRT to GND for adjusting the BURST triangle oscillator
15	BCT_B	External capacitor from BCT to GND for adjusting the BURST triangle oscillator for 3ch,4ch
16	BCT_A	External capacitor from BCT to GND for adjusting the BURST triangle oscillator for 1ch,2ch
17	GND	GROUND
18	CT	External capacitor from CT to GND for adjusting the triangle oscillator
19	RT	External resistor from RT to GND for adjusting the triangle oscillator
20	SRT	External resistor from SRT to RT for adjusting the triangle oscillator
21	CP_A	External capacitor from CP to GND for Timer Latch for 1ch,2ch
22	CP_B	External capacitor from CP to GND for Timer Latch for 3ch,4ch
23	SS_A	External capacitor from SS to GND for Soft Start Control 1ch,2ch
24	SS_B	External capacitor from SS to GND for Soft Start Control 3ch,4ch
25	VCC_B	Supply voltage input
26	UVLO	External Under Voltage Lock OUT
27	NA4	FET driver for 4ch
28	NB4	FET driver for 4ch
29	PGND_B	Ground for FET drivers
30	NB3	FET driver for 3ch
31	NA3	FET driver for 3ch
32	COMP_B	Over voltage detect for 3ch,4ch
33	VS4	Error amplifier input④
34	IS4	Error amplifier input④
35	FB4	Error amplifier output④
36	VS3	Error amplifier input③
37	IS3	Error amplifier input③
38	FB3	Error amplifier output③
39	FB2	Error amplifier output②
40	IS2	Error amplifier input②
41	VS2	Error amplifier input②
42	FB1	Error amplifier output①
43	IS1	Error amplifier input①
44	VS1	Error amplifier input①

○NOTE FOR USE

1. When designing the external circuit, including adequate margins for variation between external devices and the IC.Use adequate margins for steady state and transient characteristics.
2. Recommended Operating Range

   The circuit functionality is guaranteed within of ambient temperature operation range as long as it is within recommended operating range. The standard electrical characteristic values cannot be guaranteed at other voltages in the operating ranges, however, the variation will be small.
3. Mounting Failures

   Mounting failures, such as misdirection or miscounts, may harm the device.
4. Electromagnetic Fields

   A strong electromagnetic field may cause the IC to malfunction.
5. The GND pin should be the location within ±0.3V compared with the PGND(A,B) pin
6. BD9892K has the short circuit protection with Thermal Shut Down System. When STB or Vcc pin re-supplied, They enables to cancel the latch. If It rise the temperature of the chip more than 170℃(TYP), It make the external FET OFF
7. Absolute maximum ratings are those values that, if exceeded, may cause the life of a device to become significantly shortened. Moreover, the exact failure mode caused by short or open is not defined. Physical countermeasures, such as a fuse, need to be considered when using a device beyond its maximum ratings.
8. About the external FET, the parasitic Capacitor may cause the gate voltage to change, when the drain voltage is switching. Make sure to leave adequate margin for this IC variation.
9. On operating Slow Start Control (SS(A,B) is less than 2.2V), It does not operate Timer Latch.
10. By STB voltage, BD9892K is changed to 2 states. Therefore, do not input STB pin voltage between one state and the other state (0.8～2.0).
11. The pin connected a connector need to connect to the resistor for electrical surge destruction.
12. This IC is a monolithic IC which (as shown is Fig-1)has P^+ substrate and between the various pins. A P-N junction is formed from this P layer of each pin. For example, the relation between each potential is as follows,

    ○(When GND > PinB and GND > PinA, the P-N junction operates as a parasitic diode.)

    ○(When PinB > GND > PinA, the P-N junction operates as a parasitic transistor.)

Parasitic diodes can occur inevitably in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits as well as operation faults and physical damage. Accordingly you must not use methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND(P substrate)voltage to an input pin.

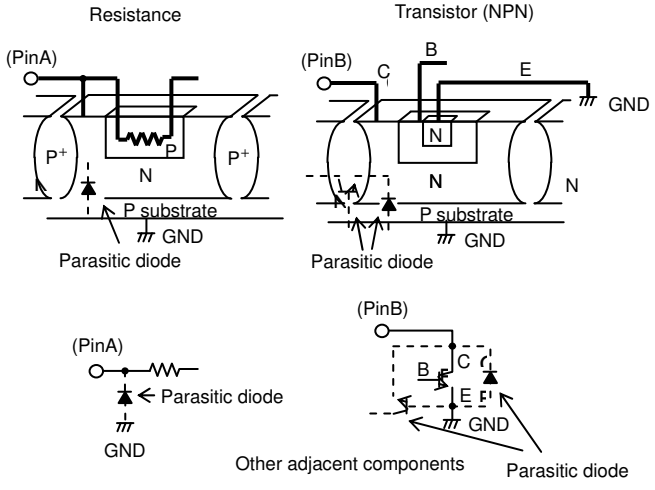


Fig.1 Simplified structure of a Bipolar IC

Notes

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