EVALUATION KIT AVAILABLE

*Click **here** to ask an associate for production status of specific part numbers.*

MAX77511/MAX77711 — 10V Input, Quad-Phase Configurable, 3A/Phase, High-Efficiency Buck Converter

General Description

The MAX77511/MAX77711 are four-phase, 3A/phase, configurable single to quad output, step-down buck regulators for 1s/2s Li+ battery inputs. Output voltage is programmable through an I²C interface between 0.25V and 5.2V. The buck has four combinable 3A switching phases (Φ) for up to four regulated outputs. Phases are configurable to higher-current multiphase outputs: 4Φ, (3+1)Φ, (2+2)Φ, (2+1+1)Φ, or (1+1+1+1)Φ.

Six GPIOs can be purposed for I/O expansion or buck status and control. Pseudo-random spread-spectrum modulation suppresses EMI. Soft-start, soft-stop, and DVS slew times are programmable with I²C. MAX77711 offers a 300mA linear regulator.

MAX77511/MAX77711 are available in a 64-bump, 3.54mm x 3.54mm wafer-level package (WLP).

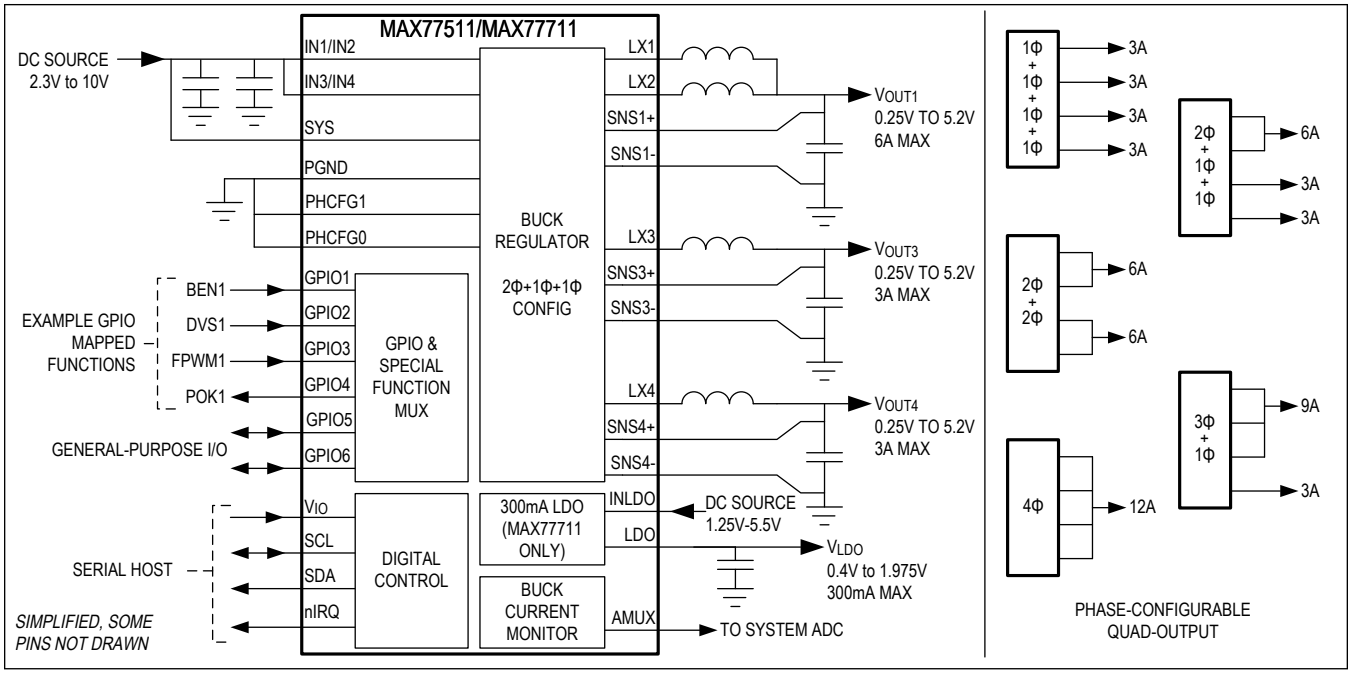
Applications

- DSLR, Mirrorless, HD Video, and Action Cameras
- 2-Cell Li+/Li-ion Equipment
- Notebook Computers and Robots
- Embedded Microprocessors, FPGAs, or ASICs

Benefits and Features

- 3A/Phase Configurable Buck Regulator
  - 3A, 6A, 9A, or 12A Output Current Capability
- 2.3V to 10V Input Voltage Range
- 0.25V to 5.2V Output Voltage Range
  - 0.25V to 1.3V (5mV steps) in Low-Range
  - 1V to 5.2V (20mV steps) in High-Range
- Pin Programmable Output/Phase (Φ) Configuration
  - 4Φ, (3+1)Φ, (2+2)Φ, (2+1+1)Φ, (1+1+1+1)Φ
- High-Efficiency and Low-Heat with 2520 Inductor
  - 94% Peak ($3.3V_{OUT}$, $7.4V_{IN}$)
  - 85% Peak ($1.1V_{OUT}$, $7.4V_{IN}$)
- 1MHz Nominal Switching Frequency per Phase
  - Pseudo-Random Spread-Spectrum Options
- Six Multi-Function GPIOs for Hardware Buck Control
  - Enable, DVS, FPWM, and Power-OK
- 300mA pMOS LDO (MAX77711 Only)
- Built-In Flexible Sequencing with Soft-Start/Stop
- Protection Features
  - Hard and Soft-Short Protection, UVLO, and Thermal Protection

Simplified Block Diagram



***Ordering Information** appears at end of data sheet.*

19-100381; Rev 5; 5/23

TABLE OF CONTENTS

TABLE OF CONTENTS (CONTINUED)

TABLE OF CONTENTS (CONTINUED)

LIST OF FIGURES

LIST OF TABLES

Absolute Maximum Ratings

IN1, IN2, IN3, IN4 to PGNDx ..... -0.3V to +12V
BSTx to LXx ..... -0.3V to +2.2V
SYS to AGND ..... -0.3V to +12V
PGNDx, DGND, SNSx- to AGND ..... -0.3V to +0.3V
IN1, IN2, IN3, IN4 Continuous Current ..... $3.2A_{RMS}$
LX1, LX2, LX3, LX4 Continuous Current (Note 1) ..... $3.2A_{RMS}$
V_{L13}, V_{L24} to AGND ..... -0.3V to +2.2V
V_{DD}, AMUX to AGND ..... -0.3V to +2.2V
PHCFG1, PHCFG0 to AGND ..... -0.3V to V_{DD} + 0.3V
GPIOx to AGND ..... -0.3V to V_{IO} + 0.3V
SDA, SCL to AGND ..... -0.3V to +6V
nIRQ, nRSTIO to AGND ..... -0.3V to +6V
V_{IO}, SNSx+ to AGND ..... -0.3V to +6V
AMUX Continuous Source/Sink Current ..... $100\mu A_{RMS}$
ENSEQ to AGND ..... -0.3V to V_{SYS} + 0.3V
INLDO to AGND ..... -0.3V to +6V
LDO to AGND
  LDO Disabled ..... -0.3V to V_{INLDO} + 0.3V
  LDO Enabled ..... -0.3 to MIN(V_{INLDO} + 0.3V, +2.2V)
Continuous Power Dissipation (Multilayer Board, T_A = +70ºC)
  64 WLP (derate 26.18mW/°C above +70°C) 2094mW
Operating Junction Temperature Range ..... -40°C to +125°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature (reflow) ..... +260°C

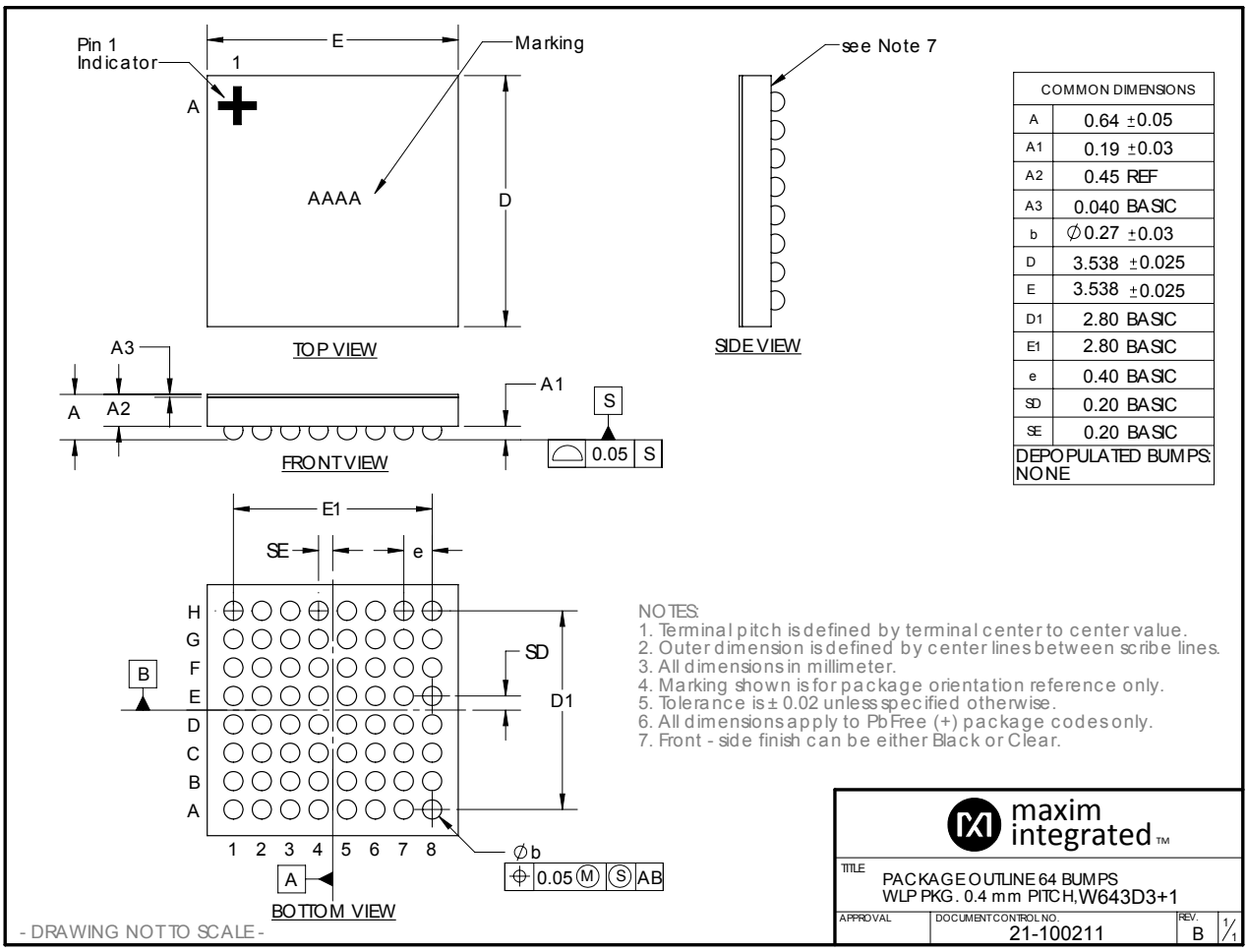
Note 1: LXx has internal clamp diodes to its corresponding PGNDx and INx. Applications that forward bias these diodes should take care not to exceed the ICs package power dissipation limits.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

64 WLP

Package Code	W643D3+1
Outline Number	21-100211
Land Pattern Number	Refer to *Application Note 1891*
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	38.20°C/W



For the latest package outline information and land patterns (footprints), go to ***www.maximintegrated.com/packages***. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to ***www.maximintegrated.com/thermal-tutorial***.

Electrical Characteristics—Top-Level

(V_{SYS} = V_{INx} = 7.4V, single-phase configuration (1+1+1+1)Φ, V_{IO} = 1.8V, V_{LDO} = 1.8V, listed conditions apply to all bucks, T_A = T_J = -40°C to +125°C, typical values are at T_A = T_J = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT VOLTAGE AND SUPPLY CURRENT						
SYS Voltage Range	V_{SYS}		2.3		10	V
SYS Undervoltage Lockout (UVLO)	V_{UVLO_R}	V_{SYS} rising	2.1	2.2	2.3	V
	V_{UVLO_F}	V_{SYS} falling	1.9	2.0	2.1	
Power-On Reset (POR) Threshold	V_{POR}	V_{SYS} falling		1.7		V

Electrical Characteristics—Top-Level (continued)

(V_{SYS} = V_{INx} = 7.4V, single-phase configuration (1+1+1+1)Φ, V_{IO} = 1.8V, V_{LDO} = 1.8V, listed conditions apply to all bucks, T_A = T_J = -40°C to +125°C, typical values are at T_A = T_J = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Shutdown Supply Current	I_{SHDN}	V_{IO} = V_{ENSEQ} = 0V, dedicated internal supplies off, regulators disabled, T_A = -40°C to +85°C (Note 3)			1.3	10	µA
Standby Supply Current	I_{STNDBY}	V_{IO} = 1.8V, V_{ENSEQ} = 0V, V_{DD} on, FTPEN = 0, T_A = -40°C to +85°C (Note 3)	V_{L13}/V_{L24} off (FVLEN = 0), bucks disabled		25	60	µA
			V_{L13}/V_{L24} on (FVLEN = 1), bucks disabled		130		
Quiescent Supply Current	I_Q	All bucks enabled in SKIP mode, LDO disabled, no load (Note 3)			600	800	µA
		All bucks enabled in Turbo SKIP mode, LDO disabled, no load (Note 3)			900	1100	
SEQUENCER ENABLE INPUT (ENSEQ)							
ENSEQ Logic High Threshold	$V_{ENSEQ-HI}$			1.6			V
ENSEQ Logic Low Threshold	$V_{ENSEQ-LO}$					0.4	V
ENSEQ Leakage Current	$I_{ENSEQ-LKG}$	V_{SYS} = 10V, V_{ENSEQ} = 0V or 10V	T_A = +25°C		±0.1		µA
			T_A = +85°C		±0.5		
Sequence Start Delay	t_{SEQDLY}	V_{IO} = 0V, time measured between rising edge of ENSEQ and first LX pulse of a buck in slot 1			200		µs
FLEXIBLE POWER SEQUENCER (FPS)							
Sequencer Slot Pitch Accuracy		Root clock accuracy		-5		+5	%
Sequencer Slot Pitch	t_{SLOT}	FPS_SLOT_T[1:0] = 0b00			0.625		ms
		FPS_SLOT_T[1:0] = 0b01			1.25		
		FPS_SLOT_T[1:0] = 0b10			2.5		
		FPS_SLOT_T[1:0] = 0b11			5		
INTERRUPT OUTPUT (nIRQ)							
nIRQ Output Low Voltage	$V_{nIRQ-LO}$	Sinking 2mA				0.4	V
nIRQ Leakage Current	$I_{nIRQ-LKG}$	V_{IO} = 5.5V, nIRQ set to be high impedance (i.e., no interrupts), V_{nIRQ} = 0V and 5.5V	T_A = +25°C	-1	±0.001	+1	µA
		V_{IO} = 5.5V, nIRQ set to be high-impedance (i.e., no interrupts), V_{nIRQ} = 0V and 5.5V	T_A = +85°C		±0.01		

Electrical Characteristics—Top-Level (continued)

(V_{SYS} = V_{INx} = 7.4V, single-phase configuration (1+1+1+1)Φ, V_{IO} = 1.8V, V_{LDO} = 1.8V, listed conditions apply to all bucks, T_A = T_J = -40°C to +125°C, typical values are at T_A = T_J = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL PURPOSE INPUTS/OUTPUTS (GPIO)							
GPIO Supply Voltage					V_{IO}		V
Input Voltage Low	V_{GPI-LO}	V_{IO} = 1.8V				0.22 x V_{IO}	V
		V_{IO} = 3.3V				0.3 x V_{IO}	
Input Voltage High	V_{GPI-HI}	V_{IO} = 1.8V		0.78 x V_{IO}			V
		V_{IO} = 3.3V		0.7 x V_{IO}			
Input Leakage Current	$I_{GPI-LKG}$	General-purpose input, V_{IO} = 5.5V, V_{GPIO} = 0V and 5.5V, per GPIO	T_A = +25°C	-1	±0.001	+1	µA
			T_A = +85°C		±0.01		
Output Voltage Low	V_{GPO-LO}	Sinking 2mA				0.4	V
Output Voltage High	V_{GPO-HI}	Sourcing 1mA		0.8 x V_{IO}			V
Input Debounce Time	t_{DB-GPI}	DBNC_SELx[1:0] = 0b01			0.11		ms
		DBNC_SELx1:0] = 0b10			0.24		
		DBNC_SELx[1:0] = 0b11			1		
Pullup Resistance	$R_{GPIO-PU}$	Internal pullup enabled to V_{IO} (PUx = 1)			100		kΩ
Pulldown Resistance	$R_{GPIO-PD}$	Internal pulldown enabled to DGND (PDx = 1)			100		kΩ
DEDICATED INTERNAL SUPPLIES							
V_{L13}, V_{L24} Regulator Voltage	V_L	(Note 4)			1.8		V
V_{DD} Regulator Voltage	V_{DD}	(Note 4)			1.8		V
THERMAL PROTECTION							
Thermal Alarm 1	T_{J120}	T_J rising, 15°C hysteresis			+120		°C
Thermal Alarm 2	T_{J140}	T_J rising, 15°C hysteresis			+140		°C
Over-Temperature Lockout (OTLO)	T_{OTLO}	T_J rising, 15°C hysteresis			+165		°C

Note 2: The MAX77511/MAX77711 is tested under pulsed load conditions such that $T_J \approx T_A$. Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range (T_J = -40°C to +125°C) are guaranteed by design and characterization using statistical process control methods. Note that the maximum ambient temperature consistent with this specification is determined by specific operating conditions, board layout, rated package thermal impedance, and other environmental factors.

Note 3: Supply current = I_{SYS} + I_{IN1} + I_{IN2} + I_{IN3} + I_{IN4}. Output voltage condition corresponds to factory option 711A defaults. See the *Ordering Information* table.

Note 4: See the *Dedicated Internal Supplies* section of the data sheet.

Electrical Characteristics—Quad-Channel Configurable Buck Regulator

(V_{SYS} = V_{INx} = 7.4V, single-phase configuration (1+1+1+1)Φ, V_{IO} = 1.8V, V_{LDO} = 1.8V, listed conditions apply to all bucks, T_A = T_J = -40°C to +125°C, typical values are at T_A = T_J = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
OUTPUT VOLTAGE							
Output Voltage Regulation Range	$V_{OUT-REGx}$	Low-range (RNGx = 0)	Programmable with VOUTREGx[7:0] in 5mV steps	0.25		1.3	V
		High-range (RNGx = 1)	Programmable with VOUTREGx[7:0] bitfield in 20mV steps	1		5.2	
Output Voltage Accuracy	V_{OUT}	I_{LOAD} = 0mA, Forced-PWM Mode, V_{OUT} = trim target (Note 5)	RNGx = 0, V_{OUT} ≥ 0.5V, T_A = +25°C	-0.3		+0.3	%
			RNGx = 0, V_{OUT} ≥ 0.5V, T_A = -40°C to +85°C	-1.1		+1.1	
			RNGx = 1, V_{OUT} ≥ 2V, T_A = +25°C	-0.3		+0.3	
			RNGx = 1, V_{OUT} ≥ 2V, T_A = -40°C to +85°C	-1.1		+1.1	
Output Voltage End-of-Range Accuracy	V_{OUT}	I_{LOAD} = 0mA, Forced-PWM Mode, T_A = -40ºC to +85°C	V_{OUT} = 0.25V and 1.3V, RNGx = 0	-15		+15	mV
			V_{OUT} = 1V and 5.2V, RNGx = 1	-60		+60	
Load Regulation		4Φ Configuration, Forced-PWM mode, I_{LOAD} = 0A to 12A			0.1		%/A
Line Regulation		V_{IN} = 2.3V to 10V, I_{OUT} = 0mA, Forced-PWM mode		-0.1		+0.1	%/V
SWITCHING CHARACTERISTICS							
High-Side MOSFET Peak Current Limit	$I_{PEAK-HSx}$	ILIMx[1:0] = 0b00		1.3	1.5	1.7	A
		ILIMx[1:0] = 0b01		2.025	2.25	2.475	
		ILIMx[1:0] = 0b10		2.7	3	3.3	
		ILIMx[1:0] = 0b11		4.05	4.5	4.95	
Low-Side MOSFET Valley Current Limit	$I_{VALLEYx}$	Tracks $I_{PEAK-HSx}$			$I_{PEAK-HSx}$ - 1A		A
Low-Side MOSFET Negative Current Limit	I_{NEG}	Forced-PWM mode		-3.6	-3.0	-2.4	A
Low-Side MOSFET Zero-Crossing Current Threshold	I_{ZX}	SKIP or Turbo SKIP mode		50	115	170	mA
LXx Leakage Current	I_{LX-LKG}	Per phase	V_{LXx} = 0V or 10V, T_A = +25°C		0.1	1	µA
			V_{LXx} = 0V or 10V, T_A = -40°C to +85°C		1		
High-Side MOSFET On-Resistance	R_{ON-HS}	Per phase	I_{LXx} = 190mA		37	74	mΩ

Electrical Characteristics—Quad-Channel Configurable Buck Regulator (continued)

(V_{SYS} = V_{INx} = 7.4V, single-phase configuration (1+1+1+1)Φ, V_{IO} = 1.8V, V_{LDO} = 1.8V, listed conditions apply to all bucks, T_A = T_J = -40°C to +125°C, typical values are at T_A = T_J = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Low-Side MOSFET On-Resistance	R_{ON-LS}	Per phase	I_{LXx} = -190mA		14	28	mΩ
Switching Frequency	F_{SW}	Per phase, nominal (Note 6)	RNG = 0, V_{OUT} = 1.1V, FPWM mode, no load, T_A = +25°C		1		MHz
Minimum Switching Frequency	F_{SW-MIN}	SKIP or Turbo SKIP mode, 711A factory option		3.7	3.9	4.1	kHz
Maximum Duty Cycle	D_{MAX}	Dropout, V_{OUT} below regulation target			98		%
SPREAD-SPECTRUM MODULATION							
Modulation Frequency	F_{SSMOD}	Profile 1			3.0		kHz
		Profile 2			5.0		
		Profile 3			7.0		
Modulation Envelope	ΔF_{SW}	All profiles			±8		%
FEEDBACK AND CONFIGURATION							
PHCFGx Input Voltage High	$V_{PHCFG-HI}$			0.8 x V_{DD}			V
PHCFGx Input Voltage Low	$V_{PHCFG-LO}$					0.2 x V_{DD}	V
PHCFGx Input Leakage Current	$I_{PHCFG-LKG}$	V_{DD} = 1.8V, V_{PHCFGx} = 0V and 1.8V	T_A = +25°C	-1	±0.001	+1	µA
			T_A = +85°C		±0.01		
OUTPUT VOLTAGE RAMP RATES							
Soft-Start, Soft-Stop, DVS Ramp Rate Accuracy		Root clock accuracy		-5		+5	%
Soft-Start, Soft-Stop, DVS Ramp Rate (Note 7)	$\Delta V_{OUTx}/\Delta t$	SFTUPDNx[2:0] = DVSRISEx[2:0] = DVSFALLx[2:0] = 0b000			0.15		mV/µs
		SFTUPDNx[2:0] = DVSRISEx[2:0] = DVSFALLx[2:0] = 0b001			0.625		
		SFTUPDNx[2:0] = DVSRISEx[2:0] = DVSFALLx[2:0] = 0b010			1.25		
		SFTUPDNx[2:0] = DVSRISEx[2:0] = DVSFALLx[2:0] = 0b011			2.5		
		SFTUPDNx[2:0] = DVSRISEx[2:0] = DVSFALLx[2:0] = 0b100			5		
		SFTUPDNx[2:0] = DVSRISEx[2:0] = DVSFALLx[2:0] = 0b101			10		
		SFTUPDNx[2:0] = DVSRISEx[2:0] = DVSFALLx[2:0] = 0b110			20		
		SFTUPDNx[2:0] = DVSRISEx[2:0] = DVSFALLx[2:0] = 0b111			40		

Electrical Characteristics—Quad-Channel Configurable Buck Regulator (continued)

(V_{SYS} = V_{INx} = 7.4V, single-phase configuration (1+1+1+1)Φ, V_{IO} = 1.8V, V_{LDO} = 1.8V, listed conditions apply to all bucks, T_A = T_J = -40°C to +125°C, typical values are at T_A = T_J = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DVS Ramp Delay	t_{DVSDLY}	Measured from DVS input (GPIO assigned special function) rising edge to first LX pulse, GPIO debounce filter disabled (DBNC_SELx[1:0] = 0) (Note 8)			3		µs
Startup Ramp Delay	t_{SUDLY}	Measured from BEN input (GPIO assigned special function) rising edge to first LX pulse, GPIO debounce filter disabled (DBNC_SELx[1:0] = 0b00)	V_{L13}/V_{L24} regulators pre-enabled (FVLEN = 1)		10	40	µs
			V_{L13}/V_{L24} regulators not pre-enabled (FVLEN = 0)		50		
LX Active Discharge Resistance	R_{LX-AD}	Buck regulator disabled, active discharge resistor enabled (ADENx = 1), resistance from LXx to corresponding PGNDx, per phase			100	170	Ω
OVERCURRENT PROTECTION							
Power-OK Threshold	V_{POK-R}	V_{OUTx} rising, expressed as a percentage of $V_{OUT-REGx}$		77	82	87	%
	V_{POK-F}	V_{OUTx} falling, expressed as a percentage of $V_{OUT-REGx}$		73	78	83	
Hard-Short Detection Threshold	V_{SCP}	V_{OUTx} falling, expressed as a percentage of target voltage ($V_{OUT-REGx}$)			20		%
Soft-Short Shutdown Timer	$t_{SFTSHRT}$	SCPWARN_TIME[1:0] = 0b01			25		ms
		SCPWARN_TIME[1:0] = 0b10			50		
		SCPWARN_TIME[1:0] = 0b11			100		
nRSTIO Input Voltage Low	$V_{nRSTI-LO}$	V_{DD} = 1.8V				0.3 x V_{DD}	V
nRSTIO Input Voltage High	$V_{nRSTI-HI}$	V_{DD} = 1.8V		0.7 x V_{DD}			V
nRSTIO Output Voltage Low	$V_{nRSTO-LO}$	Sinking 2mA				0.4	V
nRSTIO Input Leakage	$I_{nRSTIO-LKG}$	V_{DD} = 1.8V, V_{nRSTIO} = 3.3V and 0V	T_A = +25°C	-1	±0.001	+1	µA
			T_A = +85°C		±0.01		
nRSTIO Input Glitch Filter					100		µs
OUTPUT CURRENT MONITOR (AMUX)							
Full-Scale Voltage	V_{FS}				1		V
Output Current Monitor Gain	G_{DCIMON}				1.0/3.0		V/A
DC Current Monitor Accuracy		Per phase, V_{OUT} = 1.0V, T_A = +25°C	I_{LOAD} = 1A	-30		+30	%
			I_{LOAD} = 3A	-10		+10	
Channel Switching Time		Includes signal settling time (Note 9)			0.2		ms

Electrical Characteristics—Quad-Channel Configurable Buck Regulator (continued)

(V_{SYS} = V_{INx} = 7.4V, single-phase configuration (1+1+1+1)Φ, V_{IO} = 1.8V, V_{LDO} = 1.8V, listed conditions apply to all bucks, T_A = T_J = -40°C to +125°C, typical values are at T_A = T_J = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Off Leakage Current		V_{AMUX} = 0V, AMUX is high impedance	T_A = +25°C		1	500	nA
			T_A = +85°C		1		µA

Note 5: See the *Ordering Information* table for V_{OUT} trim targets associated with each part number.

Note 6: Switching frequency is not set by a clock oscillator. F_{SW} varies depending on input voltage, output voltage, load, and spread-spectrum settings.

Note 7: Soft-start, soft-stop, DVS rising, and DVS falling ramps are all controlled by the same internal digital-to-analog converter circuit and share the same test set. Soft-start and soft-stop share the same control bits and are equal in magnitude but opposite in direction. DVS rising and DVS falling ramps are independently controlled. See the *Register Map* for details.

Note 8: Digitally debounced for three consecutive 1µs clock periods. Typical debounce time is at least 3µs and up to 4µs due to synchronization to the digital clock.

Note 9: Not production tested. Design guidance only.

Electrical Characteristics—Linear Regulator (MAX77711 Only)

(V_{SYS} = 7.4V, V_{INLDO} = 3.3V, V_{LDO} = 1.8V, C_{INLDO} = 10µF, C_{LDO} = 2.2µF, T_A = T_J = -40°C to +125°C, typical values are at T_A = T_J = +25°C, MAX77711 only, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LDO (MAX77711 Only)							
INLDO Voltage Range	V_{INLDO}			1.25		5.5	V
INLDO Undervoltage Lockout Threshold	$V_{INLDO-UVLO}$	DC rising (130mV hysteresis)		1.15	1.2	1.25	V
INLDO Shutdown Current	$I_{INLDO-SHDN}$	LDO disabled			0.1		µA
INLDO Supply Current	$I_{INLDO-Q}$	V_{LDO} = 1.8V, no load			20		µA
LDO Output Voltage Range	$V_{LDO-REG}$	Target regulation voltage, programmable in 25mV steps with LDO_VREG[6:0]		0.4		1.975	V
LDO Output Voltage Accuracy	V_{LDO}	V_{INLDO} = V_{LDO} + 0.3V to 5.5V, across all $V_{LDO-REG}$ settings, I_{LDO} = 0.1mA to 300mA, T_A = -40°C to +85°C		-2		+2	%
LDO Maximum Output Current	I_{LDO}	(Note 10)		300			mA
Load Regulation		V_{INLDO} = V_{LDO} + 0.3V to 5.5V, across all $V_{LDO-REG}$ settings, I_{LDO} = 0.1mA to 300mA			0.5		%
Line Regulation		I_{LDO} = 0.1mA, V_{INLDO} = V_{LDO} + 0.3V to 5.5V, across all $V_{LDO-REG}$ settings			0.05		%/V
Dropout Voltage	V_{DO}	I_{LDO} = 300mA (Note 11)	V_{INLDO} = 1.7V, $V_{LDO-REG}$ = 1.85V		120		mV
LDO Current Limit		V_{LDO} = 90% of programmed target		320	550	1000	mA
LDO Output Capacitance for Stability	C_{LDO}	(Note 12)		2.2	4.7		µF
LDO Startup Ramp Rate	$\Delta V_{LDO}/\Delta t$	10% to 90% of final value			4		mV/µs

Electrical Characteristics—Linear Regulator (MAX77711 Only) (continued)

(V_{SYS} = 7.4V, V_{INLDO} = 3.3V, V_{LDO} = 1.8V, C_{INLDO} = 10µF, C_{LDO} = 2.2µF, T_A = T_J = -40°C to +125°C, typical values are at T_A = T_J = +25°C, MAX77711 only, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Noise		f = 10Hz to 100kHz, I_{LDO} = 15mA	V_{INLDO} = 2.7V, V_{LDO} = 1V		137		μV_{RMS}
			V_{INLDO} = 3.7V, V_{LDO} = 1V		138		
			V_{INLDO} = 5.5V, V_{LDO} = 1V		133		
Power-Supply Rejection Ratio	PSRR	V_{INLDO} = 3.3V + 20mV_{P-P}, f = 10Hz to 10kHz, V_{LDO} = 0.8V, I_{LDO} = 30mA			75		dB
Active Discharge Resistance	R_{AD_LDO}				100		Ω
Power-OK Threshold	$V_{POKLDO-R}$	V_{LDO} rising, expressed as a percentage of $V_{LDO-REG}$		87	92	97	%
	$V_{LDOPOK-F}$	V_{LDO} falling, expressed as a percentage of $V_{LDO-REG}$		85	90	95	

Note 10: Guaranteed by the Output Voltage Accuracy tests.

Note 11: The dropout voltage is the difference between the input voltage and the output voltage when the input voltage is within the valid input voltage range, but below the output voltage setpoint. For example, if the output voltage setpoint is 1.85V, the input voltage is 1.7V, and the actual output voltage is 1.65V, then the dropout voltage is 50mV (V_{DO} = V_{INLDO} - V_{LDO}).

Note 12: For stability, guaranteed by design and not production tested.

Electrical Characteristics—I²C Serial Interface

(V_{SYS} = 7.4V, V_{IO} = 1.8V, all GPIOs unconnected, T_A = T_J = -40°C to +125°C, typical values are at T_A = T_J = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I/O Stage						
V_{IO} Voltage Range	V_{IO}		1.65		5.5	V
V_{IO} Valid Threshold	$V_{IO-VALID}$	DC Rising	1.25	1.5	1.65	V
V_{IO} Valid Threshold Hysteresis				200		mV
V_{IO} Bias Current		T_A = +25°C, all GPIOs unconnected	-1	0	+1	µA
SCL, SDA Input HIGH Voltage	V_{IH}		1.44			V
SCL, SDA Input LOW Voltage	V_{IL}				0.54	V
SCL, SDA Input Hysteresis	V_{HYS}			0.3		V
SCL, SDA Input Leakage Current	I_I	V_{IO} = 5.5V, V_{SCL} = V_{SDA} = 0V or 5.5V	-10		+10	µA
SDA Output Low Voltage	V_{OL}	Sinking 20mA			0.4	V
SCL, SDA Pin Capacitance		(Note 9)		10		pF

Electrical Characteristics—I²C Serial Interface (continued)

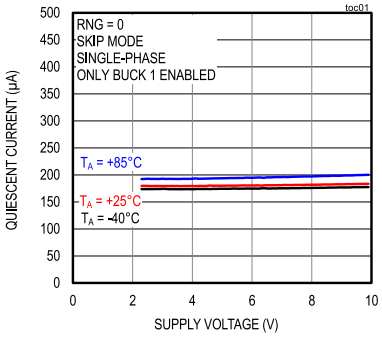
(V_{SYS} = 7.4V, V_{IO} = 1.8V, all GPIOs unconnected, T_A = T_J = -40°C to +125°C, typical values are at T_A = T_J = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING (STANDARD, FAST, AND FAST-MODE PLUS)						
Clock Frequency	f_{SCL}				1	MHz
Bus Free Time between STOP and START Condition	t_{BUF}		0.5			µs
Setup Time REPEATED START Condition	$t_{SU;STA}$		260			ns
Hold Time REPEATED START Condition	$t_{HD;STA}$		260			ns
SCL LOW Period	t_{LOW}		500			ns
SCL HIGH Period	t_{HIGH}		260			ns
Data Setup Time	$t_{SU;DAT}$		50			ns
Data Hold Time	$t_{HD;DAT}$		0			µs
Setup Time for STOP Condition	$t_{SU;STO}$		260			ns
Input Filter Suppressed Spike Pulse Width	t_{SP}	(Note 9)		50		ns
TIMING (HIGH-SPEED MODE)						
Clock Frequency	f_{SCL}	High-speed mode			3.4	MHz
Setup Time REPEATED START Condition	$t_{SU;STA}$		160			ns
Hold Time REPEATED START Condition	$t_{HD;STA}$		160			ns
SCL LOW Period	t_{LOW}		160			ns
SCL HIGH Period	t_{HIGH}		60			ns
Data Setup Time	$t_{SU;DAT}$		10			ns
Data Hold Time	$t_{HD;DAT}$		0			µs
Setup Time for STOP Condition	$t_{SU;STO}$		160			ns
Input Filter Suppressed Spike Pulse Width	t_{SP}	(Note 9)		10		ns

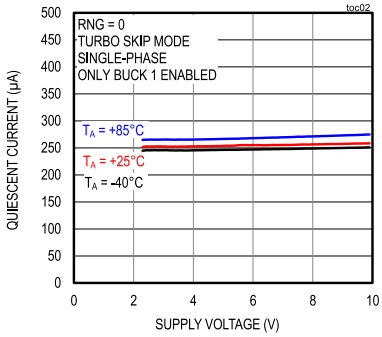
Typical Operating Characteristics

(V_{INx} = V_{SYS} = 7.4V, V_{OUT} = 1.2V, single-phase configuration, RNGx = 0, L = 0.47µH (Murata 2520 metric case size), Turbo SKIP mode, transient performance option on, $I_{PEAK-HSx}$ = 4.5A, T_A = +25°C, unless otherwise noted.)

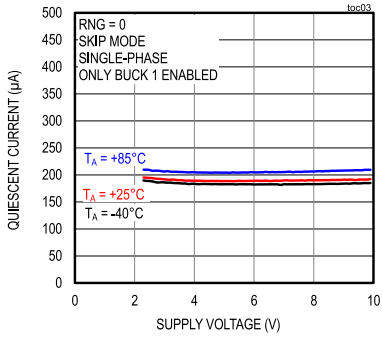
QUIESCENT CURRENT vs. SUPPLY VOLTAGE 0.6V OUTPUT



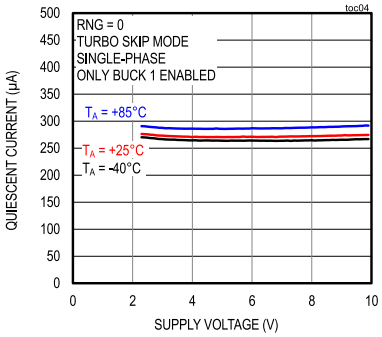
QUIESCENT CURRENT vs. SUPPLY VOLTAGE 0.6V OUTPUT



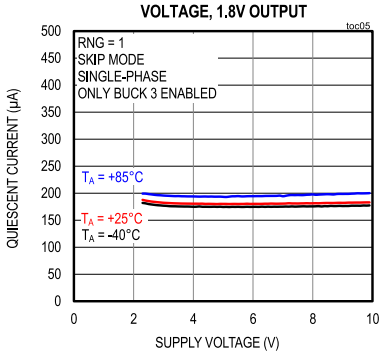
QUIESCENT CURRENT vs. SUPPLY VOLTAGE 1.2V OUTPUT



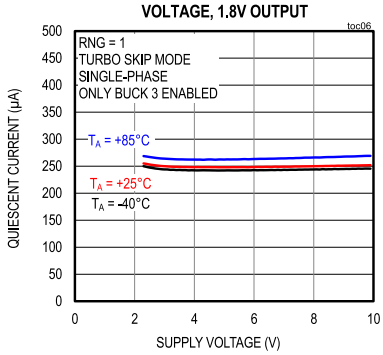
QUIESCENT CURRENT vs. SUPPLY VOLTAGE 1.2V OUTPUT



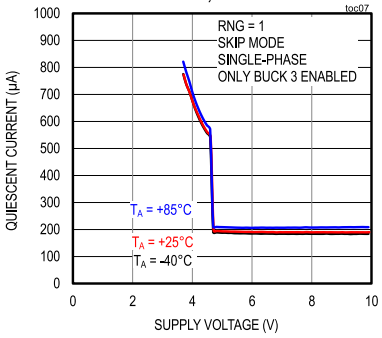
QUIESCENT CURRENT vs. SUPPLY VOLTAGE, 1.8V OUTPUT



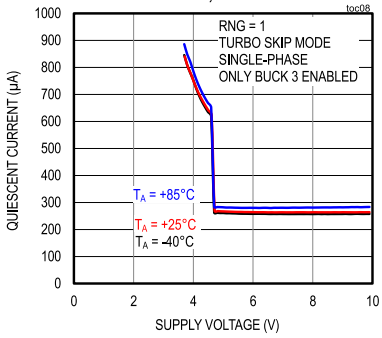
QUIESCENT CURRENT vs. SUPPLY VOLTAGE, 1.8V OUTPUT



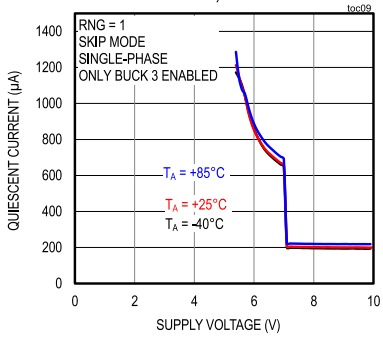
QUIESCENT CURRENT vs. SUPPLY VOLTAGE, 3.3V OUTPUT



QUIESCENT CURRENT vs. SUPPLY VOLTAGE, 3.3V OUTPUT



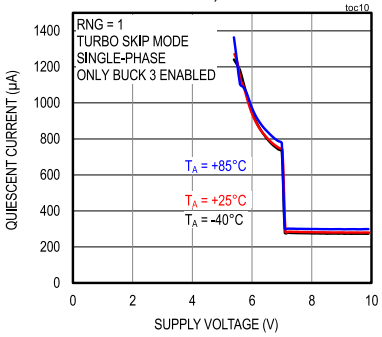
QUIESCENT CURRENT vs. SUPPLY VOLTAGE, 5V OUTPUT



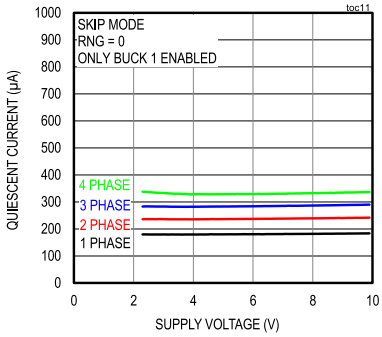
Typical Operating Characteristics (continued)

(V_{INx} = V_{SYS} = 7.4V, V_{OUT} = 1.2V, single-phase configuration, RNGx = 0, L = 0.47µH (Murata 2520 metric case size), Turbo SKIP mode, transient performance option on, $I_{PEAK-HSx}$ = 4.5A, T_A = +25°C, unless otherwise noted.)

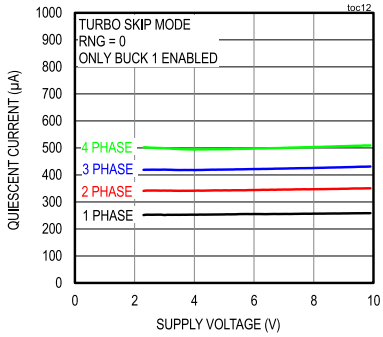
QUIESCENT CURRENT vs. SUPPLY VOLTAGE, 5V OUTPUT



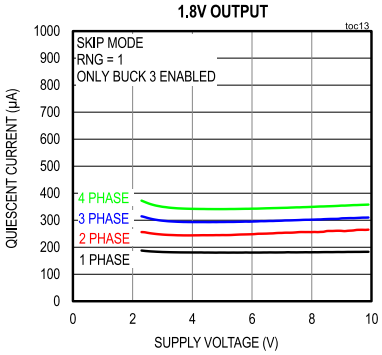
QUIESCENT CURRENT vs. SUPPLY VOLTAGE vs. PHASE 0.6V OUTPUT



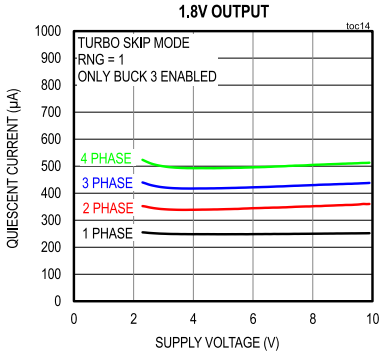
QUIESCENT CURRENT vs. SUPPLY VOLTAGE vs. PHASE 0.6V OUTPUT



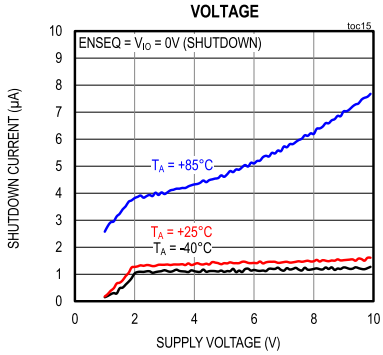
QUIESCENT CURRENT vs. SUPPLY VOLTAGE vs. PHASE 1.8V OUTPUT



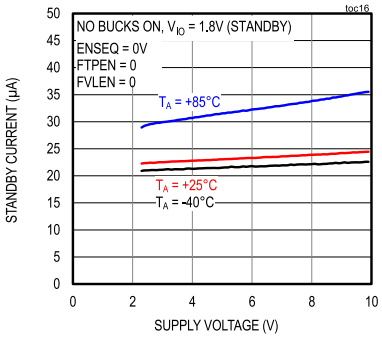
QUIESCENT CURRENT vs. SUPPLY VOLTAGE vs. PHASE 1.8V OUTPUT



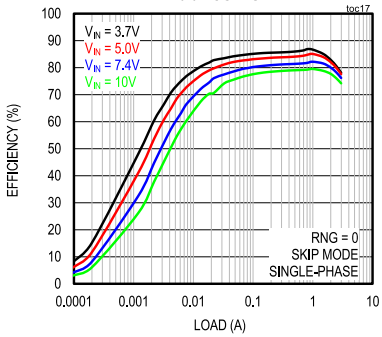
SHUTDOWN CURRENT vs. SUPPLY VOLTAGE



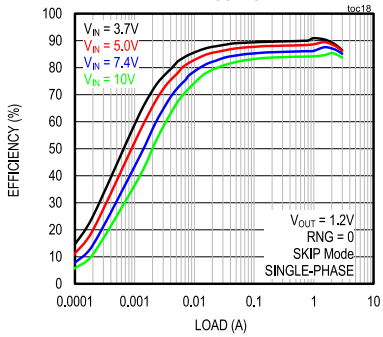
STANDBY CURRENT vs. SUPPLY VOLTAGE



EFFICIENCY vs. LOAD 0.6V OUTPUT



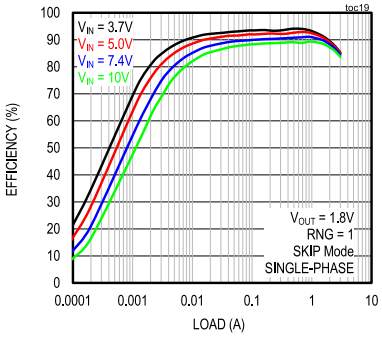
EFFICIENCY vs. LOAD 1.2V OUTPUT



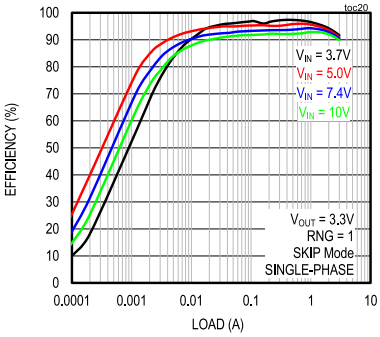
Typical Operating Characteristics (continued)

(V_{INx} = V_{SYS} = 7.4V, V_{OUT} = 1.2V, single-phase configuration, RNGx = 0, L = 0.47µH (Murata 2520 metric case size), Turbo SKIP mode, transient performance option on, $I_{PEAK-HSx}$ = 4.5A, T_A = +25°C, unless otherwise noted.)

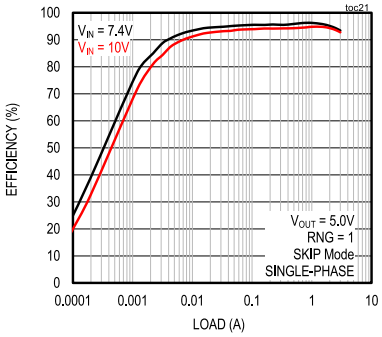
EFFICIENCY vs. LOAD
1.8V OUTPUT



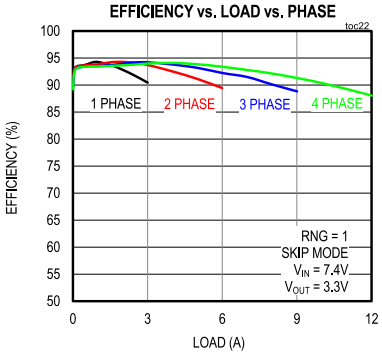
EFFICIENCY vs. LOAD
3.3V OUTPUT



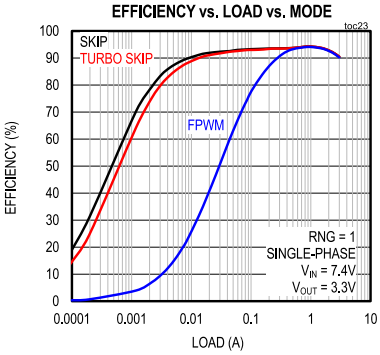
EFFICIENCY vs. LOAD
5V OUTPUT



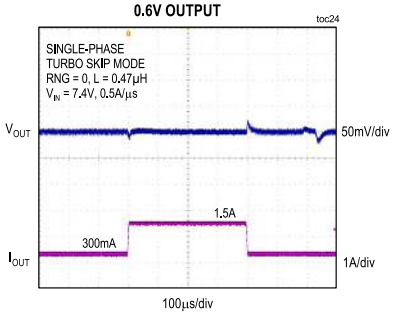
EFFICIENCY vs. LOAD vs. PHASE



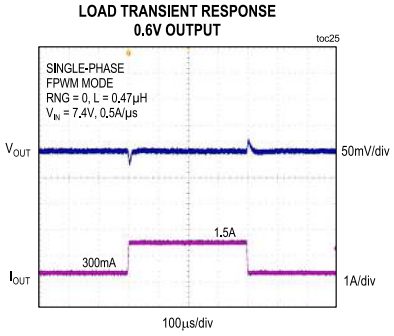
EFFICIENCY vs. LOAD vs. MODE



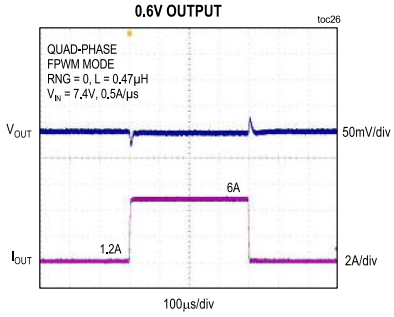
LOAD TRANSIENT RESPONSE
0.6V OUTPUT



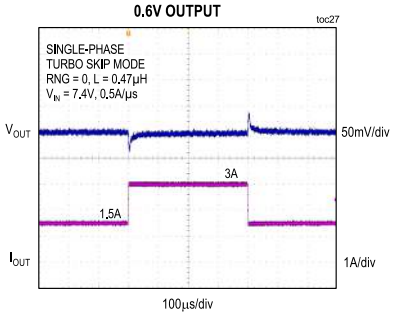
LOAD TRANSIENT RESPONSE
0.6V OUTPUT



LOAD TRANSIENT RESPONSE
0.6V OUTPUT



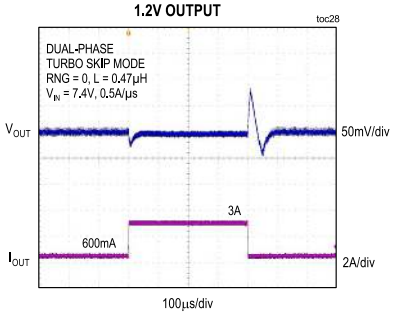
LOAD TRANSIENT RESPONSE
0.6V OUTPUT



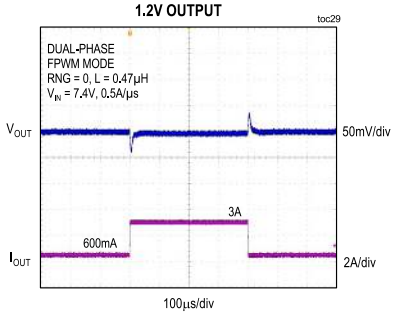
Typical Operating Characteristics (continued)

(V_{INx} = V_{SYS} = 7.4V, V_{OUT} = 1.2V, single-phase configuration, RNGx = 0, L = 0.47µH (Murata 2520 metric case size), Turbo SKIP mode, transient performance option on, $I_{PEAK-HSx}$ = 4.5A, T_A = +25ºC, unless otherwise noted.)

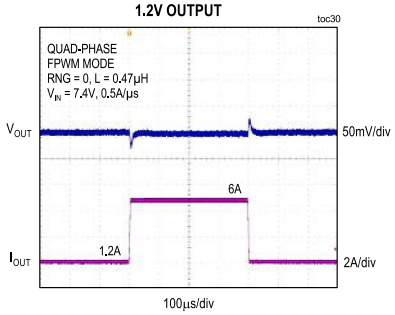
LOAD TRANSIENT RESPONSE
1.2V OUTPUT



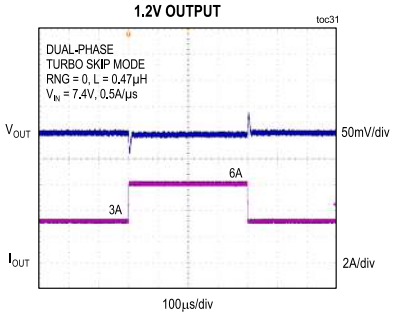
LOAD TRANSIENT RESPONSE
1.2V OUTPUT



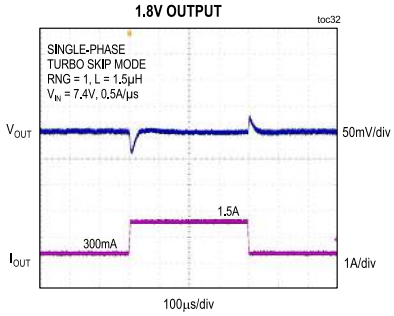
LOAD TRANSIENT RESPONSE
1.2V OUTPUT



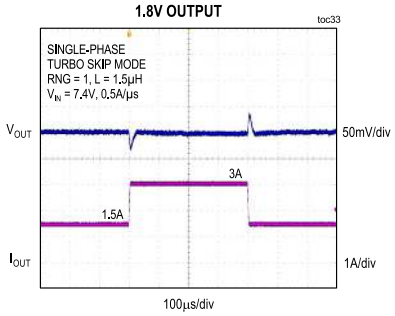
LOAD TRANSIENT RESPONSE
1.2V OUTPUT



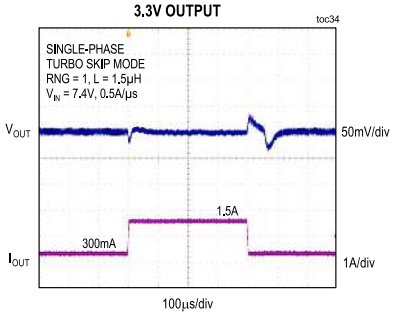
LOAD TRANSIENT RESPONSE
1.8V OUTPUT



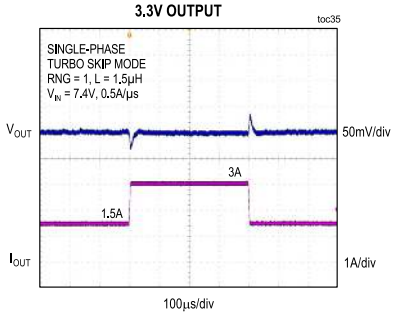
LOAD TRANSIENT RESPONSE
1.8V OUTPUT



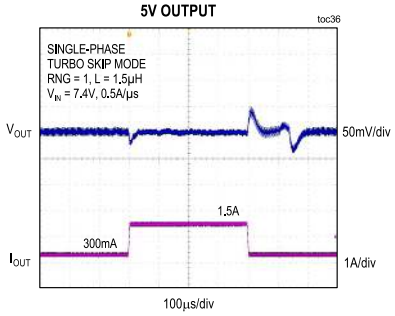
LOAD TRANSIENT RESPONSE
3.3V OUTPUT



LOAD TRANSIENT RESPONSE
3.3V OUTPUT



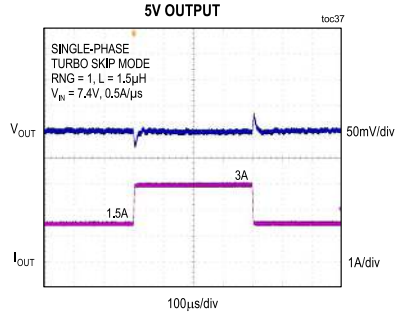
LOAD TRANSIENT RESPONSE
5V OUTPUT



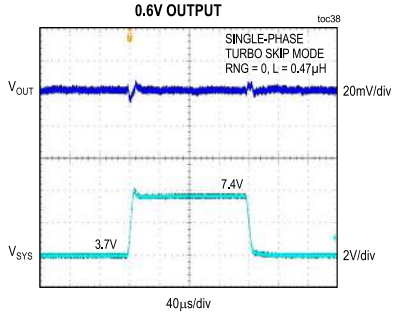
Typical Operating Characteristics (continued)

(V_{INx} = V_{SYS} = 7.4V, V_{OUT} = 1.2V, single-phase configuration, RNGx = 0, L = 0.47µH (Murata 2520 metric case size), Turbo SKIP mode, transient performance option on, $I_{PEAK-HSx}$ = 4.5A, T_A = +25ºC, unless otherwise noted.)

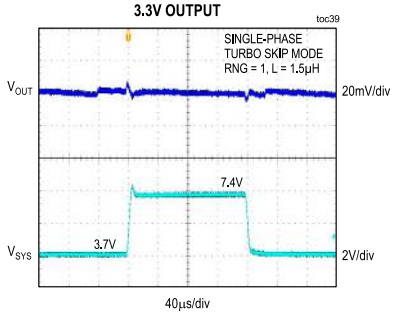
LOAD TRANSIENT RESPONSE
5V OUTPUT



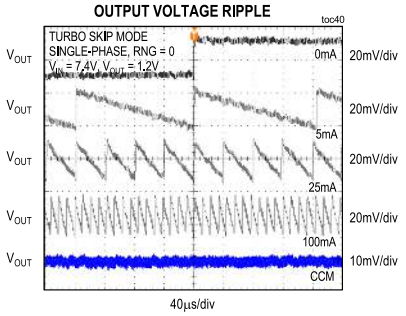
LINE TRANSIENT RESPONSE
0.6V OUTPUT



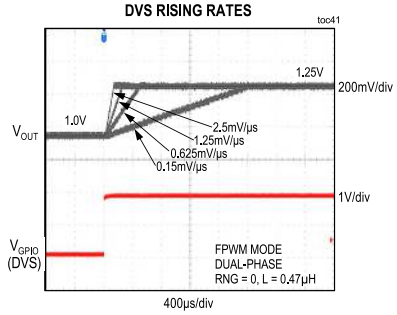
LINE TRANSIENT RESPONSE
3.3V OUTPUT



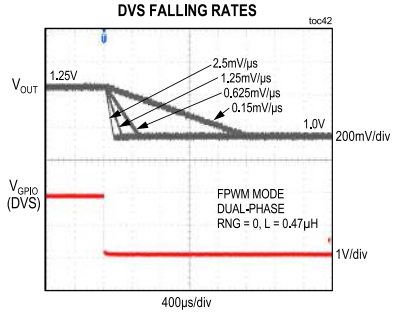
OUTPUT VOLTAGE RIPPLE



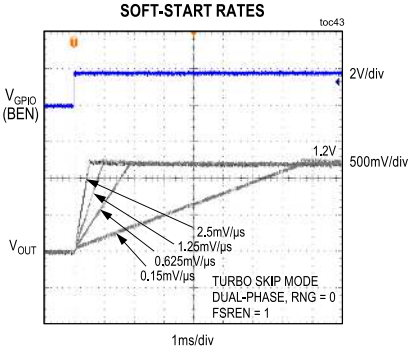
DVS RISING RATES



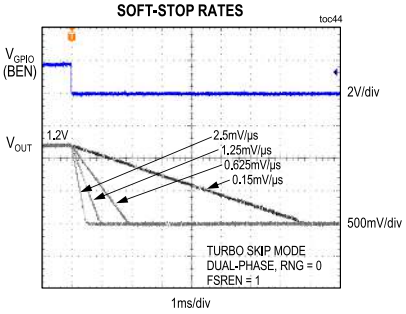
DVS FALLING RATES



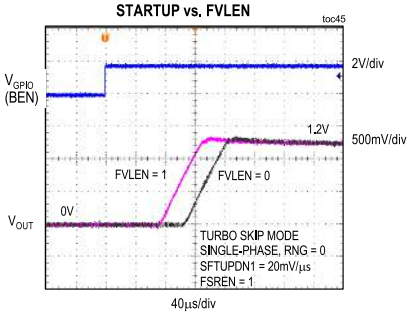
SOFT-START RATES



SOFT-STOP RATES



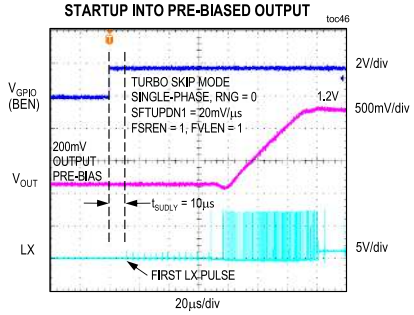
STARTUP vs. FVLEN



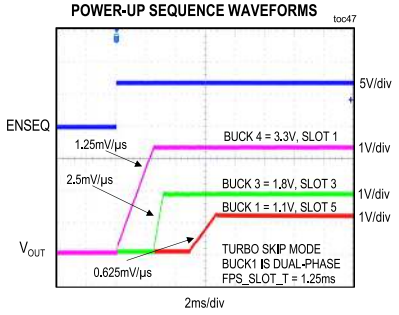
Typical Operating Characteristics (continued)

(V_{INx} = V_{SYS} = 7.4V, V_{OUT} = 1.2V, single-phase configuration, RNGx = 0, L = 0.47µH (Murata 2520 metric case size), Turbo SKIP mode, transient performance option on, $I_{PEAK-HSx}$ = 4.5A, T_A = +25ºC, unless otherwise noted.)

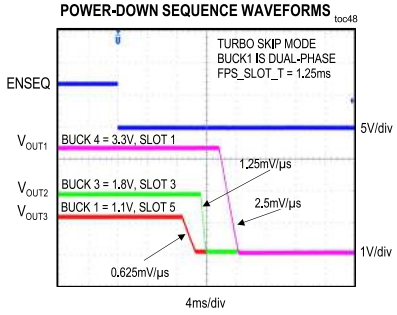
STARTUP INTO PRE-BIASED OUTPUT



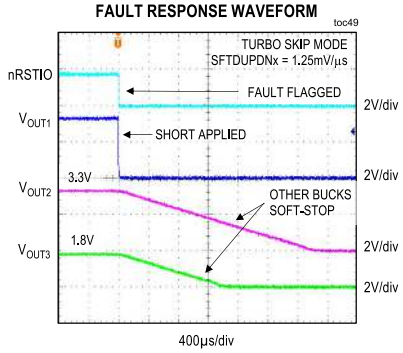
POWER-UP SEQUENCE WAVEFORMS



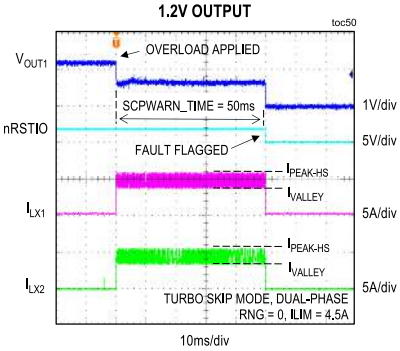
POWER-DOWN SEQUENCE WAVEFORMS



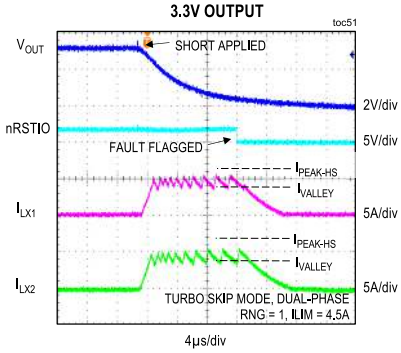
IMMEDIATE SHUTDOWN HARD-SHORT FAULT RESPONSE WAVEFORM



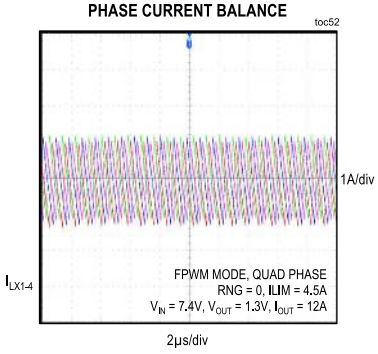
SOFT-SHORT RESPONSE WAVEFORM 1.2V OUTPUT



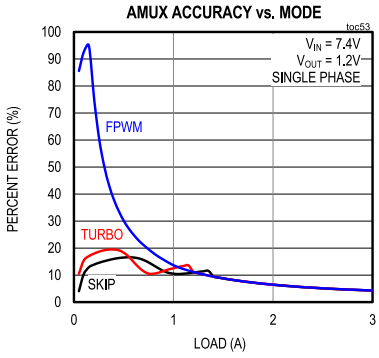
HARD-SHORT RESPONSE WAVEFORM 3.3V OUTPUT



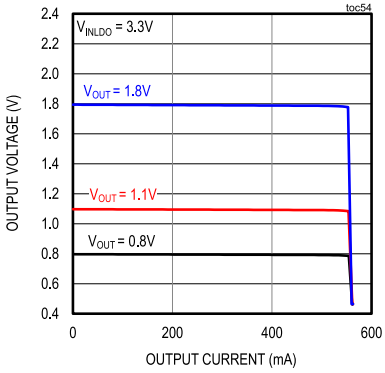
PHASE CURRENT BALANCE



AMUX ACCURACY vs. MODE



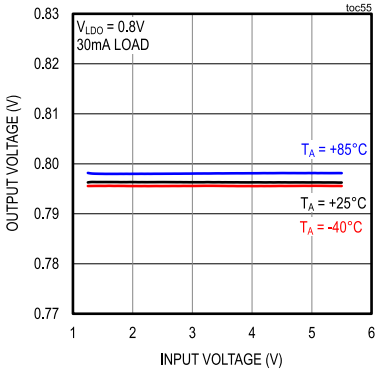
LDO LOAD REGULATION AND CURRENT LIMIT



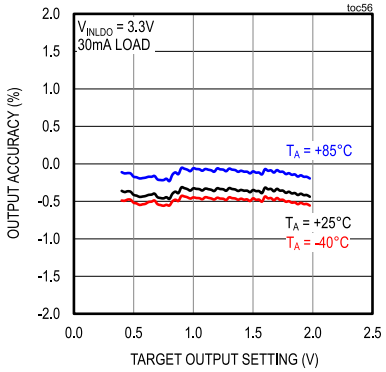
Typical Operating Characteristics (continued)

(V_{INx} = V_{SYS} = 7.4V, V_{OUT} = 1.2V, single-phase configuration, RNGx = 0, L = 0.47µH (Murata 2520 metric case size), Turbo SKIP mode, transient performance option on, $I_{PEAK-HSx}$ = 4.5A, T_A = +25°C, unless otherwise noted.)

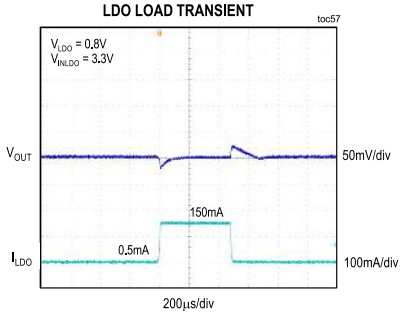
LDO LINE REGULATION



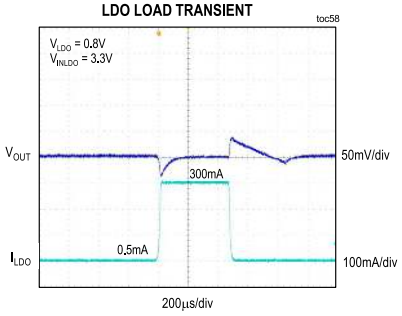
LDO OUTPUT ACCURACY vs. SETTING



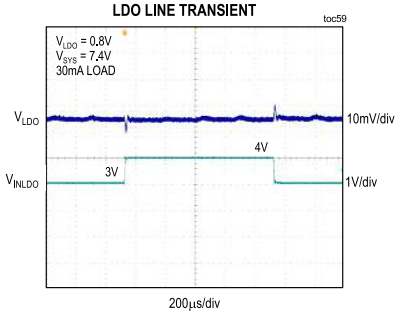
LDO LOAD TRANSIENT



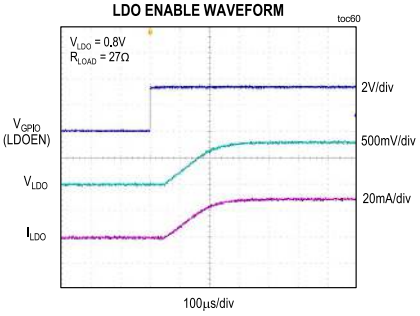
LDO LOAD TRANSIENT



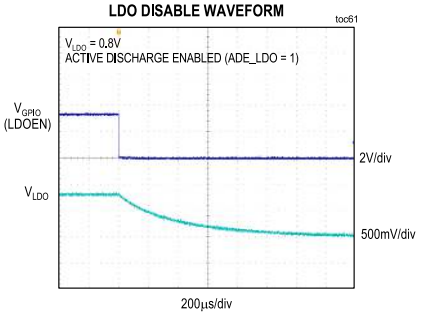
LDO LINE TRANSIENT



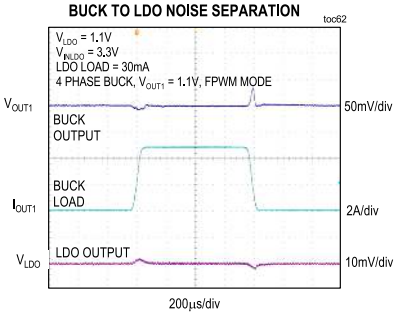
LDO ENABLE WAVEFORM



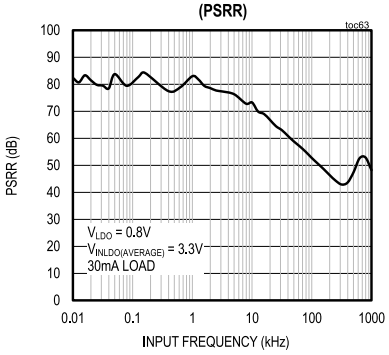
LDO DISABLE WAVEFORM



BUCK TO LDO NOISE SEPARATION

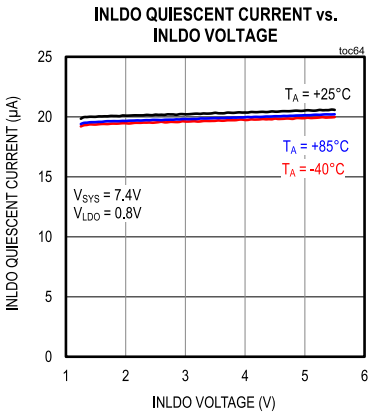


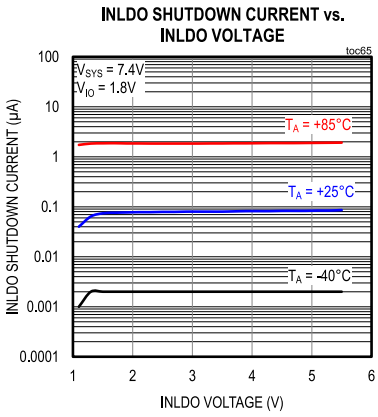
LDO POWER SUPPLY REJECTION RATIO (PSRR)



Typical Operating Characteristics (continued)

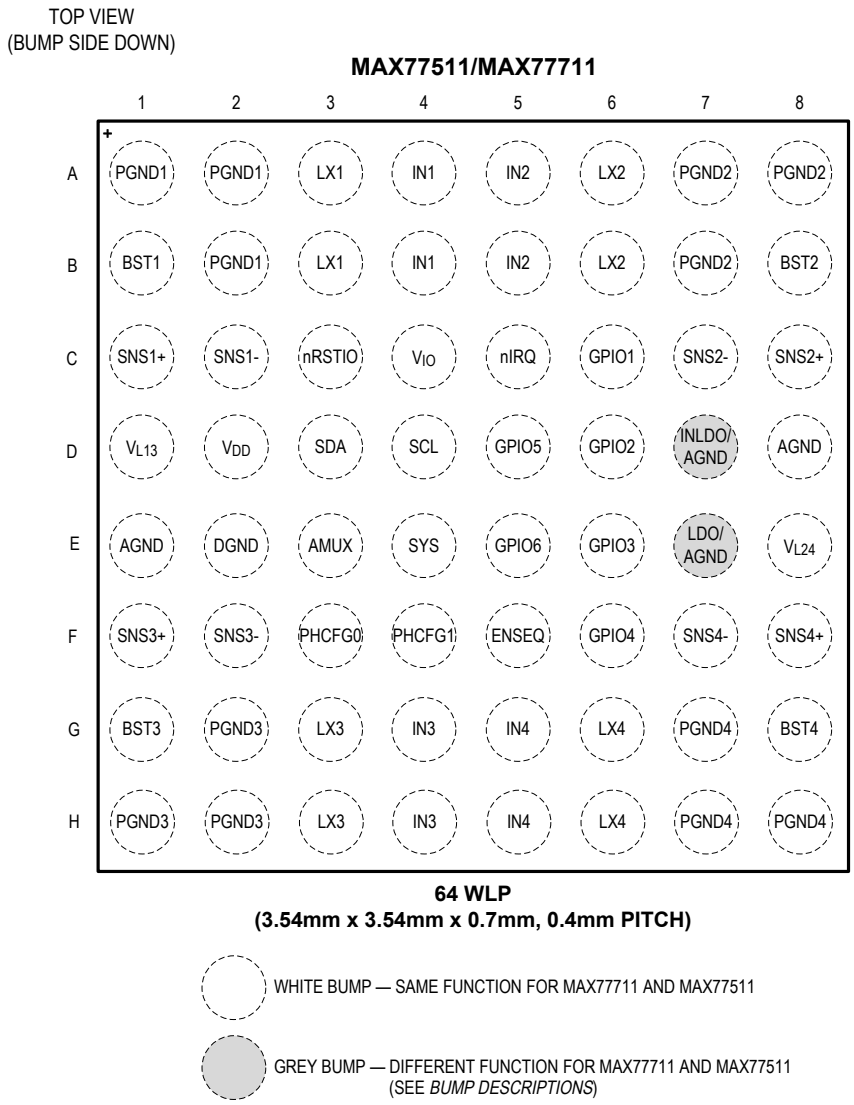
(V_{INx} = V_{SYS} = 7.4V, V_{OUT} = 1.2V, single-phase configuration, RNGx = 0, L = 0.47µH (Murata 2520 metric case size), Turbo SKIP mode, transient performance option on, $I_{PEAK-HSx}$ = 4.5A, T_A = +25ºC, unless otherwise noted.)





Bump Configuration

64 WLP



Bump Descriptions

PIN	NAME	FUNCTION	TYPE
BUCK SWITCHING PHASES			
A4, B4	IN1	Phase 1 Input. Bypass to PGND1 with a 10µF ceramic capacitor.	power input
A5, B5	IN2	Phase 2 Input. Bypass to PGND2 with a 10µF ceramic capacitor.	power input

Bump Descriptions (continued)

PIN	NAME	FUNCTION	TYPE
G4, H4	IN3	Phase 3 Input. Bypass to PGND3 with a 10µF ceramic capacitor.	power input
G5, H5	IN4	Phase 4 Input. Bypass to PGND4 with a 10µF ceramic capacitor.	power input
B1	BST1	Phase 1 High-Side FET Driver Supply. Connect a 0.1µF ceramic capacitor between BST1 and LX1.	power input
A3, B3	LX1	Phase 1 Switching Node	power I/O
B8	BST2	Phase 2 High-Side FET Driver Supply. Connect a 0.1µF ceramic capacitor between BST2 and LX2.	power input
A6, B6	LX2	Phase 2 Switching Node	power I/O
G1	BST3	Phase 3 High-Side FET Driver Supply. Connect a 0.1µF ceramic capacitor between BST3 and LX3.	power input
G3, H3	LX3	Phase 3 Switching Node	power I/O
G8	BST4	Phase 4 High-Side FET Driver Supply. Connect a 0.1µF ceramic capacitor between BST4 and LX4.	power input
G6, H6	LX4	Phase 4 Switching Node	power I/O
A1, A2, B2	PGND1	Phase 1 Power Ground. Connect to all other power grounds on the PCB.	ground
A7, A8, B7	PGND2	Phase 2 Power Ground. Connect to all other power grounds on the PCB.	ground
G2, H1, H2	PGND3	Phase 3 Power Ground. Connect to all other power grounds on the PCB.	ground
G7, H7, H8	PGND4	Phase 4 Power Ground. Connect to all other power grounds on the PCB.	ground
PHASE CONFIGURATION AND FEEDBACK			
C1	SNS1+	Buck 1 Output Voltage Positive Feedback Input. Connect to the output at the point-of-load.	analog input
C2	SNS1-	Buck 1 Output Voltage Negative Feedback Input. Connect to ground at the point-of-load.	analog input
C8	SNS2+	Buck 2 Output Voltage Positive Feedback Input. Connect to the output at the point-of-load. Connect to AGND if not used.	analog input
C7	SNS2-	Buck 2 Output Voltage Negative Feedback Input. Connect to ground at the point-of-load. Connect to AGND if not used.	analog input
F1	SNS3+	Buck 3 Output Voltage Positive Feedback Input. Connect to the output at the point-of-load. Connect to AGND if not used.	analog input
F2	SNS3-	Buck 3 Output Voltage Negative Feedback Input. Connect to ground at the point-of-load. Connect to AGND if not used.	analog input
F8	SNS4+	Buck 4 Output Voltage Positive Feedback Input. Connect to the output at the point-of-load. Connect to AGND if not used.	analog input
F7	SNS4-	Buck 4 Output Voltage Negative Feedback Input. Connect to ground at the point-of-load. Connect to AGND if not used.	analog input
F3	PHCFG0	Tri-State Phase Configuration Selection Input 0. Connect to V_{DD}, ground, or leave unconnected to configure the buck phases. See the *Phase Configuration* section of the data sheet for more information.	digital input
F4	PHCFG1	Tri-State Phase Configuration Selection Input 1. Connect to V_{DD}, ground, or leave unconnected to configure the buck phases. See the *Phase Configuration* section of the data sheet for more information.	digital input
GENERAL PURPOSE INPUTS/OUTPUTS			
C6	GPIO1	General-Purpose Input/Output. Powered from V_{IO}. Mappable to *Special Functions*.	digital I/O

Bump Descriptions (continued)

PIN	NAME	FUNCTION	TYPE
D6	GPIO2	General-Purpose Input/Output. Powered from V_{IO}. Mappable to *Special Functions*.	digital I/O
E6	GPIO3	General-Purpose Input/Output. Powered from V_{IO}. Mappable to *Special Functions*.	digital I/O
F6	GPIO4	General-Purpose Input/Output. Powered from V_{IO}. Mappable to *Special Functions*.	digital I/O
D5	GPIO5	General-Purpose Input/Output. Powered from V_{IO}. Mappable to *Special Functions*.	digital I/O
E5	GPIO6	General-Purpose Input/Output. Powered from V_{IO}. Mappable to *Special Functions*.	digital I/O
I²C SERIAL INTERFACE			
C4	V_{IO}	I²C Serial Interface and GPIO Voltage Supply. Registers are held in reset when this pin's voltage is invalid.	power input
D3	SDA	I²C Serial Interface Data	digital I/O
D4	SCL	I²C Serial Interface Clock	digital input
DEDICATED INTERNAL SUPPLIES			
E4	SYS	System Voltage Input. Power input to the internal V_L and V_{DD} linear regulators. Bypass to AGND with a 2.2µF ceramic capacitor. See Figure 16.	power input
D1	V_{L13}	Phase 1 and 3 Low-Voltage Internal Bias Supply. Provides power to switching FET drivers. Powered from SYS. Bypass V_{L13} to PGND1/PGND3 with a 2.2µF ceramic capacitor. Do not load this pin externally.	power output
E8	V_{L24}	Phase 2 and 4 Low-Voltage Internal Bias Supply. Provides power to switching FET drivers. Powered from SYS. Bypass V_{L24} to PGND2/PGND4 with a 2.2µF ceramic capacitor. Do not load this pin externally.	power output
D2	V_{DD}	Low-Voltage Internal Supply. Powered from SYS. Bypass to AGND with a 1µF ceramic capacitor. Do not load this pin externally.	power output
E1, D8	AGND	Quiet Ground. Connect to all other grounds on the PCB. See Figure 15.	ground
E2	DGND	Digital Ground. Connect to all other grounds on the PCB.	ground
TOP-LEVEL CONTROL AND MONITORING			
F5	ENSEQ	Active-High Sequencer Enable Input. Compatible with the SYS voltage domain. Connect to DGND if automatic power sequencing is not required.	digital input
C3	nRSTIO	Active-Low, Open-Drain, Reset Input/Output. Use for fault monitoring (Figure 10). Connect to other MAX77511/MAX77711s on the PCB for a synchronized fault response. This pin requires a pullup resistor to V_{DD} or some other always-present rail.	digital I/O
E3	AMUX	Analog Multiplexer Output. Connect to system ADC to perform conversions on output load monitors. Leave this pin unconnected if not used.	analog output
C5	nIRQ	Active-Low, Open-Drain Interrupt Output. This pin requires a pullup resistor.	digital output
LINEAR REGULATOR (LDO)			
E7	LDO/AGND	**MAX77711**: Linear Regulator Output. Bypass to ground on the PCB with a 4.7µF ceramic capacitor. Connect to ground on the PCB if not used. **MAX77511**: Unused pin. Connect to ground on the PCB.	power output
D7	INLDO/AGND	**MAX77711**: Linear Regulator Input. Bypass to ground on the PCB with a 10µF ceramic capacitor. Connect to ground on the PCB if unused. **MAX77511**: Unused pin. Connect to ground on the PCB.	power input

Detailed Description—Top-Level

The MAX77511/MAX77711 is a high-efficiency, power-management integrated circuit (IC) that combines a quad-phase configurable buck regulator, six GPIOs, and a flexible power sequencer. The MAX77711 includes a 300mA, PMOS, low-dropout linear regulator (LDO).

Flexible Power Sequencer (FPS)

The IC integrates a FPS that controls the power-up/down timing of the system. The functionality of the FPS (Figure 1) is described as follows:

- The power-up/down sequence consists of 12 slots that count sequentially in time.
  - Slots count upwards from 1 to 12 in the power-up sequence (Figure 2, left).
  - Slots count downwards from 12 to 1 in the power-down sequence (Figure 2, right).
- Regulators enable in their assigned slot in the power-up sequence. Regulators disable in their assigned slot in the power-down sequence.
- GPIOs assert logic-high in their assigned slot in the power-up sequence. GPIOs assert logic-low in their assigned slot in the power-down sequence. Only GPIO5 and GPIO6 can be assigned to the sequencer.
- The slot pitch (t_{SLOT}, time between slots) is programmable between 0.625ms and 5ms in binary-weighted steps with the FPS_SLOT_T[1:0] bitfield. The default value of these bits can be set at the factory.
- Any IC resource (bucks, LDO, GPIOs) can be assigned to power-up/down in any slot. Multiple resources may assign to the same slot.
- Use the buck enable bitfield (BENx[3:0]) to assign the bucks to one of the FPS slots. The default value of these bits can be set at the factory.
- Use the LDO enable bitfield (LDOEN[3:0]) to assign the LDO to one of the FPS slots. The default value of these bits can be set at the factory.
- Use the GPIO function control bitfield (FUNCx[2:0]) to program GPIO5 and GPIO6 to be controlled by the FPS. Use the corresponding GPIOSEQx[3:0] bitfield to control slot assignment. The default value of these bits can be set at the factory. A GPIO programmed to be an FPS digital output (FPSDO) can not be assigned to any other GPIO function.

Assert the ENSEQ pin logic-high to activate the IC from shutdown and begin the power-up sequence. Maintain a logic-high on ENSEQ to keep the IC in the on through sequencer state. Bring ENSEQ logic-low to begin the power-down sequence. The power-down sequence also starts if a SYS undervoltage lockout (UVLO) is detected.

The immediate shutdown sequence (Figure 3) begins if any of the following happen:

1. Over-temperature lockout (OTLO) is detected (FLT = 1 due to OTLO).
2. Short-circuit protection (SCP) fault is detected in any buck regulator (FLT = 1 due to SCP).
3. nRSTIO pin is pulled low externally.

The power-up sequence is prevented if the IC is in UVLO, OTLO, FLT, or the nRSTIO pin is low.

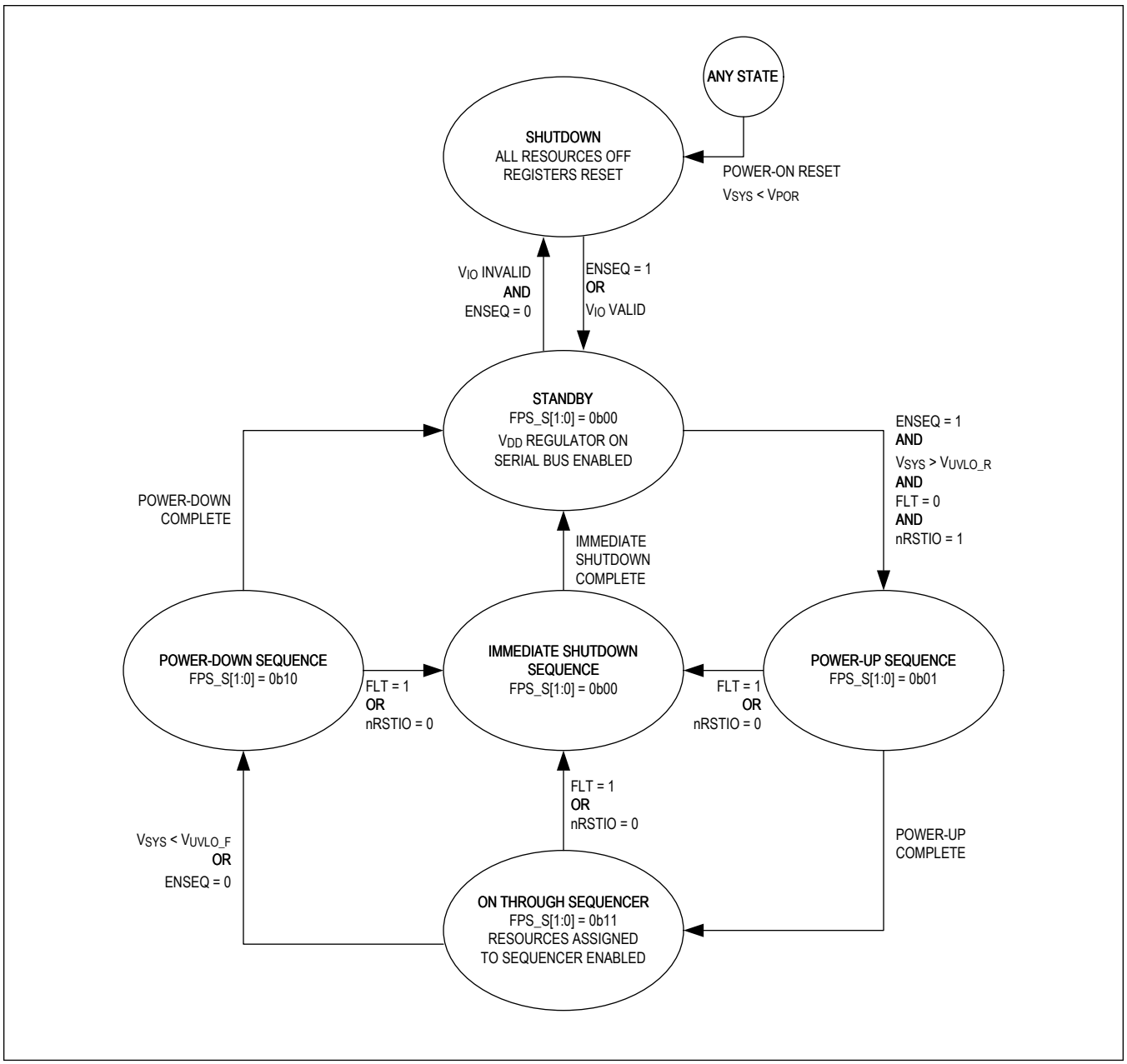


Figure 1. Flexible Power Sequencer State Diagram

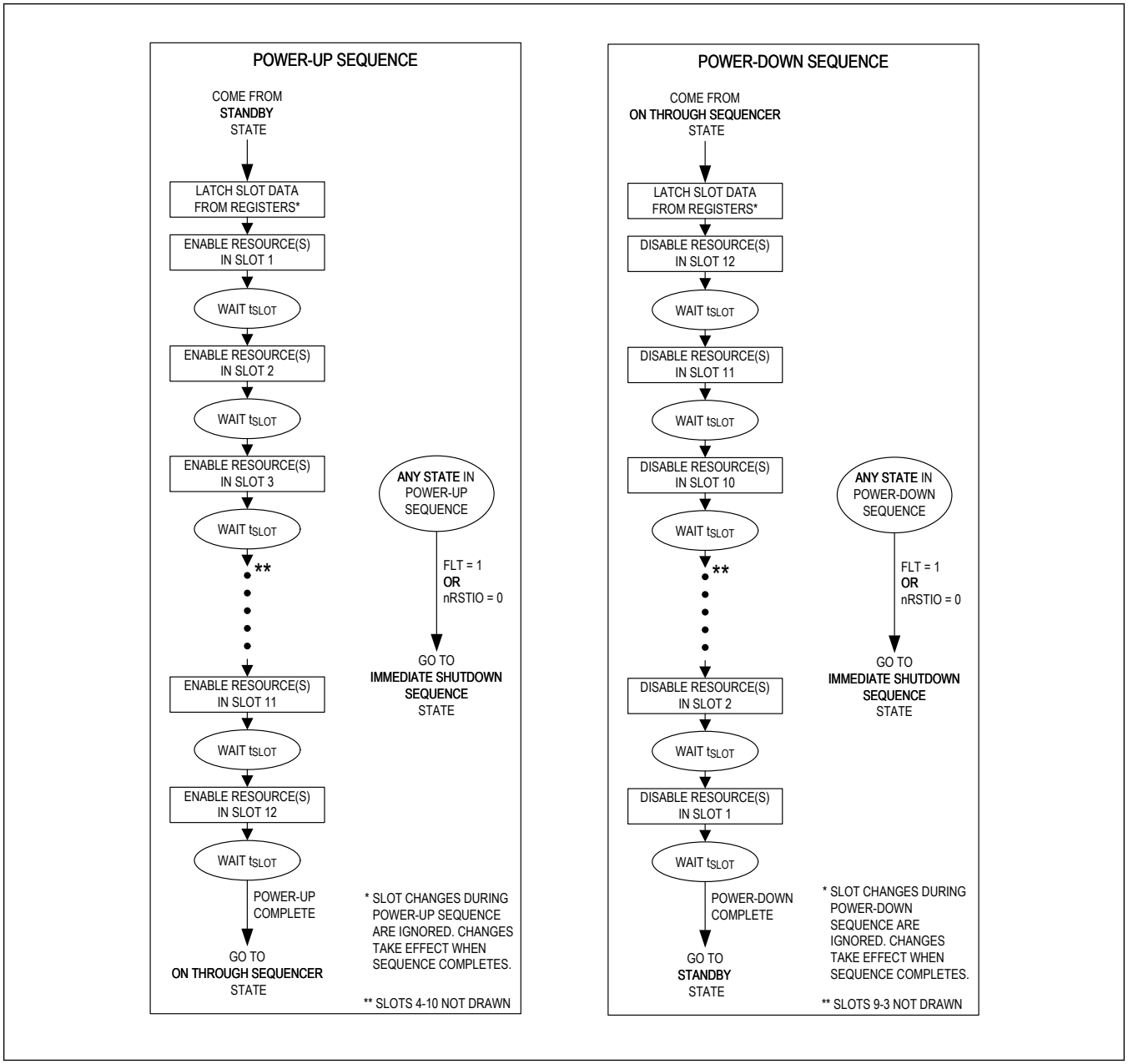


Figure 2. Power-Up/Down Sequence State Actions

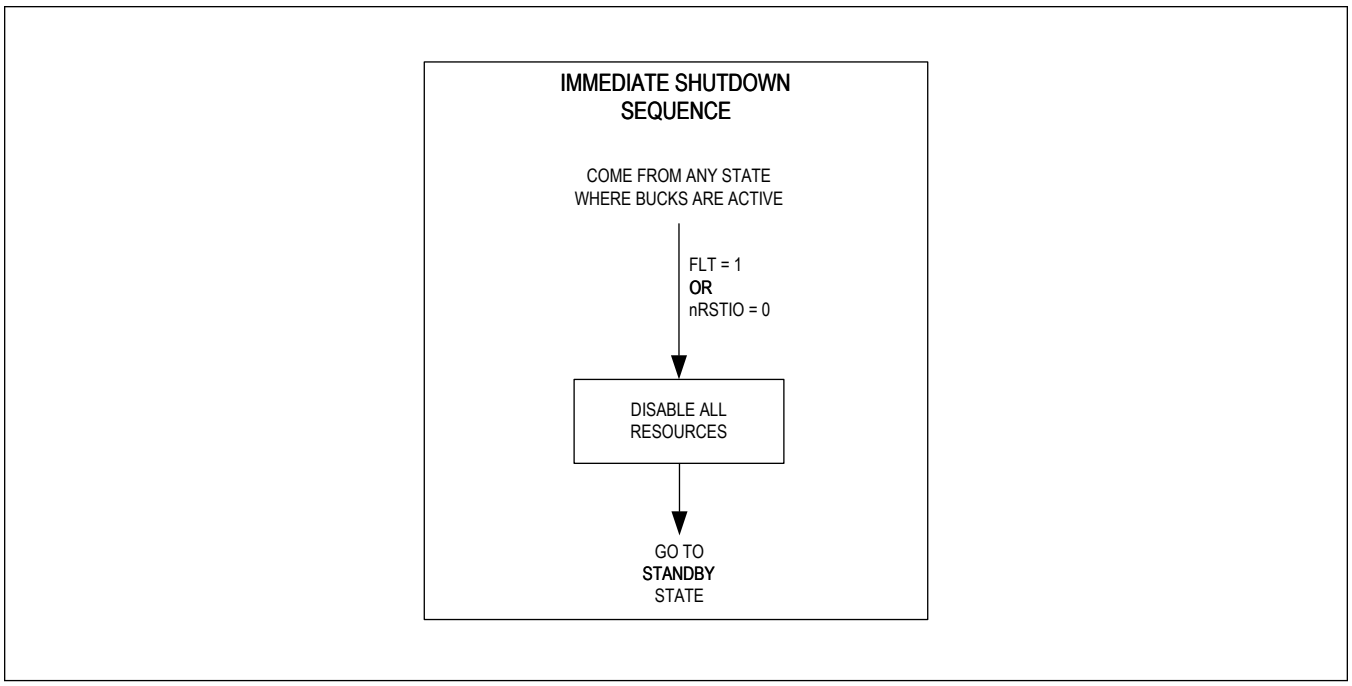


Figure 3. Immediate Shutdown Sequence State Actions

General Purpose Input/Output (GPIO)

Six GPIOs provide system I/O expansion or hardware control options for the buck regulators. See the *GPIO Buck Control* section for details on how these pins are used to control the buck regulators. See the *Register Map* for full details.

GPIOx direction is controlled by the corresponding DIRx[1:0] bitfield. GPIO function is controlled by FUNCx[2:0]. The default values of these bitfields can be factory-programmed. Registers can be reprogrammed any time while I^2C is active. The GPIO voltage domain (V_{IO}) must be valid for GPIOs to operate.

Interrupts are available to signal a change in any GPIO's state. Interrupts are configurable to trigger on rising edge, falling edge, or any edge.

Output Mode

Program DIRx[1:0] to 0b00 to configure the GPIO as a general-purpose output (GPO). Use the corresponding DATAx bit to assert the pin logic high or low. The GPIOs function bitfield (FUNCx[2:0]) is a *don't care* while DIRx[1:0] = 0b00.

The GPO can be used in push-pull mode (DRVx = 1) or open-drain mode (DRVx = 0).

- Use push-pull output mode for applications that need fast edges and low power consumption.
- Open-drain mode requires a pullup resistor. Set the corresponding PUx bit to enable an on-chip pullup resistor between that GPIO and V_{IO}. An on-chip pulldown resistor is also available by setting the corresponding PDx bit. Each resistor is typically 100kΩ.
  - Use open-drain mode to communicate between different voltage domains. For example, to send a signal from a GPO on a 1.8V logic domain (V_{IO} = 1.8V) to a device on a 1.2V logic domain, disable the on-chip pullup resistor (PU = 0) and connect an external pullup resistor to 1.2V on the PCB.
  - The open-drain mode can be used to connect several open-drain (or open-collector) devices together on the same bus to create wired logic (wired AND logic is positive-true; wired OR logic is negative-true).

Special Output Mode

Program DIRx[1:0] to 0b01 to configure the GPIO as a special purpose output. Program the corresponding FUNCx[2:0] bits to map a function to the output. There are two possible functions:

- The GPIO can output the buck power-OK status value (BPOKx). See the *GPIO Buck Control* section.
- The GPIO can be assigned to the *Flexible Power Sequencer (FPS)*. GPIO5 and GPIO6 only.

Input Mode

Program DIRx[1:0] to 0b11 to configure the GPIO as an input. Program the corresponding FUNCx[2:0] to map the logic input to a function. See the *GPIO Buck Control* and *Register Map* sections for full details.

The corresponding DBNC_SELx[1:0] bitfield selects the input debounce time (t_{DB-GPI}).

- Enable the debounce timer if the GPI is connected to a device that can bounce or chatter (like a mechanical switch).
- If the GPI is connected to a circuit with clean logic transitions and no risk of bounce then, disable the debounce timer to eliminate logic delays.
- Use the on-chip pullup or pulldown resistors to provide the GPI with a defined input to prevent logic chatter. Set the corresponding PUx bit to enable the pullup. Set PDx to enable the pulldown. Each resistor is typically 100kΩ.
  - If both corresponding PUx and PDx bits are set concurrently, then internal logic gives the pulldown resistor priority. The pullup resistor is not enabled.

GPIO Buck Control

Assign the GPIOs special alternate functions to control the buck regulators. Use the FUNCx[2:0] bitfield to program the corresponding GPIO to control buck enable, DVS, power-OK, or FPWM. Program which buck regulator to control using the corresponding BSELx[1:0] bitfield. See Table 1 for details. The special functions are exclusive (e.g., the same GPIO cannot control enable and DVS at the same time). FUNCx[2:0] can be programmed at the factory (see *GPIO Factory Options*). See the *Register Map* for details.

Table 1. GPIO Special Functions

FUNCx[2:0]	CONTROL FUNCTION	TYPE	LOGIC LEVEL	SELECTED BUCK BEHAVIOR
0b001	Enable	INPUT	0	Follows register control (BENx[3:0])
			1	Output enabled
0b010	DVS	INPUT	0	V_{OUTx} set by VOUTREGx[7:0]
			1	V_{OUTx} set by VOUTREGDVSx7:0]
0b011	Forced-PWM (FPWM)	INPUT	0	Operating mode set by MODEx[1:0] when buck is enabled
			1	Operating in FPWM when buck is enabled
0b101	Power-OK (POK)	OUTPUT	0	Buck V_{OUTx} is < V_{POK} or disabled
			1 (or Hi-Z)	V_{OUTx} is > V_{POK}

For example, set FUNC1[2:0] to 0b001 to program GPIO1 as an enable pin. Set BSEL1[1:0] to 0b10 to program this enable pin to control buck 3. Multiple GPIOs controlling the same function for the same buck logic *OR* together. The BSELx[1:0] bitfield is a *don't care* if the corresponding GPIO is not assigned a special buck control function.

Bring GPIO above V_{GPI-HI} to assert a logic-high. Lower GPIO below V_{GPI-LO} to assert a logic-low. The logic thresholds are derived from the V_{IO} pin. V_{IO} must be valid for the GPIOs to work as buck special functions or GPIOs.

GPIO LDO Control

When using the MAX77711, use any GPIO to control LDO enable by assigning the corresponding FUNCx[2:0] bitfield to 0b100. See the *LDO Hardware Enable* section for more information.

GPIO Factory Options

Each GPIOs corresponding FUNCx[2:0] bitfield is factory-programmable. The GPIOs default pullup, pulldown, interrupt, debounce, direction, and drive control registers depend on the factory-set FUNCx[2:0] code. In other words, the default

bit combination in FUNCx[2:0] determines the default value of the other GPIO control fields. See Table 2, Table 3 and the *GPIO Buck Control* section for more information.

GPIO control registers are reconfigurable any time I²C is active. See the *Register Map* for full details. Contact the factory to request the default GPIO configurations corresponding to each MAX77511/MAX77711 part number.

Table 2. GPIO Default Factory Options (Simple Decode)

FUNCx[2:0]	DEFAULT FUNCTION OPTIONS (SEE Table 3 ALSO)
0x0 - Output Data	Push-pull output driving DATAx
0x1 - Buck Enable	Input with pulldown, no interrupt, no debounce
0x2 - Buck DVS	Input with pulldown, no interrupt, no debounce
0x3 - Buck FPWM	Input with pulldown, no interrupt, no debounce
0x4 - LDO Enable*	Input with pulldown, no interrupt, no debounce
0x5 - Buck POK	Open-drain output with no pullup driving selected buck POK
0x6 - FPS Output**	Push-pull output driving selected FPS slot
0x7 - FPS Output**	Open-drain output with no pullup driving selected FPS slot

**MAX77711 only*
***GPIO5 and GPIO6 only. Codes 0x6 and 0x7 set the same function (FPS Digital Output) but have different default drive options.*

Table 3. GPIO Default Factory Options (Full Decode)

FUNCx[2:0]	PUx	PDx	IRQ_SELx[1:0]	DBNC_SELx[1:0]	DIRx[1:0]	DRVx
0x0 - Output Data	0	0	0b00	0b00	0b00	1
0x1 - Buck Enable	0	1	0b00	0b00	0b10	0
0x2 - Buck DVS	0	1	0b00	0b00	0b10	0
0x3 - Buck FPWM	0	1	0b00	0b00	0b10	0
0x4 - LDO Enable*	0	1	0b00	0b00	0b10	0
0x5 - Buck POK	0	0	0b00	0b00	0b01	0
0x6 - FPS Output**	0	0	0b00	0b00	0b01	1
0x7 - FPS Output**	0	0	0b00	0b00	0b01	0

**MAX77711 only*
***GPIO5 and GPIO6 only. Codes 0x6 and 0x7 set the same function (FPS Digital Output) but have different default drive options.*

Interrupts (nIRQ)

nIRQ is an active-low, open-drain output that is typically routed to the host processor's interrupt input to signal an important change in the ICs status. See the *Register Map* for a full list of available status and interrupt bits.

An external pullup resistor is required for this node. nIRQ is the logical *NOR* of all unmasked interrupt bits in the ICs register map.

All interrupts are masked by default. Masked interrupt bits do not cause the nIRQ pin to change. Unmask the interrupt bits to allow nIRQ to assert.

Dedicated Internal Supplies

V_{L13}, V_{L24}, and V_{DD} are 1.8V linear regulators powered from SYS. V_{L13} and V_{L24} provide power for the switching FET gate drivers. V_{DD} provides power for internal logic and control.

Bypass V_{L13} and V_{L24} to PGNDx with a minimum 2.2µF ceramic capacitor each. Bypass V_{DD} to AGND with a minimum 1µF ceramic capacitor. Position the bypass capacitors as close to the IC as possible. See the *PCB Layout Guidelines* for more information. Do not load these regulators externally.

V_{DD} automatically activates when V_{IO} is valid or ENSEQ is logic high. V_{L13}/V_{L24} automatically activate when any buck regulator is enabled or if the FVLEN bit is set. Set the FVLEN bit to force enable the V_{L13}/V_{L24} regulators. The buck startup ramp delay time (t_{SUDLY}) shortens when V_{L13}/V_{L24} are enabled before the bucks enable. See the *Register Map* for details.

Thermal Alarms and OTLO

The IC has thermal alarms to monitor if the junction temperature rises above +120°C and +140°C. See Figure 4. The IC enters over-temperature lockout (OTLO) if the junction temperature exceeds T_{OTLO} (approximately +165°C typ). OTLO causes all resources to turn off immediately and latches the IC into a fault state (FLT = 1). See the *Short-Circuit and Thermal Protection* section for more information.

Thermal monitoring is active whenever any of the following conditions are true:

- Any buck enables.
- The force thermal protection enable bit sets (FTPEN = 1). See the *Register Map*.
- Thermal protection enables (for any reason) and detects T_J > 120°C (TJ_S[1:0] reads > 0b00). Protection automatically remains active until T_J < 105°C.

The TJ_S[1:0] bitfield continuously indicates the junction temperature status. A maskable interrupt (TJ_I) is available to signal a change in TJ_S[1:0]. See the *Register Map* for details.

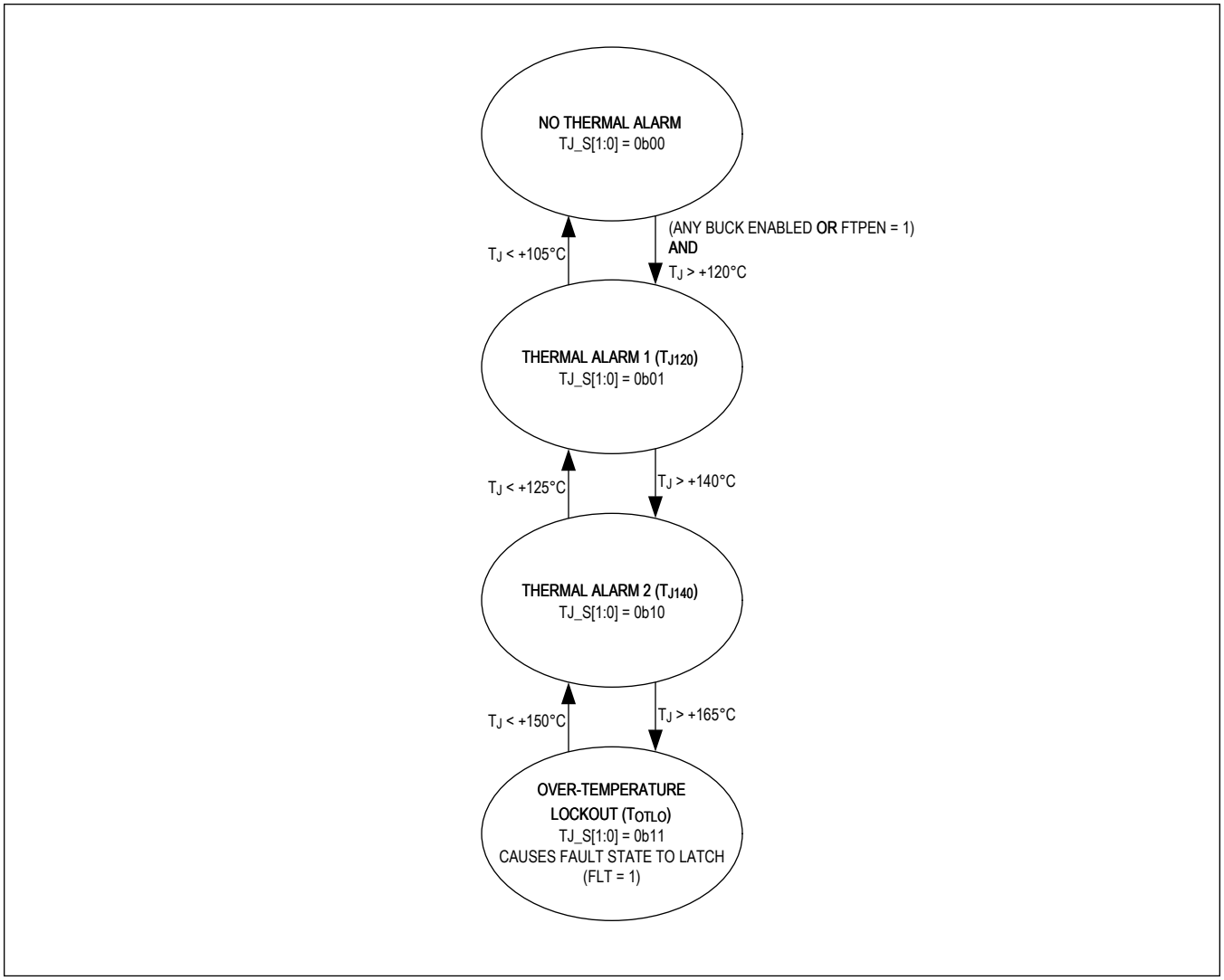


Figure 4. Thermal Alarms and OTLO State Diagram

Register Reset Condition

The ICs configuration registers reset to default values when V_{IO} becomes invalid or SYS falls below the POR threshold. Contact the factory to request a version of the IC that does not reset registers when V_{IO} becomes invalid.

Factory Options

The IC is factory-configurable with a variety of one-time programmable (OTP) options. The *Register Map* denotes factory-programmable options by showing *OTP* in the *Reset* value field. See Table 4 and Table 5 for selector guides.

Table 4. MAX77711 Factory-Programmed Defaults (OTP Options)

	MAX77711AEWB	MAX77711BEWB	MAX77711CEWB	MAX77711DEWB	MAX77711EEWB
Option	711A	711B	711C	711D	711E
Chip ID CID[3:0]	0x0	0x2	0x4	0x5	0x6
Register Reset	V_{IO} or SYS Invalid	V_{IO} or SYS Invalid	V_{IO} or SYS Invalid	V_{IO} or SYS Invalid	V_{IO} or SYS Invalid
Sequencer Slot Pitch FPS_SLOT_T[1:0]	1.25ms 0b01	1.25ms 0b01	1.25ms 0b01	0.625ms 0b00	2.50ms 0b10
BUCK OPTIONS					
FVLEN	0 (auto)	0 (auto)	0 (auto)	0 (auto)	0 (auto)
$t_{SFTSHRT}$ SCPWARN_TIME[1:0]	50ms 0b10	25ms 0b01	50ms 0b10	25ms 0b01	25ms 0b01
RNGLOCK	0 (unlocked)	1 (locked)	0 (unlocked)	0 (unlocked)	0 (unlocked)
RNG1	0	0	0	0	0
RNG2	0	0	0	0	0
RNG3	1	0	1	0	1
RNG4	1	0	1	0	1
V_{OUT1} VOUTREG1[7:0]	0.7V 0x5A	0.93V 0x88	1.1V 0xAA	0.25V 0x00	1.0V 0x96
V_{OUT2} VOUTREG2[7:0]	1.2V 0xBE	0.93V 0x88	1.2V 0xBE	0.25V 0x00	1.0V 0x96
V_{OUT3} VOUTREG3[7:0]	1.8V 0x28	0.93V 0x88	1.8V 0x28	0.25V 0x00	3.3V 0x73
V_{OUT4} VOUTREG4[7:0]	3.3V 0x73	1.23V 0xC4	3.3V 0x73	0.25V 0x00	1.38V 0x13
$I_{PEAK-HS1}$ ILIM1[1:0]	4.5A 0b11	4.5A 0b11	4.5A 0b11	1.5A 0b00	4.5A 0b11
$I_{PEAK-HS2}$ ILIM2[1:0]	4.5A 0b11	4.5A 0b11	4.5A 0b11	1.5A 0b00	4.5A 0b11
$I_{PEAK-HS3}$ ILIM3[1:0]	4.5A 0b11	4.5A 0b11	4.5A 0b11	1.5A 0b00	4.5A 0b11
$I_{PEAK-HS4}$ ILIM4[1:0]	4.5A 0b11	4.5A 0b11	4.5A 0b11	1.5A 0b00	4.5A 0b11
Buck 1 Enable/FPS Slot BEN1[3:0]	Slot 1 0x2	Slot 1 0x2	Slot 3 0x4	Force Disabled 0x0	Slot 3 0x4
Buck 2 Enable/FPS Slot BEN2[3:0]	Slot 2 0x3	Slot 1 0x2	Slot 3 0x4	Force Disabled 0x0	Slot 2 0x3
Buck 3 Enable/FPS Slot BEN3[3:0]	Slot 3 0x4	Slot 2 0x3	Slot 2 0x3	Force Disabled 0x0	Slot 1 0x2
Buck 4 Enable/FPS Slot BEN4[3:0]	Slot 4 0x5	Slot 4 0x5	Slot 4 0x5	Force Disabled 0x0	Slot 2 0x3
Buck 1 Soft Start/Stop SFTUPDN[2:0]	±1.25mV/µs 0x2	±1.25mV/µs 0x2	±1.25mV/µs 0x2	0.15mV/µs 0x0	±0.625mV/µs 0x1

Table 4. MAX77711 Factory-Programmed Defaults (OTP Options) (continued)

	MAX77711AEWB	MAX77711BEWB	MAX77711CEWB	MAX77711DEWB	MAX77711EEWB
Buck 2 Soft Start/Stop SFTUPDN2[2:0]	±1.25mV/µs 0x2	±1.25mV/µs 0x2	±1.25mV/µs 0x2	0.15mV/µs 0x0	±1.25mV/µs 0x2
Buck 3 Soft Start/Stop SFTUPDN3[2:0]	±1.25mV/µs 0x2	±1.25mV/µs 0x2	±1.25mV/µs 0x2	0.15mV/µs 0x0	±0.625mV/µs 0x1
Buck 4 Soft Start/Stop SFTUPDN4[2:0]	±1.25mV/µs 0x2	±1.25mV/µs 0x2	±1.25mV/µs 0x2	0.15mV/µs 0x0	±0.625mV/µs 0x1
Soft-Start $I_{PEAK-HSx}$ Override	Off	On	On	On	Off
Spread Spectrum Profile	Pseudo-Random	Pseudo-Random	Triangular	Triangular	Pseudo-Random
Assisted Active Discharge	Off	Off	On	Off	Off
Transient Performance Option	Off	Off	Off	Off	Off
LDO OPTIONS					
LDO Enable/FPS Slot LDOEN[3:0]	Slot 5 0x6	Disabled 0x0	Slot 5 0x6	Disabled 0x0	Enabled 0x1
V_{LDO} LDO_VREG[5:0]	1.8V 0x38	0.4V 0x00	0.6V 0x08	0V 0x0	1.8V 0x38
GPIO OPTIONS (SEE Table 2 AND Table 3)					
GPIOLOCK	0 (unlocked)	0 (unlocked)	0 (unlocked)	0 (unlocked)	0 (unlocked)
GPIO1 Function FUNC1[2:0]; BSEL1[1:0]	Buck 1 Enable 0x1; 0x0	Buck 1 FPWM 0x3; 0x0	Buck 1 Enable 0x1; 0x0	Buck 1 DVS Input 0x0; 0x2	Buck 1 Enable 0x1; 0x0
GPIO2 Function FUNC2[2:0]; BSEL2[1:0]	Buck 2 Enable 0x1; 0x1	Buck 2 FPWM 0x3; 0x1	Buck 3 Enable 0x1; 0x2	Buck 1 DVS Input 0x0; 0x2	Buck 2 Enable 0x1; 0x1
GPIO3 Function FUNC3[2:0]; BSEL3[1:0]	Buck 3 Enable 0x1; 0x2	Buck 3 FPWM 0x3; 0x2	Buck 4 Enable 0x1; 0x3	Buck 1 DVS Input 0x0; 0x2	Buck 3 Enable 0x1; 0x2
GPIO4 Function FUNC4[2:0]; BSEL4[1:0]	Buck 4 Enable 0x1; 0x3	Buck 4 FPWM 0x3; 0x3	Buck 1 FPWM 0x3; 0x0	Buck 1 DVS Input 0x0; 0x2	Buck 4 Enable 0x1; 0x3
GPIO5 Function FUNC5[2:0]; BSEL5[1:0]	LDO Enable 0x4; 0x0	FPS Output 0x6; 0x0	Buck 3 FPWM 0x3; 0x2	Buck 1 DVS Input 0x0; 0x2	LDO Enable 0x4; 0x0
GPIO6 Function FUNC6[2:0]; BSEL6[1:0]	FPS Output 0x7; 0x0	FPS Output 0x6; 0x0	Buck 4 FPWM 0x3; 0x3	Buck 1 DVS Input 0x0; 0x2	FPS Output 0x7; 0x0
GPIO5 FPS Slot GPIOSEQ5[3:0]	Slot 6 0x5	Slot 4 0x3	Slot 1 0x0	Slot 1 0x0	Slot 6 0x5
GPIO6 FPS Slot GPIOSEQ6[3:0]	Slot 12 0xF	Slot 6 0x5	Slot 1 0x0	Slot 1 0x0	Slot 12 0xF

Table 5. MAX77511 Factory-Programmed Defaults (OTP Options)

	MAX77511AEWB	MAX77511LEWB	MAX77511MEWB	MAX7511REWB
Option	511A	511L	511M	511R
Chip ID CID[3:0]	0x1	0x9	0x7	0x8
Register Reset	V_{IO} or SYS Invalid	V_{IO} or SYS Invalid	V_{IO} or SYS Invalid	V_{IO} or SYS Invalid
Sequencer Slot Pitch FPS_SLOT_T[1:0]	5ms 0b11	1.25ms 0b01	5ms 0b11	1.25ms 0b01
BUCK OPTIONS				

Table 5. MAX77511 Factory-Programmed Defaults (OTP Options) (continued)

	MAX77511AEWB	MAX77511LEWB	MAX77511MEWB	MAX7511REWB
FVLEN	0 (auto)	0 (auto)	0 (auto)	0 (auto)
$t_{SFTSHRT}$ SCPWARN_TIME[1:0]	100ms 0b11	100ms 0b11	100ms 0b11	100ms 0b11
RNGLOCK	0 (unlocked)	0 (unlocked)	0 (unlocked)	0 (unlocked)
RNG1	1	0	1	0
RNG2	1	0	1	0
RNG3	1	1	1	0
RNG4	1	0	1	1
V_{OUT1} VOUTREG1[7:0]	3.3V 0x73	1.0V 0x96	3.3V 0x73	1.2V 0xBE
V_{OUT2} VOUTREG2[7:0]	1.8V 0x28	1.0V 0x96	3.3V 0x73	1.2V 0xBE
V_{OUT3} VOUTREG3[7:0]	5.0V 0xC8	3.3V 0x73	5.0V 0xC8	1.2V 0xBE
V_{OUT4} VOUTREG4[7:0]	2.5V 0x4B	0.95V 0x8C	5.0V 0xC8	1.8V 0x28
$I_{PEAK-HS1}$ ILIM1[1:0]	4.5A 0b11	4.5A 0b11	4.5A 0b11	4.5A 0b11
$I_{PEAK-HS2}$ ILIM2[1:0]	4.5A 0b11	4.5A 0b11	4.5A 0b11	4.5A 0b11
$I_{PEAK-HS3}$ ILIM3[1:0]	4.5A 0b11	4.5A 0b11	4.5A 0b11	4.5A 0b11
$I_{PEAK-HS4}$ ILIM4[1:0]	4.5A 0b11	4.5A 0b11	4.5A 0b11	4.5A 0b11
Buck 1 Enable/FPS Slot BEN1[3:0]	Slot 3 0x4	Slot 4 0x5	Slot 3 0x4	Disabled 0x0
Buck 2 Enable/FPS Slot BEN2[3:0]	Disabled 0x0	Slot 4 0x5	Slot 1 0x2	Disabled 0x0
Buck 3 Enable/FPS Slot BEN3[3:0]	Disabled 0x0	Slot 2 0x3	Disabled 0x0	Disabled 0x0
Buck 4 Enable/FPS Slot BEN4[3:0]	Disabled 0x0	Slot 3 0x4	Slot 3 0x4	Disabled 0x0
Buck 1 Soft Start/Stop SFTUPDN[2:0]	±0.625mV/µs 0x1	±0.625mV/µs 0x1	±0.625mV/µs 0x1	±0.625mV/µs 0x1
Buck 2 Soft Start/Stop SFTUPDN2[2:0]	±0.625mV/µs 0x1	±0.625mV/µs 0x1	±0.625mV/µs 0x1	±0.625mV/µs 0x1
Buck 3 Soft Start/Stop SFTUPDN3[2:0]	±0.625mV/µs 0x1	±2.5mV/µs 0x3	±0.625mV/µs 0x1	±0.625mV/µs 0x1
Buck 4 Soft Start/Stop SFTUPDN4[2:0]	±0.625mV/µs 0x1	±0.625mV/µs 0x1	±0.625mV/µs 0x1	±0.625mV/µs 0x1
Soft-Start $I_{PEAK-HSx}$ Override	On	On	On	On
Spread Spectrum Profile	Triangular	Triangular	Triangular	Triangular
Assisted Active Discharge	Off	Off	Off	Off

Table 5. MAX77511 Factory-Programmed Defaults (OTP Options) (continued)

	MAX77511AEWB	MAX77511LEWB	MAX77511MEWB	MAX7511REWB
Transient Performance Option	On	On	On	On
LDO OPTIONS				
LDO Enable/FPS Slot LDOEN[3:0]	Disabled 0x0	Disabled 0x0	Disabled 0x0	Disabled 0x0
V_{LDO} LDO_VREG[5:0]	Do not use	Do not use	Do not use	Do not use
GPIO OPTIONS (SEE Table 2 AND Table 3)				
GPIOLOCK	0 (unlocked)	0 (unlocked)	0 (unlocked)	0 (unlocked)
GPIO1 Function FUNC1[2:0]; BSEL1[1:0]	Buck 1 Enable 0x1; 0x0	Buck 4 POK 0x5; 0x3	GPO 0x0; 0x0	Buck 1 Enable 0x1; 0x0
GPIO2 Function FUNC2[2:0]; BSEL2[1:0]	Buck 3 Enable 0x1; 0x2	Buck 1 POK 0x5, 0x0	Buck 3 Enable 0x1; 0x2	GPO 0x0; 0x0
GPIO3 Function FUNC3[2:0]; BSEL3[1:0]	Buck 3 Enable 0x1; 0x2	Buck 3 POK 0x5; 0x2	Buck 3 Enable 0x1; 0x2	Buck 4 Enable 0x1; 0x3
GPIO4 Function FUNC4[2:0]; BSEL4[1:0]	Buck 1 POK 0x5; 0x0	GPO 0x0; 0x3	Buck 1 POK 0x5; 0x0	GPO 0x0; 0x0
GPIO5 Function FUNC5[2:0]; BSEL5[1:0]	Buck 3 POK 0x5; 0x2	GPO 0x0; 0x1	Buck 3 POK 0x5; 0x2	Buck 4 POK 0x5; 0x3
GPIO6 Function FUNC6[2:0]; BSEL6[1:0]	Buck 2 Enable 0x1; 0x1	GPO 0x0; 0x0	GPO 0x0; 0x0	Buck 1 POK 0x5; 0x0
GPIO5 FPS Slot GPIOSEQ5[3:0]	Slot 7 0x6	Slot 7 0x6	Slot 7 0x6	Slot 7 0x6
GPIO6 FPS Slot GPIOSEQ6[3:0]	Slot 4 0x3	Slot 4 0x3	Slot 4 0x3	Slot 4 0x3

Detailed Description—Quad-Channel Configurable Buck Regulator

The IC integrates a high-efficiency, phase-configurable step-down (buck) regulator with four 3A phases (Φ). Four feedback inputs allow up to four different regulated outputs (channels). Each regulator operates on an input supply between 2.3V and 10V. Output voltage is programmable with an I^2C serial interface between 0.25V and 5.2V in 5mV or 20mV steps depending on the RNGx bit. See the *Output Voltage Selection* section.

Each switching phase supports 3A. The phase configuration is selectable by strapping programming pins on the PCB. Any multiphase or single phase combination can be set: 4Φ, 3Φ+1Φ, 2Φ+2Φ, 2Φ+1Φ+1Φ, or 1Φ+1Φ+1Φ+1Φ. (See the *Phase Configuration section*.) Load capability adds linearly as phases combine (1Φ supports 3A, 2Φ supports 6A, etc.). Maximum load capability is 12A in the 4Φ (single output channel) configuration. Four individual 3A outputs can be regulated in the (1+1+1+1)Φ configuration.

Six general-purpose input/outputs (GPIO) add additional flexibility. The GPIOs can be programmed as digital I/O or assigned to special functions: buck enable inputs, buck DVS inputs, buck FPWM mode inputs, or power-OK monitor outputs. See the *GPIO Buck Control section*.

Buck Regulator Control Scheme

MAX77511/MAX77711 uses Maxim's proprietary Quick-PWM™ adaptive on-time control scheme. Adaptive on-time control provides fast response to load transients, inherent compensation to input voltage variation, and stable performance at low duty cycles. Buck 1 is referenced in the following explanation.

On-times (MOSFET Q1 on) are controlled by the on-time generator circuit. See Figure 5. This circuit calculates an on-time based on the output voltage target ($V_{OUT-REG1}$), the input voltage (V_{IN1}), and the target switching frequency (F_{SW}).

Off-times (MOSFET Q2 on) begin when the on-time ends. Shoot-through current from IN1 to PGND1 is avoided by

introducing a brief period of dead time between switching events when neither MOSFET is on. Inductor current conducts through Q2s intrinsic body diode during dead time.

The PWM comparator regulates V_{OUT1} by modulating off-time. The negative input of the PWM comparator is a voltage proportional to the actual output voltage error added to the inductor current sense. The positive input is a compensation ramp. The PWM comparator begins an on-time (and resets the compensation ramp) when the error voltage plus inductor current becomes less than the ramp. The off-time automatically begins again when the calculated on-time expires.

A phase scheduler receives the output of the PWM comparator and prioritizes the on-times of each phase under buck 1 control. The scheduler controls phase spacing (i.e., 2Φ is spaced 180° apart, 3Φ is spaced 120°, 4Φ is spaced 90°). Multiphase configurations permanently have all phases activated and always switch in sequence during steady-state operation. Phases do not add or shed.

Switching frequency (F_{SW}) of the adaptive on-time buck is variable and heavily influenced by the instantaneous load. More on-time pulses in a given time (higher F_{SW}) is observed as load increases. Fewer on-times in a given time (lower F_{SW}) is observed as load decreases.

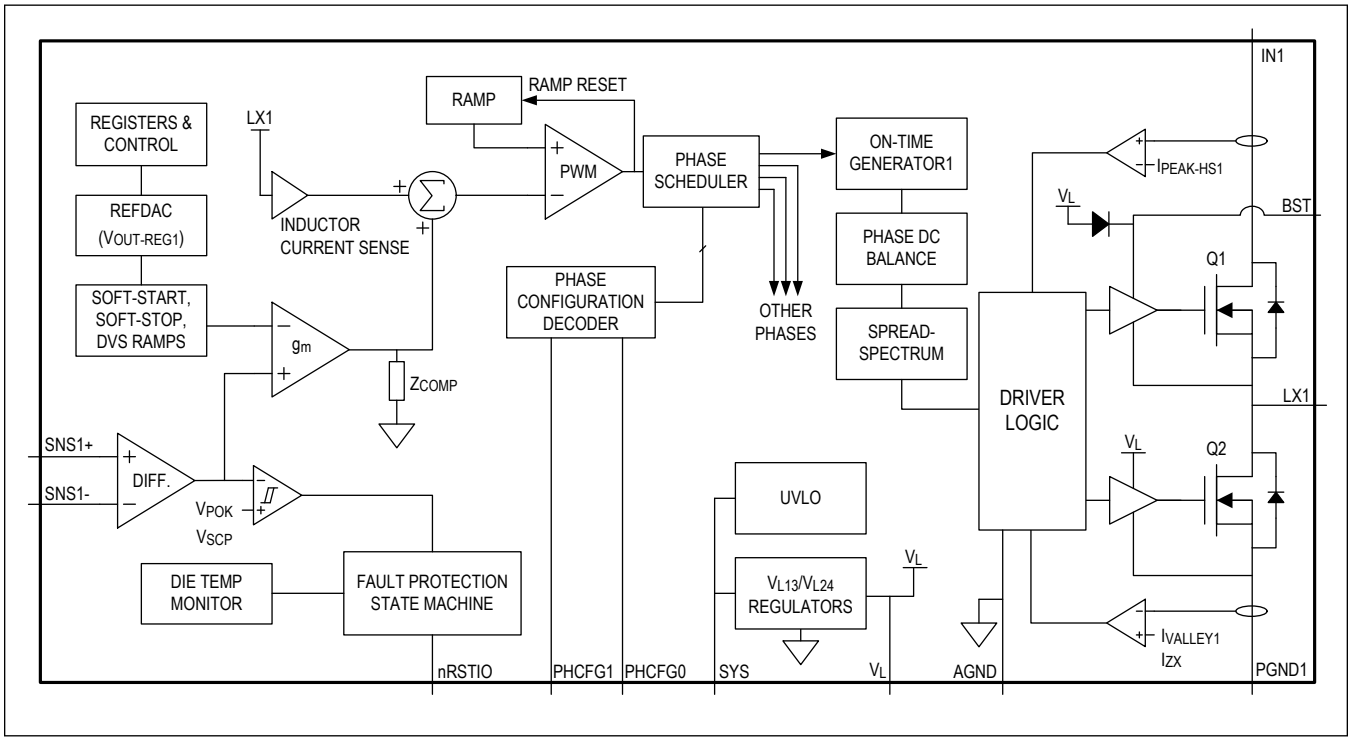


Figure 5. Buck Control Scheme Diagram

Adaptive Off-Time Control

The buck regulator automatically switches from adaptive on-time control to adaptive off-time control when the IC detects duty cycle above 80%. Adaptive off-time control uses an off-time generator circuit and regulates the output voltage by modulating on-time. Changing control methods allows the regulator to maintain high stability and low jitter at high duty cycles.

Phase Configuration

The IC has four 3A switching phases which can be configured into single phase or multiphase bucks. Use the PHCFG1 and PHCFG0 pins to program the buck phase configuration. PHCFG1/PHCFG0 are tri-state digital inputs. I²C device address is also configured using these pins. See Table 6 for programming information.

Table 6. Phase Configuration Programming

PHCFG1	PHCFG0	PHASE (Φ) CONFIGURATION	NUMBER OF OUTPUTS	I²C DEVICE ADDRESS (7-BIT)
0	0	4Φ	1	0x71
0	1	3Φ + 1Φ	2	0x72
0	Z	2Φ + 2Φ	2	0x73
1	0	2Φ + 1Φ + 1Φ	3	0x74
1	1	2Φ + 1Φ + 1Φ	3	0x75
1	Z	1Φ + 1Φ + 1Φ + 1Φ	4	0x76
Z	0	1Φ + 1Φ + 1Φ + 1Φ	4	0x77
Z	1	1Φ + 1Φ + 1Φ + 1Φ	4	0x4E
Z	Z	1Φ + 1Φ + 1Φ + 1Φ	4	0x4F

0 = connected to DGND
1 = connected to V_{DD}
Z = unconnected

Permanently strap PHCFG1/PHCFG0 to one logic value on the PCB. The logic value of these inputs latches when the device exits shutdown.

The PHCFGS[3:0] status bitfield reflects the latched value of the PHCFG1/PHCFG0 pins and can be used to check for errors before the host controller enables the bucks through I²C. See the *Register Map* for details.

The buck feedback configuration is specific to the phase configuration. For example, a quad-phase (4Φ) buck regulates a single output voltage using only the SNS1+/SNS1- pins for feedback. The other feedback pins are unused. See Table 7 for how to configure the feedback sense pins for each phase configuration. Ground unused feedback sense pins. See the *Typical Applications Circuits* section of the data sheet for more information.

Table 7. Buck Feedback Assignment vs. Phase Configuration

PHASE (Φ) CONFIGURATION	PHASES USED	BUCK NAMING CONVENTION	FEEDBACK INPUTS
4Φ (1 output)	LX1 LX2 LX3 LX4	Buck 1 (V_{OUT1})	SNS1+ SNS1-
3Φ + 1Φ (2 outputs)	LX1 LX2 LX3	Buck 1 (V_{OUT1})	SNS1+ SNS1-
	LX4	Buck 4 (V_{OUT4})	SNS4+ SNS4-
2Φ + 2Φ (2 outputs)	LX1 LX2	Buck 1 (V_{OUT1})	SNS1+ SNS1-
	LX3 LX4	Buck 3 (V_{OUT3})	SNS3+ SNS3-

Table 7. Buck Feedback Assignment vs. Phase Configuration (continued)

PHASE (Φ) CONFIGURATION	PHASES USED	BUCK NAMING CONVENTION	FEEDBACK INPUTS
2Φ + 1Φ + 1Φ (3 outputs)	LX1 LX2	Buck 1 (V_{OUT1})	SNS1+ SNS1-
	LX3	Buck 3 (V_{OUT3})	SNS3+ SNS3-
	LX4	Buck 4 (V_{OUT4})	SNS4+ SNS4-
1Φ + 1Φ + 1Φ + 1Φ (4 outputs)	LX1	Buck 1 (V_{OUT1})	SNS1+ SNS1-
	LX2	Buck 2 (V_{OUT2})	SNS2+ SNS2-
	LX3	Buck 3 (V_{OUT3})	SNS3+ SNS3-
	LX4	Buck 4 (V_{OUT4})	SNS4+ SNS4-

Output Voltage Selection

Target regulation voltage ($V_{OUT-REG}$) is adjustable between 0.25V and 1.3V in 5mV steps, while the range bit is low (RNGx = 0) and between 1V and 5.2V in 20mV steps, while the range bit is high (RNGx = 1). See Table 8. Each buck regulator has an independent corresponding RNGx bit.

Table 8. Buck Output Voltage Range

RANGE BIT (RNG)	$V_{OUT-REG}$ PROGRAMMING RANGE (V)	STEP PER LSB (mV)	REQUIRED INDUCTOR VALUE (µH)
RNG = 0 (low-range)	0.25 to 1.3	5	0.47
RNG = 1 (high-range)	1 to 5.2	20	1.5

The same registers (VOUTREGx[7:0] and VOUTREGDVSx[7:0]) set $V_{OUT-REG}$ regardless of RNG. The default state of the RNG bit is factory-programmable. The range lock OTP bit (RNGLOCK) prevents serial writes from changing RNG from the factory-default value. See the *Register Map* for details.

The VOUTREGx[7:0] bitfield sets the buck output voltage while the corresponding DVS input is logic-low. VOUTREGDVSx[7:0] sets the output voltage when the DVS input is logic-high. DVS is always logic-low if no GPIO is assigned as a DVS input for that particular buck. See the *Digital Voltage Scaling (DVS)* section for more details.

Buck Enable Control

Buck Software Enable

Use the I^2C serial interface to program the BENx[3:0] bitfield to 0b001 to enable the corresponding buck output. Program BENx[3:0] to 0b000 to disable the buck. The serial interface is active whenever V_{IO} is valid.

Buck Hardware Enable

A buck enable pin is available by assigning a GPIO as a special function buck enable input. When a GPIO is programmed as an enable input, then the interaction between the enable pin and the software (I^2C) enable command is a logical *OR*. The GPIOs derive logic thresholds from the V_{IO} pin. V_{IO} must be valid for the GPIOs to function.

Program any GPIOs FUNCx[2:0] bitfield to 0b001 to configure that GPIO as a buck enable pin. Program which buck the enable pin controls using the corresponding BSELx[1:0] bitfield. The logical relationship between multiple GPIOs assigned to enable the same buck is a logical *OR*. See the *GPIO Buck Control* and the *Register Map* sections for more information.

Buck Flexible Power Sequencer Enable

Use the ENSEQ pin to control the bucks using the Flexible Power Sequencer (FPS). Assert ENSEQ logic-high (or connect to SYS) to cause bucks assigned to the FPS to power-up in a factory-programmed sequence. Bring ENSEQ logic-low to begin the power-down sequence. Power-down starts only after power-up is completed.

The sequence consists of 12 time slots. The BENx[3:0] bitfield controls the corresponding buck's slot assignment. The default value of this bitfield can be programmed at the factory and reprogrammed anytime while I^2C is active.

Buck regulators cannot be assigned to a FPS slot and forced-enabled/disabled through software at the same time. However, a GPIO buck enable pin can be assigned while the same buck is assigned to a sequencer slot. The logical interaction between the FPS (ENSEQ) and the GPIO enable pin is a logical *OR*.

V_{IO} does not need to be valid for ENSEQ to activate the sequencer. The LDO (MAX77711 only) and GPIOs can also be assigned to the sequencer's slots. See the *Flexible Power Sequencer (FPS)* and *Register Map* sections of the data sheet for more information.

Buck Power-OK Monitors

The IC features power-OK (POK) comparators to monitor the voltage quality of each buck output. The BPOKx status bits continuously reflect the status of these monitors. BPOKx goes high when the corresponding buck enables, the soft-start finishes, and its output rises above V_{POK-R} (82% of V_{OUT} target typ). BPOKx goes low when the corresponding buck disables or its output falls below V_{POK-F} (78% of V_{OUT} target typ).

The BPOK_I interrupt is available to signal whenever any of the BPOKx status bits change from 1 to 0. Each BPOK bit is separately maskable to prevent BPOK_I from asserting. See the *Register Map* for more details.

A hardware POK is available by assigning one of the GPIO pins as a POK output. See the *GPIO Buck Control* section for more information.

Digital Voltage Scaling (DVS)

Use the digital voltage scaling (DVS) function to command buck output voltages to change quickly. Assign a GPIO as a DVS special function input to enable DVS for the selected buck. See the *GPIO Buck Control* section for details.

When the DVS pin is asserted logic-low, then the selected buck's output voltage is programmed by the VOUTREGx[7:0] register. When DVS is asserted high, then the buck's output follows the VOUTREGDVSx[7:0] register. If a buck converter has no DVS pin assigned by a GPIO special function, then the output voltage always follows VOUTREGx[7:0].

When V_{OUTx} is increased by a DVS command, the target voltage is ramped at a positive rate set by the corresponding DVSRISEx[2:0] bitfield. When V_{OUTx} is decreased by DVS, the target voltage is ramped at a negative rate set by the corresponding DVSFALLx[2:0] bitfield.

Set the FSRENx bit to enable the corresponding buck to automatically enter FPWM mode (regardless of MODEx[1:0]) when the target voltage is commanded to ramp. FPWM mode allows the buck output to sink current from C_{OUT} to PGND which enables V_{OUTx} to track the negative rate set by DVSFALLx[2:0] (DVS down) or SFTUPDN[2:0] (soft-stop). See Table 9.

Table 9. FSREN Effect on Buck Behavior

MODEx[1:0]	FSRENx	BUCK BEHAVIOR IN DC (V_{OUTx} NO CHANGE)	BUCK BEHAVIOR DURING RAMP (V_{OUTx} CHANGING)
SKIP or Turbo SKIP	0	Source Only	Source Only
	1	Source Only	Source or Sink
Forced-PWM	X	Source or Sink	Source or Sink

Note: *Buck outputs capable of sinking current can follow changes to V_{OUTx} with negative ramp rates set by DVSFALLx[2:0] or SFTUPDN[2:0] (soft-stop).*

Buck Regulator Mode

Use the MODEx[1:0] bitfield to program the bucks to one of three modes. The default mode is Turbo SKIP mode. All modes are described as follows:

- Forced-PWM (FPWM) mode ensures continuous inductor current at all output loads. Negative inductor current is allowed no less than I_{NEG} (-3A typ). The converter can sink DC current from the output capacitor to maintain output voltage regulation. All internal control circuits remain on in FPWM mode to achieve the fastest load transient response.
- SKIP mode forces discontinuous inductor current at light loads. The controller prevents negative inductor current by forcing LX to a high-impedance state if inductor current is detected near 0mA. SKIP mode deactivates a portion of the internal control circuitry to conserve quiescent supply current (I_Q). SKIP mode improves light-load efficiency of the buck by reducing the total number of switching cycles needed to regulate the output. Only use SKIP mode if expected load current is less than 10mA per phase.
- Turbo SKIP mode is similar to SKIP mode. Turbo SKIP mode prevents negative inductor current but keeps the internal control circuitry activated to improve the converter's response to load transients. Use Turbo SKIP when expected load currents are more than 10mA per phase. This is the default recommended mode.

Mode can be reprogrammed any time while I^2C is active. See the *Typical Operating Characteristics* for a performance overview of the three modes.

A GPIO special buck control function is available to force the selected buck into FPWM mode using a hardware pin. See the *GPIO Buck Control* section for details. If a GPIO is assigned as an FPWM input, then the selected buck operates in FPWM mode when the pin is asserted logic-high. The buck operates in the mode programmed by its MODEx[1:0] bitfield when the pin is asserted logic-low.

Soft-Start and Soft-Stop

The IC has internal soft-start and soft-stop ramps that control the slew rate of V_{OUTx} as the bucks startup and shutdown. Ramp rate magnitude is programmed by the SFTUPDNx[2:0] bitfield. This bitfield controls both soft-start and soft-stop slew rate. Each buck has unique control of output ramp rate.

The bucks always soft-start whenever enabled by any source (sequencer, hardware input, software command). The bucks soft-start when recovering from a short-circuit protection (SCP) fault or over-temperature lockout (OTLO).

The bucks always soft-stop when disabled by the sequencer, hardware enable inputs, or software commands. If any buck regulator causes an SCP fault, then that buck stops switching immediately without soft-stop (LX becomes high-impedance). All other enabled bucks soft-stop in a controlled manner. If OTLO is detected, then all bucks stop switching immediately without soft-stop.

Bucks only follow their commanded soft-stop ramp if the buck is capable of sinking current. Use the FSRENx bit to enable the corresponding buck output to sink current and follow soft-stop ramp regardless of MODEx[1:0]. See Table 9 for more information.

Active Discharge Resistor

The IC integrates a 100Ω active discharge resistor (R_{LX-AD}) between LXx and the corresponding PGNDx that discharges the output capacitor when the buck disables and the soft-stop ramp finishes. Write ADENx = 1 through I^2C to enable the active discharge resistor function for all phases under the master buck's control. For example, if buck 3 is configured as a 2Φ (6A) channel, then writing ADEN3 = 1 activates the active discharge resistor on both LX3 *and* LX4 when buck 3 disables and soft-stop finishes.

An internal option for advanced users is discussed in the *Assisted Active Discharge after Soft-Stop* section of the data sheet.

Spread-Spectrum Modulation

The bucks are capable of dithering their switching frequency for noise-sensitive applications. Program the bits in the SPECTMODx[1:0] bitfield to enable spread-spectrum modulation for the corresponding buck regulator. Each buck can activate or deactivate spread-spectrum individually.

The spread-spectrum modulation pattern is either pseudo-random or triangular. The choice of pseudo-random or triangular is only programmable at the factory.

Spread-spectrum modulation is characterized by two parameters: modulation envelope and modulation rate.

- The modulation envelope (ΔF_{SW}) determines the maximum difference between the modulated switching frequency and the nominal switching frequency. This controls *how much* the frequency dithers. The modulation envelope is nominally ±8% for all profiles regardless of pseudo-random or triangular.
- The modulation rate determines how quickly the switching frequency changes from one value to another. This controls *how fast* the frequency dithers.

Pseudo-Random Pattern

The pseudo-random engine uses a 4-bit linear feedback shift register (LFSR) to create a pseudo-random value. Refer to Figure 6. The LFSR value is converted to an analog signal and then amplified before being added to the output of the on-time generator circuit. The pseudo-random value shortens or lengthens the on-time of the converter. This causes the control loop to increase or decrease the switching frequency to maintain voltage regulation. Each buck has its own pseudo-random pattern generator.

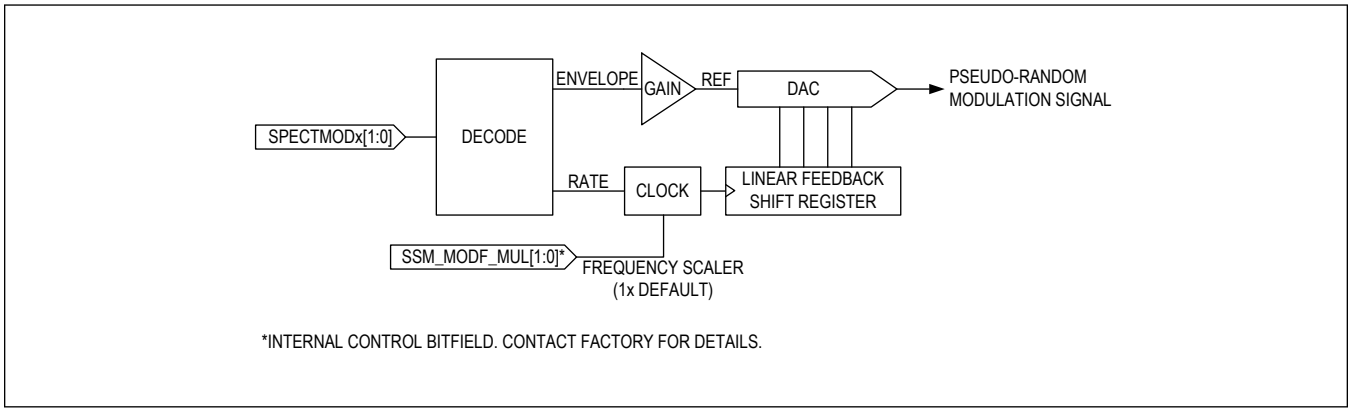


Figure 6. Pseudo-Random Modulator Engine

Use the SPECTMODx[1:0] bitfield to enable spread-spectrum to one of three modulation rates (F_{SSMOD}). F_{SSMOD} sets the frequency at which the LFSR wraps back to the seed value. The clock rate of the LFSR is F_{LFSR}. This is the frequency at which one pseudo-random value changes to another. Refer to Figure 7 for an illustration.

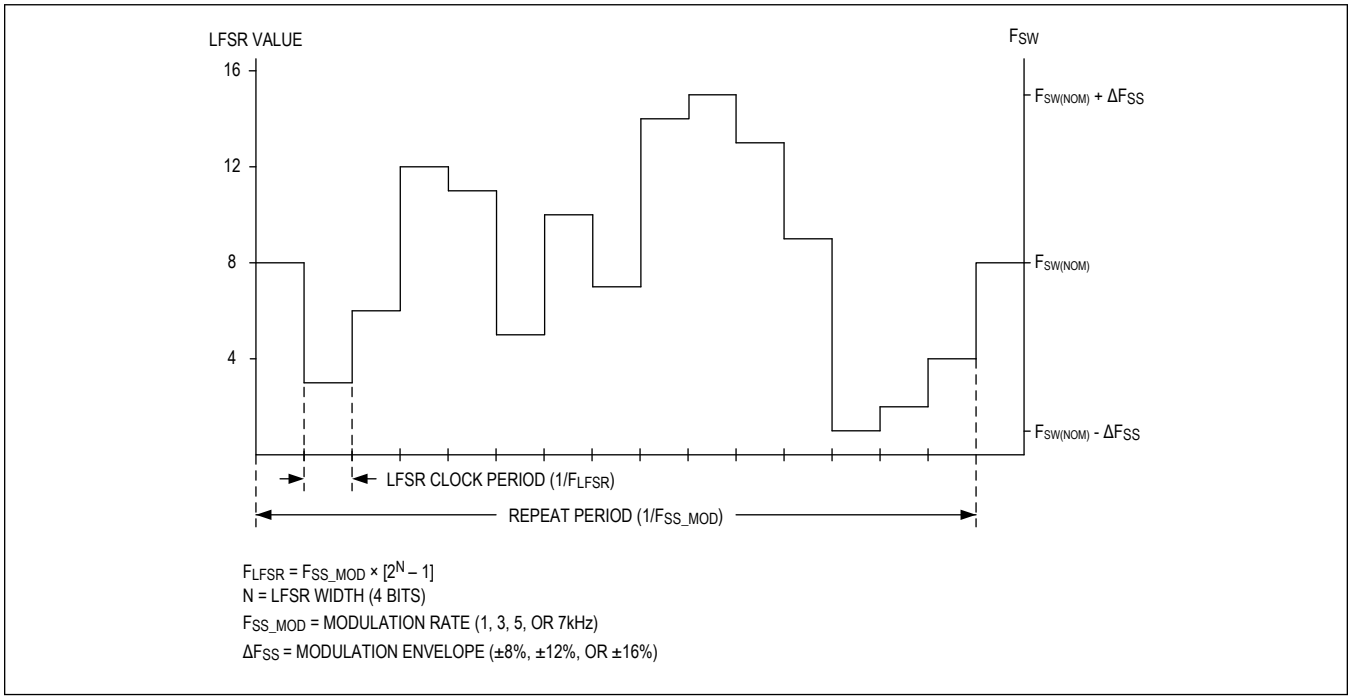


Figure 7. 4-Bit Pseudo-Random Modulation Signal Example

Triangular Pattern

The triangular engine uses a 4-bit up/down synchronous counter to create a stepped triangle pattern. Refer to Figure 8. The counter value is converted to an analog signal and then amplified before being added to the output of the on-time generator circuit. The counter value progressively shortens and lengthens the on-time of the converter. This causes the control loop to progressively increase and decrease the switching frequency to maintain voltage regulation. Each buck has its own triangular pattern generator.

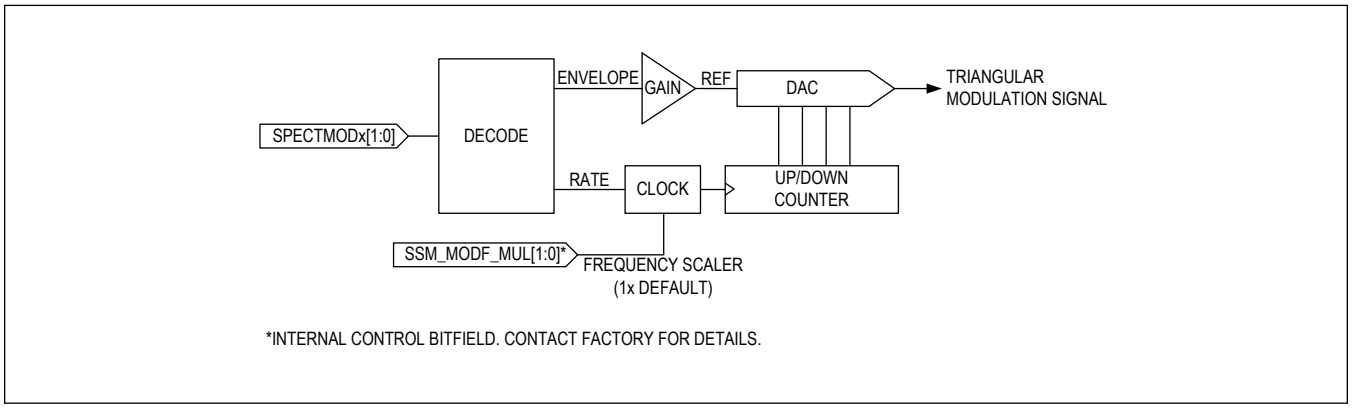


Figure 8. Triangular Modulator Engine

Use the SPECTMODx[1:0] bitfield to enable spread-spectrum to one of three modulation rates (F_{SSMOD}). F_{SSMOD} sets the frequency at which the counter returns to the same value. The clock rate of the counter is F_{COUNT}. This is the frequency at which the frequency changes from one value to another. Refer to Figure 9 for an illustration.

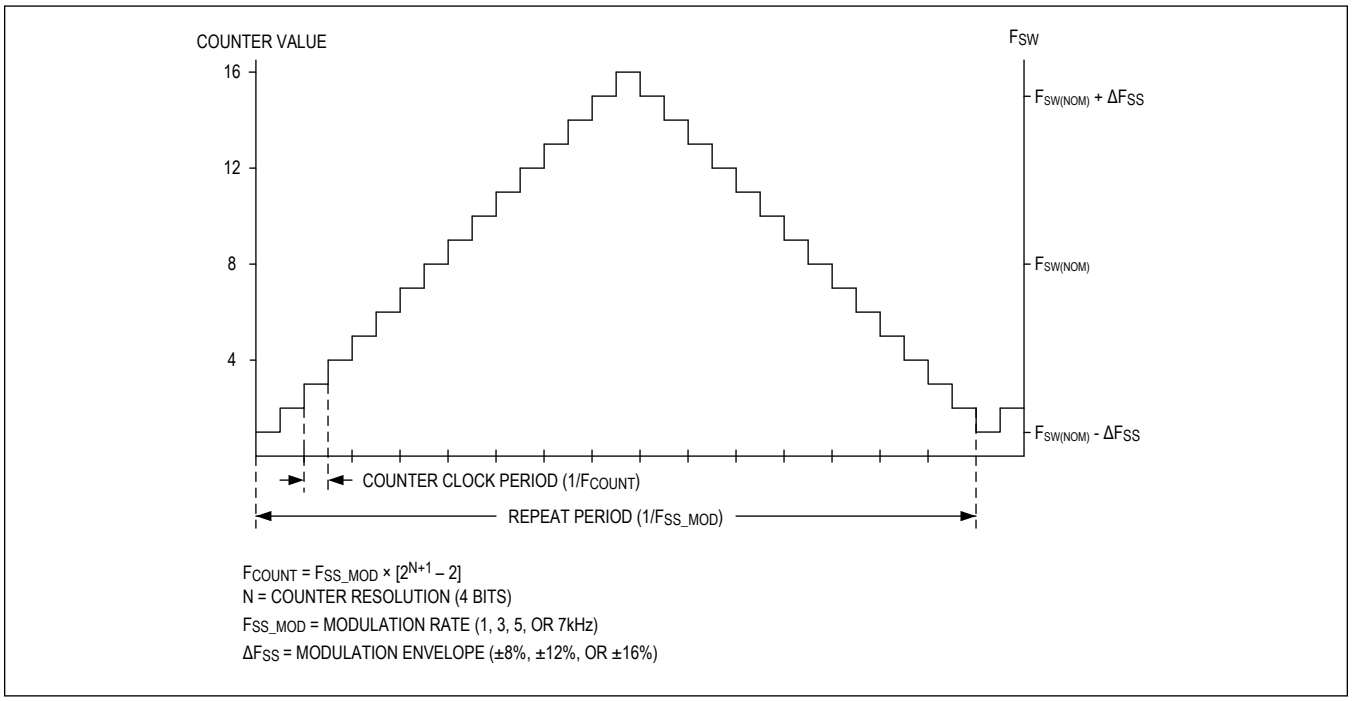


Figure 9. 4-Bit Triangular Modulation Signal Example

Output Current Monitoring

The IC is capable of sensing DC current in each switching phase.

The output of the circuit is the AMUX pin. The signal on AMUX ranges from 0V to V_{FS} (1.0V typ). Use the MUX_SEL[2:0] bitfield to select which phase the AMUX pin is monitoring current from.

For measuring current in multiphase buck configurations, the host controller must convert current in each phase and then perform the addition. The MAX77511/MAX77711 only provides current information *per phase*. Current information is not summed for multiphase bucks.

Method for Measuring Buck Converter Output Current

1. Program the multiplexer to switch to the desired output phase by changing the bits in MUX_SEL[2:0].
2. Wait the appropriate channel switching and signal settling time (200µs typ).
3. Convert the voltage on the AMUX pin and use Equation 1 to determine the average current in that phase.
4. If using a multiphase buck configuration, then multiply the result of Equation 1 by the number of phases in the buck to approximate the total current (Equation 2).

Equation 1

$$I_{PHASE(AVG)} = V_{AMUX} / G_{DCIMON}$$

where G_{DCIMON} is the gain of the current monitor (0.333V/A typ).

Equation 2

$$I_{OUT(AVG)} = I_{PHASE(AVG)} \times N$$

where $I_{PHASE(AVG)}$ is the result of the current measurement of a single phase (Equation 1) and N is the number of switching phases configured for the corresponding buck.

A more accurate output current measurement is possible by converting the current in a multiphase buck's individual phases and then adding the results. For example, measure the output current of a 3Φ buck configuration by repeating steps 1-3 for each of the three phases in sequence. Add the individual phase measurements together to find the total buck output current.

Short-Circuit and Thermal Protection

The IC has fault protection designed to protect itself from abnormal conditions. If any buck is overloaded, cycle-by-cycle current limit prevents inductor current (in each phase) from increasing beyond $I_{PEAK-HSx}$. If an on-time is ended by current limit, then the buck prevents a new on-time from starting until the inductor current falls below I_{VALLEY} (1A less than $I_{PEAK-HS}$ typ). This prevents inductor current from increasing uncontrollably due to the overloaded output.

The bucks have additional short-circuit protection (SCP) and over-temperature lockout (OTLO) protection functions that operate according to the state machine in Figure 10. The operation of the state machine is summarized as follows:

- If any enabled buck output falls below V_{POK-F} (typically 78% of regulation target), then a warning interrupt asserts (SCPWRN_I).
- If any enabled buck output stays below V_{POK-R} (typically 82% of regulation target) for longer than $t_{SFTSHRT}$, then all resources disable and a fault interrupt asserts (FLT_I).
- If any phase has 16 consecutive on-times terminated by current limit, then a warning interrupt asserts (SCPWRN_I).
- If any phase continues to have an unbroken string of on-times terminated by current limit for longer than $t_{SFTSHRT}$, then all resources disable and a fault interrupt asserts (FLT_I).
- If any enabled output falls below V_{SCP} (typically 20% of regulation target), then all resources disable and a fault interrupt asserts (FLT_I).
- If the junction temperature exceeds T_{OTLO} (165°C typ), then all resources disable and a fault interrupt asserts (FLT_I).
- If the FLT_I interrupt asserts, then the IC pulls the nRSTIO pin low and latches into an internal fault state (FLT = 1). Resources may not enable until the fault state clears.
- If there is no fault condition but the nRSTIO pin is pulled low externally, then all resources disable. No interrupt asserts when nRSTIO is driven low externally. Resources may not enable until nRSTIO = 1.

SCP monitoring is not active during soft-start and soft-stop ramps. SCP is active during DVS ramps.

OTLO monitoring is active whenever any of the following conditions are true:

- Any buck enables.
- The force thermal protection enable bit sets (FTPEN = 1). See the *Register Map*.
- Thermal protection enables (for any reason) and detects T_J > 120°C (TJ_S[1:0] reads > 0b00). Protection automatically remains active until T_J < 105°C.

The internal fault state is exited when all of the following conditions are true:

- The die temperature falls below T_{OTLO} by approximately 15°C (TJ_S[1:0] < 0b11).
- ENSEQ pin is logic-low.
- All or some bucks are programmed disabled:
  - If the fault state was latched due to SCP, then only the buck that caused the SCP needs to be disabled.
  - If the fault state was latched due to OTLO, then all bucks must be disabled.

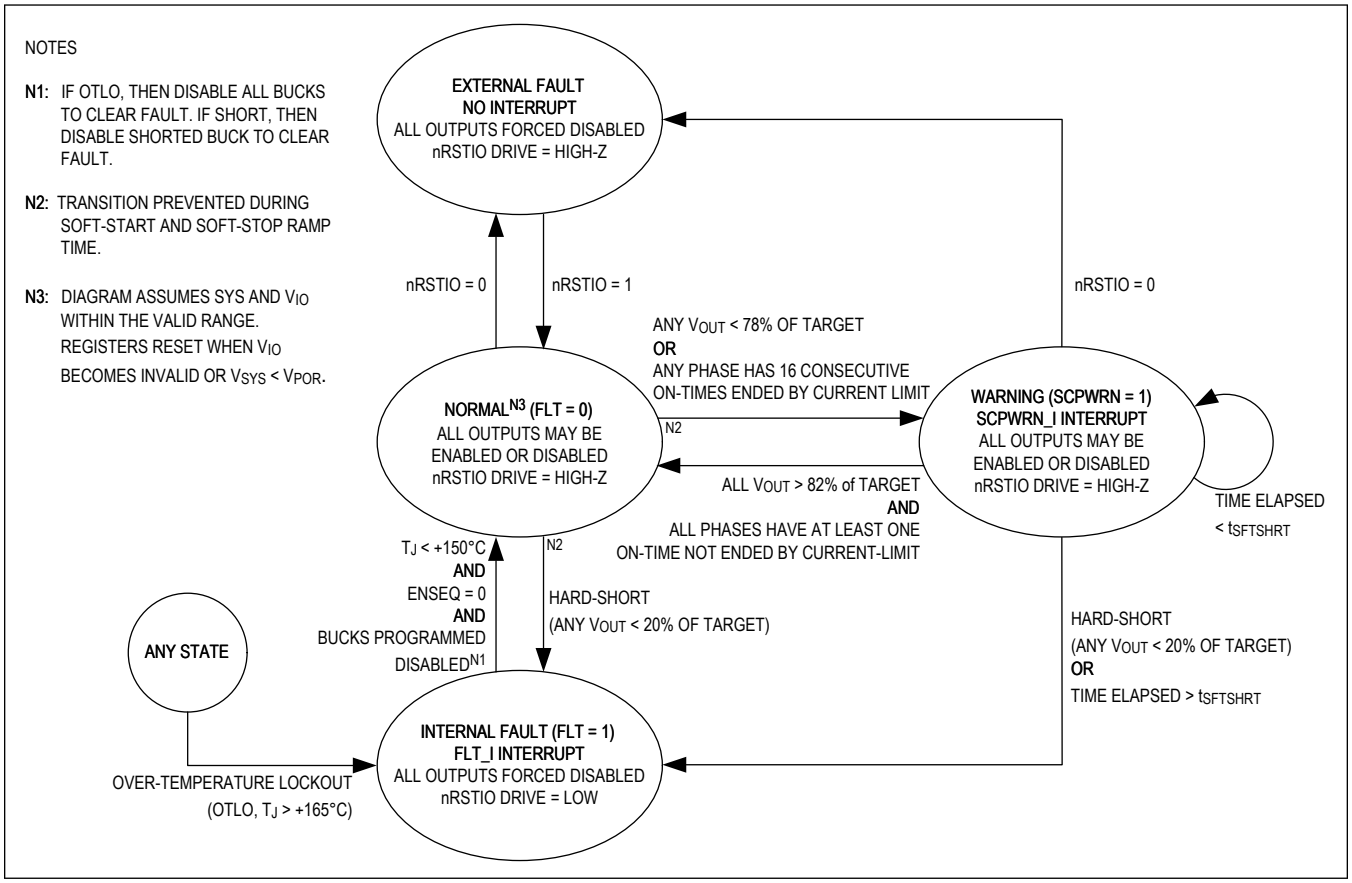


Figure 10. Fault Protection State Machine

Reset Input/Ouput (nRSTIO)

nRSTIO is an active-low, open-drain input/output pin that is typically connected to all other MAX77511/MAX77711 nRSTIO pins on the PCB. Use nRSTIO in systems using multiple MAX77511/MAX77711 devices that need all outputs to shut off simultaneously if any one output detects a fault (short-circuit or OTLO). See Figure 11 for a recommended system diagram.

The IC asserts nRSTIO low if FLT = 1. The IC stops driving nRSTIO low when the fault state is cleared (FLT = 0). See Figure 10 for details about the IC fault protection logic.

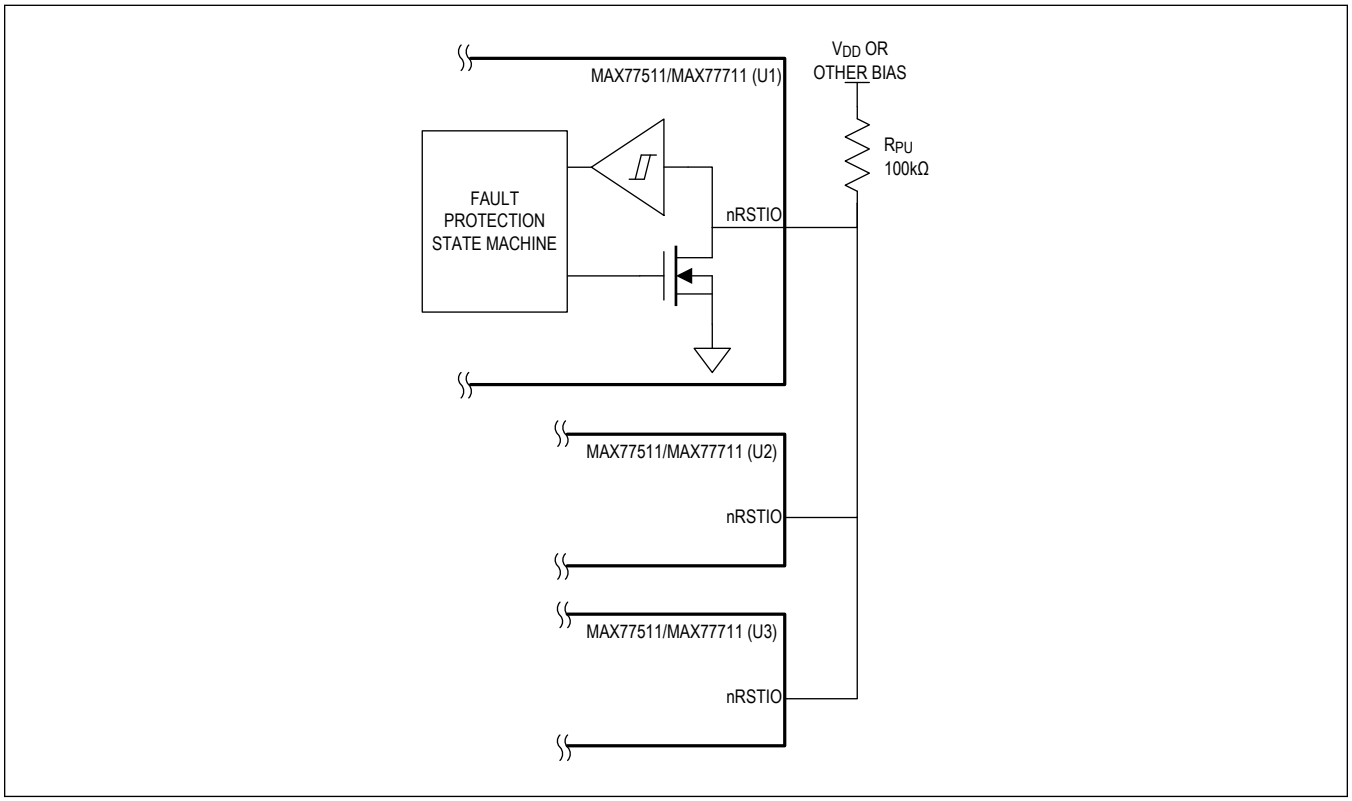


Figure 11. Common nRSTIO for Fault Signaling

Detailed Description—Linear Regulator (MAX77711 Only)

The MAX77711 integrates a 300mA PMOS low-dropout linear voltage regulator (LDO). Output voltage is programmable through I²C between 0.4V and 1.975V in 25mV steps using the LDO_VREG[5:0] bitfield. A 100Ω (typ) active-discharge resistor is available to quickly discharge the LDOs output after the regulator has been disabled.

The LDO is not available in the MAX77511. When using MAX77511, connect the INLDO and LDO pins to ground on the PCB and do not make changes to the LDO control registers.

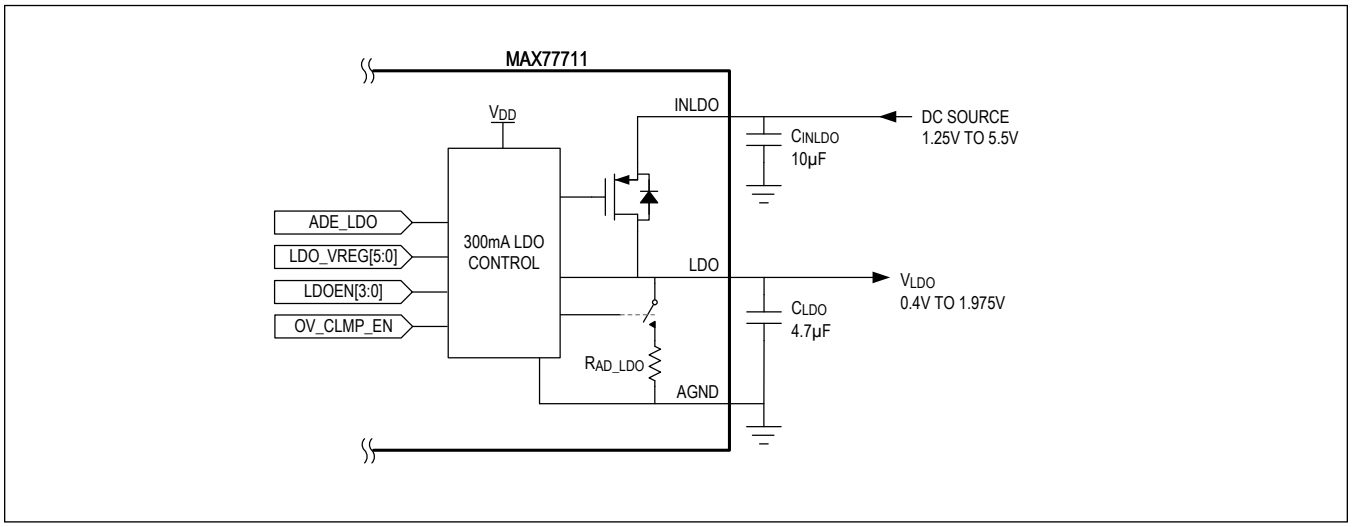


Figure 12. LDO Simplified Block Diagram

LDO Enable Control

LDO Software Enable

Use the I²C serial interface to program the LDOEN[3:0] bitfield to 0b001 to enable the LDO. Program LDOEN[3:0] to 0b000 to disable the LDO. The serial interface is active whenever V_{IO} is valid. Do not make changes to this bitfield if using the MAX77511.

LDO Hardware Enable

An LDO enable pin is available by assigning a GPIO as a special function LDO enable input (LDOEN). When a GPIO is programmed as an enable input, then the interaction between the enable pin and the software (I²C) enable command is a logical *OR*. The GPIOs derive logic thresholds from the V_{IO} pin. V_{IO} must be valid for the GPIOs to function.

Program any GPIOs FUNCx[2:0] bitfield to 0b100 to configure that GPIO as an LDO enable pin. The logical relationship between multiple GPIOs assigned to enable the LDO is a logic *OR*. See the *Register Map* section for more information. Do not configure a GPIO as an LDO enable pin when using the MAX77511.

LDO Flexible Power Sequencer Enable

The LDO can be controlled using the Flexible Power Sequencer (FPS). See the *Flexible Power Sequencer (FPS)* section for a full description.

The LDOEN[3:0] bitfield controls the LDOs slot assignment in the FPS. The default value of this bitfield can be programmed at the factory. The LDO cannot be assigned to a FPS slot and forced-enabled/disabled through software at the same time. However, a GPIO LDO enable pin can be assigned while the same LDO is assigned to a sequencer slot. The logical interaction between the FPS (ENSEQ) and the GPIO enable pin is a logical *OR*. See the *Register Map* section of the data sheet for more information. Do not assign the LDO to the FPS when using the MAX77511.

Detailed Description—I²C Serial Interface

All MAX77511/MAX77711 versions feature a revision 3.0 I²C-compatible, 2-wire serial interface consisting of a bidirectional serial data line (SDA) and a serial clock line (SCL). The MAX77511/MAX77711 is a slave-only device that relies on an external bus master to generate SCL. SCL clock rates from 0Hz to 3.4MHz are supported. I²C is an open-drain bus, and therefore, SDA and SCL require pullups.

The device's I²C communication controller implements 7-bit slave addressing. An I²C bus master initiates communication with the slave by issuing a START condition followed by the slave address. The slave address is pin-programmable on the PCB using the PHCFG1 and PHCFG0 pins (see Table 10). These pins also set the buck regulator's phase configuration (see *Phase Configuration*). All slave addresses not mentioned in Table 10 are not acknowledged.

The device uses 8-bit registers with 8-bit register addressing. They support standard communication protocols: (1) Writing to a single register, (2) Writing to multiple sequential registers with an automatically incrementing data pointer, (3) Reading from a single register, (4) Reading from multiple sequential registers with an automatically incrementing data pointer. For additional information on the I²C protocols, refer to the *MAX77511/MAX77711 I²C Implementation Guide.*

Table 10. I²C Slave Address Options

[PHCFG1, PHCFG0]	PHASE (Φ) CONFIGURATION	7-BIT SLAVE ADDRESS	8-BIT WRITE ADDRESS	8-BIT READ ADDRESS
[0, 0]	4Φ	0x71 0b 111 0001	0xE2 0b 1110 0010	0xE3 0b 1110 0011
[0, 1]	3Φ+1Φ	0x72 0b 111 0010	0xE4 0b 1110 0100	0xE5 0b 1110 0101
[0, Z]	2Φ+2Φ	0x73 0b 111 0011	0xE6 0b 1110 0110	0xE7 0b 1110 0111
[1, 0]	2Φ+1Φ+1Φ	0x74 0b 111 0100	0xE8 0b 1110 1000	0xE9 0b 1110 1001
[1, 1]	2Φ+1Φ+1Φ	0x75 0b 111 0101	0xEA 0b 1110 1010	0xEB 0b 1110 1011
[1, Z]	1Φ+1Φ+1Φ+1Φ	0x76 0b 111 0110	0xEC 0b 1110 1100	0xED 0b 1110 1101
[Z, 0]	1Φ+1Φ+1Φ+1Φ	0x77 0b 111 0111	0xEE 0b 1110 1110	0xEF 0b 1110 1111
[Z, 1]	1Φ+1Φ+1Φ+1Φ	0x4E 0b 100 1110	0x9C 0b 1001 1100	0x9D 0b 1001 1101
[Z, Z]	1Φ+1Φ+1Φ+1Φ	0x4F 0b 100 1111	0x9E 0b 1001 1110	0x9F 0b 1001 1111

See Phase Configurations for more information on the PHCFG1 and PHCFG0 pins.

Test Mode

The MAX77511/MAX77711 acknowledges the 8-bit device write address 0x50 when test mode is unlocked. Test mode details are confidential. The IC remains out of test mode during normal operation.

If possible, leave the test mode address unallocated to allow for the rare event that debugging needs to be performed in cooperation with Maxim.

Register Map

MAX77511/MAX77711

ADDRESS	NAME	MSB							LSB
Global									
0x00	INTERRUPT[7:0]	TJ_I	SYSUV_I	FLT_I	SCPWRN_I	RSVD	GPIO_I	LDOPOK_I	BPOK_I
0x01	GLBL_STATUS_A[7:0]	RNGLOCK	SYSUV	FLT	SCPWRN	BPOK4	BPOK3	BPOK2	BPOK1
0x02	GLBL_STATUS_B[7:0]	GPIOLOCK	IRQ_S	FPS_S[1:0]		TJ_S[1:0]		LDOPOK	nRSTIO_S
0x03	GPIO_STATUS[7:0]	RSVD	RSVD	GPIO_DI6	GPIO_DI5	GPIO_DI4	GPIO_DI3	GPIO_DI2	GPIO_DI1
0x04	CHIP_DTLS_A[7:0]	RSVD[3:0]				RSVD[3:0]			
0x05	CHIP_DTLS_B[7:0]	PHCFGS[3:0]				CID[3:0]			
0x06	GLBL_CNFG_A[7:0]	MUX_SEL[2:0]			FVLEN	FPS_SLOT_T[1:0]		SCPWARN_TIME[1:0]	
0x07	GLBL_CNFG_B[7:0]	TJ_IM	SYSUV_IM	FLT_IM	SCPWRN_IM	RSVD[3:0]			
0x08	GLBL_CNFG_C[7:0]	RSVD[6:0]							FTPEN
Buck 1 Configuration									
0x10	B1_CNFG_A[7:0]	ILIM1[1:0]		MODE1[1:0]		BEN1[3:0]			
0x11	B1_CNFG_B[7:0]	BPOK1_IM	ADEN1	SPECTMOD1[1:0]		FSREN1	SFTUPDN1[2:0]		
0x12	B1_CNFG_C[7:0]	RSVD	RNG1	DVSRISE1[2:0]			DVSFALL1[2:0]		
0x13	B1_CNFG_D[7:0]	VOUTREG1[7:0]							
0x14	B1_CNFG_E[7:0]	VOUTREGDVS1[7:0]							
Buck 2 Configuration									
0x20	B2_CNFG_A[7:0]	ILIM2[1:0]		MODE2[1:0]		BEN2[3:0]			
0x21	B2_CNFG_B[7:0]	BPOK2_IM	ADEN2	SPECTMOD2[1:0]		FSREN2	SFTUPDN2[2:0]		
0x22	B2_CNFG_C[7:0]	RSVD	RNG2	DVSRISE2[2:0]			DVSFALL2[2:0]		
0x23	B2_CNFG_D[7:0]	VOUTREG2[7:0]							
0x24	B2_CNFG_E[7:0]	VOUTREGDVS2[7:0]							
Buck 3 Configuration									
0x30	B3_CNFG_A[7:0]	ILIM3[1:0]		MODE3[1:0]		BEN3[3:0]			
0x31	B3_CNFG_B[7:0]	BPOK3_IM	ADEN3	SPECTMOD3[1:0]		FSREN3	SFTUPDN3[2:0]		
0x32	B3_CNFG_C[7:0]	RSVD	RNG3	DVSRISE3[2:0]			DVSFALL3[2:0]		
0x33	B3_CNFG_D[7:0]	VOUTREG3[7:0]							
0x34	B3_CNFG_E[7:0]	VOUTREGDVS3[7:0]							
Buck 4 Configuration									
0x40	B4_CNFG_A[7:0]	ILIM4[1:0]		MODE4[1:0]		BEN4[3:0]			
0x41	B4_CNFG_B[7:0]	BPOK4_IM	ADEN4	SPECTMOD4[1:0]		FSREN4	SFTUPDN4[2:0]		

ADDRESS	NAME	MSB							LSB
0x42	B4_CNFG_C[7:0]	RSVD	RNG4	DVSRISE4[2:0]			DVSFALL4[2:0]		
0x43	B4_CNFG_D[7:0]	VOUTREG4[7:0]							
0x44	B4_CNFG_E[7:0]	VOUTREGDVS4[7:0]							
LDO Configuration (MAX77711 Only)									
0x50	LDO_CNFG_A[7:0]	OV_CLMP_EN	RSVD	LDOPOK_IM	ADE_LDO	LDOEN[3:0]			
0x51	LDO_CNFG_B[7:0]	RSVD	RSVD	LDO_VREG[5:0]					
GPIO Configuration									
0x60	GPIO_INT[7:0]	RSVD	RSVD	INT6	INT5	INT4	INT3	INT2	INT1
0x61	GPIO_PULLUP[7:0]	RSVD	RSVD	PU6	PU5	PU4	PU3	PU2	PU1
0x62	GPIO_PULLDN[7:0]	RSVD	RSVD	PD6	PD5	PD4	PD3	PD2	PD1
0x64	GPIO_CNFG1[7:0]	IRQ_SEL1[1:0]		DBNC_SEL1[1:0]		DATA1	DIR1[1:0]		DRV1
0x65	GPIO_CNFG2[7:0]	IRQ_SEL2[1:0]		DBNC_SEL2[1:0]		DATA2	DIR2[1:0]		DRV2
0x66	GPIO_CNFG3[7:0]	IRQ_SEL3[1:0]		DBNC_SEL3[1:0]		DATA3	DIR3[1:0]		DRV3
0x67	GPIO_CNFG4[7:0]	IRQ_SEL4[1:0]		DBNC_SEL4[1:0]		DATA4	DIR4[1:0]		DRV4
0x68	GPIO_CNFG5[7:0]	IRQ_SEL5[1:0]		DBNC_SEL5[1:0]		DATA5	DIR5[1:0]		DRV5
0x69	GPIO_CNFG6[7:0]	IRQ_SEL6[1:0]		DBNC_SEL6[1:0]		DATA6	DIR6[1:0]		DRV6
0x6A	GPIO_FUNC1[7:0]	RSVD	RSVD	RSVD	BSEL1[1:0]		FUNC1[2:0]		
0x6B	GPIO_FUNC2[7:0]	RSVD	RSVD	RSVD	BSEL2[1:0]		FUNC2[2:0]		
0x6C	GPIO_FUNC3[7:0]	RSVD	RSVD	RSVD	BSEL3[1:0]		FUNC3[2:0]		
0x6D	GPIO_FUNC4[7:0]	RSVD	RSVD	RSVD	BSEL4[1:0]		FUNC4[2:0]		
0x6E	GPIO_FUNC5[7:0]	RSVD	RSVD	RSVD	BSEL5[1:0]		FUNC5[2:0]		
0x6F	GPIO_FUNC6[7:0]	RSVD	RSVD	RSVD	BSEL6[1:0]		FUNC6[2:0]		
0x70	GPIO_FPS[7:0]	GPIOSEQ6[3:0]				GPIOSEQ5[3:0]			

Register Details

INTERRUPT (0x00)

BIT	7	6	5	4	3	2	1	0
Field	TJ_I	SYSUV_I	FLT_I	SCPWRN_I	RSVD	GPIO_I	LDOPOK_I	BPOK_I
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
TJ_I	7	Thermal Status Interrupt. Operation of this interrupt is affected by FTPEN.	0 = Die temperature has not risen. TJ_S[1:0] digital code has not increased. 1 = Die temperature has risen. TJ_S[1:0] has increased.
SYSUV_I	6	SYS Undervoltage Lockout Interrupt	0 = SYS has not fallen below V_{UVLO_F}. 1 = SYS has fallen below V_{UVLO_F}. SYSUV has changed to 1.
FLT_I	5	Fault Interrupt	0 = No fault happened. 1 = Fault happened. FLT has changed to 1.

BITFIELD	BITS	DESCRIPTION	DECODE
SCPWRN_I	4	Short-Circuit Protection Warning Interrupt	0 = No Short-Circuit Warning happened. 1 = Short-Circuit Warning happened. SCPWRN has changed to 1.
RSVD	3	Reserved. Reads back 0.	N/A
GPIO_I	2	GPIO Logic State Change Interrupt	0 = None of the bits in the GPIO_INT register have changed state. 1 = At least one of the bits in the GPIO_INT register has changed.
LDOPOK_I	1	LDO Power-OK Interrupt. Disabling the LDO does not cause an interrupt.	0 = The LDO has not fallen below $V_{POKLDO-F}$. 1 = The LDO has fallen below $V_{POKLDO-F}$. The LDO is enabled and LDOPOK has changed to 0.
BPOK_I	0	Buck Power-OK Interrupt. Disabling any buck does not cause an interrupt.	0 = All unmasked and enabled buck(s) have not fallen below V_{POK-F}. 1 = One or more unmasked and enabled buck(s) have fallen below the power-OK threshold (V_{POK-F}). One or more BPOKx bits changed to 0 while enabled.

GLBL_STATUS_A (0x01)

BIT	7	6	5	4	3	2	1	0
Field	RNGLOCK	SYSUV	FLT	SCPWRN	BPOK4	BPOK3	BPOK2	BPOK1
Reset	OTP	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
RNGLOCK	7	Factory-set safety bit for all buck output voltage range control bits (RNGx).	0 = RNGx can be changed. 1 = RNGx can not be changed. Writes to RNGx are ignored.
SYSUV	6	SYS Undervoltage Lockout Status	0 = V_{SYS} is OK. 1 = $V_{SYS} < V_{UVLO\_F}$
FLT	5	Short-Circuit Protection (SCP) and Over-Temperature Lockout (OTLO) Fault Status. This bit indicates the IC is latched in a fault state. Clear the fault state according to Figure 10.	0 = No SCP or OTLO fault. This IC has not detected a short in any buck regulator and the junction temperature has remained below T_{OTLO}. 1 = SCP or OTLO fault. This IC detected a short in at least one buck regulator or $T_J > T_{OLTO}$. This IC is pulling nRSTIO low.
SCPWRN	4	Short-Circuit Protection Warning Status	0 = No Short-Circuit Warning. This IC is not in the short-circuit warning state. 1 = Short-Circuit Warning. This IC is in the short-circuit warning state.
BPOK4	3	Buck 4 Power-OK Status	0 = Output not OK ($V_{OUT4} < V_{POK-F}$) or disabled. 1 = Output OK ($V_{OUT4} > V_{POK-R}$).
BPOK3	2	Buck 3 Power-OK Status	0 = Output not OK ($V_{OUT3} < V_{POK-F}$) or disabled. 1 = Output OK ($V_{OUT3} > V_{POK-R}$).
BPOK2	1	Buck 2 Power-OK Status	0 = Output not OK ($V_{OUT2} < V_{POK-F}$) or disabled. 1 = Output OK ($V_{OUT2} > V_{POK-R}$).
BPOK1	0	Buck 1 Power-OK Status	0 = Output not OK ($V_{OUT1} < V_{POK-F}$) or disabled. 1 = Output OK ($V_{OUT1} > V_{POK-R}$).

GLBL_STATUS_B (0x02)

BIT	7	6	5	4	3	2	1	0
Field	GPIOLOCK	IRQ_S	FPS_S[1:0]		TJ_S[1:0]		LDOPOK	nRSTIO_S
Reset	OTP	0b0	0b00		0b00		0b0	0b0
Access Type	Read Only	Read Only	Read Only		Read Only		Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
GPIOLOCK	7	Factory-set safety bit for all GPIO functions. Determines if the function assignment of the GPIOs can be changed by serial writes.	0 = FUNCx[2:0] and BSELx[1:0] can be changed. 1 = FUNCx[2:0] and BSELx[1:0] can not be changed. Writes to these bitfields are ignored.
IRQ_S	6	Interrupt Status. Continuous *inverted* software mirror of the nIRQ pin as if all interrupts were unmasked.	0 = No interrupts pending. nIRQ would be high if all interrupts were unmasked. 1 = Interrupts pending. nIRQ would be low if all interrupts were unmasked.
FPS_S	5:4	Flexible Power Sequencer (FPS) Status	00 = FPS is off. 01 = FPS in in power-up sequence. 10 = FPS is in power-down sequence. 11 = FPS is on.
TJ_S	3:2	Junction Temperature (T_J) Status. Operation of this status is affected by FTPEN. If FPTEN = 1, this bitfield always works and thermal protection is continuously active regardless of buck enable. If FTPEN = 0, this bitfield only works when any buck is enabled.	00 = No Alarm (T_J < 120°C) 01 = Thermal Alarm 1 (120°C < T_J < 140°C) 10 = Thermal Alarm 2 (140°C < T_J < 165°C) 11 = OTLO (T_J > 165°C). This condition causes fault (FLT = 1).
LDOPOK	1	LDO Power-OK Status	0 = LDO output not OK (V_{LDO} < $V_{LDOPOK-F}$) or disabled 1 = LDO output OK (V_{LDO} > $V_{LDOPOK-R}$)
nRSTIO_S	0	Reset I/O (nRSTIO) Status. Continuously mirrors the debounced logic status of the nRSTIO pin.	0 = nRSTIO is logic-low. 1 = nRSTIO is logic-high.

GPIO_STATUS (0x03)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	GPIO_DI6	GPIO_DI5	GPIO_DI4	GPIO_DI3	GPIO_DI2	GPIO_DI1
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	Reserved. Reads back 0.	N/A
RSVD	6	Reserved. Reads back 0.	N/A
GPIO_DI6	5	GPIO6 Digital Input Value. Reflects the debounced status of the GPIO when DIR6[1:0] = 0b10 or 0b11.	0 = Input logic low 1 = Input logic high
GPIO_DI5	4	GPIO5 Digital Input Value. Reflects the debounced status of the GPIO when DIR5[1:0] = 0b10 or 0b11.	0 = Input logic low 1 = Input logic high

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_DI4	3	GPIO4 Digital Input Value. Reflects the debounced status of the GPIO when DIR4[1:0] = 0b10 or 0b11.	0 = Input logic low 1 = Input logic high
GPIO_DI3	2	GPIO3 Digital Input Value. Reflects the debounced status of the GPIO when DIR3[1:0] = 0b10 or 0b11.	0 = Input logic low 1 = Input logic high
GPIO_DI2	1	GPIO2 Digital Input Value. Reflects the debounced status of the GPIO when DIR2[1:0] = 0b10 or 0b11.	0 = Input logic low 1 = Input logic high
GPIO_DI1	0	GPIO1 Digital Input Value. Reflects the debounced status of the GPIO when DIR1[1:0] = 0b10 or 0b11.	0 = Input logic low 1 = Input logic high

CHIP_DTLS_A (0x04)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[3:0]				RSVD[3:0]			
Reset	0b0000				0b0010			
Access Type	Read Only				Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7:4	Reserved. Reads back 0b0000.	N/A
RSVD	3:0	Reserved. Bits for internal use only.	N/A

CHIP_DTLS_B (0x05)

BIT	7	6	5	4	3	2	1	0
Field	PHCFGS[3:0]				CID[3:0]			
Reset	0b0000				OTP			
Access Type	Read Only				Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
PHCFGS	7:4	Phase Configuration Status. Indicates the latched phase (Φ) configuration from the [PHCFG1,PHCFG0] tri-state logic inputs.	0000 = [0,0] 4Φ 0001 = [0,1] 3Φ + 1Φ 0010 = [0,Z] 2Φ + 2Φ 0011 = Invalid 0100 = [1,0] 2Φ + 1Φ + 1Φ 0101 = [1,1] 2Φ + 1Φ + 1Φ 0110 = [1,Z] 1Φ + 1Φ + 1Φ + 1Φ 0111 = Invalid 1000 = [Z,0] 1Φ + 1Φ + 1Φ + 1Φ 1001 = [Z,1] 1Φ + 1Φ + 1Φ + 1Φ 1010 = [Z,Z] 1Φ + 1Φ + 1Φ + 1Φ 1011-1111 = Invalid

BITFIELD	BITS	DESCRIPTION	DECODE
CID	3:0	Chip Identification Code for OTP Options. Refer to the *Ordering Information* for production status.	0x0 = MAX77711A 0x2 = MAX77711B 0x4 = MAX77711C 0x5 = MAX77711D 0x1 = MAX77511A 0x7 = MAX77511M 0x8 = MAX77511R 0x9 = MAX77511L All other codes reserved for future use.

GLBL_CNFG_A (0x06)

BIT	7	6	5	4	3	2	1	0
Field	MUX_SEL[2:0]			FVLEN	FPS_SLOT_T[1:0]		SCPWARN_TIME[1:0]	
Reset	0b000			OTP	OTP		OTP	
Access Type	Write, Read			Write, Read	Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MUX_SEL	7:5	DC Current Monitor Selection	000 = Multiplexer is disabled and AMUX is high-impedance. 001 = Phase 1 Current Monitor. 010 = Phase 2 Current Monitor. 011 = Phase 3 Current Monitor. 100 - 111 = Phase 4 Current Monitor.
FVLEN	4	Force V_{L13} and V_{L24} Pre-Enable Control. Clear this bit to reduce standby supply current (I_{STNDBY}). Set this bit to shorten buck startup delay time (t_{SUDLY}).	0 = The V_{L13}/V_{L24} regulators are not forced pre-enabled. V_{L13}/V_{L24} automatically turn on when needed. 1 = The V_{L13}/V_{L24} regulators are forced pre-enabled regardless of buck enable.
FPS_SLOT_T	3:2	Flexible Power Sequencer Slot Pitch Control. Sets t_{SLOT} (time between startup slots).	00 = 0.625ms 01 = 1.25ms 10 = 2.5ms 11 = 5ms
SCPWARN_TIME	1:0	Short-Circuit Protection Shutdown Timer. Sets $t_{SFTSHRT}$. The IC shuts down all outputs and drives nRSTIO low if any enabled buck output remains less than 80% of target output voltage for this time.	00 = Timer disabled (infinity) 01 = 25ms 10 = 50ms 11 = 100ms

GLBL_CNFG_B (0x07)

BIT	7	6	5	4	3	2	1	0
Field	TJ_IM	SYSUV_IM	FLT_IM	SCPWRN_IM	RSVD[3:0]			
Reset	0b1	0b1	0b1	0b1	0b0000			
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
TJ_IM	7	Thermal Status Interrupt Mask	0 = TJ_I is unmasked. 1 = TJ_I is masked.

BITFIELD	BITS	DESCRIPTION	DECODE
SYSUV_IM	6	SYS Undervoltage Lockout Interrupt Mask	0 = SYSUV_I is unmasked. 1 = SYSUV_I is masked.
FLT_IM	5	Fault Protection Interrupt Mask	0 = FLT_I is unmasked. 1 = FLT_I is masked.
SCPWRN_IM	4	Short-Circuit Protection Warning Interrupt Mask	0 = SCPWRN_I is unmasked. 1 = SCPWRN_I is masked.
RSVD	3:0	Reserved. Bitfield is a *don't care*.	N/A

GLBL_CNFG_C (0x08)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[6:0]							FTPEN
Reset	0b0000000							0b0
Access Type	Write, Read							Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7:1	Reserved. Bitfield is a *don't care*.	N/A
FTPEN	0	Force Thermal Protection Enable	0 = Thermal protection automatically enables when any buck enables. 1 = Thermal protection is always enabled even if all bucks are disabled.

B1_CNFG_A (0x10)

BIT	7	6	5	4	3	2	1	0
Field	ILIM1[1:0]		MODE1[1:0]		BEN1[3:0]			
Reset	OTP		0b01		OTP			
Access Type	Write, Read		Write, Read		Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
ILIM1	7:6	Buck 1 Peak Inductor Current Limit Control. Sets $I_{PEAK-HS}$ for all buck 1 phases.	00 = 1.5A 01 = 2.25A 10 = 3.0A 11 = 4.5A
MODE1	5:4	Buck 1 Mode Control. Turbo SKIP is the recommended default setting. Use SKIP mode when loads are expected <10mA/phase. Use FPWM mode for the highest V_{OUT} accuracy and lowest ripple.	00 = SKIP Mode 01 = Turbo SKIP Mode 10-11 = Forced-PWM (FPWM) Mode

BITFIELD	BITS	DESCRIPTION	DECODE
BEN1	3:0	Buck 1 Enable Control. Hardware enable inputs (using GPIO) are a logical *OR* with the control output from this bitfield.	0000 = Disabled 0001 = Enabled 0010 = FPS Slot 1 0011 = FPS Slot 2 0100 = FPS Slot 3 0101 = FPS Slot 4 0110 = FPS Slot 5 0111 = FPS Slot 6 1000 = FPS Slot 7 1001 = FPS Slot 8 1010 = FPS Slot 9 1011 = FPS Slot 10 1100 = FPS Slot 11 1101 = FPS Slot 12 1110-1111 = FPS Slot 12

B1_CNFG_B (0x11)

BIT	7	6	5	4	3	2	1	0
Field	BPOK1_IM	ADEN1	SPECTMOD1[1:0]		FSREN1	SFTUPDN1[2:0]		
Reset	0b1	0b1	0b00		0b1	OTP		
Access Type	Write, Read	Write, Read	Write, Read		Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
BPOK1_IM	7	Buck 1 POK Interrupt Mask	0 = Unmasked. The buck power-OK interrupt (BPOK_I) asserts when buck 1 is enabled and BPOK1 changes from 1 to 0. 1 = Masked. The buck power-OK interrupt (BPOK_I) does not assert due to buck 1.
ADEN1	6	Buck 1 Active Discharge Resistor Enable	0 = Disabled 1 = Enabled
SPECTMOD1	5:4	Buck 1 Pseudo-Random Spread-Spectrum Modulation Profile. Sets the modulation frequency (F_{SSMOD}) and envelope. Buck 1 F_{SSMOD} is further modified by a multiplication factor set by FSSMOD_MUL1[1:0].	00 = Disabled (no spread-spectrum) 01 = Profile 1 (3kHz, ±8% envelope) 10 = Profile 2 (5kHz, ±8% envelope) 11 = Profile 3 (7kHz, ±8% envelope)
FSREN1	3	Buck 1 Falling Slew Rate Enable	0 = Strictly follows MODE1[1:0] at all times. 1 = Automatically enters forced-PWM mode for DVS and soft-stop events.
SFTUPDN1	2:0	Buck 1 Soft-Start/Stop Ramp Rate Control. V_{OUT1} increases/decreases with this slope whenever the buck is enabled or disabled.	000 = ±0.15mV/µs 001 = ±0.625mV/µs 010 = ±1.25mV/µs 011 = ±2.5mV/µs 100 = ±5mV/µs 101 = ±10mV/µs 110 = ±20mV/µs 111 = ±40mV/µs

B1_CNFG_C (0x12)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RNG1	DVSRISE1[2:0]			DVSFALL1[2:0]		
Reset	0b0	OTP	0b000			0b000		
Access Type	Write, Read	Write, Read	Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	Reserved. Bit is a *don't care*.	N/A
RNG1	6	Buck 1 Output Voltage Range Control. Sets the output voltage range of VOUTREG1[7:0] and VOUTREGDVS1[1:0].	0 = (Low-range) 0.25V to 1.3V in 5mV steps 1 = (High-range) 1V to 5.2V in 20mV steps
DVSRISE1	5:3	Buck 1 DVS Rising Ramp Rate Control. V_{OUT1} increases with this slope whenever the output voltage is modified while the buck is enabled.	000 = +0.15mV/µs 001 = +0.625mV/µs 010 = +1.25mV/µs 011 = +2.5mV/µs 100 = +5mV/µs 101 = +10mV/µs 110 = +20mV/µs 111 = +40mV/µs
DVSFALL1	2:0	Buck 1 DVS Falling Ramp Rate Control. V_{OUT1} decreases with this slope whenever the output voltage is modified while the buck is enabled.	000 = -0.15mV/µs 001 = -0.625mV/µs 010 = -1.25mV/µs 011 = -2.5mV/µs 100 = -5mV/µs 101 = -10mV/µs 110 = -20mV/µs 111 = -40mV/µs

B1_CNFG_D (0x13)

BIT	7	6	5	4	3	2	1	0
Field	VOUTREG1[7:0]							
Reset	OTP							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VOUTREG1	7:0	Buck 1 Output Voltage Control while DVS1 = 0. If no GPIO is assigned as a special-function DVS input for this buck, then DVS1 = 0 always. Valid codes between 0x00 and 0xD2 (inclusive). Writes above 0xD2 clamp to 0xD2.	**If RNG1 = 0 (low-range):** 5mV/LSB in a linear transfer function between 0x00 (0.25V) and 0xD2 (1.3V) **If RNG1 = 1 (high-range):** 20mV/LSB in a linear transfer function between 0x00 (1V) and 0xD2 (5.2V)

B1_CNFG_E (0x14)

BIT	7	6	5	4	3	2	1	0
Field	VOUTREGDVS1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VOUTREGDVS1	7:0	Buck 1 Output Voltage Control while DVS1 = 1. If no GPIO is assigned as a special-function DVS input for this buck, then DVS1 = 0 always and this register is a *don't care*. Valid codes between 0x00 and 0xD2 (inclusive). Writes above 0xD2 clamp to 0xD2.	**If RNG1 = 0 (low-range):** 5mV/LSB in a linear transfer function between 0x00 (0.25V) and 0xD2 (1.3V) **If RNG1 = 1 (high-range):** 20mV/LSB in a linear transfer function between 0x00 (1V) and 0xD2 (5.2V)

B2_CNFG_A (0x20)

BIT	7	6	5	4	3	2	1	0
Field	ILIM2[1:0]		MODE2[1:0]		BEN2[3:0]			
Reset	OTP		0b01		OTP			
Access Type	Write, Read		Write, Read		Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
ILIM2	7:6	Buck 2 Peak Inductor Current Limit Control. Sets $I_{PEAK-HS}$ for all buck 2 phases.	00 = 1.5A 01 = 2.25A 10 = 3.0A 11 = 4.5A
MODE2	5:4	Buck 2 Mode Control. Turbo SKIP is the recommended default setting. Use SKIP mode when loads are expected <10mA/phase. Use FPWM mode for the highest V_{OUT} accuracy and lowest ripple.	00 = SKIP Mode 01 = Turbo SKIP Mode 10-11 = Forced-PWM (FPWM) Mode
BEN2	3:0	Buck 2 Enable Control Hardware enable inputs (using GPIO) are a logical *OR* with the control output from this bitfield.	0000 = Disabled 0001 = Enabled 0010 = FPS Slot 1 0011 = FPS Slot 2 0100 = FPS Slot 3 0101 = FPS Slot 4 0110 = FPS Slot 5 0111 = FPS Slot 6 1000 = FPS Slot 7 1001 = FPS Slot 8 1010 = FPS Slot 9 1011 = FPS Slot 10 1100 = FPS Slot 11 1101 = FPS Slot 12 1110-1111 = FPS Slot 12

B2_CNFG_B (0x21)

BIT	7	6	5	4	3	2	1	0
Field	BPOK2_IM	ADEN2	SPECTMOD2[1:0]		FSREN2	SFTUPDN2[2:0]		
Reset	0b1	0b1	0b00		0b1	OTP		
Access Type	Write, Read	Write, Read	Write, Read		Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
BPOK2_IM	7	Buck 2 POK Interrupt Mask	0 = Unmasked. The buck power-OK interrupt (BPOK_I) asserts when buck 2 is enabled and BPOK2 changes from 1 to 0. 1 = Masked. The buck power-OK interrupt (BPOK_I) does not assert due to buck 2.
ADEN2	6	Buck 2 Active Discharge Resistor Enable	0 = Disabled 1 = Enabled
SPECTMOD 2	5:4	Buck 2 Pseudo-Random Spread-Spectrum Modulation Profile. Sets the modulation frequency (F_{SSMOD}) and envelope. Buck 2 F_{SSMOD} is by further modified by a multiplication factor set by FSSMOD_MUL2[1:0].	00 = Disabled (no spread-spectrum) 01 = Profile 1 (3kHz, ±8% envelope) 10 = Profile 2 (5kHz, ±8% envelope) 11 = Profile 3 (7kHz, ±8% envelope)
FSREN2	3	Buck 2 Falling Slew Rate Enable	0 = Strictly follows MODE2[1:0] at all times. 1 = Automatically enters forced-PWM mode for DVS and soft-stop events.
SFTUPDN2	2:0	Buck 2 Soft-Start/Stop Ramp Rate Control. V_{OUT2} increases/decreases with this slope whenever the buck is enabled or disabled.	000 = ±0.15mV/µs 001 = ±0.625mV/µs 010 = ±1.25mV/µs 011 = ±2.5mV/µs 100 = ±5mV/µs 101 = ±10mV/µs 110 = ±20mV/µs 111 = ±40mV/µs

B2_CNFG_C (0x22)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RNG2	DVSRISE2[2:0]			DVSFALL2[2:0]		
Reset	0b0	OTP	0b000			0b000		
Access Type	Write, Read	Write, Read	Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	Reserved. Bit is a *don't care*.	N/A
RNG2	6	Buck 2 Output Voltage Range Control. Sets the output voltage range of VOUTREG2[7:0] and VOUTREGDVS2[1:0].	0 = (Low-range) 0.25V to 1.3V in 5mV steps 1 = (High-range) 1V to 5.2V in 20mV steps

BITFIELD	BITS	DESCRIPTION	DECODE
DVSRISE2	5:3	Buck 2 DVS Rising Ramp Rate Control. V_{OUT2} increases with this slope whenever the output voltage is modified while the buck is enabled.	000 = +0.15mV/µs 001 = +0.625mV/µs 010 = +1.25mV/µs 011 = +2.5mV/µs 100 = +5mV/µs 101 = +10mV/µs 110 = +20mV/µs 111 = +40mV/µs
DVSFALL2	2:0	Buck 2 DVS Falling Ramp Rate Control. V_{OUT2} decreases with this slope whenever the output voltage is modified while the buck is enabled.	000 = -0.15mV/µs 001 = -0.625mV/µs 010 = -1.25mV/µs 011 = -2.5mV/µs 100 = -5mV/µs 101 = -10mV/µs 110 = -20mV/µs 111 = -40mV/µs

B2_CNFG_D (0x23)

BIT	7	6	5	4	3	2	1	0
Field	VOUTREG2[7:0]							
Reset	OTP							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VOUTREG2	7:0	Buck 2 Output Voltage Control while DVS2 = 0. If no GPIO is assigned as a special-function DVS input for this buck, then DVS2 = 0 always. Valid codes between 0x00 and 0xD2 (inclusive). Writes above 0xD2 clamp to 0xD2.	**If RNG2 = 0 (low-range):** 5mV/LSB in a linear transfer function between 0x00 (0.25V) and 0xD2 (1.3V) **If RNG2 = 1 (high-range):** 20mV/LSB in a linear transfer function between 0x00 (1V) and 0xD2 (5.2V)

B2_CNFG_E (0x24)

BIT	7	6	5	4	3	2	1	0
Field	VOUTREGDVS2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VOUTREGDVS2	7:0	Buck 2 Output Voltage Control while DVS2 = 1. If no GPIO is assigned as a special-function DVS input for this buck, then DVS2 = 0 always and this register is a *don't care*. Valid codes between 0x00 and 0xD2 (inclusive). Writes above 0xD2 clamp to 0xD2.	**If RNG2 = 0 (low-range):** 5mV/LSB in a linear transfer function between 0x00 (0.25V) and 0xD2 (1.3V) **If RNG2 = 1 (high-range):** 20mV/LSB in a linear transfer function between 0x00 (1V) and 0xD2 (5.2V)

B3_CNFG_A (0x30)

BIT	7	6	5	4	3	2	1	0
Field	ILIM3[1:0]		MODE3[1:0]		BEN3[3:0]			
Reset	OTP		0b01		OTP			
Access Type	Write, Read		Write, Read		Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
ILIM3	7:6	Buck 3 Peak Inductor Current Limit Control. Sets $I_{PEAK-HS}$ for all buck 3 phases.	00 = 1.5A 01 = 2.25A 10 = 3.0A 11 = 4.5A
MODE3	5:4	Buck 3 Mode Control. Turbo SKIP is the recommended default setting. Use SKIP mode when loads are expected <10mA/phase. Use FPWM mode for the highest V_{OUT} accuracy and lowest ripple.	00 = SKIP Mode 01 = Turbo SKIP Mode 10-11 = Forced-PWM (FPWM) Mode
BEN3	3:0	Buck 3 Enable Control Hardware enable inputs (using GPIO) are a logical *OR* with the control output from this bitfield.	0000 = Disabled 0001 = Enabled 0010 = FPS Slot 1 0011 = FPS Slot 2 0100 = FPS Slot 3 0101 = FPS Slot 4 0110 = FPS Slot 5 0111 = FPS Slot 6 1000 = FPS Slot 7 1001 = FPS Slot 8 1010 = FPS Slot 9 1011 = FPS Slot 10 1100 = FPS Slot 11 1101 = FPS Slot 12 1110-1111 = FPS Slot 12

B3_CNFG_B (0x31)

BIT	7	6	5	4	3	2	1	0
Field	BPOK3_IM	ADEN3	SPECTMOD3[1:0]		FSREN3	SFTUPDN3[2:0]		
Reset	0b1	0b1	0b00		0b1	OTP		
Access Type	Write, Read	Write, Read	Write, Read		Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
BPOK3_IM	7	Buck 3 POK Interrupt Mask	0 = Unmasked. The buck power-OK interrupt (BPOK_I) asserts when buck 3 is enabled and BPOK3 changes from 1 to 0. 1 = Masked. The buck power-OK interrupt (BPOK_I) does not assert due to buck 3.
ADEN3	6	Buck 3 Active Discharge Resistor Enable	0 = Disabled 1 = Enabled
SPECTMOD3	5:4	Buck 3 Pseudo-Random Spread-Spectrum Modulation Profile. Sets the modulation frequency (F_{SSMOD}) and envelope. Buck 3 F_{SSMOD} is by further modified by a multiplication factor set by FSSMOD_MUL3[1:0].	00 = Disabled (no spread-spectrum) 01 = Profile 1 (3kHz, ±8% envelope) 10 = Profile 2 (5kHz, ±8% envelope) 11 = Profile 3 (7kHz, ±8% envelope)
FSREN3	3	Buck 3 Falling Slew Rate Enable	0 = Strictly follows MODE3[1:0] at all times. 1 = Automatically enters forced-PWM mode for DVS and soft-stop events.
SFTUPDN3	2:0	Buck 3 Soft Start/Stop Ramp Rate Control. V_{OUT3} increases/decreases with this slope whenever the buck is enabled or disabled.	000 = ±0.15mV/µs 001 = ±0.625mV/µs 010 = ±1.25mV/µs 011 = ±2.5mV/µs 100 = ±5mV/µs 101 = ±10mV/µs 110 = ±20mV/µs 111 = ±40mV/µs

B3_CNFG_C (0x32)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RNG3	DVSRISE3[2:0]			DVSFALL3[2:0]		
Reset	0b0	OTP	0b000			0b000		
Access Type	Write, Read	Write, Read	Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	Reserved. Bit is a *don't care*.	N/A
RNG3	6	Buck 3 Output Voltage Range Control. Sets the output voltage range of VOUTREG3[7:0] and VOUTREGDVS3[1:0].	0 = (Low-range) 0.25V to 1.3V in 5mV steps 1 = (High-range) 1V to 5.2V in 20mV steps
DVSRISE3	5:3	Buck 3 DVS Rising Ramp Rate Control. V_{OUT3} increases with this slope whenever the output voltage is modified while the buck is enabled.	000 = +0.15mV/µs 001 = +0.625mV/µs 010 = +1.25mV/µs 011 = +2.5mV/µs 100 = +5mV/µs 101 = +10mV/µs 110 = +20mV/µs 111 = +40mV/µs
DVSFALL3	2:0	Buck 3 DVS Falling Ramp Rate Control. V_{OUT3} decreases with this slope whenever the output voltage is modified while the buck is enabled.	000 = -0.15mV/µs 001 = -0.625mV/µs 010 = -1.25mV/µs 011 = -2.5mV/µs 100 = -5mV/µs 101 = -10mV/µs 110 = -20mV/µs 111 = -40mV/µs

B3_CNFG_D (0x33)

BIT	7	6	5	4	3	2	1	0
Field	VOUTREG3[7:0]							
Reset	OTP							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VOUTREG3	7:0	Buck 3 Output Voltage Control while DVS3 = 0. If no GPIO is assigned as a special-function DVS input for this buck, then DVS3 = 0 always. Valid codes between 0x00 and 0xD2 (inclusive). Writes above 0xD2 clamp to 0xD2.	**If RNG3 = 0 (low-range):** 5mV/LSB in a linear transfer function between 0x00 (0.25V) and 0xD2 (1.3V) **If RNG3 = 1 (high-range):** 20mV/LSB in a linear transfer function between 0x00 (1V) and 0xD2 (5.2V)

B3_CNFG_E (0x34)

BIT	7	6	5	4	3	2	1	0
Field	VOUTREGDVS3[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VOUTREGDVS3	7:0	Buck 3 Output Voltage Control while DVS3 = 1. If no GPIO is assigned as a special-function DVS input for this buck, then DVS3 = 0 always and this register is a *don't care*. Valid codes between 0x00 and 0xD2 (inclusive). Writes above 0xD2 clamp to 0xD2.	**If RNG3 = 0 (low-range):** 5mV/LSB in a linear transfer function between 0x00 (0.25V) and 0xD2 (1.3V) **If RNG3 = 1 (high-range):** 20mV/LSB in a linear transfer function between 0x00 (1V) and 0xD2 (5.2V)

B4_CNFG_A (0x40)

BIT	7	6	5	4	3	2	1	0
Field	ILIM4[1:0]		MODE4[1:0]		BEN4[3:0]			
Reset	OTP		0b01		OTP			
Access Type	Write, Read		Write, Read		Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
ILIM4	7:6	Buck 4 Peak Inductor Current Limit Control. Sets $I_{PEAK-HS}$ for all buck 4 phases.	00 = 1.5A 01 = 2.25A 10 = 3.0A 11 = 4.5A

BITFIELD	BITS	DESCRIPTION	DECODE
MODE4	5:4	Buck 4 Mode Control. Turbo SKIP is the recommended default setting. Use SKIP mode when loads are expected <10mA/phase. Use FPWM mode for the highest V_{OUT} accuracy and lowest ripple.	00 = SKIP Mode 01 = Turbo SKIP Mode 10-11 = Forced-PWM (FPWM) Mode
BEN4	3:0	Buck 4 Enable Control Hardware enable inputs (using GPIO) are a logical *OR* with the control output from this bitfield.	0000 = Disabled 0001 = Enabled 0010 = FPS Slot 1 0011 = FPS Slot 2 0100 = FPS Slot 3 0101 = FPS Slot 4 0110 = FPS Slot 5 0111 = FPS Slot 6 1000 = FPS Slot 7 1001 = FPS Slot 8 1010 = FPS Slot 9 1011 = FPS Slot 10 1100 = FPS Slot 11 1101 = FPS Slot 12 1110-1111 = FPS Slot 12

B4_CNFG_B (0x41)

BIT	7	6	5	4	3	2	1	0
Field	BPOK4_IM	ADEN4	SPECTMOD4[1:0]		FSREN4	SFTUPDN4[2:0]		
Reset	0b1	0b1	0b00		0b1	OTP		
Access Type	Write, Read	Write, Read	Write, Read		Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
BPOK4_IM	7	Buck 4 POK Interrupt Mask	0 = Unmasked. The buck power-OK interrupt (BPOK_I) asserts when buck 4 is enabled and BPOK4 changes from 1 to 0. 1 = Masked. The buck power-OK interrupt (BPOK_I) does not assert due to buck 4.
ADEN4	6	Buck 4 Active Discharge Resistor Enable	0 = Disabled 1 = Enabled
SPECTMOD4	5:4	Buck 4 Pseudo-Random Spread-Spectrum Modulation Profile. Sets the modulation frequency (F_{SSMOD}) and envelope. Buck 4 F_{SSMOD} is by further modified by a multiplication factor set by FSSMOD_MUL4[1:0].	00 = Disabled (no spread-spectrum) 01 = Profile 1 (3kHz, ±8% envelope) 10 = Profile 2 (5kHz, ±8% envelope) 11 = Profile 3 (7kHz, ±8% envelope)
FSREN4	3	Buck 4 Falling Slew Rate Enable	0 = Strictly follows MODE4[1:0] at all times. 1 = Automatically enters forced-PWM mode for DVS and soft-stop events.
SFTUPDN4	2:0	Buck 4 Soft Start/Stop Ramp Rate Control. V_{OUT4} increases/decreases with this slope whenever the buck is enabled or disabled.	000 = ±0.15mV/µs 001 = ±0.625mV/µs 010 = ±1.25mV/µs 011 = ±2.5mV/µs 100 = ±5mV/µs 101 = ±10mV/µs 110 = ±20mV/µs 111 = ±40mV/µs

B4_CNFG_C (0x42)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RNG4	DVSRISE4[2:0]			DVSFALL4[2:0]		
Reset	0b0	OTP	0b000			0b000		
Access Type	Write, Read	Write, Read	Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	Reserved. Bit is a *don't care*.	N/A
RNG4	6	Buck 4 Output Voltage Range Control. Sets the output voltage range of VOUTREG4[7:0] and VOUTREGDVS4[1:0].	0 = (Low-range) 0.25V to 1.3V in 5mV steps 1 = (High-range) 1V to 5.2V in 20mV steps
DVSRISE4	5:3	Buck 4 DVS Rising Ramp Rate Control. V_{OUT4} increases with this slope whenever the output voltage is modified while the buck is enabled.	000 = +0.15mV/µs 001 = +0.625mV/µs 010 = +1.25mV/µs 011 = +2.5mV/µs 100 = +5mV/µs 101 = +10mV/µs 110 = +20mV/µs 111 = +40mV/µs
DVSFALL4	2:0	Buck 4 DVS Falling Ramp Rate Control. V_{OUT4} decreases with this slope whenever the output voltage is modified while the buck is enabled.	000 = -0.15mV/µs 001 = -0.625mV/µs 010 = -1.25mV/µs 011 = -2.5mV/µs 100 = -5mV/µs 101 = -10mV/µs 110 = -20mV/µs 111 = -40mV/µs

B4_CNFG_D (0x43)

BIT	7	6	5	4	3	2	1	0
Field	VOUTREG4[7:0]							
Reset	OTP							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VOUTREG4	7:0	Buck 4 Output Voltage Control while DVS4 = 0. If no GPIO is assigned as a special-function DVS input for this buck, then DVS4 = 0 always. Valid codes between 0x00 and 0xD2 (inclusive). Writes above 0xD2 clamp to 0xD2.	**If RNG4 = 0 (low-range):** 5mV/LSB in a linear transfer function between 0x00 (0.25V) and 0xD2 (1.3V) **If RNG4 = 1 (high-range):** 20mV/LSB in a linear transfer function between 0x00 (1V) and 0xD2 (5.2V)

B4_CNFG_E (0x44)

BIT	7	6	5	4	3	2	1	0
Field	VOUTREGDVS4[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VOUTREGDVS4	7:0	Buck 4 Output Voltage Control while DVS3 = 1. If no GPIO is assigned as a special-function DVS input for this buck, then DVS4 = 0 always and this register is a *don't care*. Valid codes between 0x00 and 0xD2 (inclusive). Writes above 0xD2 clamp to 0xD2.	**If RNG4 = 0 (low-range):** 5mV/LSB in a linear transfer function between 0x00 (0.25V) and 0xD2 (1.3V) **If RNG4 = 1 (high-range):** 20mV/LSB in a linear transfer function between 0x00 (1V) and 0xD2 (5.2V)

LDO_CNFG_A (0x50)

BIT	7	6	5	4	3	2	1	0
Field	OV_CLMP_EN	RSVD	LDOPOK_IM	ADE_LDO	LDOEN[3:0]			
Reset	0b1	0b1	0b1	0b1	OTP			
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
OV_CLMP_EN	7	Overvoltage Clamp Enable. Enables the LDO current sink function.	0 = Overvoltage clamp disabled. The LDO output can not sink current in the event that the output is over-regulated. 1 = Clamp enabled. The LDO output can sink current when the output is over-regulated.
RSVD	6	Reserved. Bit is a *don't care*.	N/A
LDOPOK_IM	5	LDOPOK_I Interrupt Mask	0 = Unmasked. The LDO power-OK interrupt (LDOPOK_I) asserts when LDOPOK changes. 1 = Masked. The buck power-OK interrupt (LDOPOK_I) does not assert when LDOPOK changes.
ADE_LDO	4	LDO Active Discharge Resistor Enable	0 = Disabled 1 = Enabled

BITFIELD	BITS	DESCRIPTION	DECODE
LDOEN	3:0	LDO Enable and Mode Control. Use only with MAX77711. Do not modify this bitfield in the MAX77511.	0000 = Disabled 0001 = Enabled 0010 = FPS Slot 1 0011 = FPS Slot 2 0100 = FPS Slot 3 0101 = FPS Slot 4 0110 = FPS Slot 5 0111 = FPS Slot 6 1000 = FPS Slot 7 1001 = FPS Slot 8 1010 = FPS Slot 9 1011 = FPS Slot 10 1100 = FPS Slot 11 1101 = FPS Slot 12 1110-1111 = FPS Slot 12

LDO_CNFG_B (0x51)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	LDO_VREG[5:0]					
Reset	0b0	0b0	OTP					
Access Type	Write, Read	Write, Read	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	Reserved. Bit is a *don't care*.	N/A
RSVD	6	Reserved. Bit is a *don't care*.	N/A
LDO_VREG	5:0	LDO Target Regulation Voltage (VLDO-REG). This 6-bit configuration is a linear transfer function that starts at 0.4V and ends at 1.975V in 25mV increments.	0x00 = 0.400V 0x01 = 0.425V 0x02 = 0.450V ... 0x30 = 1.600V ... 0x38 = 1.800V ... 0x3D = 1.925V 0x3E = 1.950V 0x3F = 1.975V

GPIO_INT (0x60)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	INT6	INT5	INT4	INT3	INT2	INT1
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read Clears All	Write, Read Clears All	Write, Read Clears All	Write, Read Clears All	Write, Read Clears All	Write, Read Clears All	Write, Read Clears All	Write, Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	Reserved. Bit is a *don't care*.	N/A
RSVD	6	Reserved. Bit is a *don't care*.	N/A
INT6	5	GPIO5 Interrupt Status.	0 = No edge detected since last read 1 = New edge detected since last read

BITFIELD	BITS	DESCRIPTION	DECODE
INT5	4	GPIO5 Interrupt Status.	0 = No edge detected since last read 1 = New edge detected since last read
INT4	3	GPIO4 Interrupt Status.	0 = No edge detected since last read 1 = New edge detected since last read
INT3	2	GPIO3 Interrupt Status.	0 = No edge detected since last read 1 = New edge detected since last read
INT2	1	GPIO2 Interrupt Status.	0 = No edge detected since last read 1 = New edge detected since last read
INT1	0	GPIO1 Interrupt Status.	0 = No edge detected since last read 1 = New edge detected since last read

GPIO_PULLUP (0x61)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	PU6	PU5	PU4	PU3	PU2	PU1
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	Reserved. Bit is a *don't care*.	N/A
RSVD	6	Reserved. Bit is a *don't care*.	N/A
PU6	5	GPIO5 Pullup Resistor Enable	0 = Pullup resistor disabled 1 = Pullup resistor to V_{IO}
PU5	4	GPIO5 Pullup Resistor Enable	0 = Pullup resistor disabled 1 = Pullup resistor to V_{IO}
PU4	3	GPIO4 Pullup Resistor Enable	0 = Pullup resistor disabled 1 = Pullup resistor to V_{IO}
PU3	2	GPIO3 Pullup Resistor Enable	0 = Pullup resistor disabled 1 = Pullup resistor to V_{IO}
PU2	1	GPIO2 Pullup Resistor Enable	0 = Pullup resistor disabled 1 = Pullup resistor to V_{IO}
PU1	0	GPIO1 Pullup Resistor Enable	0 = Pullup resistor disabled 1 = Pullup resistor to V_{IO}

GPIO_PULLDN (0x62)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	PD6	PD5	PD4	PD3	PD2	PD1
Reset	0b0	0b0	OTP	OTP	OTP	OTP	OTP	OTP
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	Reserved. Bit is a *don't care*.	N/A
RSVD	6	Reserved. Bit is a *don't care*.	N/A
PD6	5	GPIO6 Pulldown Resistor Enable	0 = Pulldown resistor disabled 1 = Pulldown resistor to AGND

BITFIELD	BITS	DESCRIPTION	DECODE
PD5	4	GPIO5 Pulldown Resistor Enable	0 = Pulldown resistor disabled 1 = Pulldown resistor to AGND
PD4	3	GPIO4 Pulldown Resistor Enable	0 = Pulldown resistor disabled 1 = Pulldown resistor to AGND
PD3	2	GPIO3 Pulldown Resistor Enable	0 = Pulldown resistor disabled 1 = Pulldown resistor to AGND
PD2	1	GPIO2 Pulldown Resistor Enable	0 = Pulldown resistor disabled 1 = Pulldown resistor to AGND
PD1	0	GPIO1 Pulldown Resistor Enable	0 = Pulldown resistor disabled 1 = Pulldown resistor to AGND

GPIO_CNFG1 (0x64)

BIT	7	6	5	4	3	2	1	0
Field	IRQ_SEL1[1:0]		DBNC_SEL1[1:0]		DATA1	DIR1[1:0]		DRV1
Reset	0b00		0b00		0b0	OTP		OTP
Access Type	Write, Read		Write, Read		Write, Read	Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
IRQ_SEL1	7:6	GPIO1 Interrupt Configuration. Programs the condition for INT1 to go high. Interrupts only occur when GPIO1 is configured as an input (DIR1[1:0] = 0b10/0b11).	00 = No interrupt 01 = Interrupt on falling edge detection 10 = Interrupt on rising edge detection 11 = Interrupt on any edge detection
DBNC_SEL1	5:4	GPIO1 Debounce Configuration. Sets t_{DB-GPI}.	00 = No debounce 01 = 0.11ms debounce 10 = 0.24ms debounce 11 = 0.5ms debounce
DATA1	3	GPIO1 Data Value. Reads back 0.	0 = Output logic-low 1 = Output logic-high
DIR1	2:1	GPIO1 Direction Configuration	00 = Digital Output. Driven by DATA1. 01 = Digital Output. Function determined by FUNC1[2:0]. 10-11 = Digital Input. Function determined by FUNC1[2:0].
DRV1	0	GPIO1 Output Driver Selection	0 = Open-drain 1 = Push-pull

GPIO_CNFG2 (0x65)

BIT	7	6	5	4	3	2	1	0
Field	IRQ_SEL2[1:0]		DBNC_SEL2[1:0]		DATA2	DIR2[1:0]		DRV2
Reset	0b00		0b00		0b0	OTP		OTP
Access Type	Write, Read		Write, Read		Write, Read	Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
IRQ_SEL2	7:6	GPIO2 Interrupt Configuration. Programs the condition for INT2 to go high. Interrupts only occur when GPIO2 is configured as an input (DIR2[1:0] = 0b10/0b11).	00 = No interrupt 01 = Interrupt on falling edge detection 10 = Interrupt on rising edge detection 11 = Interrupt on any edge detection

BITFIELD	BITS	DESCRIPTION	DECODE
DBNC_SEL2	5:4	GPIO2 Debounce Configuration. Sets t_{DB-GPI}.	00 = No debounce 01 = 0.11ms debounce 10 = 0.24ms debounce 11 = 0.5ms debounce
DATA2	3	GPIO2 Data Value. Reads back 0.	0 = Output logic-low 1 = Output logic-high
DIR2	2:1	GPIO2 Direction Configuration	00 = Digital Output. Driven by DATA2. 01 = Digital Output. Function determined by FUNC2[2:0]. 10-11 = Digital Input. Function determined by FUNC2[2:0].
DRV2	0	GPIO2 Output Driver Selection	0 = Open-drain 1 = Push-pull

GPIO_CNFG3 (0x66)

BIT	7	6	5	4	3	2	1	0
Field	IRQ_SEL3[1:0]		DBNC_SEL3[1:0]		DATA3	DIR3[1:0]		DRV3
Reset	0b00		0b00		0b0	OTP		OTP
Access Type	Write, Read		Write, Read		Write, Read	Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
IRQ_SEL3	7:6	GPIO3 Interrupt Configuration. Programs the condition for INT3 to go high. Interrupts only occur when GPIO3 is configured as an input (DIR3[1:0] = 0b10/0b11).	00 = No interrupt 01 = Interrupt on falling edge detection 10 = Interrupt on rising edge detection 11 = Interrupt on any edge detection
DBNC_SEL3	5:4	GPIO3 Debounce Configuration. Sets t_{DB-GPI}.	00 = No debounce 01 = 0.11ms debounce 10 = 0.24ms debounce 11 = 0.5ms debounce
DATA3	3	GPIO3 Data Value. Reads back 0.	0 = Output logic-low 1 = Output logic-high
DIR3	2:1	GPIO0 Direction Configuration	00 = Digital Output. Driven by DATA3. 01 = Digital Output. Function determined by FUNC3[2:0]. 10-11 = Digital Input. Function determined by FUNC3[2:0].
DRV3	0	GPIO3 Output Driver Selection	0 = Open-drain 1 = Push-pull

GPIO_CNFG4 (0x67)

BIT	7	6	5	4	3	2	1	0
Field	IRQ_SEL4[1:0]		DBNC_SEL4[1:0]		DATA4	DIR4[1:0]		DRV4
Reset	0b00		0b00		0b0	OTP		OTP
Access Type	Write, Read		Write, Read		Write, Read	Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
IRQ_SEL4	7:6	GPIO4 Interrupt Configuration. Programs the condition for INT4 to go high. Interrupts only occur when GPIO4 is configured as an input (DIR4[1:0] = 0b10/0b11).	00 = No interrupt 01 = Interrupt on falling edge detection 10 = Interrupt on rising edge detection 11 = Interrupt on any edge detection
DBNC_SEL4	5:4	GPIO4 Debounce Configuration. Sets t_{DB-GPI}.	00 = No debounce 01 = 0.11ms debounce 10 = 0.24ms debounce 11 = 0.5ms debounce
DATA4	3	GPIO4 Data Value. Reads back 0.	0 = Output logic-low 1 = Output logic-high
DIR4	2:1	GPIO0 Direction Configuration	00 = Digital Output. Driven by DATA4. 01 = Digital Output. Function determined by FUNC4[2:0]. 10-11 = Digital Input. Function determined by FUNC4[2:0].
DRV4	0	GPIO4 Output Driver Selection	0 = Open-drain 1 = Push-pull

GPIO_CNFG5 (0x68)

BIT	7	6	5	4	3	2	1	0
Field	IRQ_SEL5[1:0]		DBNC_SEL5[1:0]		DATA5	DIR5[1:0]		DRV5
Reset	0b00		0b00		0b0	OTP		OTP
Access Type	Write, Read		Write, Read		Write, Read	Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
IRQ_SEL5	7:6	GPIO5 Interrupt Configuration. Programs the condition for INT5 to go high. Interrupts only occur when GPIO5 is configured as an input (DIR5[1:0] = 0b10/0b11).	00 = No interrupt 01 = Interrupt on falling edge detection 10 = Interrupt on rising edge detection 11 = Interrupt on any edge detection
DBNC_SEL5	5:4	GPIO5 Debounce Configuration. Sets t_{DB-GPI}.	00 = No debounce 01 = 0.11ms debounce 10 = 0.24ms debounce 11 = 0.5ms debounce
DATA5	3	GPIO5 Data Value. Reads back 0.	0 = Output logic-low 1 = Output logic-high
DIR5	2:1	GPIO5 Direction Configuration	00 = Digital Output. Driven by DATA5. 01 = Digital Output. Function determined by FUNC5[2:0]. 10-11 = Digital Input. Function determined by FUNC5[2:0].
DRV5	0	GPIO5 Output Driver Selection	0 = Open-drain 1 = Push-pull

GPIO_CNFG6 (0x69)

BIT	7	6	5	4	3	2	1	0
Field	IRQ_SEL6[1:0]		DBNC_SEL6[1:0]		DATA6	DIR6[1:0]		DRV6
Reset	0b00		0b00		0b0	OTP		OTP
Access Type	Write, Read		Write, Read		Write, Read	Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
IRQ_SEL6	7:6	GPIO6 Interrupt Configuration. Programs the condition for INT6 to go high. Interrupts only occur when GPIO6 is configured as an input (DIR6[1:0] = 0b10/0b11).	00 = No interrupt 01 = Interrupt on falling edge detection 10 = Interrupt on rising edge detection 11 = Interrupt on any edge detection
DBNC_SEL6	5:4	GPIO6 Debounce Configuration. Sets t_{DB-GPI}.	00 = No debounce 01 = 0.11ms debounce 10 = 0.24ms debounce 11 = 0.5ms debounce
DATA6	3	GPIO6 Data Value. Reads back 0.	0 = Output logic-low 1 = Output logic-high
DIR6	2:1	GPIO6 Direction Configuration	00 = Digital Output. Driven by DATA6. 01 = Digital Output. Function determined by FUNC6[2:0]. 10-11 = Digital Input. Function determined by FUNC6[2:0].
DRV6	0	GPIO6 Output Driver Selection	0 = Open-drain 1 = Push-pull

GPIO_FUNC1 (0x6A)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	BSEL1[1:0]		FUNC1[2:0]		
Reset	0b0	0b0	0b0	OTP		OTP		
Access Type	Write, Read	Write, Read	Write, Read	Write, Read		Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	Reserved. Bit is a *don't care*.	N/A
RSVD	6	Reserved. Bit is a *don't care*.	N/A
RSVD	5	Reserved. Bit is a *don't care*.	N/A
BSEL1	4:3	GPIO1 Buck Control Regulator Selection. This bitfield is a *don't care* if a buck control function is not selected.	00 = Buck 1 01 = Buck 2 10 = Buck 3 11 = Buck 4
FUNC1	2:0	GPIO1 Function Control. Buck control functions work on the buck regulator specified by BSEL1[1:0].	**When DIR1[1:0] = 0b00:** 000-111 = GPIO1 drives the output in DATA1. This bitfield is a *don't care*. **When DIR1[1:0] = 0b01:** 000-100 = GPIO1 drives logic-low 101 = Buck Power-OK Output (POKx) 110-111 = GPIO4 drives logic-low **When DIR1[1:0] = 0b10 or 0b11:** 000 = General-Purpose Input (GPI). No other special function. 001 = Buck Enable Input (BENx) 010 = Buck DVS Input (DVSx) 011 = Buck FPWM Input (FPWMx) 100 = LDO Enable Input (LDOEN) 101-111 = No Function. GPIO1 input is a *don't care*.

GPIO_FUNC2 (0x6B)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	BSEL2[1:0]		FUNC2[2:0]		
Reset	0b0	0b0	0b0	OTP		OTP		
Access Type	Write, Read	Write, Read	Write, Read	Write, Read		Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	Reserved. Bit is a *don't care*.	N/A
RSVD	6	Reserved. Bit is a *don't care*.	N/A
RSVD	5	Reserved. Bit is a *don't care*.	N/A
BSEL2	4:3	GPIO2 Buck Control Regulator Selection. This bitfield is a *don't care* if a buck control function is not selected.	00 = Buck 1 01 = Buck 2 10 = Buck 3 11 = Buck 4
FUNC2	2:0	GPIO2 Function Control. Buck control functions work on the buck regulator specified by BSEL2[1:0].	**When DIR2[1:0] = 0b00:** 000-111 = GPIO2 drives the output in DATA2. This bitfield is a *don't care*. **When DIR2[1:0] = 0b01:** 000-100 = GPIO2 drives logic-low 101 = Buck Power-OK Output (POKx) 110-111 = GPIO4 drives logic-low **When DIR2[1:0] = 0b10 or 0b11:** 000 = General-Purpose Input (GPI). No other special function. 001 = Buck Enable Input (BENx) 010 = Buck DVS Input (DVSx) 011 = Buck FPWM Input (FPWMx) 100 = LDO Enable Input (LDOEN) 101-111 = No Function. GPIO2 input is a *don't care*.

GPIO_FUNC3 (0x6C)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	BSEL3[1:0]		FUNC3[2:0]		
Reset	0b0	0b0	0b0	OTP		OTP		
Access Type	Write, Read	Write, Read	Write, Read	Write, Read		Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	Reserved. Bit is a *don't care*.	N/A
RSVD	6	Reserved. Bit is a *don't care*.	N/A
RSVD	5	Reserved. Bit is a *don't care*.	N/A
BSEL3	4:3	GPIO3 Buck Control Regulator Selection. This bitfield is a *don't care* if a buck control function is not selected.	00 = Buck 1 01 = Buck 2 10 = Buck 3 11 = Buck 4

BITFIELD	BITS	DESCRIPTION	DECODE
FUNC3	2:0	GPIO3 Function Control. Buck control functions work on the buck regulator specified by BSEL3[1:0].	**When DIR3[1:0] = 0b00:** 000-111 = GPIO3 drives the output in DATA3. This bitfield is a *don't care*. **When DIR3[1:0] = 0b01:** 000-100 = GPIO3 drives logic-low 101 = Buck Power-OK Output (POKx) 110-111 = GPIO4 drives logic-low **When DIR3[1:0] = 0b10 or 0b11:** 000 = General-Purpose Input (GPI). No other special function. 001 = Buck Enable Input (BENx) 010 = Buck DVS Input (DVSx) 011 = Buck FPWM Input (FPWMx) 100 = LDO Enable Input (LDOEN) 101-111 = No Function. GPIO3 input is a *don't care*.

GPIO_FUNC4 (0x6D)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	BSEL4[1:0]		FUNC4[2:0]		
Reset	0b0	0b0	0b0	OTP		OTP		
Access Type	Write, Read	Write, Read	Write, Read	Write, Read		Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	Reserved. Bit is a *don't care*.	N/A
RSVD	6	Reserved. Bit is a *don't care*.	N/A
RSVD	5	Reserved. Bit is a *don't care*.	N/A
BSEL4	4:3	GPIO4 Buck Control Regulator Selection. This bitfield is a *don't care* if a buck control function is not selected.	00 = Buck 1 01 = Buck 2 10 = Buck 3 11 = Buck 4
FUNC4	2:0	GPIO4 Function Control. Buck control functions work on the buck regulator specified by BSEL4[1:0].	**When DIR4[1:0] = 0b00:** 000-111 = GPIO4 drives the output in DATA4. This bitfield is a *don't care*. **When DIR4[1:0] = 0b01:** 000-100 = GPIO4 drives logic-low 101 = Buck Power-OK Output (POKx) 110-111 = GPIO4 drives logic-low **When DIR4[1:0] = 0b10 or 0b11:** 000 = General-Purpose Input (GPI). No other special function. 001 = Buck Enable Input (BENx) 010 = Buck DVS Input (DVSx) 011 = Buck FPWM Input (FPWMx) 100 = LDO Enable Input (LDOEN) 101-111 = No Function. GPIO4 input is a *don't care*.

GPIO_FUNC5 (0x6E)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	BSEL5[1:0]		FUNC5[2:0]		
Reset	0b0	0b0	0b0	OTP		OTP		
Access Type	Write, Read	Write, Read	Write, Read	Write, Read		Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	Reserved. Bit is a *don't care*.	N/A
RSVD	6	Reserved. Bit is a *don't care*.	N/A
RSVD	5	Reserved. Bit is a *don't care*.	N/A
BSEL5	4:3	GPIO5 Buck Control Regulator Selection. This bitfield is a *don't care* if a buck control function is not selected.	00 = Buck 1 01 = Buck 2 10 = Buck 3 11 = Buck 4
FUNC5	2:0	GPIO5 Function Control. Buck control functions work on the buck regulator specified by BSEL5[1:0]. Flexible Power Sequencer Digital Output (FPSDO5) causes GPIO5 to go high in the seqeuencer slot specified by GPIOSEQ5[3:0].	**When DIR5[1:0] = 0b00:** 000-111 = GPIO5 drives the output in DATA5. This bitfield is a *don't care*. **When DIR5[1:0] = 0b01:** 000-100 = GPIO5 drives logic-low. 101 = Buck Power-OK Output (POKx) 110-111 = FPS Digital Output (FPSDO5) **When DIR5[1:0] = 0b10 or 0b11:** 000 = General-Purpose Input (GPI). No other special function. 001 = Buck Enable Input (BENx) 010 = Buck DVS Input (DVSx) 011 = Buck FPWM Input (FPWMx) 100 = LDO Enable Input (LDOEN) 101-111 = No Function. GPIO5 input is a *don't care*.

GPIO_FUNC6 (0x6F)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	BSEL6[1:0]		FUNC6[2:0]		
Reset	0b0	0b0	0b0	OTP		OTP		
Access Type	Write, Read	Write, Read	Write, Read	Write, Read		Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	Reserved. Bit is a *don't care*.	N/A
RSVD	6	Reserved. Bit is a *don't care*.	N/A
RSVD	5	Reserved. Bit is a *don't care*.	N/A
BSEL6	4:3	GPIO6 Buck Control Regulator Selection. This bitfield is a *don't care* if a buck control function is not selected.	00 = Buck 1 01 = Buck 2 10 = Buck 3 11 = Buck 4

BITFIELD	BITS	DESCRIPTION	DECODE
FUNC6	2:0	GPIO6 Function Control. Buck control functions work on the buck regulator specified by BSEL6[1:0]. Flexible Power Sequencer Digital Output (FPSDO6) causes GPIO6 to go high in the seqeuencer slot specified by GPIOSEQ6[3:0].	**When DIR6[1:0] = 0b00:** 000-111 = GPIO6 drives the output in DATA6. This bitfield is a *don't care*. **When DIR6[1:0] = 0b01:** 000-100 = GPIO6 drives logic-low. 101 = Buck Power-OK Output (POKx) 110-111 = FPS Digital Output (FPSDO6) **When DIR6[1:0] = 0b10 or 0b11:** 000 = General-Purpose Input (GPI). No other special function. 001 = Buck Enable Input (BENx) 010 = Buck DVS Input (DVSx) 011 = Buck FPWM Input (FPWMx) 100 = LDO Enable Input (LDOEN) 101-111 = No Function. GPIO6 input is a *don't care*.

GPIO_FPS (0x70)

BIT	7	6	5	4	3	2	1	0
Field	GPIOSEQ6[3:0]				GPIOSEQ5[3:0]			
Reset	OTP				OTP			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
GPIOSEQ6	7:4	GPIO6 Flexible Power Sequencer Slot Assignment	0000 = FPS Slot 1 0001 = FPS Slot 2 0010 = FPS Slot 3 0011 = FPS Slot 4 0100 = FPS Slot 5 0101 = FPS Slot 6 0110 = FPS Slot 7 0111 = FPS Slot 8 1000 = FPS Slot 9 1001 = FPS Slot 10 1010 = FPS Slot 11 1011 = FPS Slot 12 1100-1111 = FPS Slot 12
GPIOSEQ5	3:0	GPIO5 Flexible Power Sequencer Slot Assignment	0000 = FPS Slot 1 0001 = FPS Slot 2 0010 = FPS Slot 3 0011 = FPS Slot 4 0100 = FPS Slot 5 0101 = FPS Slot 6 0110 = FPS Slot 7 0111 = FPS Slot 8 1000 = FPS Slot 9 1001 = FPS Slot 10 1010 = FPS Slot 11 1011 = FPS Slot 12 1100-1111 = FPS Slot 12

Applications Information—Quad-Channel Configurable Buck Regulator

Buck Enable Options

The MAX77511/MAX77711 offer a high degree of control flexibility. See Figure 13 for suggested methods of controlling the buck regulators.

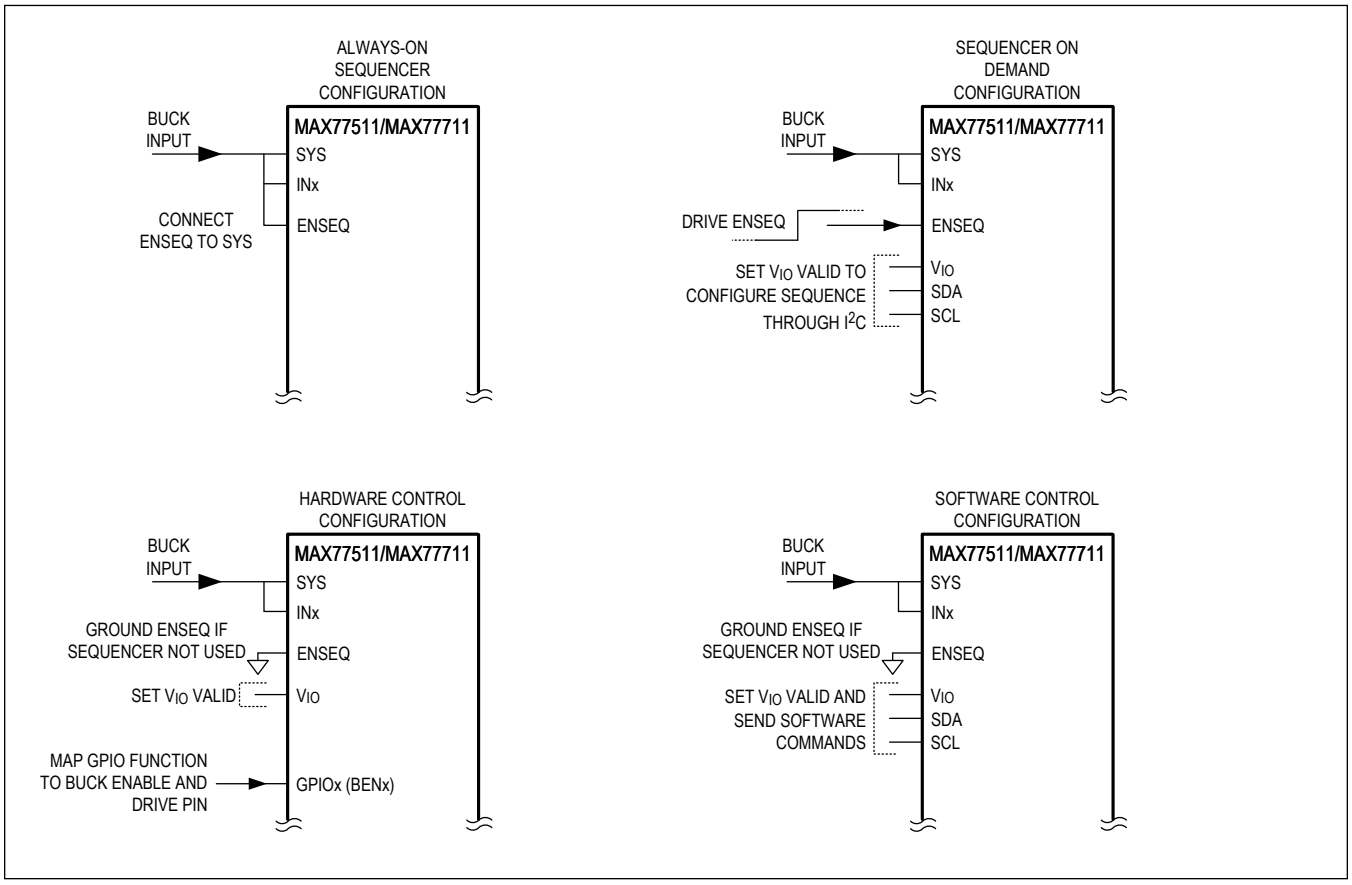


Figure 13. Buck Enable Options

Sequencer Control (Always-On)

Strap the ENSEQ pin to SYS to configure the IC in an *always-on* configuration. See Figure 13 (top left). The ICs built-in *Flexible Power Sequencer (FPS)* begins the power-up sequence whenever V_{SYS} is valid, FLT = 0, and nRSTIO = 1.

ENSEQ activates the factory-programmed (default) power-up sequence regardless of the validity of the V_{IO}. Ensure that registers remain in factory reset by connecting V_{IO} to ground on the PCB.

See Table 4 and Table 5 for the default sequence options corresponding to each MAX77511/MAX77711 part number.

Sequencer Control (On Demand)

Control the buck regulators using the built-in *Flexible Power Sequencer (FPS)*. See Figure 13 (top right). Configure the power-up sequence through I^2C and assert the ENSEQ pin logic-high to begin a sequenced startup. The buck regulators activate whenever FLT = 0, nRSTIO = 1, and V_{SYS} is valid. Always drive the ENSEQ pin to prevent chatter in the FPS state machine.

Hardware (GPIO) Control

Enable the buck regulators with hardware enable pins by mapping GPIOs to special buck control functions. See Figure 13 (bottom left). Program FUNCx[2:0] = 0b001 to set the corresponding GPIO as a buck enable input. Set the buck target (which buck the pin controls) using the corresponding BSELx[1:0] bitfield. See *GPIO Buck Control* for full details and an example. V_{IO} must be valid for the GPIOs to operate regardless of GPIO function map.

Software (I^2C) Control

Control the buck regulators using software commands sent over the I^2C serial interface. See Figure 13 (bottom right).

Assert V_{IO} valid and connect SDA and SCL to a serial host to enable the serial bus and full software control of the MAX77511/MAX77711. When using software, the serial host can do the following:

- Set the target output voltage, $V_{OUT-REGx}$.
- Set the DVS target output voltage, $V_{OUT-REG(DVS)x}$.
- Set the desired soft-start and soft-stop ramp rate ($\Delta V_{OUTx}/\Delta t$).
- Set the peak inductor current limit, $I_{PEAK-HSx}$.
- Enable the buck regulator directly using the BENx[3:0] bitfield.
- Configure the buck regulator's sequencer slot assignment using the BENx[3:0] bitfield.
- Change regulator mode (SKIP, Turbo SKIP, FPWM) dynamically.
- Control the active discharge resistor using the ADENx bit.
- Set DVS rise and DVS fall ramp rates ($\Delta V_{OUTx}/\Delta t$).
- Manage and clear faults (FLT) without external circuitry or system power cycling.
- Configure specialized GPIO function maps.
- Utilize spare GPIO to expand system I/O.
- Directly control the LDO (MAX77711 only).
- Selectively unmask important interrupt sources.

See the *I^2C Serial Interface* and *Register Map* sections for more information. Configuration registers reset if V_{IO} becomes invalid or if SYS falls below the POR threshold.

Input Capacitor Selection

Bypass each input pin with a 10µF nominal input capacitor (C_{INx}) that maintains 1µF or higher effective capacitance at its working voltage. Larger values improve decoupling of the buck regulator, but increase inrush current from the voltage supply when connected. C_{INx} reduces the current peaks drawn from the input power source during buck operation and reduces switching noise in the system. The ESR/ESL of C_{INx} and its series PCB trace should be very low (i.e., <15mΩ + <2nH) for frequencies up to 2MHz.

Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients. All ceramic capacitors derate with DC bias voltage (effective capacitance goes down as DC bias goes up). Generally, small case size capacitors derate heavily compared to larger case sizes (0603 case size performs better than 0402). Consider the effective capacitance value carefully by consulting the manufacturer's data sheet. Refer to *Tutorial 5527* for more information.

Output Capacitor Selection

Sufficient output capacitance (C_{OUT}) is required for stable operation of the buck. Choose the effective C_{OUT} to be 60µF per phase, minimum. (A single phase configuration requires 60µF, dual-phase requires 120µF, etc.)

Effective C_{OUT} is the actual capacitance value seen by the buck output during operation. Choose effective C_{OUT} carefully by considering the capacitor's initial tolerance, variation with temperature, and derating with DC bias. Refer to *Tutorial 5527* for more information.

Larger values of C_{OUT} (above the required effective minimum) improve load transient performance, but increase the input surge currents during soft-start and output voltage changes. The output filter capacitor must have low enough ESR to meet output ripple and load transient requirements. The output capacitance must be high enough to absorb the inductor energy while transitioning from full-load to no-load conditions. When using high-capacitance, low-ESR capacitors, the filter capacitor's ESR dominates the output voltage ripple in continuous conduction mode. Therefore, the size of the output capacitor depends on the maximum ESR required to meet the output voltage ripple ($V_{RIPPLE(P-P)}$) specifications:

$$V_{RIPPLE(P-P)} = ESR \times I_{LOAD} \times LIR$$

where LIR is the inductor's ripple current to average current ratio. Compute LIR with Equation 3.

Equation 3:

$$LIR = \frac{V_{OUT} \times \left(V_{IN} - V_{OUT}\right)}{V_{IN} \times F_{SW} x I_{LOAD} x L}$$

where I_{LOAD} is the buck's output current in the particular application (3A/phase max), V_{IN} is the application's input voltage, and F_{SW} is the switching frequency (1MHz nominal).

Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients. All ceramic capacitors derate with DC bias voltage (effective capacitance goes down as DC bias goes up). Generally, small case size capacitors derate heavily compared to larger case sizes (0603 case size performs better than 0402). Consider the effective capacitance value carefully by consulting the manufacturer's data sheet.

Inductor Selection

Choose an inductor with a saturation current that is greater than or equal to the maximum peak current limit setting ($I_{PEAK-HSx}$). Inductors with lower saturation current and higher DCR ratings tend to be physically small. Higher values of DCR reduce buck efficiency. Choose the RMS current rating of the inductor (the current at which temperature rises appreciably) based on the system's expected load current per phase.

Choose an inductor value based on the range bit (RNGx).

- RNG = 0 requires 0.47µH
- RNG = 1 requires 1.5µH

See Table 8 for additional information.

One inductor is required per phase. Do not short different LX nets together on the PCB. Do not use a single inductor on a 2Φ configuration and short LX1 to LX2, etc.

Use the same inductor value for all phases under a single buck's control. For example, if buck 1 is configured in a 3Φ, RNG = 0 configuration, then use 0.47µH for all inductors under buck 1 control (LX1, LX2, and LX3). See Table 7 and the *Typical Application Circuits* section of the data sheet for more information regarding different phase configurations.

Unused Bucks

Follow these guidelines when the application has unused buck converters:

- Connect unused inputs (INx) to SYS.
- Leave unused LXx and BSTx pins unconnected (open).
- Connect unused SNSx+ and SNSx- feedback inputs to ground.
- Connect PGNDx pins to ground on the PCB.

Do not confuse unused bucks with unused phases. Phases configured under a master controller must connect according to Table 7. Refer to the *Typical Application Circuits* section of the data sheet for more information about how phases connect together in different IC configurations.

Do not enable unused bucks. If an unused buck (following the guidelines above) enables, then a fault state latches (FLT = 1). Clear the fault state by disabling the buck according to Figure 10.

If using a version of the device that has an unused buck assigned to the flexible power sequencer (FPS) by default, choose one of the following options to prevent fault latching:

1. Do not use the FPS. (Follow the pin guidelines above and strap ENSEQ = 0 on the PCB.) Use software or GPIO special functions to enable the regulators.
2. Populate the buck's external components. (Treat the unused buck as a utilized buck.) Disable the buck through software after the power-up sequence completes to achieve quiescent power savings.

PCB Layout Guidelines

Careful circuit board layout is critical to achieve low switching power losses and clean, stable operation. Figure 14 shows an example PCB layout for the 1Φ+1Φ+1Φ+1Φ configuration of the MAX77711.

Follow these guidelines when designing the PCB:

1. Place the inductors next to their corresponding LX bumps (as close as possible) to minimize PCB trace impedance. Excessive PCB impedance reduces converter efficiency.
2. Make the trace between the LX bumps and their corresponding inductor short and wide. Do not take up an excessive amount of area. The voltage on this node switches very quickly and additional area creates more radiated emissions.
3. Place the IN capacitors (C_{IN}) as close to the IC as possible, typically next to their corresponding inductors. Use at least one input capacitor per switching phase. Connect the negative terminal of C_{IN} as close as possible to the negative terminal of C_{OUT} with a low-impedance high-priority path to the corresponding PGNDx bumps. This practice minimizes the switching current path length (i.e., the *hot loop* length).
4. The routing between LX and its corresponding BST capacitor should be as short as possible. Prioritize BST capacitor (C_{BST}) placement to reduce trace length to the IC.
5. Connect each phase's corresponding PGND to the low-impedance ground plane on the PCB as close to the IC as possible. Do not create ground islands (PGND islands risk interrupting the hot loops).
6. Prioritize the low-impedance ground plane of the PCB directly underneath the IC, C_{OUT}, C_{IN}, and inductor. Cutting this ground plane risks interrupting the switching current hot loops.
7. Place each phase's corresponding output capacitor (C_{OUT}) as close to the IC as possible. Minimize the switching current hot loop by placing the negative terminal of C_{IN} as close as possible to the negative terminal of the corresponding C_{OUT}.
8. Connect the negative terminal of the V_{DD} bypass capacitor (C_{VDD}) to AGND. Connect the negative terminal of the V_{L13}/V_{L24} bypass capacitors (C_{VL13}/C_{VL24}) to PGND.
9. AGND must carefully connect to PGND on the PCBs low-impedance ground plane. Kelvin connect AGND to the low-impedance ground plane on the PCB (the same net as PGND) at least 3 millimeters away from the ICs edge. See Figure 15 for an illustration.
10. The IC requires a quiet supply input (SYS) which is often the same net as INx. Carefully bypass SYS to AGND with a dedicated capacitor (C_{SYS}). Route a dedicated trace between C_{SYS} and the SYS bump. Avoid connecting SYS directly to the nearest IN bumps without dedicated bypassing. See Figure 16 for an illustration.
11. The value of C_{INLDO} should be larger than C_{LDO}. If C_{LDO} = 4.7µF, choose C_{INLDO} = 10µF or greater (MAX77711 only).
12. For the MAX77511, connect LDO and INLDO to ground. The LDO is unavailable for use for MAX77511.
13. Do not neglect ceramic capacitor DC voltage derating. Choose capacitor values and case sizes carefully. See the *Output Capacitor Selection* section and refer to *Tutorial 5527* for more information.

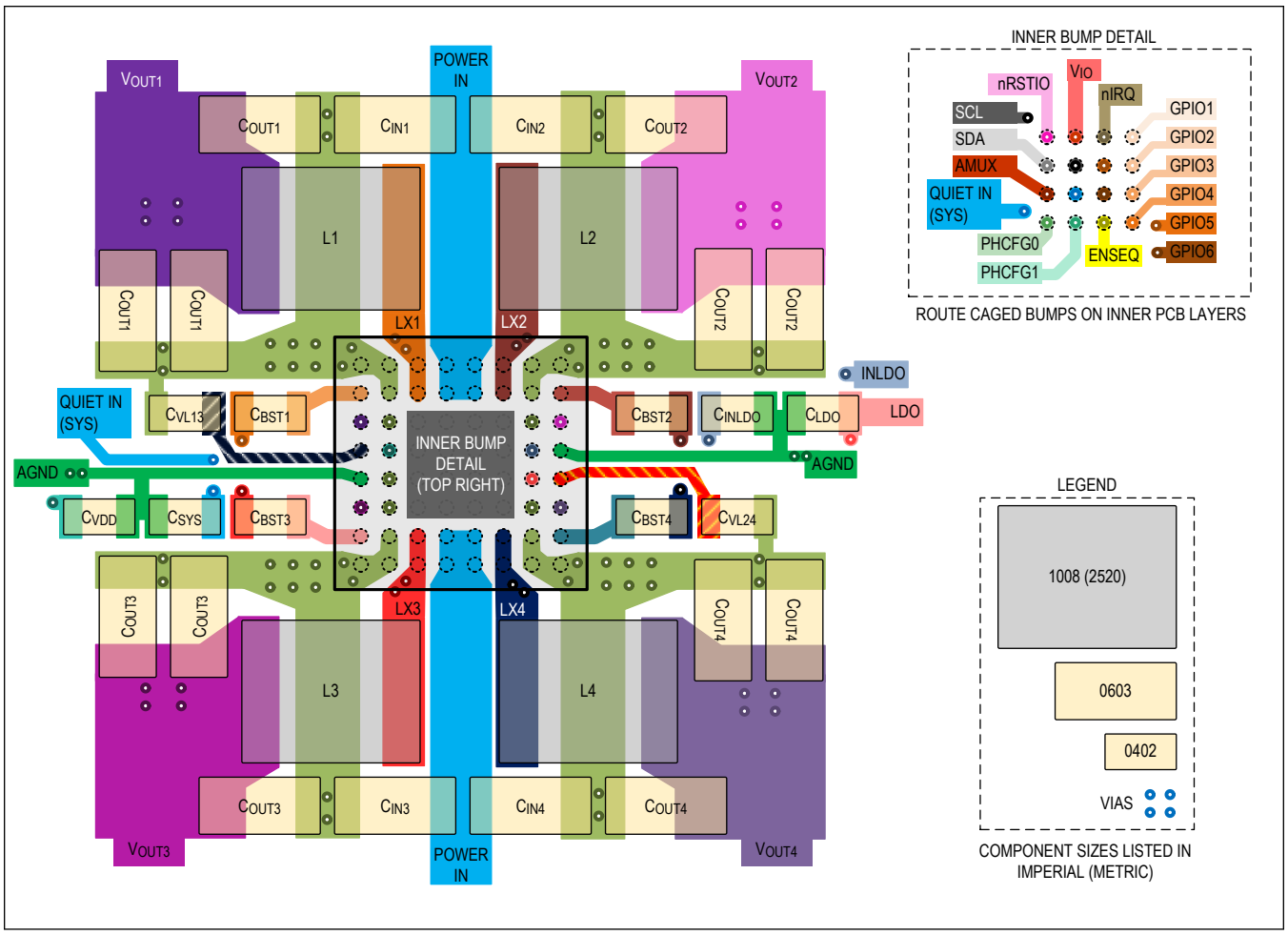


Figure 14. PCB Layout Example

LAYOUT NOTES
(ONLY TOP METAL GROUND NET DRAWN)

N1: USE THE SAME NET FOR AGND AND PGND. (THEY MUST CONNECT TOGETHER ON THE PCB.)

N2: CONNECT PGND TO PCB INNER GROUND LAYER CLOSE TO THE IC.

N3: KELVIN CONNECT AGND TO PCB INNER GROUND LAYER AT LEAST 3mm AWAY FROM IC EDGE AND AWAY FROM OTHER PGND CONNECTIONS.

N4: CONNECT V_{L13}/V_{L24} BYPASS CAPACITOR NEGATIVE TERMINAL TO PGND.

N5: CONNECT V_{DD} AND SYS BYPASS CAPACITOR NEGATIVE TERMINAL TO AGND.

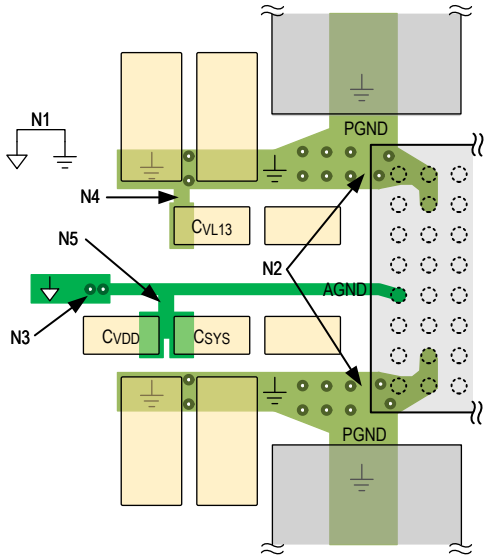


Figure 15. Recommended Ground Connection

LAYOUT NOTES
(ONLY SUPPLY INPUT NET DRAWN)

N1: ROUTE QUIET IN (SYS) SEPARATELY FROM POWER IN (EVEN IF THEY ARE THE SAME NET).

N2: DECOUPLE SYS WITH A DEDICATED CAPACITOR (C_{SYS}).

N3: ROUTE ON INNER SIGNAL LAYERS AS REQUIRED.

N4: ROUTE A DEDICATED TRACE BETWEEN C_{SYS} AND THE SYS BUMP (APART FROM POWER IN).

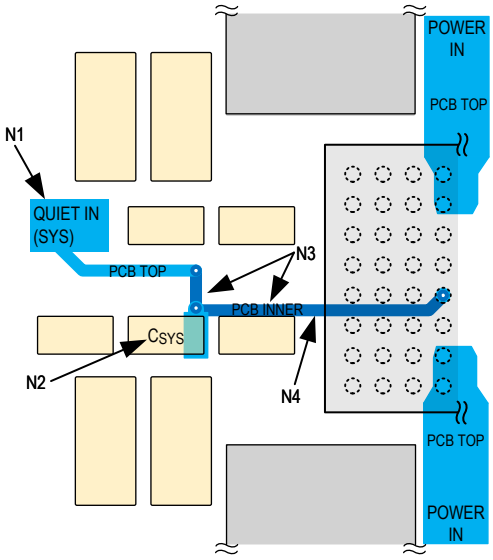


Figure 16. Recommended SYS Connection

Advanced User Information

The following sections outline advanced user information for the buck converter. Contact the factory for additional information.

Transient Performance Option

Internal options allow the MAX77511/MAX77711 to improve SKIP and Turbo SKIP mode transient response. See Table 4 and Table 5 to find if the *transient performance option* is enabled for each MAX77511/MAX77711 part number.

Figure 17 details the effect of the *transient performance option* under a load transient while the buck is in Turbo SKIP mode. The *transient performance option*:

- Reduces undershoot upon load attack.
- Has no effect upon load release.
- Has no effect when the buck is in FPWM mode.

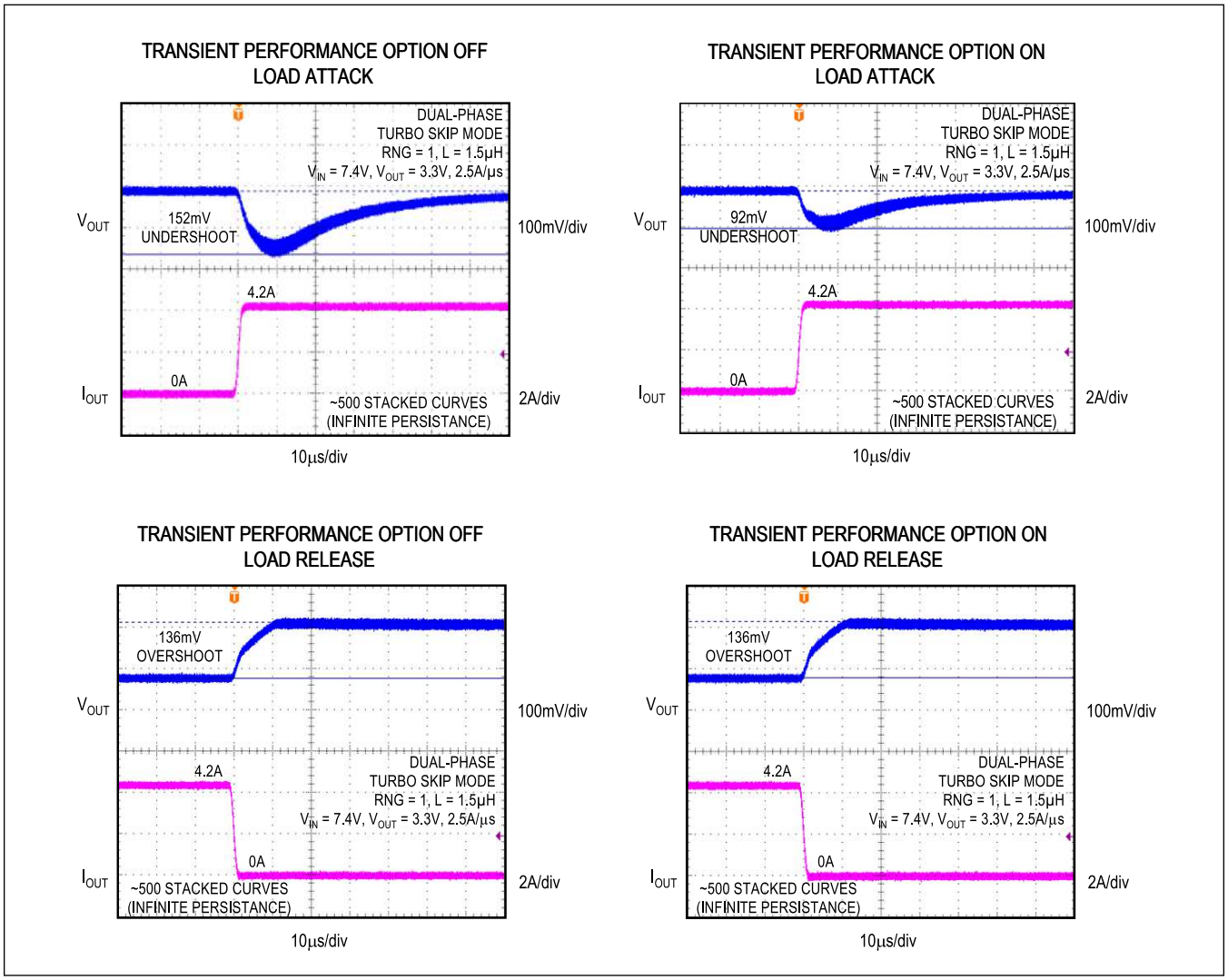


Figure 17. Effect of Transient Performance Option on Load Transient Response

The *transient performance option* also affects mode change behavior under static load. See Figure 18. Enabling the *transient performance option*:

- Reduces undershoot upon mode change from FPWM to Turbo SKIP.
- Has no effect upon mode change from Turbo SKIP to FPWM.

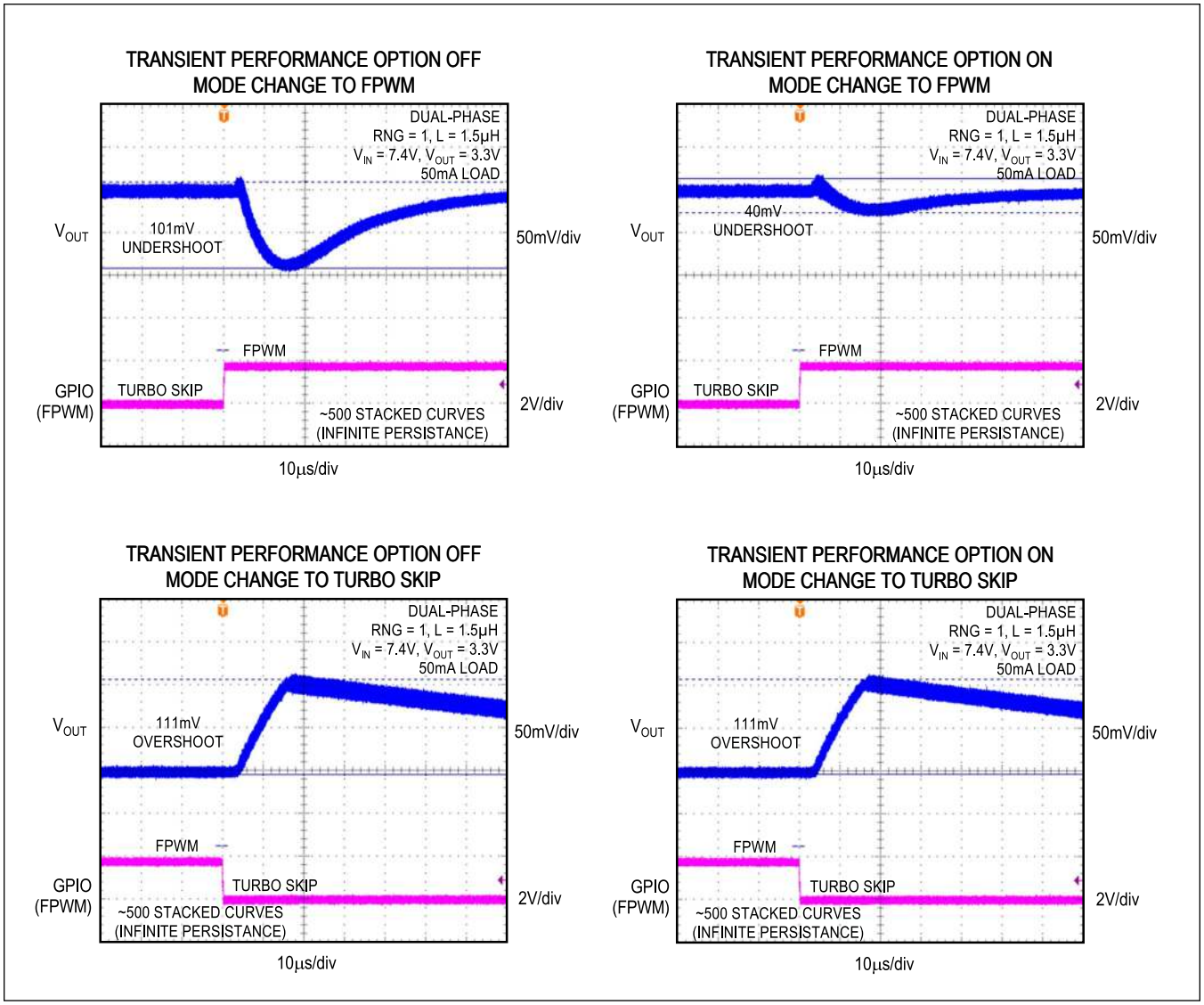


Figure 18. Effect of Transient Performance Option on Mode Change

While the *transient performance option* helps reduce the output disturbance during transients and mode changes, it also causes unintentional mode chatter which results in extra V_{OUT} ripple at certain loads. Figure 19 details the unintended side effect of the *transient performance option* when the load is near the CCM/DCM boundary.

- The *transient performance option* causes the device to chatter between its low-power SKIP mode and full-power CCM mode when inductor current is close to the CCM/DCM boundary. This causes extra V_{OUT} ripple.
- Mode chatter stops when the *transient performance option* is off. A single mode-change ripple event is observed upon mode change.

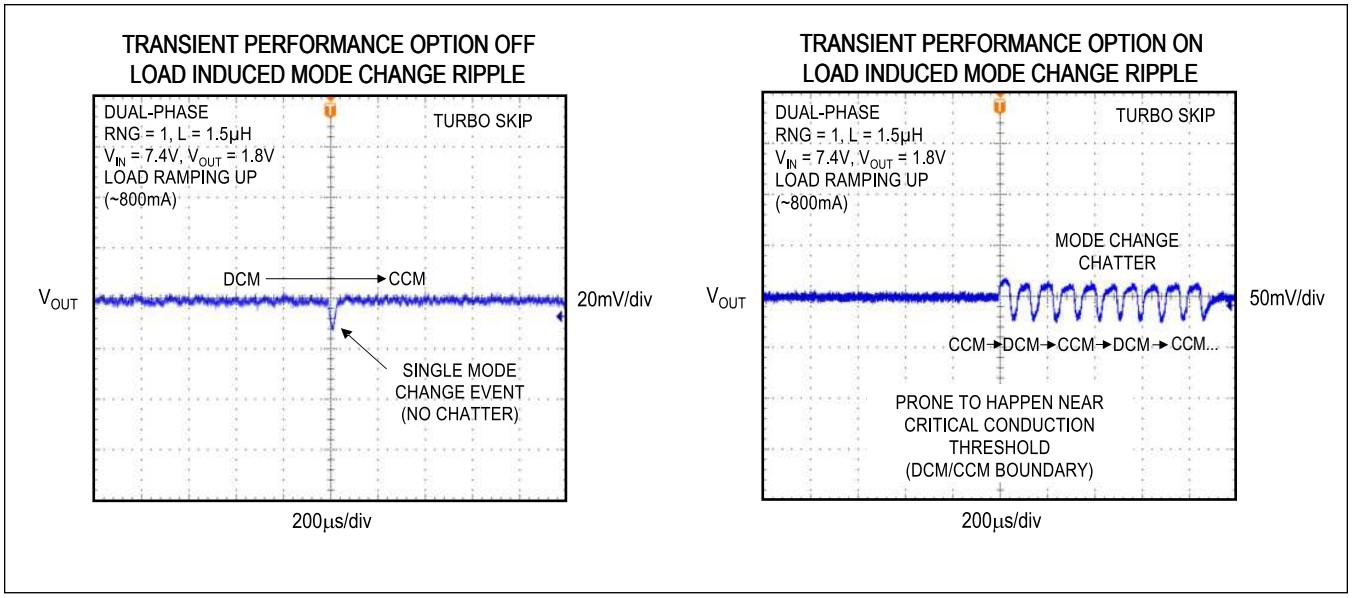


Figure 19. Effect of Transient Performance Option on Mode Chatter

Applications must decide if the extra ripple around the critical conduction load (DCM/CCM boundary) is tolerable when requesting a version of the IC with the *transient performance option* on. Use Equation 5 to estimate the buck's critical conduction load (I_{CRIT}).

Equation 5:

$$I_{CRIT} = \frac{N}{2} \times \frac{V_{OUT} \times \left(V_{IN} - V_{OUT}\right)}{V_{IN} \times F_{SW} \times L}$$

where N is the number of phases, F_{SW} is 1MHz, and L is either 0.47µH or 1.5µH depending on the range setting (RNGx bit).

Assisted Active Discharge after Soft-Stop

An internal option improves the effectiveness of the *Active Discharge Resistor* function.

The active discharge function is either *assisted* or *normal* depending on the part number (see Table 4 and Table 5). Active discharge (*normal* or *assisted*) only works when the corresponding ADENx bit is set.

- *Normal* active discharge connects an internal 100Ω resistor (R_{LX-AD}) between LXx and PGNDx to discharge the output capacitor after soft-stop finishes. Any residual voltage remaining on C_{OUT} after soft-stop discharges through R_{LX-AD}.
- *Assisted* active discharge connects an internal 0.6Ω (on-resistance) MOSFET between LXx and PGNDx to quickly discharge the output capacitor for 3ms after soft-stop finishes. During this 3ms, the buck converter cannot re-enable. Applications must wait for the 3ms hold-off time to expire before the buck can enable again.

The 3ms active discharge timer starts counting down after soft-stop completes and is subject to the root oscillator accuracy. See Figure 20.

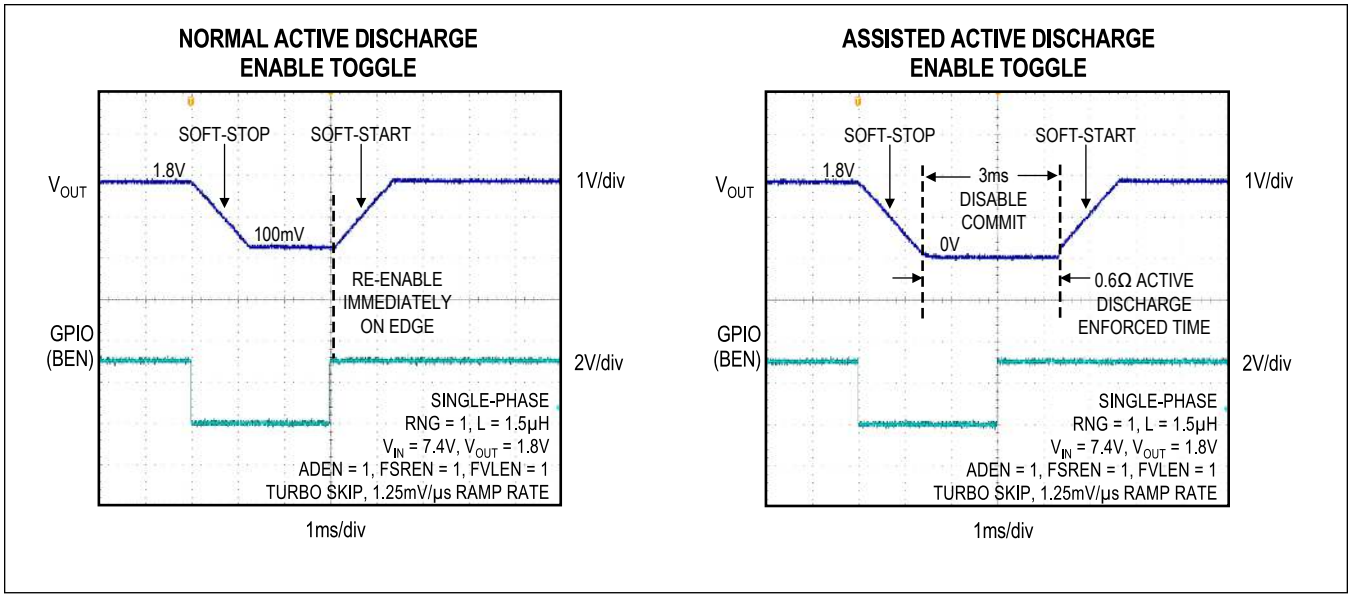


Figure 20. Normal vs. Assisted Active Discharge

Soft-Start Peak Inductor Current Limit Override

An available internal option overrides the peak inductor current limit ($I_{PEAK-HSx}$) to 1.5A during soft-start. Table 4 and Table 5 list whether the override is enabled for each MAX77511/MAX77711 part number.

If the override is enabled, the inductor peak current limit is forced to 1.5A regardless of the ILIMx[1:0] control bitfield during the soft-start ramp. The ILIMx[1:0] bitfield still controls the peak current limit after soft-start finishes. If the override is disabled, then inductor peak current limit follows the ILIMx[1:0] control field at all times while the buck is enabled.

Carefully consider the following to determine if this override is needed:

- Each buck has a soft-start ramp rate control (SFTUPDNx[2:0]) configurable from 0.15mV/µs to 40mV/µs. This ramp rate is factory-programmable. Use slower ramp rates to minimize input current during buck startup.
- Each buck has an inductor peak current limit (ILIMx[1:0]) control from 1.5A to 4.5A. This value is also factory-programmable. Use smaller limit values to minimize input current in the event of startup into excessive C_{OUT} or short-circuit.

The soft-start rate and $I_{PEAK-HSx}$ factory options provide most applications a method of limiting inrush current during buck startup. Choose to override the soft-start current limit to 1.5A for additional safety.

Consider that a low inductor current limit during soft-start might result in a non-linear soft-start ramp. It is possible that the override affects normal startup behavior. Figure 21 shows an example of the override not affecting soft-start. The soft-start rate is slow enough that inductor current does not exceed 1.5A during the ramp time.

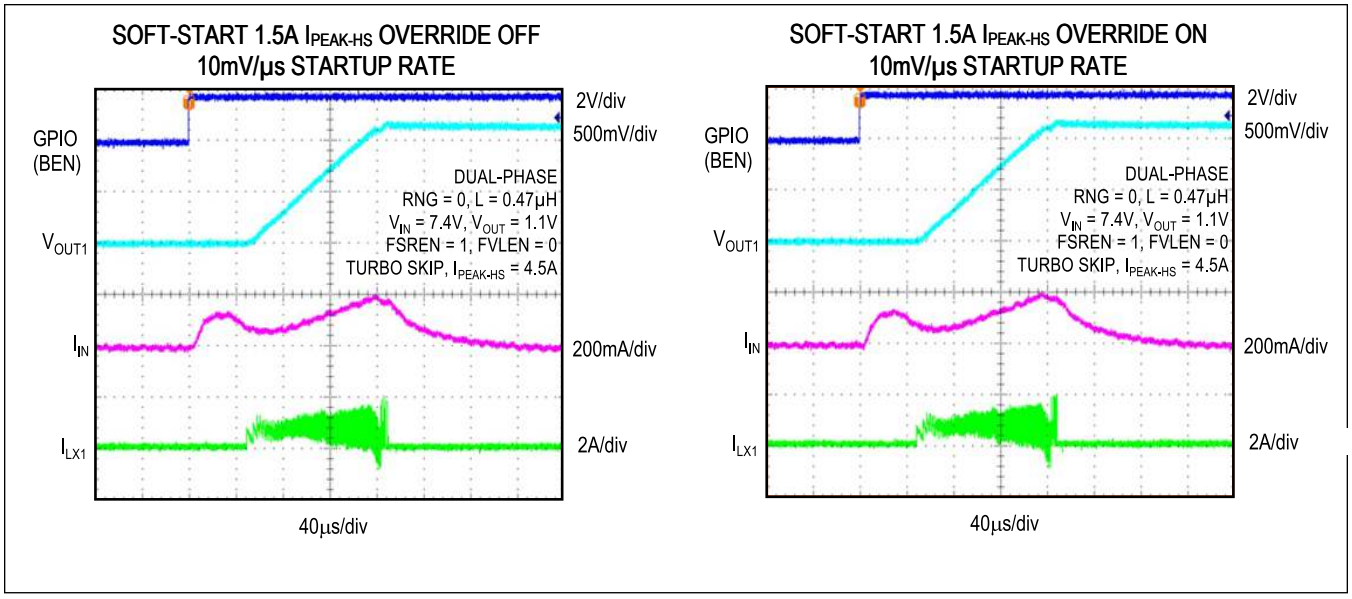


Figure 21. Override Not Affecting Soft-Start Ramp Comparison

Figure 22 shows an example where the override slows down the soft-start. The soft-start rate is fast enough such that the 1.5A peak limit interferes with the buck's ability to produce the commanded V_{OUT} ramp rate. To compensate for the slowed ramp during the override period, inductor current rises very quickly to the normal limit (set by ILIMx[1:0]) after the soft-start time finishes. Note how the override causes a *higher* peak input current as a result of the slowed V_{OUT} ramp rate during the override.

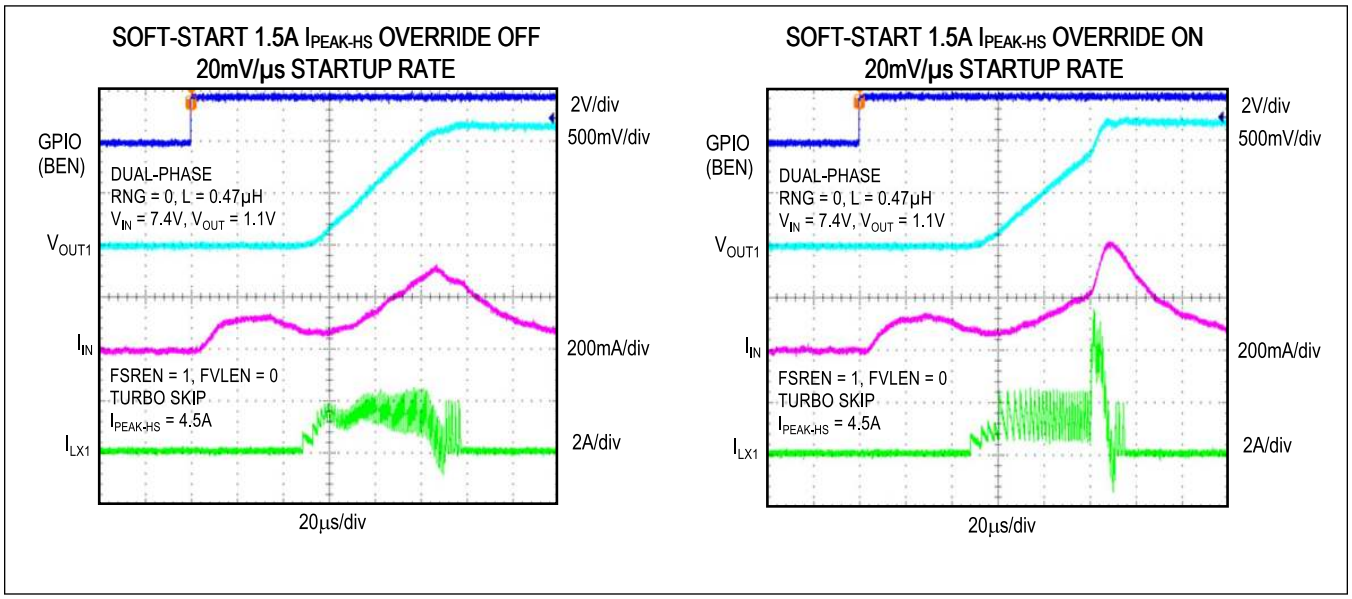


Figure 22. Override Slowing Soft-Start Rate Causing Higher Inrush Current Comparison

Applications Information—Linear Regulator (MAX77711 Only)

LDO Input/Output Capacitor Selection

Bypass INLDO to ground on the PCB with a minimum 10µF ceramic capacitor. If INLDO is connected to the output of a buck regulator, then the buck's C_{OUT} has sufficient bypassing if the capacitors are placed close to the edge of the die and the INLDO pin routing is high-priority. Buck 2 and buck 4 are physically close to INLDO and are good candidates for INLDO power.

Bypass the LDO output to ground on the PCB with a minimum 4.7µF ceramic capacitor that maintains at least 2.2µF of effective capacitance at bias.

Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients. All ceramic capacitors derate with DC bias voltage (effective capacitance goes down as DC bias goes up). Generally, small case size capacitors derate heavily compared to larger case sizes (0603 case size performs better than 0402). Consider the effective capacitance value carefully by consulting the manufacturer's data sheet.

LDO Startup Rate and Inrush Current

LDO startup rate is controlled by a 4mV/µs typical soft-start ramp ($\Delta V_{LDO}/\Delta t$). Larger values of output capacitance (C_{LDO}) result in higher input current surges during startup.

Calculate the input current surges during startup using Equation 4.

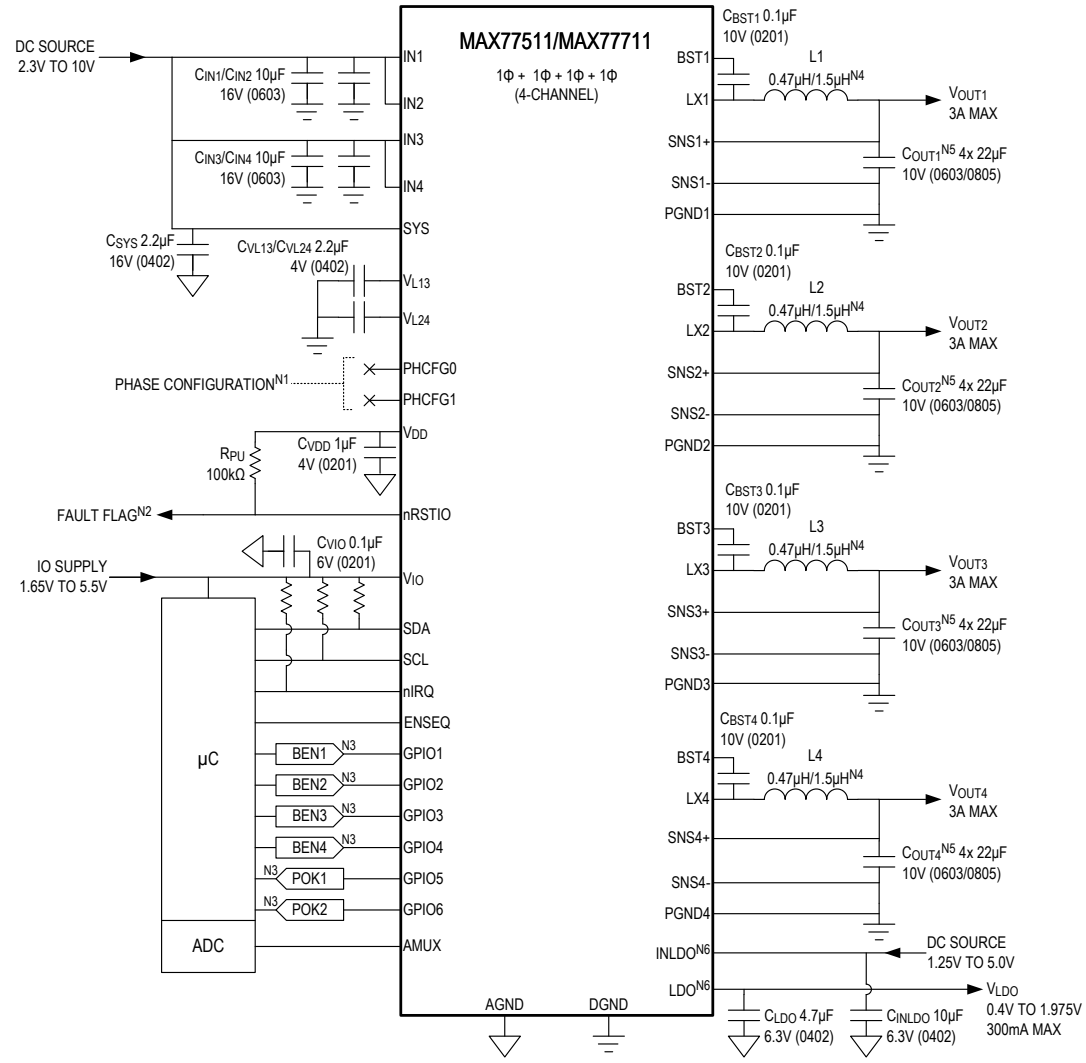
Equation 4:

$$I_{INLDO} = C_{LDO} \times \frac{\Delta V_{LDO}}{\Delta t}$$

where $\Delta V_{LDO}/\Delta t$ is the startup ramp rate of the LDO output (4mV/µs typ) and C_{LDO} is the LDO output capacitance (2.2µF minimum required). Applications that are sensitive to inrush current from the DC source should select an LDO output capacitor as close to the minimum stability requirement as possible, while at the same time, maximizing the INLDO capacitance to filter any large current spikes from the DC source.

Typical Application Circuits

1Φ+1Φ+1Φ+1Φ Configuration (4 Outputs)



SCHEMATIC NOTES

N1: [FLOAT, FLOAT] = 1Φ+1Φ+1Φ+1Φ CONFIG, 0x4F (7-BIT) I^2C DEVICE ADDRESS. SEE *PHASE CONFIGURATION*.

N2: CONNECT TO OTHER ICs FOR SYNCHRONIZED FAULT RESPONSE. SEE *RESET INPUT/OUTPUT (nRSTIO)*.

N3: EXAMPLE GPIO FUNCTION MAP. RECONFIGURABLE USING I^2C. SEE *GPIO BUCK CONTROL*.

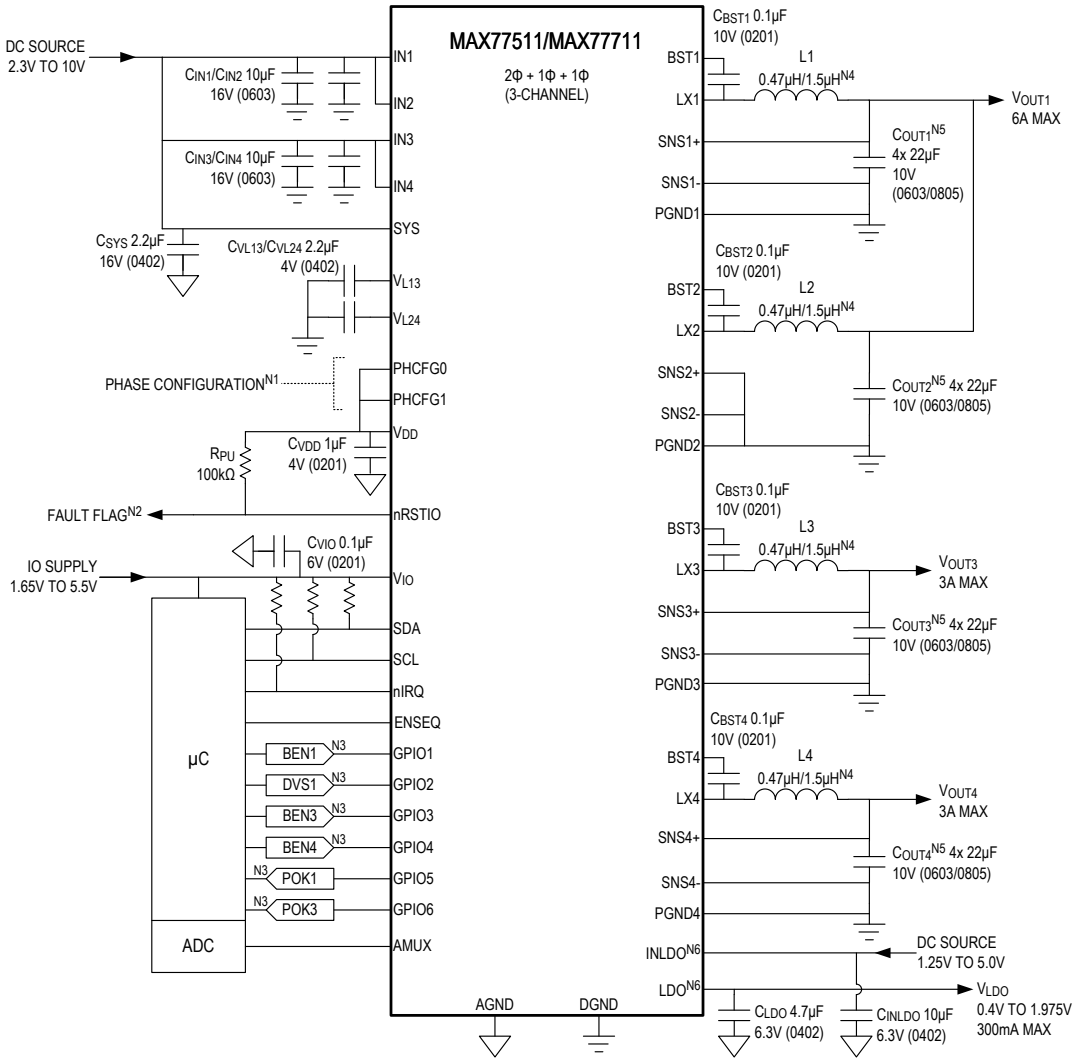
N4: USE 0.47µH FOR RNG = 0. USE 1.5µH FOR RNG = 1. SEE *INDUCTOR SELECTION*.

N5: CHOOSE C_{OUT} CAREFULLY. SEE *OUTPUT CAPACITOR SELECTION*.

N6: MAX77711 ONLY. CONNECT TO GROUND FOR MAX77511.

Typical Application Circuits (continued)

2Φ+1Φ+1Φ Configuration (3 Outputs)



SCHEMATIC NOTES

N1: [HIGH, HIGH] = 2Φ+1Φ+1Φ CONFIG, 0x75 (7-BIT) I²C DEVICE ADDRESS. SEE *PHASE CONFIGURATION*.

N2: CONNECT TO OTHER ICs FOR SYNCHRONIZED FAULT RESPONSE. SEE *RESET INPUT/OUTPUT (nRSTIO)*.

N3: EXAMPLE GPIO FUNCTION MAP. RECONFIGURABLE USING I²C. SEE *GPIO BUCK CONTROL*.

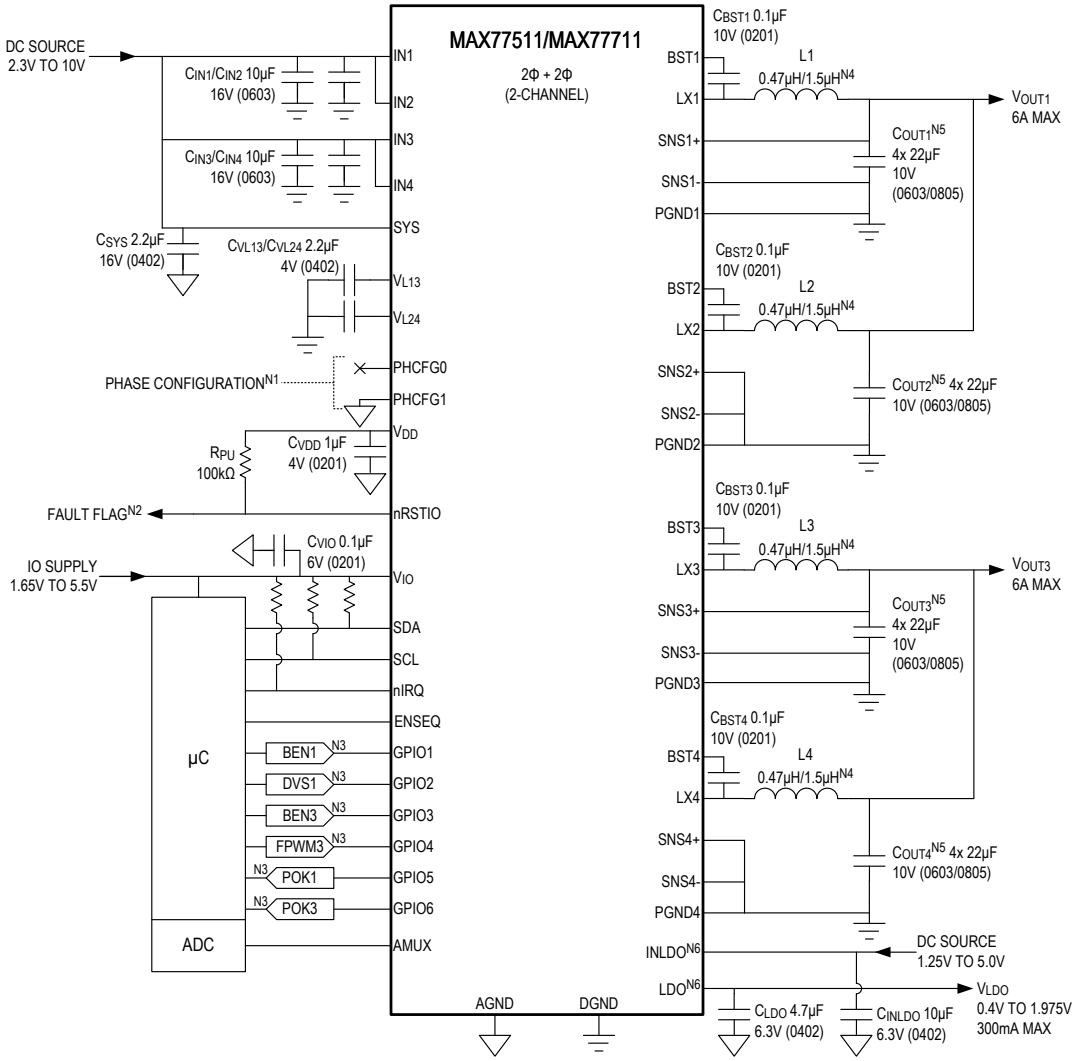
N4: USE 0.47µH FOR RNG = 0. USE 1.5µH FOR RNG = 1. SEE *INDUCTOR SELECTION*.

N5: CHOOSE C_{OUT} CAREFULLY. SEE *OUTPUT CAPACITOR SELECTION*.

N6: MAX77711 ONLY. CONNECT TO GROUND FOR MAX77511.

Typical Application Circuits (continued)

2Φ+2Φ Configuration (2 Outputs)



SCHEMATIC NOTES

N1: [LOW, FLOAT] = 2Φ+2Φ CONFIG, 0x73 (7-BIT) I²C DEVICE ADDRESS. SEE *PHASE CONFIGURATION*.

N2: CONNECT TO OTHER ICs FOR SYNCHRONIZED FAULT RESPONSE. SEE *RESET INPUT/OUTPUT (nRSTIO)*.

N3: EXAMPLE GPIO FUNCTION MAP. RECONFIGURABLE USING I²C. SEE *GPIO BUCK CONTROL*.

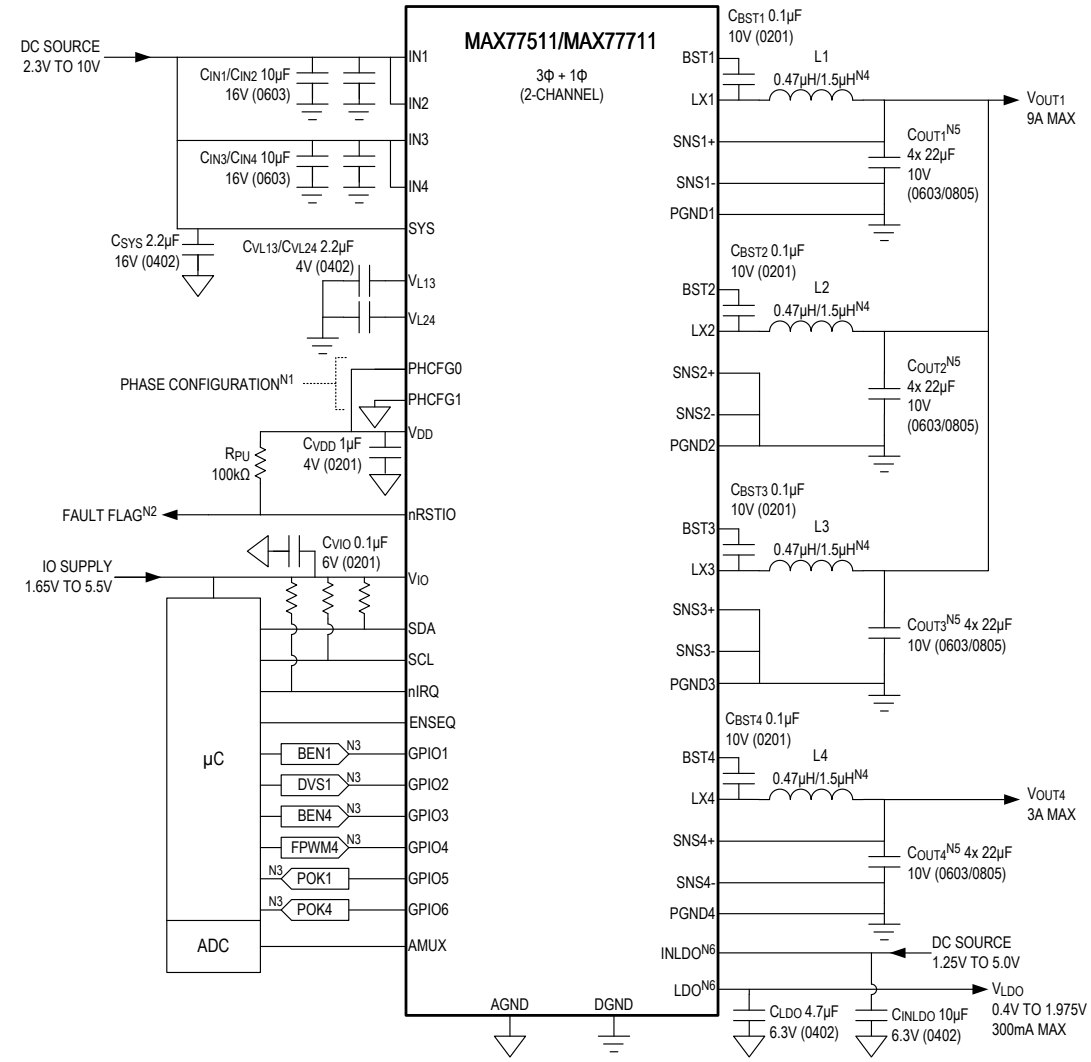
N4: USE 0.47µH FOR RNG = 0. USE 1.5µH FOR RNG = 1. SEE *INDUCTOR SELECTION*.

N5: CHOOSE C_{OUT} CAREFULLY. SEE *OUTPUT CAPACITOR SELECTION*.

N6: MAX77711 ONLY. CONNECT TO GROUND FOR MAX77511.

Typical Application Circuits (continued)

3Φ+1Φ Configuration (2 Outputs)



SCHEMATIC NOTES

N1: [LOW, HIGH] = 3Φ+1Φ CONFIG, 0x72 (7-BIT) I^2C DEVICE ADDRESS. SEE *PHASE CONFIGURATION*.

N2: CONNECT TO OTHER MAX77711s FOR SYNCHRONIZED FAULT RESPONSE. SEE *RESET INPUT/OUTPUT (nRSTIO)*.

N3: EXAMPLE GPIO FUNCTION MAP. RECONFIGURABLE USING I^2C. SEE *GPIO BUCK CONTROL*.

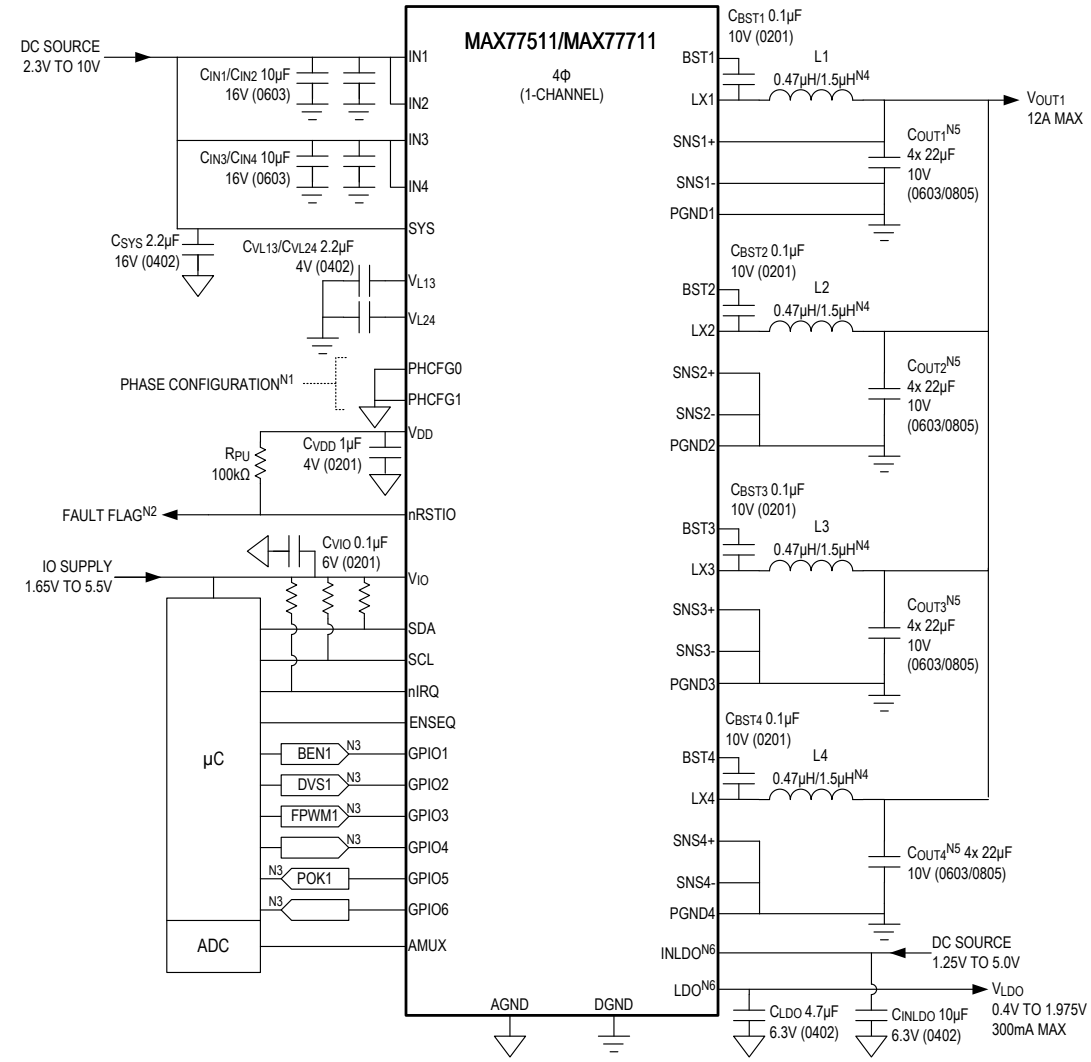
N4: USE 0.47µH FOR RNG = 0. USE 1.5µH FOR RNG = 1. SEE *INDUCTOR SELECTION*.

N5: CHOOSE C_{OUT} CAREFULLY. SEE *OUTPUT CAPACITOR SELECTION*.

N6: MAX77711 ONLY. CONNECT TO GROUND FOR MAX77511.

Typical Application Circuits (continued)

4Φ Configuration (1 Output)



SCHEMATIC NOTES

N1: [LOW, LOW] = 4Φ CONFIG, 0x71 (7-BIT) I²C DEVICE ADDRESS. SEE *PHASE CONFIGURATION*.

N2: CONNECT TO OTHER MAX77711s FOR SYNCHRONIZED FAULT RESPONSE. SEE *RESET INPUT/OUTPUT (nRSTIO)*.

N3: EXAMPLE GPIO FUNCTION MAP. RECONFIGURABLE USING I²C. SEE *GPIO BUCK CONTROL*.

N4: USE 0.47µH FOR RNG = 0. USE 1.5µH FOR RNG = 1. SEE *INDUCTOR SELECTION*.

N5: CHOOSE C_{OUT} CAREFULLY. SEE *OUTPUT CAPACITOR SELECTION*.

N6: MAX77711 ONLY. CONNECT TO GROUND FOR MAX77511.

Ordering Information

PART NUMBER	OUTPUT VOLTAGE DEFAULTS***	CHIP IDENTIFICATION	FACTORY OPTIONS**
MAX77511AEWB+T	V_{OUT1} = 3.3V (RNG1 = 1) V_{OUT2} = 1.8V (RNG2 = 1) V_{OUT3} = 5.0V (RNG3 = 1) V_{OUT4} = 2.5V (RNG4 = 1) LDO unavailable	CID[3:0] = 0x1	511A
MAX77511LEWB+T	V_{OUT1} = 1.0V (RNG1 = 0) V_{OUT2} = 1.0V (RNG2 = 0) V_{OUT3} = 3.3V (RNG3 = 1) V_{OUT4} = 0.95V (RNG4 =) LDO unavailable	CID[3:0] = 0x9	511L
MAX77511MEWB+T	V_{OUT1} = 3.3V (RNG1 = 1) V_{OUT2} = 3.3V (RNG2 = 1) V_{OUT3} = 5.0V (RNG3 = 1) V_{OUT4} = 5.0V (RNG4 = 1) LDO unavailable	CID[3:0] = 0x7	511M
MAX77511REWB+T	V_{OUT1} = 1.2V (RNG1 = 0) V_{OUT2} = 1.2V (RNG2 = 0) V_{OUT3} = 1.2V (RNG3 = 0) V_{OUT4} = 1.8V (RNG4 = 1) LDO unavailable	CID[3:0] = 0x8	511R
MAX77711AEWB+T	V_{OUT1} = 0.7V (RNG1 = 0) V_{OUT2} = 1.2V (RNG2 = 0) V_{OUT3} = 1.8V (RNG3 = 1) V_{OUT4} = 3.3V (RNG4 = 1) V_{LDO} = 1.8V	CID[3:0] = 0x0	711A
MAX77711BEWB+T	V_{OUT1} = 0.93V (RNG1 = 0) V_{OUT2} = 0.93V (RNG2 = 0) V_{OUT3} = 0.93V (RNG3 = 0) V_{OUT4} = 1.23V (RNG4 = 0) V_{LDO} = 0.4V	CID[3:0] = 0x2	711B
MAX77711CEWB+T	V_{OUT1} = 1.1V (RNG1 = 0) V_{OUT2} = 1.2V (RNG2 = 0) V_{OUT3} = 1.8V (RNG3 = 1) V_{OUT4} = 3.3V (RNG4 = 1) V_{LDO} = 0.6V	CID[3:0] = 0x4	711C
MAX77711DEWB+T	V_{OUT1} = 0.25V (RNG1 = 0) V_{OUT2} = 0.25V (RNG2 = 0) V_{OUT3} = 0.25V (RNG3 = 1) V_{OUT4} = 0.25V (RNG4 = 1) V_{LDO} = 0V	CID[3:0] = 0x5	711D
MAX77711EEWB+T	V_{OUT1} = 1.0V (RNG1 = 0) V_{OUT2} = 1.0V (RNG2 = 0) V_{OUT3} = 3.3V (RNG3 = 1) V_{OUT4} = 1.38V (RNG4 = 1) V_{LDO} = 1.8V	CID[3:0] = 0x6	711E

T = Tape and reel.

***See Table 4 and Table 5 for a selector guide.*

****Default voltage and trim target for each buck master controller. See Table 7.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/19	Initial release	—
1	6/19	Updated *Electrical Characteristics* tables, *Typical Operating Characteristics, Bump Descriptions* table, Figures 4, 10, 12, and 14, *Factory Options* section, *Active Discharge Resistor* section, *LDO Software Enable* section, *Register Details* tables, *Sequencer Control (Always-On)* section, *PCB Layout Guidelines* section, and *Ordering Information* table, added Table 4, *Test Mode* section, *Unused Bucks* section, *Advanced User Information* section	8, 9, 12, 13, 17–24, 27, 36–38, 44, 49, 51, 52, 58, 71, 82, 84–86, 88–92, 99
2	2/20	Updated Table 4 and *Ordering Information* table; added Table 5	38–41, 102
3	3/20	Updated *Ordering Information* table	102
4	6/21	Updated *Benefits and Features* section, Note 2, Table 4, Figure 7, Figure 9, *Register Details*, and *Ordering Information* table	1, 10, 36, 37, 46, 47, 59, 99
5	5/23	Updated Table 4 and *Ordering Information* table	36, 37, 98