

# LF198, LF198A, LF398, LF398A PRECISION SAMPLE-AND-HOLD AMPLIFIERS

D3218, JULY 1988 – REVISED MARCH 1989

- Acquisition Time . . . 4  $\mu$ s Typ
- Gain Error . . . 0.01% Max,  
0.001% Typ for LF198A, LF398A
- Input Offset Voltage . . .  
1 mV Max for LF198A, 2 mV Max for LF398A
- Hold Step . . . 1 mV Max for LF198A, LF398A
- Very Low Feedthrough Attenuation Ratio at  
 $f = 1$  kHz . . . 96 dB Typ
- High Input Impedance . . .  $10^{10}$   $\Omega$  Typ
- Logic Inputs Compatible With All Logic  
Families

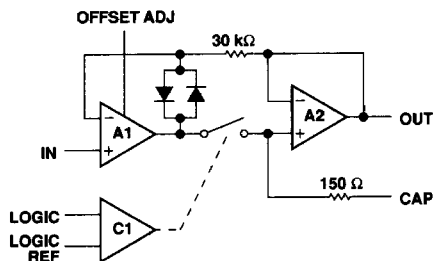
## description

These sample-and-hold amplifiers use a combination of bipolar and junction FET transistors to provide precision, high speed, and long hold times. Input offset voltages as low as 1 mV (LF198A) and gain errors as low as 0.001% (LF198A, LF398A) allow these amplifiers to be used in 12-bit systems. Properly selecting the external hold capacitor optimizes the dynamic performance. Acquisition times can be as low as 4  $\mu$ s for small capacitors, while hold step and droop errors can be held below 0.1 mV and 30  $\mu$ V/s, respectively, when using larger capacitors.

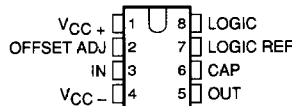
The LF198 and LF398 are fixed at unity gain with  $10^{10}$ - $\Omega$  input impedance independent of the sample or hold mode. The logic inputs are at a high differential impedance to allow easy interfacing to any logic family without ground loop problems. A separate offset adjust pin can be used to zero the input offset voltage in either the sample or hold mode. Additionally, the hold capacitor can be driven with an external signal to provide precision level shifting or "differencing" operation. The devices operate over a wide supply voltage range from  $\pm 5$  V to  $\pm 18$  V with very little change in performance. Key parameters are specified over this full supply range.

The LF198 and LF198A are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The LF398 and LF398A are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

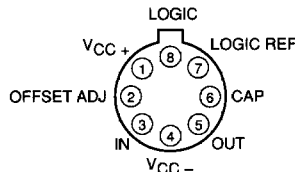
## functional block diagram



JG OR P PACKAGE  
(TOP VIEW)



L PACKAGE  
(TOP VIEW)



## AVAILABLE OPTIONS

$T_A$	$V_{IO}$ max AT $25^{\circ}\text{C}$	PACKAGE		
		CERAMIC DIP (JG)	METAL CAN (L)	PLASTIC DIP (P)
$0^{\circ}\text{C}$ to $70^{\circ}\text{C}$	2 mV	—	LF398AL	LF398AP
	7 mV	LF398JG	LF398L	LF398P
$-55^{\circ}\text{C}$ to $125^{\circ}\text{C}$	1 mV	—	LF198AL	—
	3 mV	—	LF198L	—

4

Special Functions

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS  
INSTRUMENTS

POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

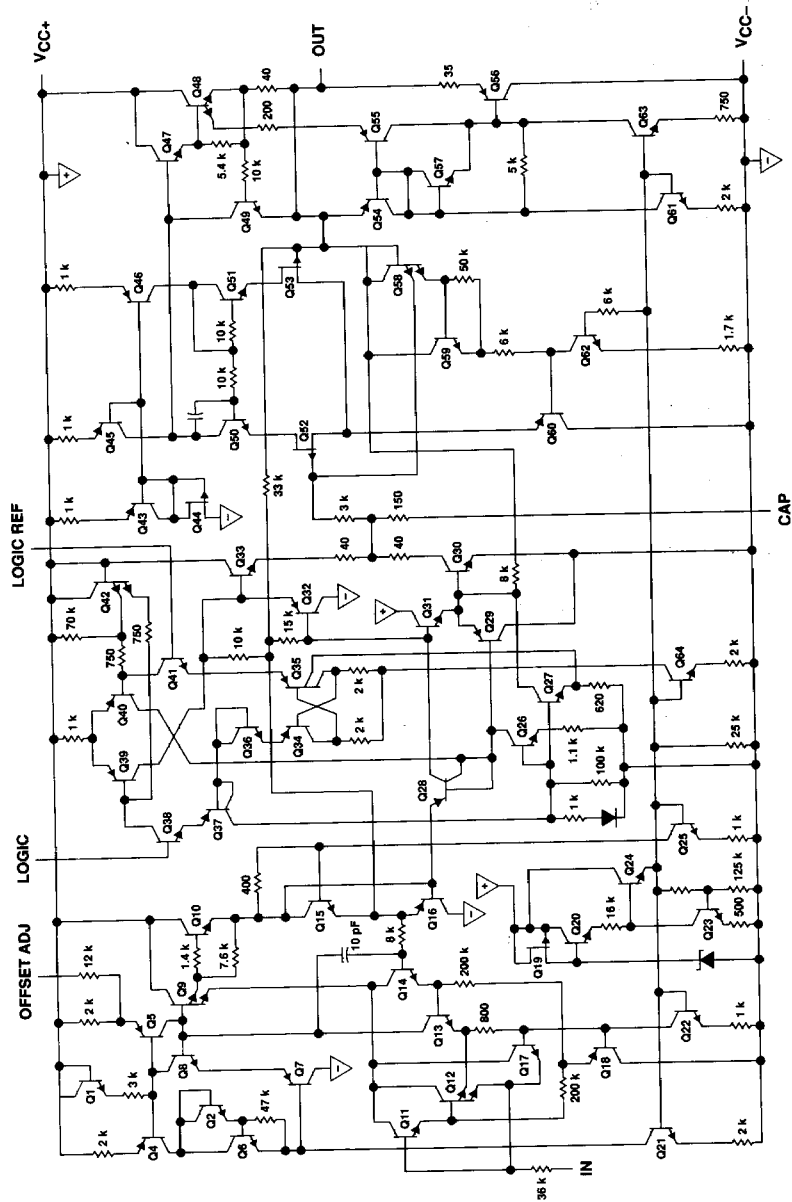
Copyright © 1988, Texas Instruments Incorporated

# LF198, LF198A, LF398, LF398A PRECISION SAMPLE-AND-HOLD AMPLIFIERS

schematic

## 4

### Special Functions



All resistor values shown are nominal and in ohms.



# LF198, LF398 PRECISION SAMPLE-AND-HOLD AMPLIFIERS

electrical characteristics in sample mode,  $V_{CC\pm} = \pm 15\text{ V}$ ,  $V_I = \pm 11.5\text{ V}$ ,  $C_h = 0.01\ \mu\text{F}$ ,  $R_L = 10\ \text{k}\Omega$ , logic reference at 0 V, logic at 2.5 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	LF198			LF398			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{IO}$ Input offset voltage	$V_{CC\pm} = \pm 5\text{ V to } \pm 18\text{ V}$	25°C		1	3		2	7	mV
		Full range			5			10	
$I_B$ Input bias current		25°C		5	25		10	50	nA
		Full range			75			100	
Differential logic threshold voltage		25°C	0.8	1.4	2.4	0.8	1.4	2.4	V
Input current, logic and logic reference		25°C		2	10		2	10	$\mu\text{A}$
Leakage current into hold capacitor terminal	$V_{CC\pm} = \pm 5\text{ V to } \pm 18\text{ V}$ , Hold mode, See Note 4	25°C		30	100		30	200	pA
Hold capacitor charging current	$V_I - V_O = 2\text{ V}$	25°C		5			5		mA
$z_i$ Input impedance	Hold mode	25°C		$10^{10}$			$10^{10}$		$\Omega$
		Full range		0.5	2		0.5	4	$\Omega$
$z_o$ Output impedance	Hold mode	25°C		0.002	0.005		0.004	0.01	%
		Full range			0.02			0.02	
Gain error (see Note 5)	$R_L = 10\ \text{k}\Omega$	25°C		86	96		80	96	dB
Feedthrough attenuation ratio	$f = 1\ \text{kHz}$	25°C		0.5	2		0.5	2.5	mV
Hold step (see Note 6)	$V_O = 0$	25°C		80	110		80	110	V
$k_{SVR}$ Supply-voltage rejection ratio	$V_{CC\pm} = \pm 5\text{ V to } \pm 18\text{ V}$ , $V_O = 0$	25°C		4.5	5.5		4.5	6.5	mA
$I_{CC}$ Supply current	$V_{CC\pm} = \pm 5\text{ V to } \pm 18\text{ V}$ , $T_A \geq 25^\circ\text{C}$	25°C		4			4		$\mu\text{s}$
		Full range		16			16		
Acquisition time to 0.1% (see Note 5)	$\Delta V_O = 10\text{ V}$ , $C_h = 1\ \mu\text{F}$ $\Delta V_O = 10\text{ V}$ , $C_h = 0.01\ \mu\text{F}$	25°C							

4

Special Functions

<sup>†</sup>Full range is  $-55^\circ\text{C}$  to  $125^\circ\text{C}$  for the LF198 and  $0^\circ\text{C}$  to  $70^\circ\text{C}$  for the LF398.

NOTES: 4. The effects of a rise in junction temperature due to power dissipation or elevated ambient free-air temperature can be approximated by doubling the 25°C value for each 11°C increase in junction temperature. The specified limit applies for the full input signal range.

5. See definition of terms.

6. See definition of terms. Hold step is sensitive to stray capacitance coupling between input logic signals and the hold capacitor. Stray capacitance of 1 pF, for example, creates an additional 0.5-mV step with a 5-V logic swing and a 0.01- $\mu\text{F}$  hold capacitor. The magnitude of the hold step is inversely proportional to the value of the hold capacitor.

# LF198A, LF398A PRECISION SAMPLE-AND-HOLD AMPLIFIERS

**electrical characteristics in sample mode,  $V_{CC\pm} = \pm 15\text{ V}$ ,  $V_I = \pm 11.5\text{ V}$ ,  $C_H = 0.01\ \mu\text{F}$ ,  $R_L = 10\ \text{k}\Omega$ , logic reference at 0 V, logic at 2.5 V (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	T <sub>A</sub> <sup>†</sup>	LF198A			LF398A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>IO</sub> Input offset voltage	V <sub>CC±</sub> = ±5 V to ±18 V	25°C		0.5	1		1	2	mV
		Full range			2		3		
I <sub>IB</sub> Input bias current		25°C		5	25		10	25	nA
		Full range			75		50		
Differential logic threshold voltage		25°C	0.8	1.4	2.4	0.8	1.4	2.4	V
Input current, logic and logic reference		25°C		2	10		2	10	μA
Leakage current into hold capacitor terminal	V <sub>CC±</sub> = ±5 V to ±18 V, Hold mode, See Note 4	25°C		10	100		10	100	pA
Hold capacitor charging current	V <sub>I</sub> - V <sub>O</sub> = 2 V	25°C		5			5		mA
z <sub>i</sub> Input impedance		25°C		10 <sup>10</sup>			10 <sup>10</sup>		Ω
z <sub>o</sub> Output impedance	Hold mode	25°C		0.5	1		0.5	1	Ω
		Full range			4		6		
Gain error (see Note 5)	R <sub>L</sub> = 10 kΩ	25°C		0.001	0.005		0.001	0.005	%
		Full range			0.01		0.01		
Feedthrough attenuation ratio	f = 1 kHz	25°C	86	96		86	96		dB
Hold step (see Note 6)	V <sub>O</sub> = 0	25°C		0.25	1		0.25	1	mV
k <sub>SVR</sub> Supply-voltage rejection ratio	V <sub>CC±</sub> = ±5 V to ±18 V, V <sub>O</sub> = 0	25°C	90	110		90	110		V
I <sub>CC</sub> Supply current	V <sub>CC±</sub> = ±5 V to ±18 V, T <sub>A</sub> ≥ 25°C	25°C		4.5	5.5		4.5	6.5	mA
Acquisition time to 0.1% (see Note 5)	ΔV <sub>O</sub> = 10 V, C <sub>H</sub> = 1 μF	25°C		4	6		4	6	μs
				16	25		16	25	

<sup>†</sup>Full range is -55°C to 125°C for the LF198A and 0°C to 70°C for the LF398A.

- NOTES: 4. The effects of a rise in junction temperature due to power dissipation or elevated ambient free-air temperature can be approximated by doubling the 25°C value for each 11°C increase in junction temperature. The specified limit applies for the full input signal range.
5. See definition of terms.
6. See definition of terms. Hold step is sensitive to stray capacitance coupling between input logic signals and the hold capacitor. Stray capacitance of 1 pF, for example, creates an additional 0.5-mV step with a 5-V logic swing and a 0.01-μF hold capacitor. The magnitude of the hold step is inversely proportional to the value of the hold capacitor.

4

Special Functions

# LF198, LF198A, LF398, LF398A PRECISION SAMPLE-AND-HOLD AMPLIFIERS

TYPICAL CHARACTERISTICS,  $V_{CC\pm} = \pm 15 V^{\dagger}$

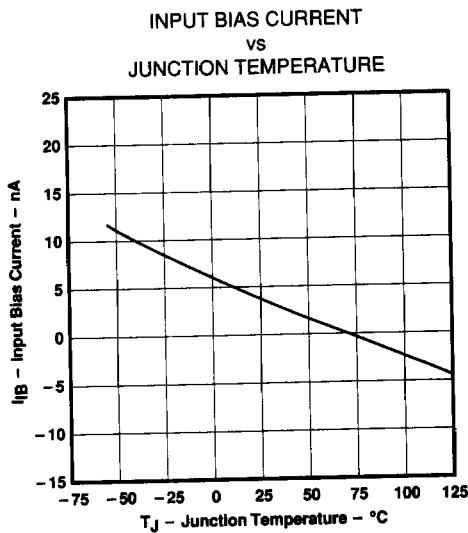


FIGURE 1

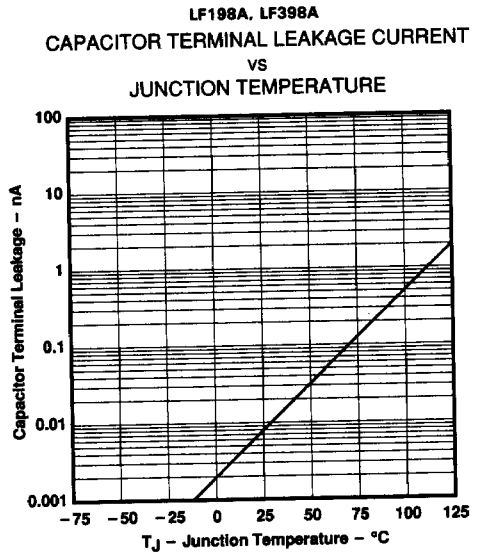


FIGURE 2

4

Special Functions

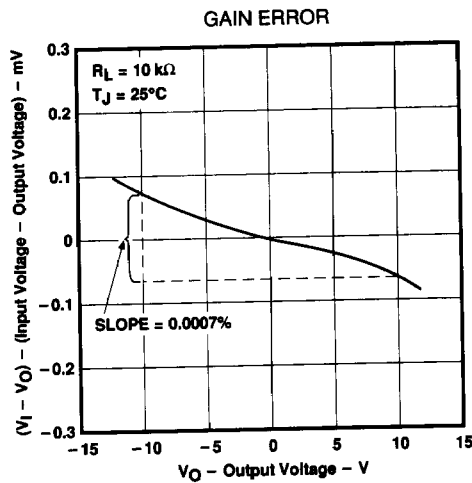


FIGURE 3

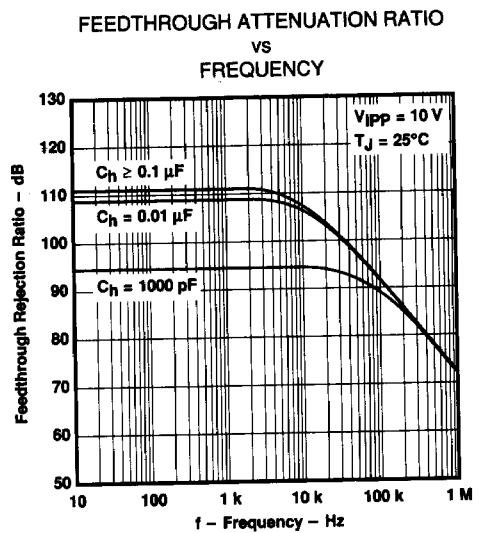


FIGURE 4

<sup>†</sup>Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS,  $V_{CC\pm} = \pm 15 V^\dagger$

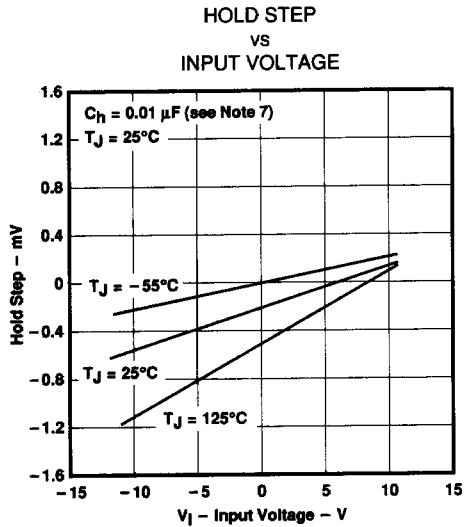


FIGURE 5

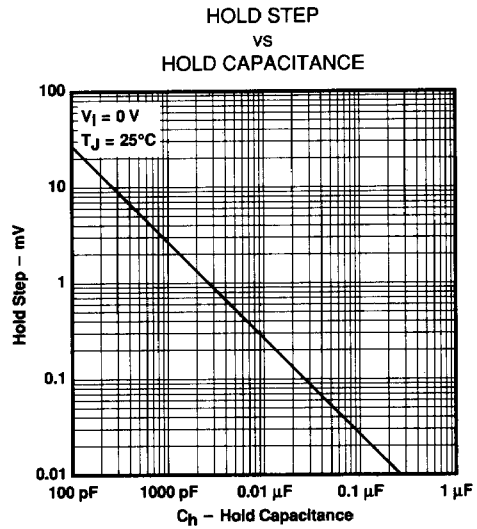


FIGURE 6

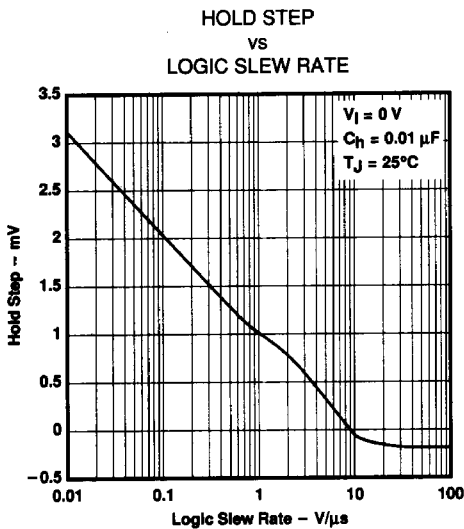


FIGURE 7

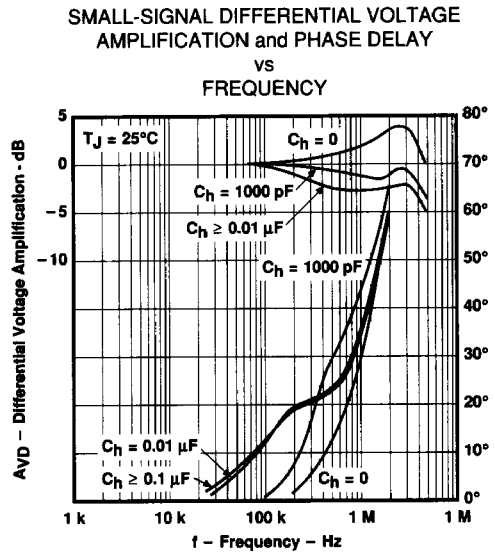


FIGURE 8

4

Special Functions

<sup>†</sup>Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.  
NOTE 7: The amplitude of the hold step varies inversely with the value of the hold capacitor.

# LF198, LF198A, LF398, LF398A PRECISION SAMPLE-AND-HOLD AMPLIFIERS

TYPICAL CHARACTERISTICS,  $V_{CC\pm} = \pm 15\text{ V}^\dagger$

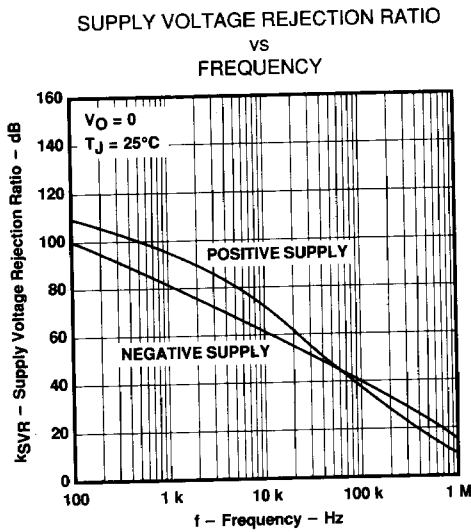


FIGURE 9

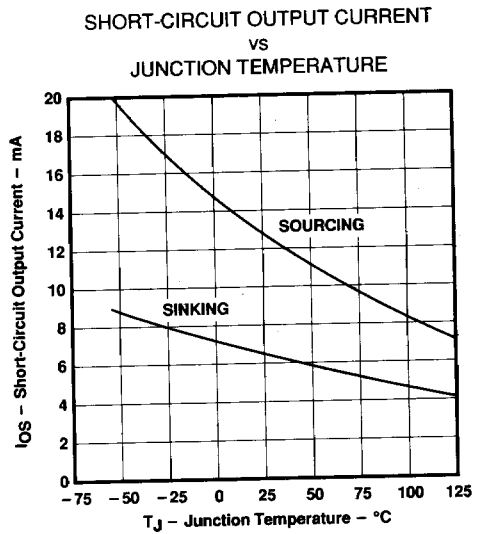


FIGURE 10

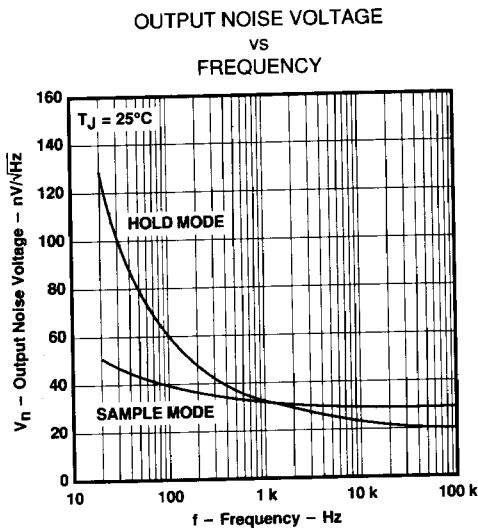


FIGURE 11

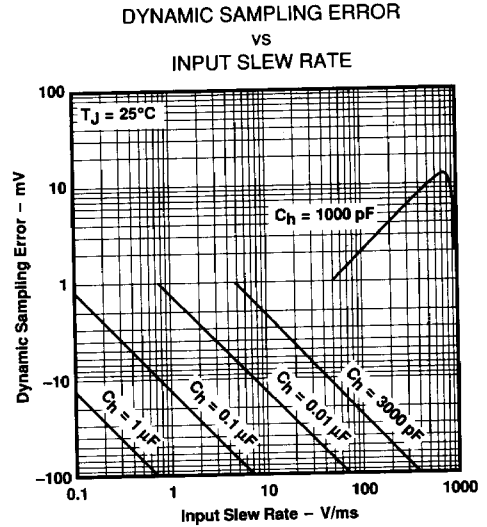


FIGURE 12

## 4 Special Functions

<sup>†</sup>Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



TYPICAL CHARACTERISTICS,  $V_{CC\pm} = \pm 15 V^{\dagger}$

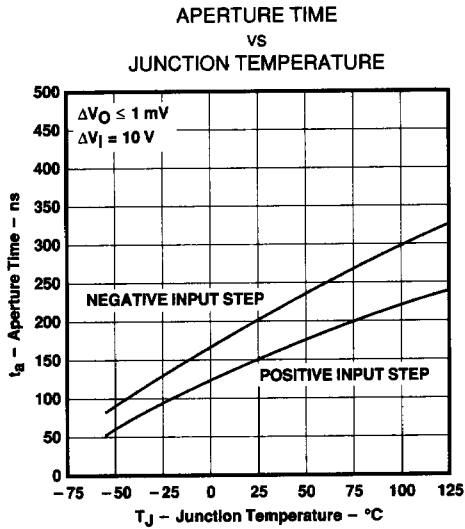


FIGURE 13

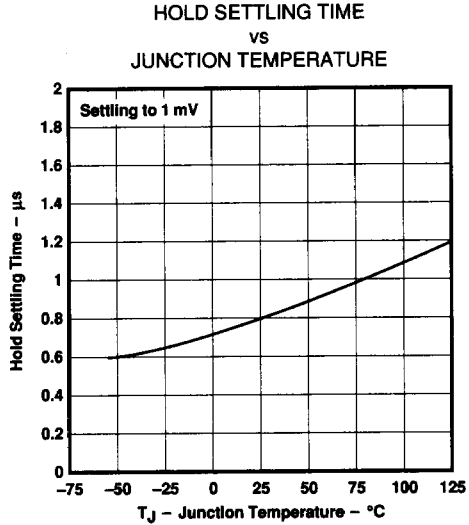


FIGURE 14

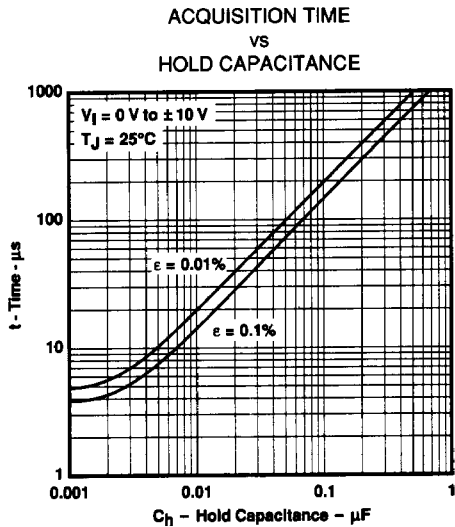


FIGURE 15

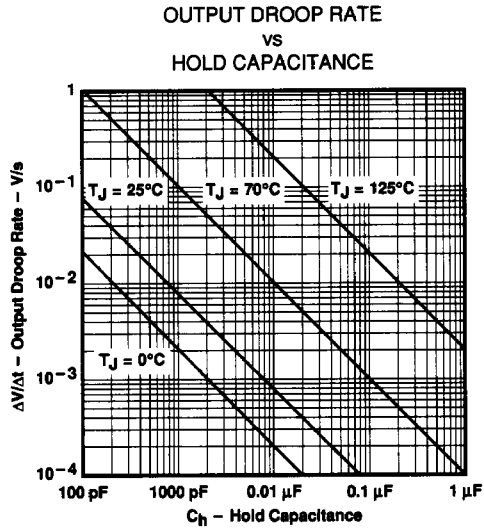


FIGURE 16

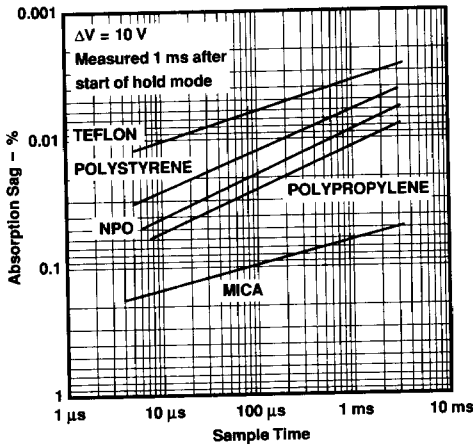
4

Special Functions

<sup>†</sup>Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

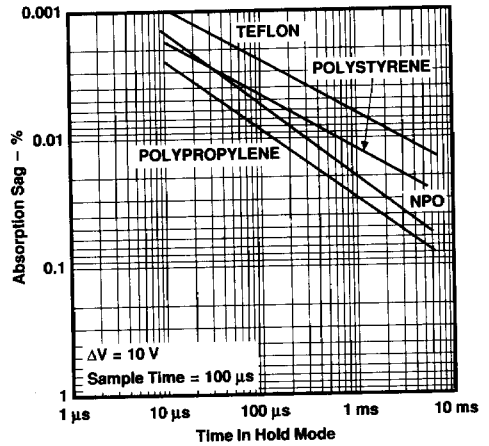
**TYPICAL CHARACTERISTICS,  $V_{CC\pm} = \pm 15 V^{\dagger}$**

**CAPACITOR DIELECTRIC ABSORPTION  
 VS  
 SAMPLE TIME**



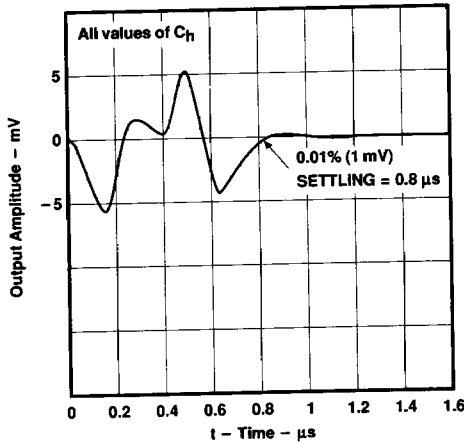
**FIGURE 17**

**CAPACITOR DIELECTRIC ABSORPTION  
 VS  
 TIME IN HOLD MODE**



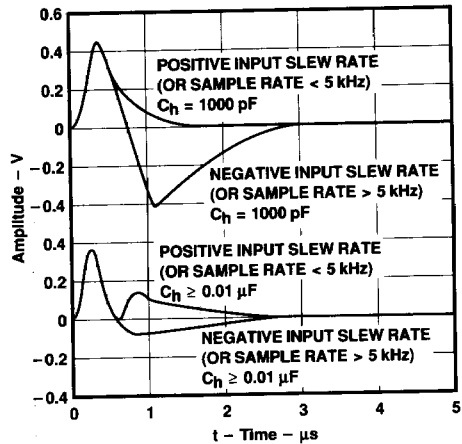
**FIGURE 18**

**OUTPUT TRANSIENT  
 AT START OF HOLD MODE**



**FIGURE 19**

**OUTPUT TRANSIENT  
 AT START OF SAMPLE PERIOD**



**FIGURE 20**

**4**

**Special Functions**

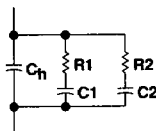
<sup>†</sup>Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL APPLICATION DATA

hold capacitor

For fast sample-and-hold applications, the value of the hold capacitor is critical. A low value gives fast acquisition but also increases errors due to hold step and droop caused by amplifier bias current. The capacitor should be made as large as possible consistent with acquisition time and dynamic sampling error requirements. Capacitors larger than 0.1  $\mu\text{F}$  are generally not available in the low-loss dielectrics like Teflon, Polystyrene, and NPO, at least not at a reasonable price and size. Mylar, even with its poor dielectric absorption properties, may be a reasonable choice when very long sample times are used and low droop rates are needed.

Dielectric absorption in the hold capacitor can often be the major source of error in a sample-and-hold amplifier. The equivalent "circuit" of a typical capacitor with parallel RC networks used to model dielectric absorption is shown in Figure 21. In this capacitor, rapid changes in capacitor voltage are not tracked by the internal parasitic capacitors because of the resistance in series with them. This leads to a "sag" effect in the hold capacitor after a sudden change in voltage followed by a rapid switch to the hold mode. The capacitor remembers its previous state via the charge in the internal parasitic capacitance and sags back slightly toward the previous voltage. The magnitude of the sag depends upon the voltage change and the time spent sampling the new voltage. Several time constants are typically evident in the sag, although some capacitors tend to exhibit a single time constant, while others show a sag that indicates a blending of many time constants. Figures 17 and 18 show the amount of sag found after a 10-V step, with sample time at the new voltage and hold time at the new voltage as variables. It is obvious that sag problems are minimized by long sample times and short hold times. While this is often in conflict with basic sampling requirements, the sample-and-hold amplifier should be kept in the "tracking", or sampling, mode as much as possible to maximize the time the hold capacitor spends near the voltage at which it eventually "holds".



NOTE: C1 and C2 are approximately equal to  $0.01C_h$  to  $0.1C_h$ . R1 and R2 generate time constants of 0.1 to 50 ms with C1 and C2.

FIGURE 21. TYPICAL HOLD CAPACITOR EQUIVALENT CIRCUIT

The best capacitor for sample-and-hold applications is Teflon, which is clearly superior with regard to dielectric absorption and operates over the full temperature range ( $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ). If size or price is a problem, the second choice for full-temperature-range operation is NPO (or COG) ceramic units. Some care must be used because not all NPO capacitors use the low-dielectric-constant ceramic necessary for low dielectric absorption. For lower temperature ( $\leq 70^{\circ}\text{C}$ ), Polystyrene has traditionally been the best hold capacitor. The best units are cylindrical and fairly large; there seems to be a strong correlation between small size and poor dielectric performance. Polypropylene has nearly the same absorption properties as polystyrene and offers  $85^{\circ}\text{C}$  operation; it also tends to be smaller. Other standard dielectrics such as mica, glass, mylar, and ordinary ceramic are much worse with regard to dielectric absorption. Mylar is sometimes used for large values when the ratio of sample to hold time is large and extremely low droop is required.

dynamic sampling error

A significant sampling error can occur in any sample-and-hold amplifier if the input is moving when the unit is put into the hold mode. The two major causes for this error are digital delay in switch opening and analog delay across the hold capacitor. The switch opening delay is obvious and leads to a "held" output error of  $(dv/dt) \times t_d$ ;  $dv/dt$  is the slew rate of the input signal and  $t_d$  is the switch delay. For this device,  $t_d$  is approximately 150 ns, giving a 4.5-mV error when sampling the zero crossing of a 5-V (peak) sine wave at 1 kHz ( $dv/dt = A \times 2\pi f = 5 \times 2\pi \times 10^3$ ). The analog delay is the difference between input signal and capacitor voltage. It is determined by the RC product of the hold capacitor and the effective series resistance, which in this device is about 150  $\Omega$ .

# LF198, LF198A, LF398, LF398A PRECISION SAMPLE-AND-HOLD AMPLIFIERS

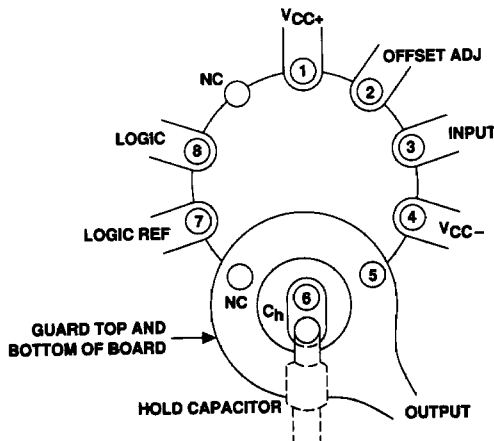
## TYPICAL APPLICATION DATA

This analog delay with a 0.01- $\mu\text{F}$  hold capacitor is  $R \times C = 150 \times 10^{-8} = 1.5 \mu\text{s}$ , or about ten times the delay of the switch. The held output is related in time to the input voltage *before* the hold command was given. The overall dynamic sampling error is the sum of the digital and analog errors. Figure 12 helps estimate these errors as a function of input slew rate and hold capacitor size.

Dynamic sampling error can be reduced by a factor of ten or more by inserting a delay in the logic input so that the "hold" command is delayed by an amount equal to the RC time constant of the device and the external hold capacitor. For a 0.01- $\mu\text{F}$  hold capacitor and the 150- $\Omega$  resistor internal to this device, this value is 1.5  $\mu\text{s}$ . A simple RC network can be used in front of the logic input for delays up to approximately 1  $\mu\text{s}$ . Longer delays require the addition of a logic gate to speed up the rise time of the delayed signal. See "logic rise time" for further details.

### hold step

Hold step is the small voltage step (after settling) seen at the output of a sample-and-hold amplifier when it is switched from the sample mode to the hold mode with a steady dc input. Hold step is typically the result of, or can be modeled as, a fixed quantity of charge transferred to the hold capacitor due to internal switching that occurs during the hold command. In the case of this device, that charge is approximately 5 pC, giving a hold step of 0.5 mV for a 0.01- $\mu\text{F}$  hold capacitor and 5 mV for a 1000-pF hold capacitor ( $V = Q/C$ ). Hold step is reasonably independent of logic amplitude if care is taken to minimize the stray capacitance between the logic input and the hold capacitor. With thoughtful layout, including the guarding technique shown in Figure 21, stray capacitance should be under 0.3 pF, limiting charge variations to less than 0.3 pC/V.



NOTE: Use 10-pin layout. The guard around  $C_h$  is tied to output.

FIGURE 22. GUARDING TECHNIQUE (BOTTOM VIEW)

Hold step varies slightly with analog input voltage (see Typical Characteristics). A typical unit changes at a rate of 0.4 pC/V. This slight variation manifests itself as a gain error when the amplifier is switched to the hold mode. With a 0.01- $\mu\text{F}$  capacitor, the resulting gain error is  $(0.4 \text{ pC/V}) / (0.01 \mu\text{F}) = 0.004\%$ . This gain error is in the opposite direction of dc (sample mode) gain error. When the hold capacitor has a high value, dc gain error dominates and gain is slightly below unity (0.002%). When the hold capacitor has a low value ( $< 0.01 \mu\text{F}$ ), gain error induced by hold step dominates, and hold-mode gain is slightly above unity. Zeroing out hold step does not change the variation of hold step with regard to input voltage.

4

Special Functions

TYPICAL APPLICATION DATA

offset zeroing

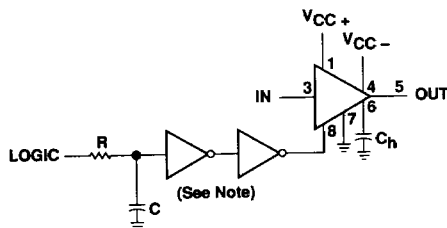
A sample-and-hold amplifier has two distinct offset voltages. The first is the dc offset voltage of the amplifier while in the sample, or "tracking," mode. It is identical to the input offset voltage of any operational amplifier. The second offset voltage is the sum of the dc offset voltage plus a dynamic term called hold step. Hold step is a change in output voltage when the amplifier is switched from sample mode to hold mode with the input held steady. This second offset voltage is often called hold-mode offset voltage. It can be less than or much greater than the dc offset voltage, depending on the magnitude and sign of hold step.

A fairly accurate model for hold step is a fixed charge injected into the hold capacitor by the switch turn-off circuitry. The magnitude of the charge is reasonably independent of logic input amplitude. The resulting change in the hold capacitor is  $Q/C_H$ . The charge  $Q$  is typically 5 pC, giving a 0.5-mV hold step with a 0.01- $\mu$ F hold capacitor. Since most sample-and-hold amplifiers are "used" (i.e., have their outputs read by an A-to-D converter), during the hold mode, hold-mode offset voltage is arguably more important than the sample-mode dc offset voltage.

Adjusting dc offset voltage is accomplished with a 1-k $\Omega$  low TC cermet potentiometer tied to  $V_{CC+}$  with 0.6 mA flowing through it and the wiper tied to pin 2. This allows pin 2 to be moved  $\pm 300$  mV around its nominal voltage (0.3 V below  $V_{CC+}$ ). The offset voltage adjustment range is  $\pm 9$  mV, and the adjustment procedure nominally improves offset voltage drift when the dc offset voltage is reduced to zero. This offset method *can* be used to zero out hold-mode offset voltage, but at the expense of some induced offset voltage drift. Each millivolt of hold-step offset corrected by this method introduces 3.3  $\mu$ V/ $^{\circ}$ C drift. For 0.002- $\mu$ F hold capacitors or larger with hold step a few millivolts or less, this is a practical solution to hold-mode offset voltage. In precision, wide-temperature-range applications, or when  $C_H$  is less than 0.002  $\mu$ F, a separate hold-mode zeroing method should be used. The circuit shown in Figure 28, which uses a logic inverter and a 5-pF capacitor, is recommended.

logic fall time

Hold step is independent of logic input fall time only for fall times faster than 10 V/ $\mu$ s. For example, as logic fall time changes from 10 V/ $\mu$ s to 1 V/ $\mu$ s, hold step with a 0.01- $\mu$ F hold capacitor typically increases from 0.25 mV to 1 mV. (See Figure 7 for more data and refer to Figure 23.) If logic slew rate is not constant, use the value at the threshold point (1.5 V with respect to logic reference). An RC network will have a discharge slew rate of  $V_L/RC$ , where  $V_L$  is the logic threshold of the LF198. The delay generated by the network will be  $RC \times \ln(V_{CC+}/V_L)$ , where  $V_{CC+}$  is logic amplitude. For a 1- $\mu$ s delay with 5-V logic, an RC time constant of 0.8  $\mu$ s is required. This has a slew rate of 2 V/ $\mu$ s at threshold, which slightly degrades hold step. It is obvious that an RC delay network significantly longer than 1  $\mu$ s will have a large effect on hold step. If longer delays are required, they should be followed by several inverter stages or a Schmitt trigger to increase slew rate.

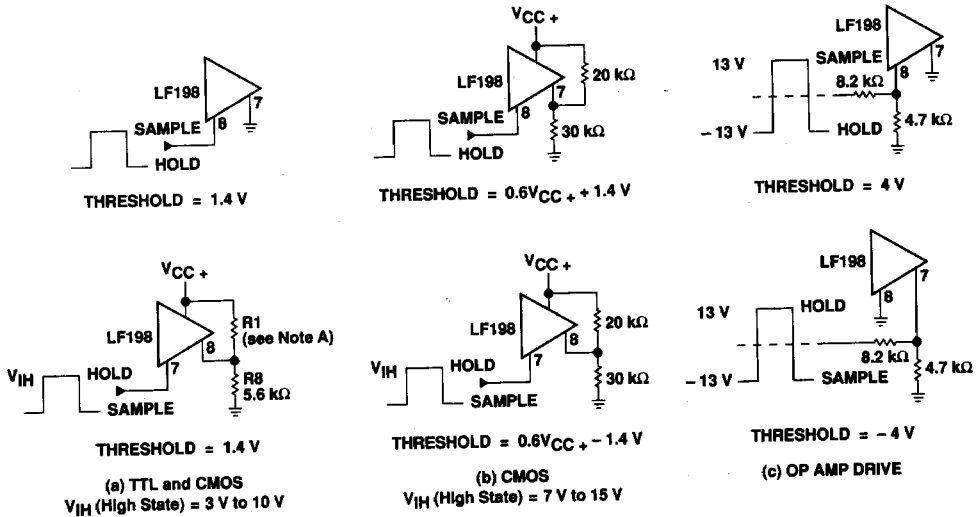


NOTE: Inverters may be eliminated for  $RC \leq 3 \mu$ s.

FIGURE 23. ADDING DELAY TO LOGIC INPUT

# LF198, LF198A, LF398, LF398A PRECISION SAMPLE-AND-HOLD AMPLIFIERS

## TYPICAL APPLICATION DATA

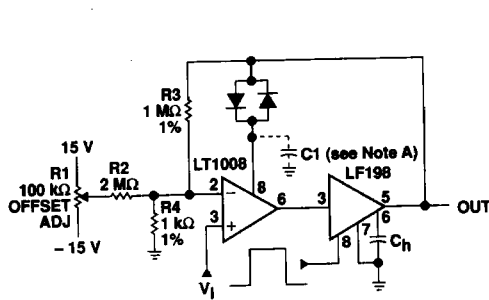


NOTES: A. Select R1 for 2.8 V at pin 8.  
 B. The logic input signal high level must be at least 2 V below the positive supply voltage of the device.

FIGURE 24. LOGIC INPUT CONFIGURATIONS

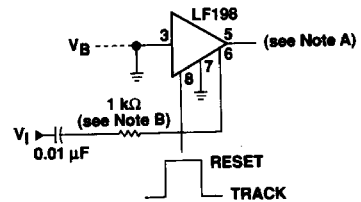
## 4

### Special Functions



NOTE A: For lower gains, the LT1008 must be frequency compensated. Use approximately  $(100/A_V)$  pF from comp2 to ground.

FIGURE 25. x1000 SAMPLE-AND-HOLD

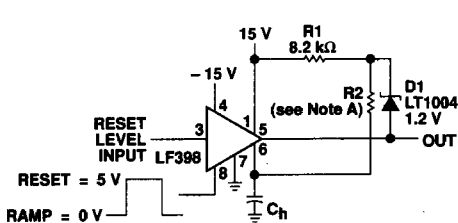


NOTES: A.  $V_O = V_B + \Delta V_I$  (Hold mode).  
 B. This resistor protects input from surge currents but increases sample time. It can be eliminated if input is otherwise protected.  
 C. Output follows input in hold mode and resets to  $V_B$  in sample mode.

FIGURE 26. SAMPLE-AND-DIFFERENCE CIRCUIT

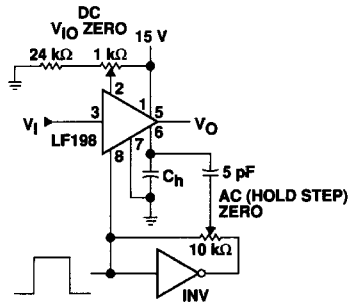
# LF198, LF198A, LF398, LF398A PRECISION SAMPLE-AND-HOLD AMPLIFIERS

## TYPICAL APPLICATION DATA

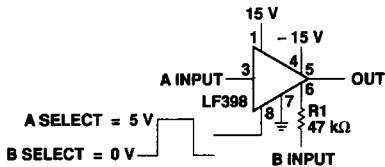


NOTE A: Select R2 for ramp rate  $\Delta V/\Delta t = 1.2 \text{ V}/(R_2)(C_H)$ ,  
 $R \geq 10 \text{ k}\Omega$ .

**FIGURE 27. RAMP GENERATOR WITH VARIABLE RESET LEVEL**

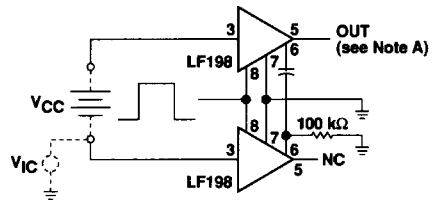


**FIGURE 28. DC AND AC ZEROING**



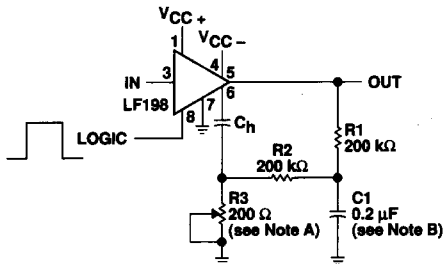
PARAMETER	A	B	UNIT
Gain	$1 \pm 0.02$	$1 \pm 0.2$	%
$z_1$	10 <sup>7</sup>	47	k $\Omega$
BW	$\approx 1000$	$\approx 400$	kHz
Crosstalk at 1 kHz	-90	-90	dB
Offset	$\leq 6$	$\leq 75$	mV

**FIGURE 29. 2-CHANNEL SWITCH**



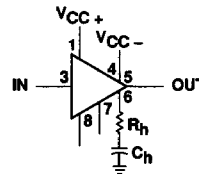
NOTE A: Output equals  $V_{CC}$  when in hold mode. Output equals  $(V_{CC} + V_{IC})$  when in sample mode.

**FIGURE 30. DIFFERENTIAL HOLD**



NOTES: A. Adjust R3 for amplitude.  
 B. Select for time constant  $C_1 = \tau / 100 \text{ k}\Omega$ .

**FIGURE 31. CAPACITOR HYSTERESIS COMPENSATION**

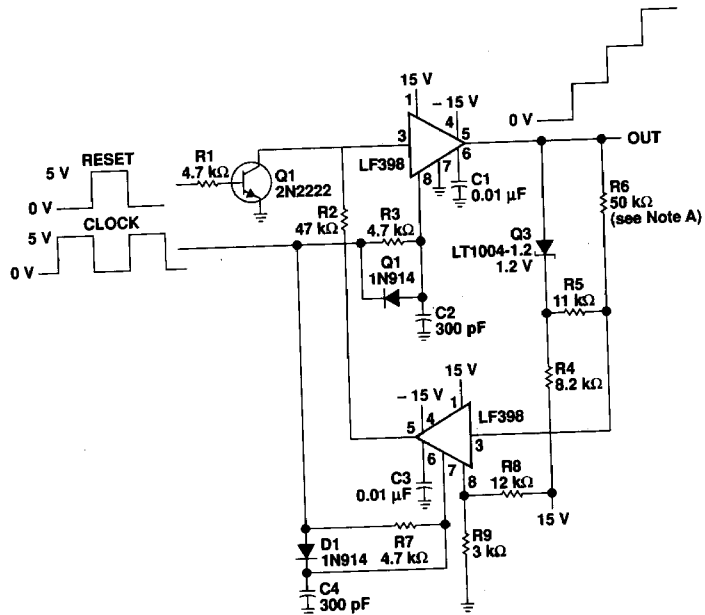


NOTE A: Select  $(R_h)(C_h) \gg \frac{1}{2\pi f_{(MIN)}}$

**FIGURE 32. OUTPUT HOLDS AT AVERAGE OF SAMPLED INPUT**

# LF198, LF198A, LF398, LF398A PRECISION SAMPLE-AND-HOLD AMPLIFIERS

## TYPICAL APPLICATION DATA

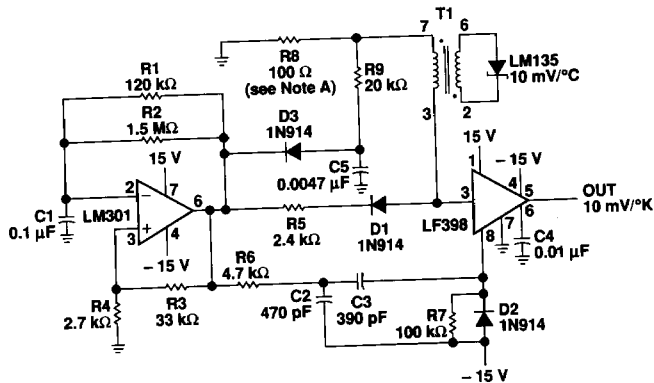


NOTE A: Select R6 for step height.  $50\text{ k}\Omega = 1\text{-V step}$ .

FIGURE 33. STAIRCASE GENERATOR

4

Special Functions

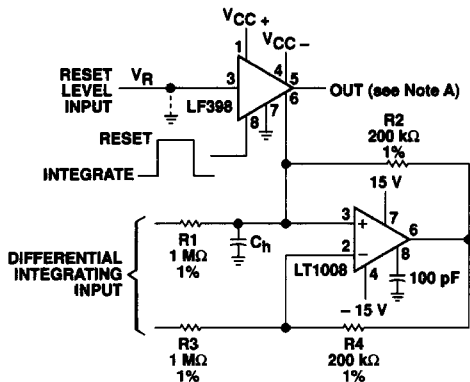


NOTE A: R8 compensates for transformer resistance. Select for flat output from LF198 while in sample mode.

FIGURE 34. ISOLATED TEMPERATURE SENSOR

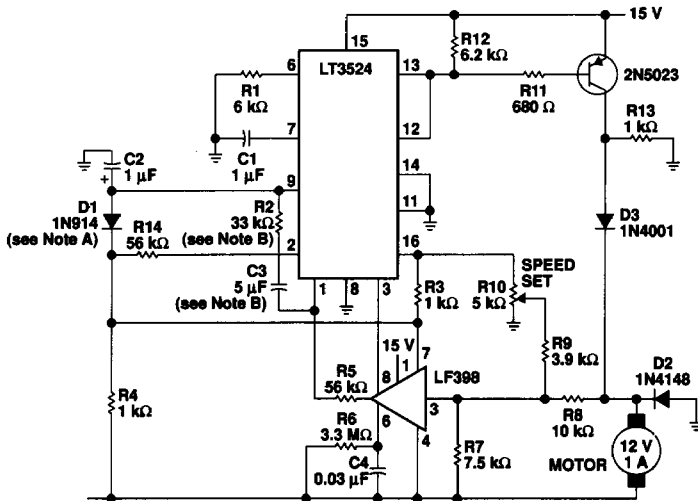


TYPICAL APPLICATION DATA



$$\text{NOTE A: } V_{O(\text{Hold mode})} = \left[ \frac{1}{(R1)(C_H)} \int_0^t V_i dt \right] + V_R$$

FIGURE 35. INTEGRATOR WITH PROGRAMMABLE RESET LEVEL



- NOTES: A. D1 is used for start-up. It limits duty cycle to approximately 75%.  
B. Select for optimum loop stability. C3 is nonpolarized.  
C. No tachometer is needed; back EMF of motor is sampled and used to control speed.

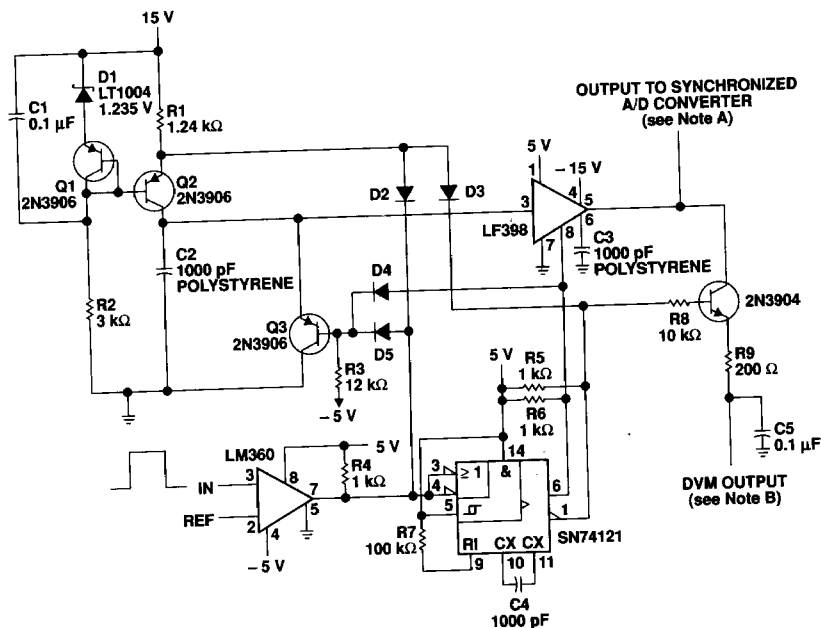
FIGURE 36. MOTOR SPEED CONTROLLER

4

Special Functions

# LF198, LF198A, LF398, LF398A PRECISION SAMPLE-AND-HOLD AMPLIFIERS

## TYPICAL APPLICATION DATA



- NOTES: A. Read  $\geq 1 \mu\text{s}$  after Q goes low.  
 B. For repetitive pulses only. Increase C5 for  $f \leq 10 \text{ kHz}$ .  
 C. D2-D5 1N914.

FIGURE 37. PULSE DURATION TO VOLTAGE CONVERTER

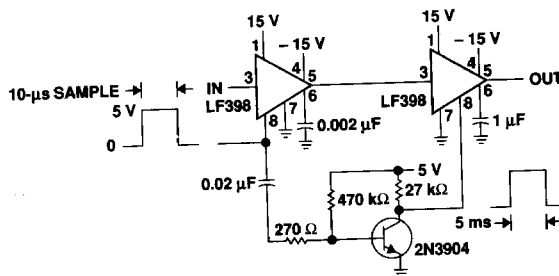


FIGURE 38. FAST-ACQUISITION, LOW-DROOP SAMPLE-AND-HOLD

4

Special Functions