CP2112

SINGLE-CHIP HID USB TO SMBUS MASTER BRIDGE

Single-Chip HID USB to SMBus Master Bridge

- Integrated USB transceiver; no external resistors or crystal required
- SMBus master device
- GPIO can be configured as Input/Output and Open-Drain/Push-Pull
- 512 Byte SMBus data buffer
- Integrated 194 Byte One-Time Programmable ROM for storing customizable product information
- On-chip power-on reset circuit
- On-chip voltage regulator: 3.45 V output

USB Peripheral Function Controller

- USB Specification 2.0 compliant; full-speed (12 Mbps)
- USB Suspend states supported via SUSPEND and SUSPEND pins

HID Interface

- Standard USB class device requires no custom driver
- Windows 7, Vista, XP, Server 2003, 2000
- Win CE 6.0, 5.0, and 4.2
- Mac OS X
- Linux
- Open access to interface specification

Windows and Mac HID-to-SMBus Libraries

- APIs for quick application development
- Supports Windows 7, Vista, XP, Server 2003, 2000
- Supports Mac OS X

SMBus Configuration Options

- Configurable Clock Speed
- Device Address: 7-bit value that is the slave address of the CP2112. The device will only ACK this address, but will not respond to any read/write requests
- Read/Write Timeouts
- SCL Low Timeout
- Retry Counter Timeout

GPIO Interface Features

- 8 GPIO pins with configurable options
- Usable as inputs, open-drain or push-pull outputs
- Configurable clock output for external devices
  - 48 MHz to 94 kHz
- Toggle LED during SMBus reads
- Toggle LED during SMBus writes

Supply Voltage

- Self-powered: 3.0 to 3.6 V
- USB bus powered: 4.0 to 5.25 V
- I/O voltage: 1.8 V to V_{DD}

Ordering Part Number

- CP2112-F02-GM

Package

- RoHS-compliant 24-pin QFN (4 x 4 mm)

Temperature Range: –40 to +85 °C

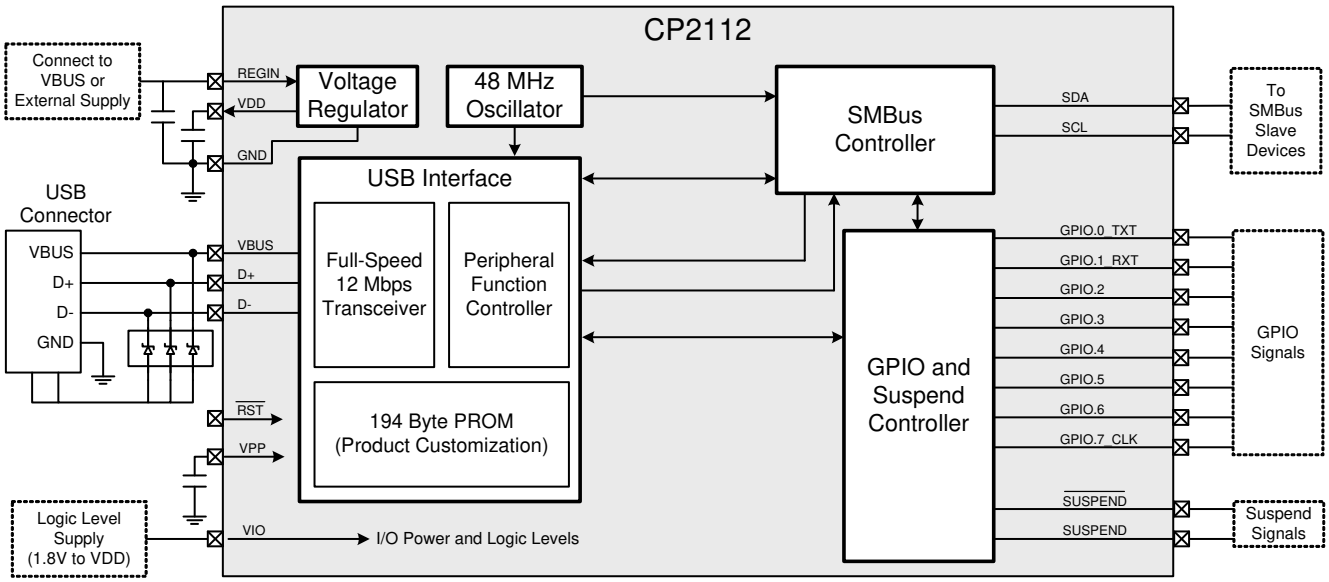

Figure 1. Example System Diagram

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1. System Overview

The CP2112 is a highly-integrated HID USB-to-SMBus Bridge providing a simple solution for controlling SMBus slave devices with USB and using a minimum of components and PCB space. The CP2112 includes a USB 2.0 full-speed function controller, USB transceiver, oscillator, and a one-time programmable ROM in a compact 4 x 4 mm QFN-24 package (sometimes called “MLF” or “MLP”).

The on-chip, one-time programmable ROM provides the option to customize the USB Vendor ID, Product ID, Manufacturer Product String, Product Description String, Power Descriptor, Device Release Number, and Device Serial Number as desired for OEM applications.

The CP2112 uses the standard USB HID device class, which is natively supported by most operating systems. A custom driver does not need to be installed for this device. Windows applications communicate with the CP2112 through a Windows DLL, which is provided by Silicon Labs. The interface specification for the CP2112 is also available to enable development of an API for any operating system that supports HID.

The CP2112 SMBus interface includes the SDA and SCL signals needed for SMBus communication and is configurable. The configurable options include the clock speed, read/write timeouts, retry counter timeout, SCL low timeouts, and a 7-bit device address. The CP2112 will only ACK the 7-bit device address assigned to it but will not respond to any read/write requests. External pull-up resistors are needed for the SCL and SDA signals.

The device also features a total of eight GPIO signals. The GPIO signals are controlled through USB and can be configured as Input/Output and Open-Drain/Push-Pull. Three of the GPIO signals support alternate features including a configurable clock output (48 MHz to 94 kHz) and TX and RX LED toggle. Support for I/O interface voltages down to 1.8 V is provided via a V_{IO} pin.

An evaluation kit for the CP2112 (Part Number: CP2112EK) is available. It includes a CP2112-based HID USB-to-SMBus evaluation board, Windows DLL and test application, USB cable, and full documentation. Go to www.silabs.com for the latest application notes and product support information for the CP2112. Contact a Silicon Labs sales representatives or go to www.silabs.com to order the CP2112 Evaluation Kit.

2. Electrical Characteristics

Table 1. Absolute Maximum Ratings

Parameter	Test Condition	Min	Typ	Max	Unit
Ambient Temperature under Bias		–55	—	125	°C
Storage Temperature		–65	—	150	°C
Voltage on $\overline{RST}$, SDA, SCL, or GPIO Pins with respect to GND	$V_{IO} \geq 2.2$ V $V_{IO} < 2.2$ V	–0.3 –0.3	— —	5.8 V_{IO} + 3.6	V
Voltage on VBUS with respect to GND	$V_{DD} \geq 3.0$ V V_{DD} not powered	–0.3 –0.3	— —	5.8 V_{DD} + 3.6	V
Voltage on V_{DD} or V_{IO} with respect to GND		–0.3	—	4.2	V
Maximum Total Current through V_{DD}, V_{IO}, and GND		—	—	500	mA
Maximum Output Current sunk by $\overline{RST}$ or any I/O pin		—	—	100	mA

Note: Stresses above those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the devices at or exceeding the conditions in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 2. Global DC Electrical Characteristics

V_{DD} = 3.0 to 3.6 V, –40 to +85 °C unless otherwise specified

Parameter	Test Condition	Min	Typ	Max	Unit
Digital Supply Voltage (V_{DD})		3.0	—	3.6	V
Digital Port I/O Supply Voltage (V_{IO})		1.8	—	V_{DD}	V
Voltage on V_{PP} with respect to GND during a ROM programming operation	$V_{IO} \geq 3.3$ V	5.75	—	V_{IO} + 3.6	V
Capacitor on V_{PP} for ROM programming		—	4.7	—	µF
Supply Current[1]	Normal Operation; V_{REG} Enabled	—	15	16	mA
Supply Current[1]	Suspended; V_{REG} Enabled	—	130	230	µA
Supply Current - USB Pull-up[2]		—	200	228	µA
Specified Operating Temperature Range		–40	—	+85	°C

Notes:
1. If the device is connected to the USB bus, the USB pull-up current should be added to the supply current to calculate total required current.
2. The USB pull-up supply current values are calculated values based on USB specifications.

Table 3. SMBus, Suspend I/O DC Electrical Characteristics

V_{DD} = 3.0 to 3.6 V, V_{IO} = 1.8 V to V_{DD}, –40 to +85 °C unless otherwise specified.

Parameter	Test Condition	Min	Typ	Max	Unit
Output High Voltage (V_{OH})	I_{OH} = –10 µA I_{OH} = –3 mA I_{OH} = –10 mA	V_{IO} – 0.1 V_{IO} – 0.2 —	— — V_{IO} – 0.4	— — —	V
Output Low Voltage (V_{OL})	I_{OL} = 10 µA I_{OL} = 8.5 mA I_{OL} = 25 mA	— — —	— — 0.6	0.1 0.4 —	V
Input High Voltage (V_{IH})		0.7 x V_{IO}	—	—	V
Input Low Voltage (V_{IL})		—	—	0.6	V
Input Leakage Current	Weak Pull-Up Off Weak Pull-Up On, V_{IO} = 0 V	— —	— 25	1 50	µA µA
Maximum Input Voltage	Open drain, logic high (1)	—	—	5.8	V

Table 4. Reset Electrical Characteristics

–40 to +85 °C unless otherwise specified

Parameter	Test Condition	Min	Typ	Max	Unit
$\overline{RST}$ Input High Voltage		0.75 x V_{IO}	—	—	V
$\overline{RST}$ Input Low Voltage		—	—	0.6	V
Minimum $\overline{RST}$ Low Time to Generate a System Reset		15	—	—	µs
V_{DD} Ramp Time for Power On		—	—	1	ms

Table 5. Voltage Regulator Electrical Specifications

–40 to +85 °C unless otherwise specified

Parameter	Test Condition	Min	Typ	Max	Unit
Input Voltage Range		3.0	—	5.25	V
Output Voltage	Output Current = 1 to 100 mA*	3.3	3.45	3.6	V
VBUS Detection Input Threshold		2.5	—	—	V
Bias Current		—	—	120	µA
***Note:** The maximum regulator supply current is 100 mA. This includes the supply current of the CP2112.					

Table 6. GPIO Output Specifications

–40 to +85 °C unless otherwise specified

Parameter	Test Condition	Min	Typ	Max	Unit
GPIO.7 Clock Output		Output x 0.985	Output*	Output x 1.015	Hz
TX Toggle Rate		—	10	—	Hz
RX Toggle Rate		—	10	—	Hz
***Note:** The output frequency is configurable from 48 MHz to 94 kHz.					

3. Pinout and Package Definitions

Table 7. CP2112 Pin Definitions

Name	Pin #	Type	Description
V_{DD}	6	Power In Power Out	Power Supply Voltage Input. Voltage Regulator Output. See Section 9.
V_{IO}	5	Power In	I/O Supply Voltage Input.
GND	2		Ground. Must be tied to ground.
$\overline{RST}$	9	D I/O	Device Reset. Open-drain output of internal POR or V_{DD} monitor. An external source can initiate a system reset by driving this pin low for the time specified in Table 4.
REGIN	7	Power In	5 V Regulator Input. This pin is the input to the on-chip voltage regulator.
VBUS	8	D In	VBUS Sense Input. This pin should be connected to the VBUS signal of a USB network.
VPP	16*	Special	Connect a 4.7 µF capacitor between this pin and ground to support ROM programming via the USB interface.
D+	3	D I/O	USB D+
D–	4	D I/O	USB D–
SCL	24	D I/O	Serial Clock signal for SMBus interface.
SDA	1	D I/O	Serial Data signal for SMBus interface.
GPIO.0 TXT	23*	D I/O D Out	This pin is a user-configurable input or output. In TXT mode, this pin is the Transmit Toggle pin and toggles to indicate SMBus transmission. The pin is logic high when a transmission is not in progress.
GPIO.1 RXT	22*	D I/O D Out	This pin is a user-configurable input or output. In RXT mode, this pin is the Receive Toggle pin and toggles to indicate SMBus transmission. The pin is logic high when a transmission is not in progress.
GPIO.2	21*	D I/O	This pin is a user-configurable input or output.
GPIO.3	20*	D I/O	This pin is a user-configurable input or output.
GPIO.4	15*	D I/O	This pin is a user-configurable input or output.
GPIO.5	14*	D I/O	This pin is a user-configurable input or output.
GPIO.6	13*	D I/O	This pin is a user-configurable input or output.
GPIO.7 CLK	12*	D I/O D Out	This pin is a user-configurable input or output. In CLK mode, this pin outputs a clock signal whose frequency is configurable.
***Note:** Pins can be left unconnected when not in use.			

Table 7. CP2112 Pin Definitions (Continued)

Name	Pin #	Type	Description
SUSPEND	11*	D Out	This pin is logic high when the CP2112 is in the USB Suspend state.
$\overline{\text{SUSPEND}}$	17*	D Out	This pin is logic low when the CP2112 is in the USB Suspend state.
NC	18*, 19*		No connect
NC	10*		This pin should be left unconnected of tied to V_{IO}
***Note:** Pins can be left unconnected when not in use.			

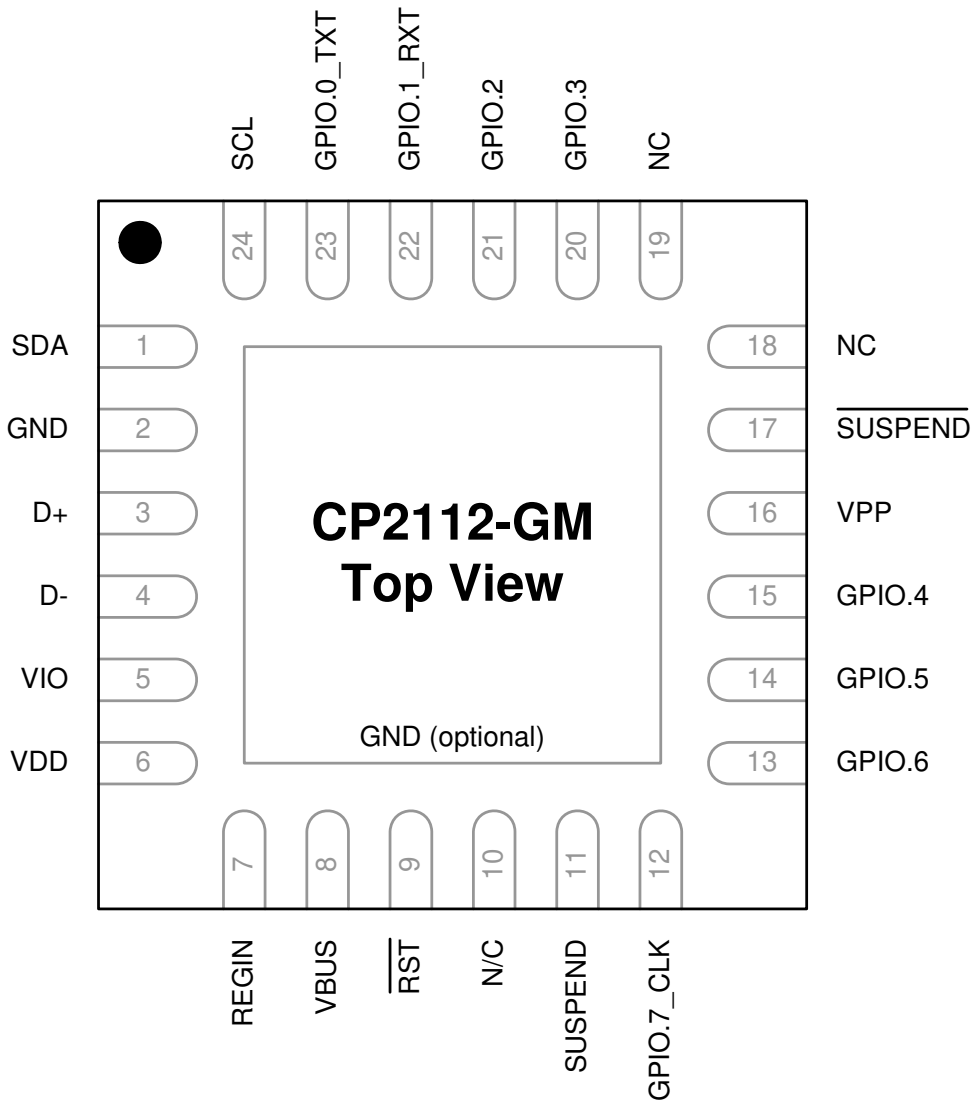


Figure 2. QFN-24 Pinout Diagram (Top View)

4. QFN-24 Package Specifications

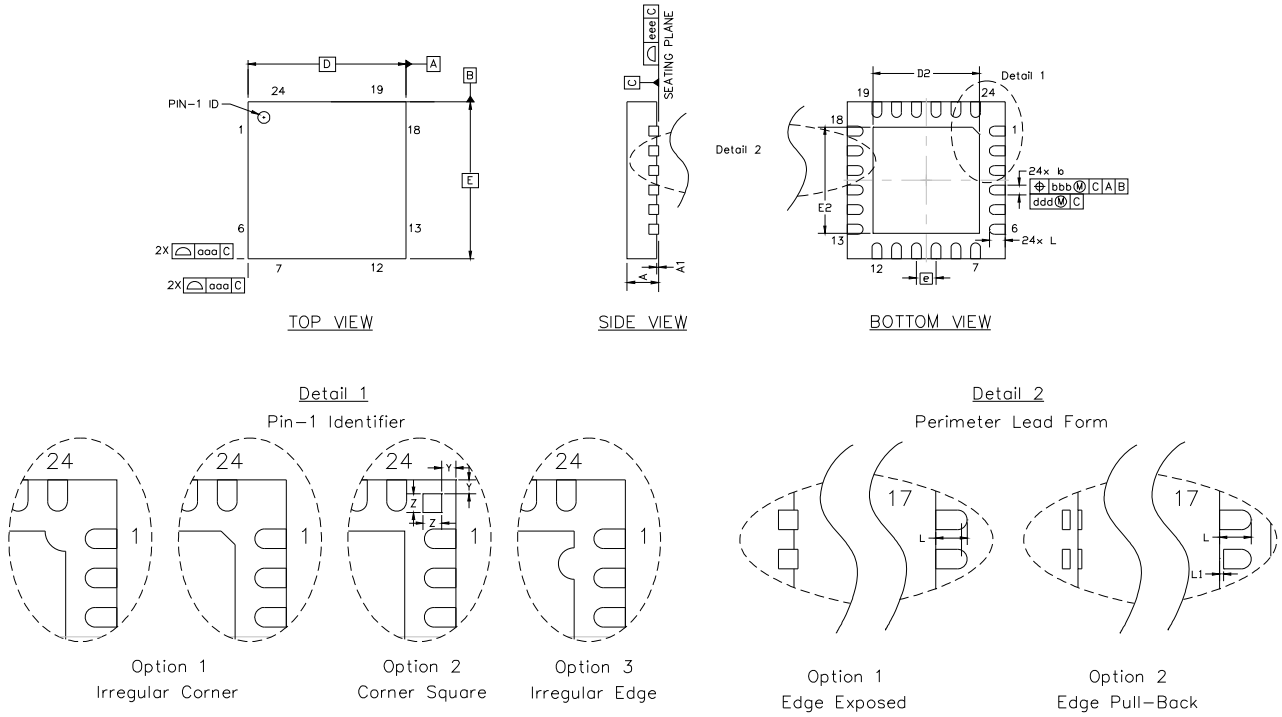


Figure 3. QFN-24 Package Drawing

Table 8. QFN-24 Package Dimensions

Dimension	Min	Typ	Max		Dimension	Min	Typ	Max
A	0.70	0.75	0.80		L	0.30	0.40	0.50
A1	0.00	0.02	0.05		L1	0.00	—	0.15
b	0.18	0.25	0.30		aaa	—	—	0.15
D		4.00 BSC.			bbb	—	—	0.10
D2	2.55	2.70	2.80		ddd	—	—	0.05
e		0.50 BSC.			eee	—	—	0.08
E		4.00 BSC.			Z	—	0.24	—
E2	2.55	2.70	2.80		Y	—	0.18	—

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Solid State Outline MO-220, variation WGGD except for custom features D2, E2, Z, Y, and L which are toleranced per supplier designation.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

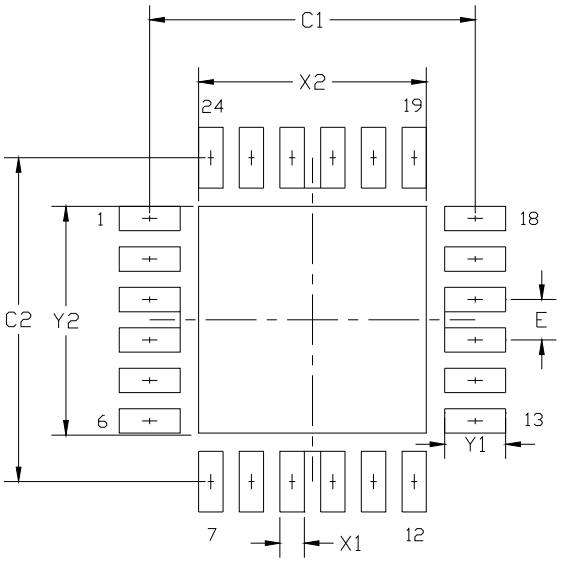


Figure 4. QFN-24 Recommended PCB Land Pattern

Table 9. QFN-24 PCB Land Pattern Dimensions

Dimension	Min	Max	Dimension	Min	Max
C1	3.90	4.00	X2	2.70	2.80
C2	3.90	4.00	Y1	0.65	0.75
E	0.50 BSC		Y2	2.70	2.80
X1	0.20	0.30			

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design

3. All metal pads are to be non-solder-mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A 2x2 array of 1.10 mm x 1.10 mm openings on a 1.30 mm pitch should be used for the center pad.

Card Assembly

8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for small body components.

5. USB Function Controller and Transceiver

The Universal Serial Bus (USB) function controller in the CP2112 is a USB 2.0 compliant full-speed device with integrated transceiver and on-chip matching and pullup resistors. The USB function controller manages all data transfers between the USB and the SMBus interface as well as command requests generated by the USB host controller and commands for controlling the function of the SMBus interface and GPIO pins.

The USB Suspend and Resume modes are supported for power management of both the CP2112 device and external circuitry. The CP2112 enters Suspend mode when Suspend signaling is detected on the bus. Upon entering Suspend mode, the Suspend signals are asserted. The Suspend signals are also asserted after a CP2112 reset until device configuration during USB enumeration is complete. SUSPEND is logic high when the device is in the Suspend state and logic low when the device is in normal mode. The SUSPEND pin has the opposite logic value of the SUSPEND pin.

The CP2112 exits Suspend mode when any of the following events occur: Resume signaling is detected or generated, a USB Reset signal is detected, or a device reset occurs. SUSPEND and SUSPEND are weakly pulled to VIO in a high-impedance state during a CP2112 reset. If this behavior is undesirable, a strong pulldown resistor (10 kΩ) can be used to ensure SUSPEND remains low during reset. The eight GPIO pins will retain their state during Suspend mode.

6. System Management Bus (SMBus) Interface

The SMBus I/O interface is a two-wire, bidirectional serial bus. The SMBus is compliant with the System Management Bus Specification, Version 1.1, and compatible with the I^2C serial bus. Reads and writes to the interface by the system controller are byte-oriented with the SMBus interface autonomously controlling the serial transfer of the data. The CP2112 operates as an SMBus master; however, it has an SMBus slave address that is configurable. The CP2112 will only ACK this address and will not respond to any read or write requests. If the least significant bit of the address is set, the device will ignore it.

6.1. SMBus Configuration

Figure 5 shows a typical SMBus configuration. The SMBus specification allows any recessive voltage between 3.0 V and 5.0 V; different devices on the bus may operate at different voltage levels. The bidirectional serial clock (SCL) and serial data (SDA) lines must be connected to a positive power supply voltage through a pullup resistor or similar circuit. Every device connected to the bus must have an open-drain or open-collector output for both the SCL and SDA lines so that both are pulled high (recessive state) when the bus is free. The maximum number of devices on the bus is limited only by the requirement that the rise and fall times on the bus not exceed 300 ns and 1000 ns, respectively. The SMBus provides control of SDA, SCL generation and synchronization, arbitration logic, and START/STOP control and generation.

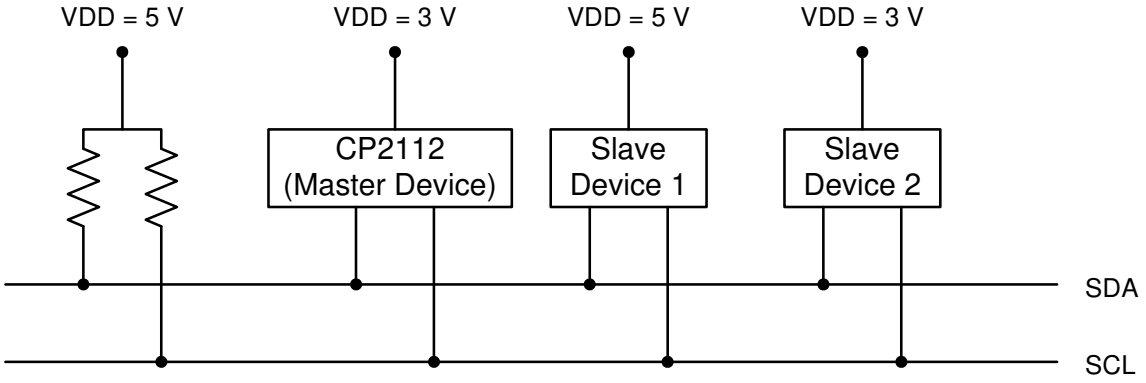


Figure 5. Typical SMBus Configuration

6.2. SMBus Operation

The CP2112 supports reads, writes, and addressed reads. The master device initiates all three types of data transfers and provides the clock pulses on SCL. The SMBus interface on the CP2112 operates as a master, but also has a configurable slave address associated with it that the CP2112 will only ACK upon receiving. Multiple master devices on the same bus are supported. If two or more masters attempt to initiate a data transfer simultaneously, an arbitration scheme is employed with a single master always winning the arbitration. Note that it is not necessary to specify one device as the Master in a system; any device that transmits a START and a slave address becomes the master for the duration of that transfer.

A typical SMBus transaction consists of a START condition followed by an address byte (Bits7–1: 7-bit slave address; Bit0: R/W direction bit), one or more bytes of data, and a STOP condition. Bytes that are received (by a master or slave) are acknowledged (ACK) with a low SDA during a high SCL (see Figures 6, 7, and 8). If the receiving device does not ACK, the transmitting device will read a NACK (not acknowledge), which is a high SDA during a high SCL.

The direction bit (R/W) occupies the least-significant bit position of the address byte. The direction bit is set to logic 1 to indicate a "READ" operation and cleared to logic 0 to indicate a "WRITE" operation. All transactions are initiated by a master, with one or more addressed slave devices as the target. The master generates the START condition and then transmits the slave address and direction bit. If the transaction is a WRITE operation from the master to the slave, the master transmits the data one byte at a time waiting for an ACK from the slave at the end of each byte. For READ operations, the slave transmits the data waiting for an ACK from the master at the end of each byte. At the end of the data transfer, the master generates a STOP condition to terminate the transaction and free the bus. Figure 6 illustrates a typical CP2112 read transaction, and Figure 7 illustrates a typical CP2112 write transaction.

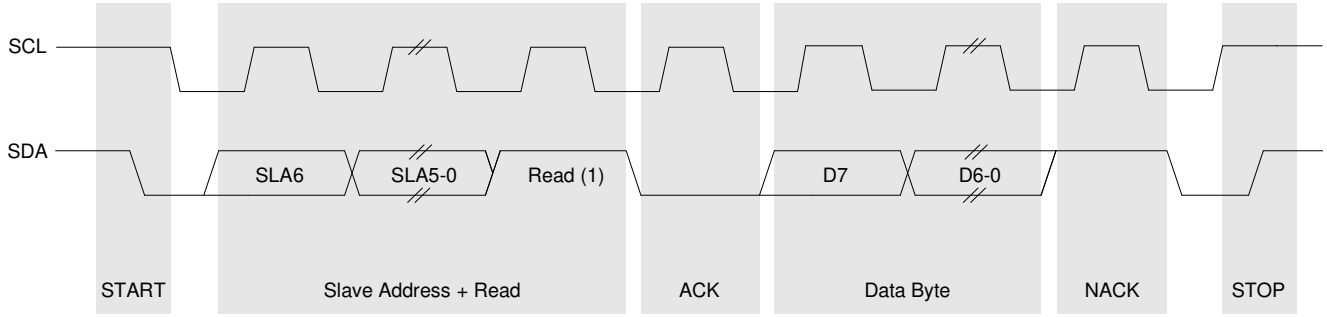


Figure 6. Typical CP2112 Read

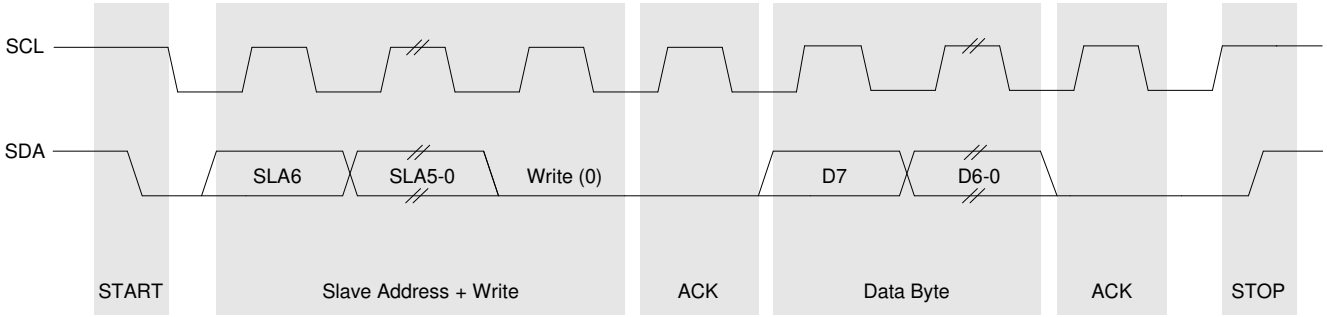


Figure 7. Typical CP2112 Write

The CP2112 performs addressed reads using a repeated start. Addressed Reads are implemented by issuing a START condition followed by a slave address write and logical address. Next the CP2112 issues a repeated START followed by a slave address read. After this sequence, the CP2112 reads bytes from the slave device. The CP2112 supports addressed reads on slave devices with up to a 16 byte logical address field. Figure 8 illustrates a typical addressed read transaction (with a one byte logical address field).

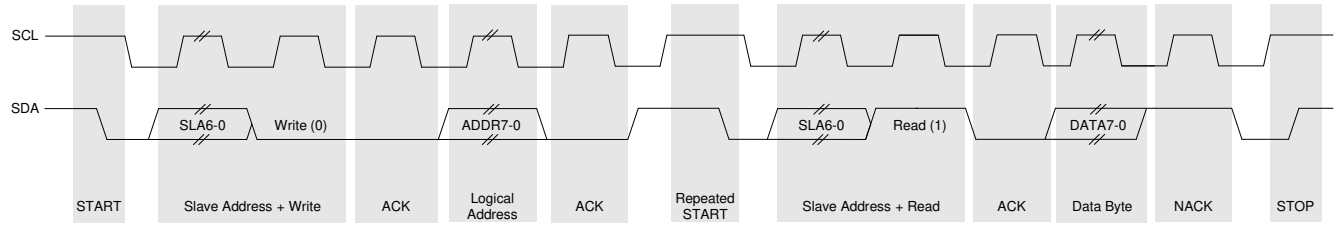


Figure 8. Typical CP2112 Addressed Read

6.3. CP2112 Configuration Options

The CP2112 has the following SMBus configuration options, which are all configured through USB: clock speed, device address, auto send read, read timeout, write timeout, SCL low timeout, and retry time.

- The SMBus clock speed is configurable with a recommended operating range of 10 kHz to 400 kHz.
- The device address is a configurable 7-bit address, which is the slave address of the CP2112. Although the CP2112 is a master device, the CP2112 will ACK this address but will not respond to any read or write requests. If the least significant bit is set, the CP2112 will ignore it.
- If auto read send is set to 0x01, the CP2112 will return the results of a read automatically. If this is set to 0x00, the device will wait for a “data read response” request to respond to data.
- The read and write timeouts are the time limit before the device will automatically cancel a transfer that has been initiated and can range from 0 to 1000 ms. If set to 0 ms, this indicates that there is no timeout.
- The SCL low timeout is either enabled or disabled. If the SCL line is held low by a slave device on the bus, no further communication is possible. Furthermore, the master cannot force the SCL line high to correct the error condition. To solve this problem, the SMBus protocol specifies that devices participating in a transfer must detect any clock cycle held low longer than 25 ms as a “timeout” condition. Devices that have detected the timeout condition must reset the communication no later than 10 ms after detecting the timeout condition.
- The retry time is the number of times the device will attempt a transfer before terminating the transfer. This can be set from 0 to 1000. If set to 0, there is no retry limit.

These configuration options cannot be changed while a transfer is in progress.

7. GPIO Pins

The CP2112 supports 8 user-configurable GPIO pins. Each of these GPIO pins are usable as inputs, open-drain outputs, or push-pull outputs. Three of these GPIO pins also have alternate functions which are listed in Table 10.

Table 10. GPIO Pin Alternate Functions

GPIO Pin	Alternate Function
GPIO.0	TX Toggle
GPIO.1	RX Toggle
GPIO.7	CLK Output

By default, all of the GPIO pins are configured as a GPIO input. The pins must be configured each time the device is reset. For example, if a device is unplugged and then plugged into a PC, the GPIO pins would be configured as inputs and would need to be reconfigured as needed.

The difference between an open-drain output and a push-pull output is when the GPIO output is driven to logic high. A logic high, open-drain output pulls the pin to the VIO rail through an internal, pull-up resistor. A logic high, push-pull output directly connects the pin to the VIO voltage. Open-drain outputs are typically used when interfacing to logic at a higher voltage than the VIO pin. These pins can be safely pulled to the higher, external voltage through an external pull-up resistor. The maximum external pull-up voltage is 5 V.

The speed of reading and writing the GPIO pins is subject to the timing of the USB bus. GPIO pins configured as inputs or outputs are not recommended for real-time signaling.

7.1. GPIO.0-1—Transmit and Receive Toggle

GPIO.0 and GPIO.1 are configurable as Transmit Toggle and Receive Toggle pins. These pins are logic high when a device is not transmitting or receiving data, and they toggle at a fixed rate as specified in Table 6 on page 7 when data transfer is in progress. Typically, these pins are connected to two LEDs to indicate data transfer.

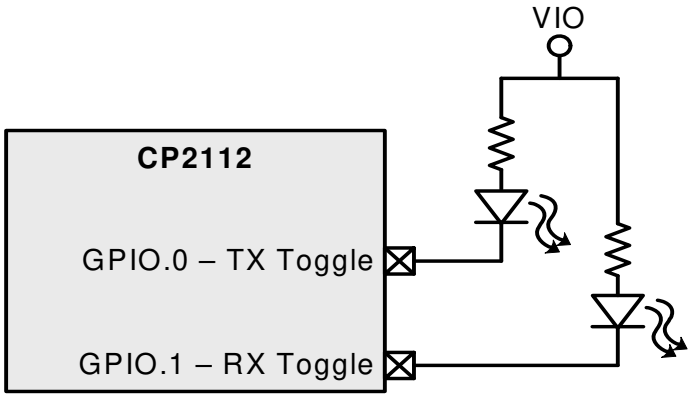


Figure 9. Transmit and Receive Toggle Typical Connection Diagram

7.2. GPIO.7—Clock Output

GPIO.7 is configurable to output a configurable CMOS clock output. The clock output appears at the pin at the same time the device completes enumeration and exits USB Suspend mode. The clock output is removed from the pin when the device enters USB Suspend mode. The output frequency is configurable through the use of a divider and the accuracy is specified in Table 6. When the divider is set to 0, the output frequency is 48 MHz. For divider values between 1 and 255, the output frequency is determined by the formula:

$$\text{GPIO.7 Clock Frequency} = \frac{48\ \text{MHz}}{2 \times \text{ClockDivider}}$$

Equation 1. GPIO.7 Clock Output Frequency

8. One-Time Programmable ROM

The CP2112 includes an internal, one-time programmable ROM that may be used to customize the USB vendor ID (VID), product ID (PID), manufacturer string, product description string, power descriptor, device release number, and device serial number as desired for OEM applications. If the programmable ROM has not been customized, the default configuration data shown in Table 11 is used.

Table 11. Default USB Configuration Data

Name	Value
Vendor ID	10C4h
Product ID	EA90h
Power Descriptor (Attributes)	80h (Bus-powered)
Power Descriptor (Max. Power)	32h (100 mA)
Release Number	0100h (Release Version 01.00)
Manufacturer String	“Silicon Laboratories” (30 ASCII characters maximum)
Product Description String	“CP2112 HID USB-to-SMBus Bridge” (30 ASCII characters maximum)
Serial String	Unique 8-character ASCII string (30 ASCII characters maximum)

While customization of the USB configuration data is optional, customizing the VID/PID combination is strongly recommended. A unique VID/PID will prevent the device from being recognized by any other manufacturer’s software application. A vendor ID can be obtained from www.usb.org, or Silicon Labs can provide a free PID for the OEM product that can be used with the Silicon Labs VID. Customizing the serial string for each individual device is also recommended if the OEM application is one in which it is possible for multiple CP2112-based devices to be connected to the same PC.

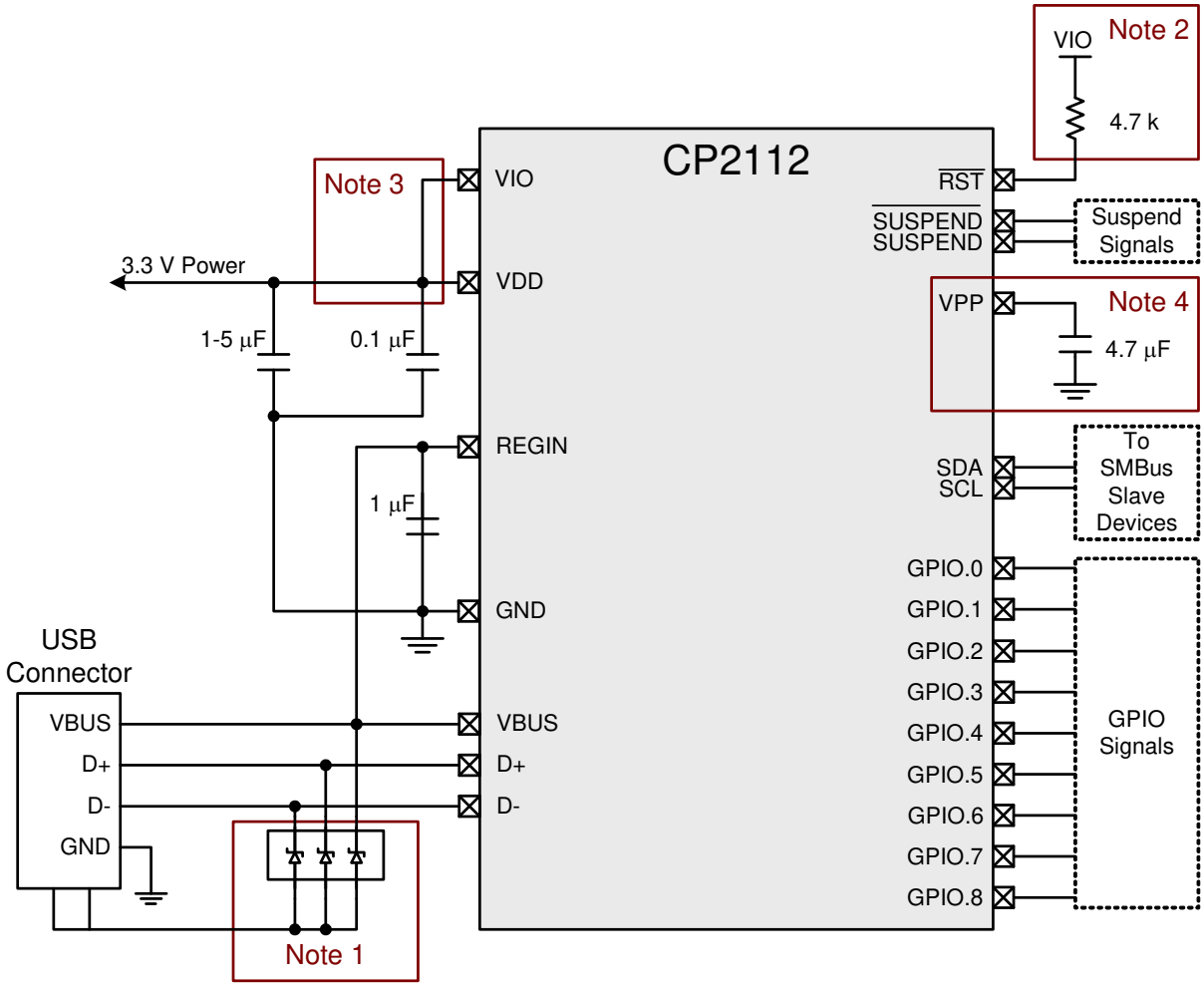
“AN495: CP2112 Interface Specification” includes more information about the programmable values and their valid options. Note that certain items in the PROM are programmed as a group, and programming one of these items in a group prevents further programming of any of the other items in the group.

The configuration data ROM is programmable by Silicon Labs prior to shipment with the desired configuration information. It can also be programmed in-system over the USB interface by adding a capacitor to the PCB. If configuration ROM is to be programmed in-system, a 4.7 µF capacitor must be added between the VPP pin and ground. No other circuitry should be connected to VPP during a programming operation, and V_{DD} must remain at 3.3 V or higher to successfully write to the configuration ROM.

9. Voltage Regulator

The CP2112 includes an on-chip 5.0 to 3.45 V voltage regulator. This allows the CP2112 to be configured as either a USB bus-powered device or a USB self-powered device. A typical connection diagram of the device in a bus-powered application using the regulator is shown in Figure 10. When enabled, the voltage regulator output appears on the V_{DD} pin and can be used to power external devices. See Table 5 for the voltage regulator electrical characteristics.

If the regulator is used to provide V_{DD} in a self-powered application, use the same connections from Figure 10, but connect REGIN to an onboard 5 V supply, and disconnect it from the VBUS pin. In addition, if REGIN may be un-powered while VBUS is 5 V, a resistor divider shown in Note 5 of Figure 11 is required to meet the absolute maximum voltage on VBUS specification in Table 1.

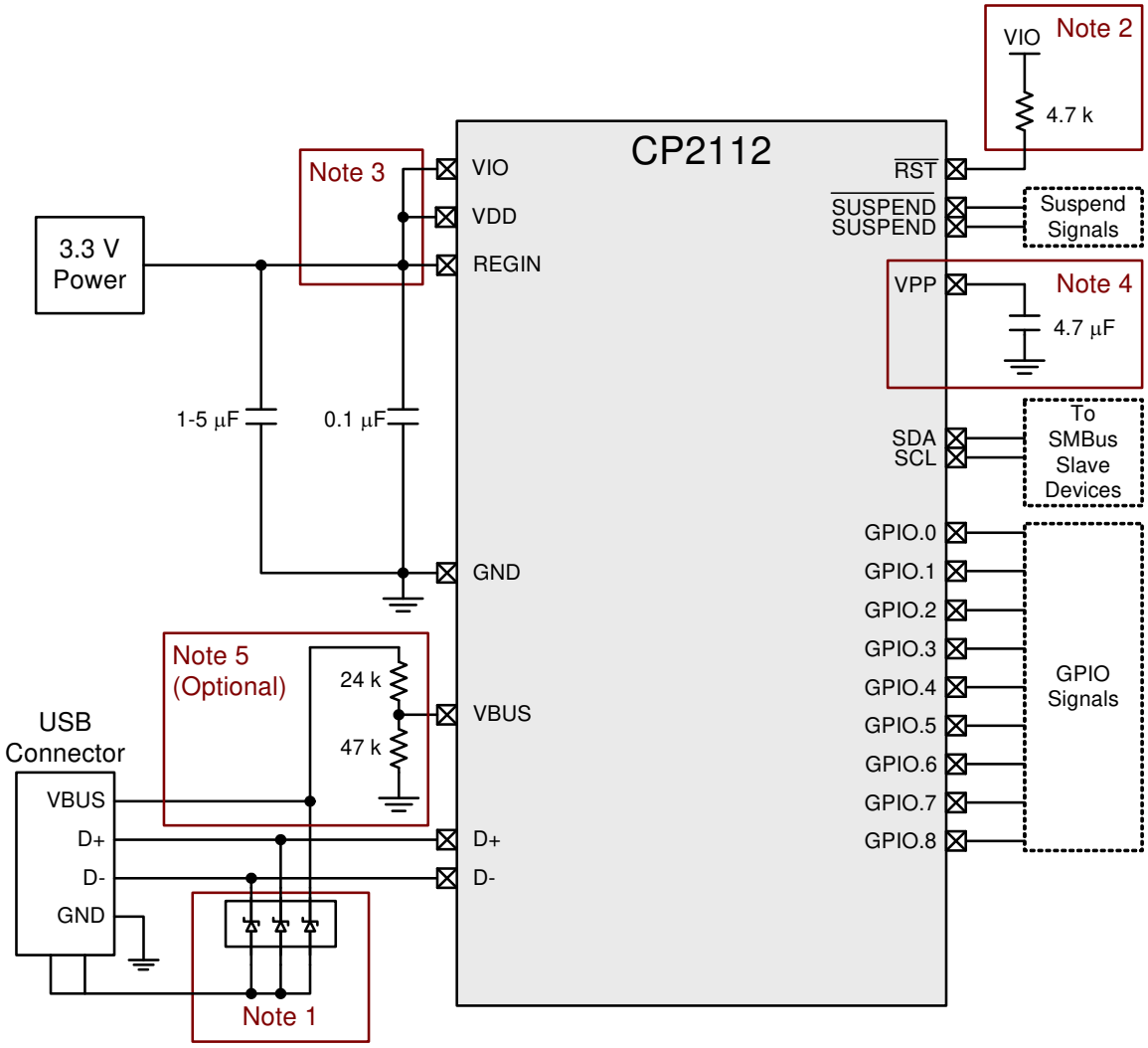


Note 1 : Avalanche transient voltage suppression diodes compatible with Full-speed USB should be added at the connector for ESD protection. Use Littelfuse p/n SP0503BAHT or equivalent.
Note 2 : An external pull-up is not required, but can be added for noise immunity.
Note 3 : VIO can be connected directly to VDD or to a supply as low as 1.8 V to set the I/O interface voltage.
Note 4 : If programming the configuration ROM via USB, add a 4.7 µF capacitor between VPP and ground. During a programming operation, do not connect the VPP pin to other circuitry, and ensure that VDD is at least 3.3 V.

Figure 10. Typical Bus-Powered Connection Diagram

Alternatively, if 3.0 to 3.6 V power is supplied to the V_{DD} pin, the CP2112 can function as a USB self-powered device with the voltage regulator bypassed. For this configuration, tie the REGIN input to V_{DD} to bypass the voltage regulator. A typical connection diagram showing the device in a self-powered application with the regulator bypassed is shown in Figure 11.

The USB max power and power attributes descriptor must match the device power usage and configuration. See the CP2112_SetIDs software included with the CP2112 Software Development Kit (SDK) for information on how to customize USB descriptors for the CP2112.



Note 1 : Avalanche transient voltage suppression diodes compatible with Full-speed USB should be added at the connector for ESD protection. Use Littelfuse p/n SP0503BAHT or equivalent.
Note 2 : An external pull-up is not required, but can be added for noise immunity.
Note 3 : VIO can be connected directly to VDD or to a supply as low as 1.8 V to set the I/O interface voltage.
Note 4 : If programming the configuration ROM via USB, add a 4.7 µF capacitor between VPP and ground. During a programming operation, do not connect the VPP pin to other circuitry, and ensure that VDD is at least 3.3 V.
Note 5 : For self-powered systems where VDD and VIO may be unpowered when VBUS is connected to 5 V, a resistor divider (or functionally-equivalent circuit) on VBUS is required to meet the absolute maximum voltage on VBUS specification in the Electrical Characteristics section.

Figure 11. Typical Self-Powered Connection Diagram (Regulator Bypass)

10. CP2112 Interface Specification and Windows Interface DLL

The CP2112 is a USB Human Interface Device (HID), and, since most operating systems include native drivers, custom drivers do not need to be installed. Because the CP2112 does not fit a standard HID device type, such as a keyboard or mouse, any CP2112 PC application needs to use the CP2112's HID specification to communicate with the device. The low-level HID specification for the CP2112 is provided in "AN495: CP2112 Interface Specification". This document describes all of the basic functions for opening, reading from, writing to, and closing the device, as well as the ROM programming functions.

A Windows DLL that encapsulates the CP2112 HID interface and also adds higher level features, such as read/write timeouts is provided by Silicon Labs. This DLL is the recommended interface for the CP2112. The Windows DLL is documented in *CP2112 Windows DLL Specification*.

Both of these documents and the DLL are available in the CP2112EK CD as well as online at www.silabs.com.

11. Relevant Application Notes and Software

The following Application Notes are applicable to the CP2112. The latest versions of these application notes and their accompanying software are available at www.silabs.com/interface-appnotes.

- AN495: CP2112 Interface Specification—describes how to interface to the CP2112 using the low-level, HID Interface.
- AN496: CP2112 HID USB-to-SMBus API Specification—describes how to interface to the CP2112 using the Windows Interface DLL.

The CP2112 Software Development Kit can be downloaded from www.silabs.com/interface-software. See the CP2112_SetIDs software included with the CP2112 Software Development Kit (SDK) for information on how to customize USB descriptors for the CP2112.

12. Device Specific Behavior

This section describes differences in behavior between the CP2112-F01-GM and the CP2112-F02-GM. The revision of the CP2112 can be read by using the Get Version Information command (Report ID 0x05) or by connecting to a CP2112 device using the HidSmbus Example application. The part number will always be 0x0C (specifying the CP2112 as the device) and the device version will be the revision of the device.

12.1. Addressed Read Requests

In F01 devices, addressed read requests are performed by issuing a start on the bus, followed by a slave address (write), logical address to read, stop, start, and slave address (read).

F02 devices handle addressed read requests by issuing a start on the bus, followed by a slave address (write), logical address to read, repeated start, and slave address (read).

12.2. Multimaster Applications

F01 devices can hold the SDA line low for approximately 3 ms if the Set SMBus Configuration command (Report ID 0x06) is received by one CP2112 master during the middle of a separate master device's transaction. A fix is implemented on F02 devices to eliminate this behavior.

DOCUMENT CHANGE LIST

Revision 0.1 to Revision 0.5

- Updated Table 3 on page 6.
- Updated Table 4 on page 6.
- Updated Table 5 on page 6.
- Updated Table 11 on page 17.

Revision 0.5 to Revision1.0

- Removed preliminary language.

Revision 1.0 to Revision 1.1

- Updated ordering part number.
- Updated "6.2. SMBus Operation" on page 14 to describe SMBus transactions supported by CP2112.
- Updated Figure 6 and added Figures 7 and 8.
- Added "12. Device Specific Behavior" on page 20.

Revision 1.1 to Revision 1.2

- Added a row for VBUS in Table 1, “Absolute Maximum Ratings,” on page 5.
- Added V_{DD} Ramp Time for Power On specification to Table 4, “Reset Electrical Characteristics,” on page 6.
- Added V_{PP} Voltage and Capacitor specifications to Table 2, “Global DC Electrical Characteristics,” on page 5.
- Removed AN144 references.
- Added references to the CP2112_SetIDs software and CP2112 SDK.
- Updated "9. Voltage Regulator" on page 18 to add absolute maximum voltage on VBUS requirements in self-powered systems.

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