

Single-Pole Quad Throw Antenna Tuning Switch

Features

- Designed for high linearity and high RF voltage tuning applications
- Multiple selectable switch configurations: Each throw directly and independently controlled
- Low R_{ON} resistance of 1.6 Ω at each port in ON state
- Low C_{OFF} capacitance of 120 fF at each port in OFF state
- High bidirectional RF operating voltage of 36 V in OFF state
- Low harmonic generation
- 2 GPIO pins control interface
- Supply voltage range: 1.65 to 3.6 V
- No RF parameter change within supply voltage range
- Small form factor 1.1 mm x 1.5 mm (MSL1, 260°C per JEDEC J-STD-020)
- RoHS and WEEE compliant package



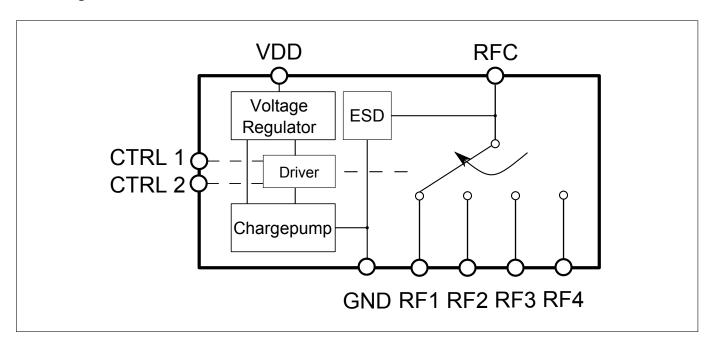
Potential Applications

- Impedance Tuning
- Antenna Tuning
- Inductance Tuning
- Tunable Filters

Product Validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Block Diagram



Single-Pole Quad Throw Antenna Tuning Switch



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Features

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Description

The BGSA14GN10 is a Single Pole Quad Throw (SP4T) RF antenna aperture switch optimized for low C OFF enabling applications up to 6.0 GHz. This single supply chip integrates on-chip CMOS logic driven by a simple, single-pin CMOS or TTL compatible control input signal. Unlike GaAs technology, the 0.1dB compression point exceeds the switch maximum input power level, resulting in linear performance at all signal levels and external DC blocking capacitors at the RF ports are only required if DC voltage is applied externally. Due to its very high RF voltage ruggedness it is suited for switching any reactive devices such as inductors and capacitors in RF matching circuits without significant losses in quality factors.

Product Name	Marking	Package
BGSA14GN10	A4	TSNP-10-1/TSNP-10-2

Single-Pole Quad Throw Antenna Tuning Switch



Maximum Ratings

2 Maximum Ratings

Table 1: Maximum Ratings, Table I at T_A = $25\,^{\circ}$ C, unless otherwise specified

Parameter	Symbol		Value	es	Unit	Note / Test Condition	
		Min.	Тур.	Max.			
Frequency Range	f	0.1	-	T -	GHz	1)	
Supply voltage ²⁾	V_{DD}	-0.5	-	3.6	V	Only for infrequent and short duration time periods	
Storage temperature range	T _{STG}	-55	-	150	°C	-	
RF input power	P _{RF_max}	-	_	39	dBm	Pulsed RF input power, duty cycle of 25 % with T_period= $4620 \mu s$, ON-state, setup as of Fig. 1	
RF voltage	V _{RF_max}	_	_	48	V	Short term peaks (1 μ s, duty cycle 0.1%), Isolation mode, test setup acc. Fig. 2 / Fig. 3 and exceeding typical linearity, R_{ON} and C_{OFF} parameters	
ESD capability, CDM ³⁾	V _{ESD_{CDM}}	-1.5	_	+1.5	kV		
ESD capability, HBM ⁴⁾	$V_{ESD_{HBM}}$	-1	_	+1	kV		
ESD capability, system level (RF port) 5)	V _{ESD_{ANT}}	-8	-	+8	kV	RF vs system GND, with 27 nH shunt inductor	
Junction temperature	T_J	_	-	125	°C	-	
Thermal resistance junction - soldering point	R _{thJS}	_	-	45	K/W	-	
Maximum DC-voltage on RF-Ports and RF- Ground	V_{RFDC}	0	-	0	V	No DC voltages allowed on RF- Ports	
Control Voltage Levels	V _{Ctrlx}	-0.7	-	V _{DD} +0.7 (max. 3.6)	V	-	
Moisture Sensitivity Level	MSL	-	1	-		_	
***	 	!	1		1	<u> </u>	

¹⁾ Switch has a low-pass response. For higher frequencies, losses have to be considered for their impact on thermal heating. The DC voltage at RF ports V_{RFDC} has to be 0.V

Warning: Stresses above the max. values listed here may cause permanent damage to the device. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit. Exposure to conditions at or below absolute maximum rating but above the specified maximum operation conditions may affect device reliability and life time. Functionality of the device might not be given under these conditions.

Note: Consider potential ripple voltages on top of V_{IO} . Including RF ripple, V_{IO} must not exceed the maximum ratings: $V_{Ctrl} = V_{DC} + V_{Ripple}$.

³⁾ Field-Induced Charged-Device Model ANSI/ESDA/JEDEC JS-002. Simulates charging/discharging events that occur in production equipment and processes. Potential for CDM ESD events occurs whenever there is metal-to-metal contact in manufacturing.

⁴⁾ Human Body Model ANSI/ESDA/JEDEC JS-001 ($R = 1.5 \text{ k}\Omega$, C = 100 pF).

⁵⁾ IEC 61000-4-2 ($R = 330 \,\Omega$, $C = 150 \,\mathrm{pF}$), contact discharge.

Single-Pole Quad Throw Antenna Tuning Switch



Maximum Ratings

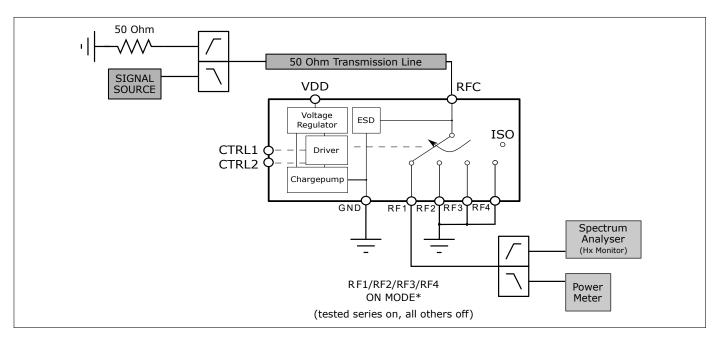


Figure 1: RF operating and Harmonics generation measurement configuration - RFx ON mode

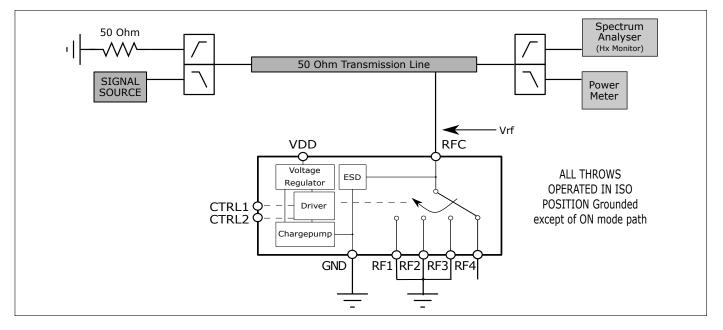


Figure 2: RF operating voltage measurement configuration - OFF mode at RFC

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DC Characteristics

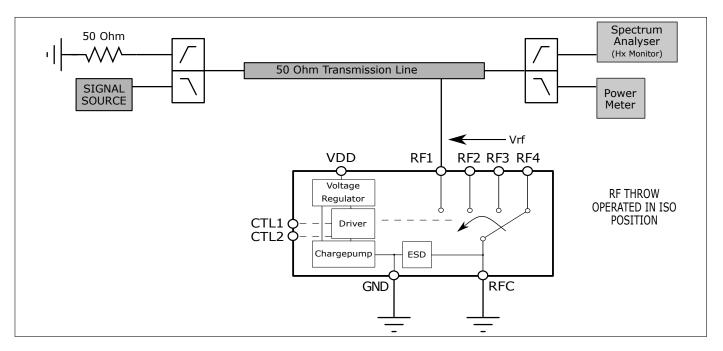


Figure 3: RF operating voltage measurement configuration - OFF mode at RFx

3 DC Characteristics

Table 2: DC Characteristics at $T_A = -40 \,^{\circ}\text{C}$ to 85 $^{\circ}\text{C}$

Parameter	Symbol	Symbol Valu			Unit	Note / Test Condition
		Min.	Тур.	Max.		
Supply voltage	V_{DD}	1.65	2.8	3.6	V	-
Supply current	I _{DD}	_	80	150	μΑ	-
Control voltage low	V _{Ctrl,low}	0	_	0.45	V	-
Control voltage high	V _{Ctrl,high}	1.2	1.8	2.85	V	$V_{Ctrl,high} < V_{DD}$
Control current low	I _{Ctrl,low}	-1	0	1	μΑ	-
Control current high	I _{Ctrl,high}	-1	0	1	μΑ	$V_{Ctrl,high} < V_{DD}$
Ambient temperature	T_A	-40	25	85	°C	-
RF switching time	t _{ST}	2	5	7	μs	P_{IN} = 0 dBm, Z_0 = 50Ω ,
						$T_A = -40 ^{\circ}\text{C} + 85 ^{\circ}\text{C}$
						$V_{DD} = 1.65 - 3.6 V$
Startup time	t _{Pup}	_	20	30	μs	Refering Fig. 4 and Fig. 5

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DC Characteristics

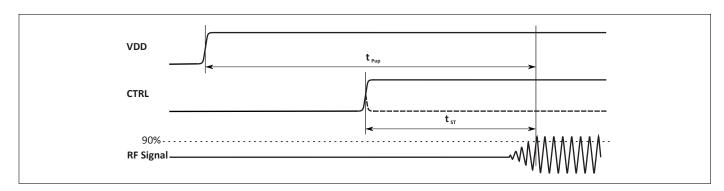


Figure 4: Switching Time Definition

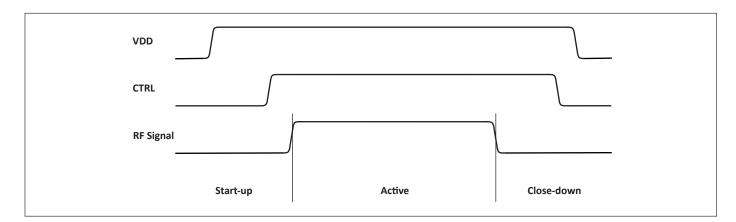


Figure 5: Timing of Control and RF signals for valid operation

Single-Pole Quad Throw Antenna Tuning Switch



RF Small Signal Characteristics

4 RF Small Signal Characteristics

Table 3: RF small signal parameter

Parameter	Symbol		Values		Unit	Note / Test Condition
		Min.	Тур.	Max.		
Frequency range	f	0.1	_	6.0	GHz	-
Switch ON resistance	R _{ON}	_	1.6		Ω	RFx to RFC
Switch OFF capacitance	C _{OFF}	_	120		fF	RFx to RFC
Parasitic RF shunt capacitance	C _{SH,PAR}	_	42		fF	RFx to GND, extracted value for
						2 GHz
Switch series inductance	L _{SER}	_	0.1		nH	
Insertion Loss (1,2)						
600 - 960 MHz		0.15	0.22	0.36	dB	$V_{DD} = 1.65 - 3.6 V,$
1710 - 1980 MHz		0.23	0.37	0.47	dB	$Z_0 = 50 \Omega,$
1980 - 2170 MHz	IL	0.29	0.39	0.49	dB	$T_A = -40 ^{\circ}\text{C} + 85 ^{\circ}\text{C}$
2170 - 2690 MHz		0.36	0.46	0.59	dB	7A - 40 C 1 65 C
Return Loss ^(1,2)						
All Ports @ 600 - 960 MHz	RL	20	22	26	dB	$V_{DD} = 1.65 - 3.6 V,$
All Ports @ 1710 - 2690 MHz	T KL	17	21	25	dB	$Z_0 = 50 \Omega, T_A = -40 ^{\circ}\text{C} + 85 ^{\circ}\text{C}$
Isolation RFx to RFC ^(1,2)						
600 - 960 MHz		29	31	38	dB	
1710 - 1980 MHz	ISO	21	25	35	dB	$V_{DD} = 1.65 - 3.6 V, Z_0 = 50 \Omega,$
1980 - 2170 MHz	130	20	23	35	dB	$T_A = -40 ^{\circ}\text{C} + 85 ^{\circ}\text{C}$
2170 - 2690 MHz		17	20	27	dB	

¹⁾ Valid for all RF power levels, no compression behavior

²⁾On application board without any matching components

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RF large signal parameter

5 RF large signal parameter

Table 4: RF large signal specifications

Parameter	Symbol		Values		Unit	Note / Test Condition	
		Min.	Тур.	Max.			
RF operating voltage	V _{RF_peak}	-			V	All Switch throws operated in isolation Mode, except one throw switched ON with open termination. Test condition schematic in Fig.2. All RF parameters in specs including harmonic distortion	
Harmonic Generation up to 12.7	5 GHz ^(1,2,3)						
All RF Ports - Second Order Harmonics	P _{H2}	-	105	_	dBc	25 dBm, 50 Ω , f_0 = 786 MHz	
All RF Ports - Third Order Harmonics	P _{H3}	-	115	-	dBc	25 dBm, 50 Ω , f_0 = 786 MHz	
All RF Ports - Second Order Harmonics	P _{H2}	-	93	-	dBc	33 dBm, 50Ω , $f_0 = 824$ MHz	
All RF Ports - Third Order Harmonics	P _{H3}	-	94	-	dBc	33 dBm, 50 Ω , f_0 = 824 MHz	
All RF Ports	P _{Hx}	105	_	_	dBc	25 dBm, 50Ω	
Intermodulation Distortion IMD	2 ^(1,2,3)	-	-		<u> </u>	ı	
IIP2, low	IIP2,l	-	110	-	dBm	UD2 diti	
IIP2, high	IIP2,h	_	120	-	dBm	IIP2 conditions table 5	
Intermodulation Distortion IMD	3 ^(1,2,3)						
IIP3	IIP3	_	75	-	dBm	IIP3 conditions table 6	
SV LTE Intermodulation (1,2,3)							
IIP3,SVLTE	IIP3,SV	-	75	-	dBm	SV-LTE conditions table 7	

¹⁾Terminating Port Impedance: $Z_0 = 50 \Omega$

²⁾ Supply Voltage: $V_{DD} = 1.65 - 3.6 V$ ³⁾ On application board without any matching components

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RF large signal parameter

Table 5: IIP2 conditions

Band	In-Band Frequency	Blocker Frequency 1	Blocker Power 1	Blocker Frequency 2	Blocker Power 2
	[MHz]	[MHz]	[dBm]	[MHz]	[dBm]
Band 1 Low	2140	1950	20	190	-15
Band 1 High	2140	1950	20	4090	-15
Band 5 Low	881.5	836.5	20	45	-15
Band 5 High	881.5	836.5	20	1718	-15

Table 6: IIP3 conditions

Band	In-Band Frequency	Blocker Frequency 1	Blocker Power 1	Blocker Frequency 2	Blocker Power 2
	[MHz]	[MHz]	[dBm]	[MHz]	[dBm]
Band 1	2140	1950	20	1760	-15
Band 5	881.5	836.5	20	791.5	-15

Table 7: SV-LTE conditions

Band	In-Band Frequency	Blocker Frequency 1	Blocker Power 1	Blocker Frequency 2	Blocker Power 2
	[MHz]	[MHz]	[dBm]	[MHz]	[dBm]
Band 5	872	827	23	872	14
Band 13	747	786	23	747	14
Band 20	878	833	23	2544	14

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Logic Truth Table

6 Logic Truth Table

Table 8: Modes of Operation

State	Mode	CTRL1	CTRL2
1	RF1 to RFc	0	0
2	RF2 to RFc	0	1
3	RF3 to RFc	1	0
4	RF4 to RFc	1	1

Mapping of Switch Rows to Bit: ON = 1, OFF = 0

Single-Pole Quad Throw Antenna Tuning Switch



Application Information

7 Application Information

Pin Configuration and Function

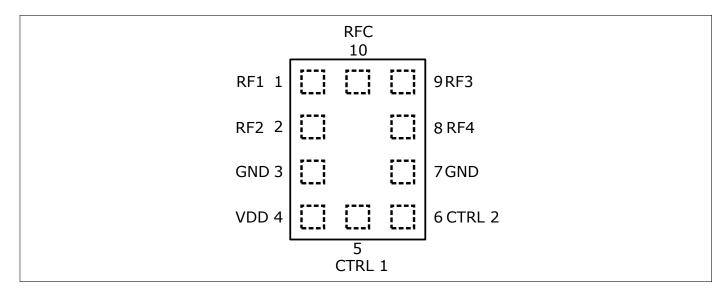


Figure 6: BGSA14GN10 Pin Configuration (top view)

Table 9: Pin Definition and Function

Pin No.	Name	Function
1	RF1	RF1 port
2	RF2	RF2 port
3	GND	Ground
4	VDD	Power Supply
5	CTRL1	GPIO digital control line
6	CTRL2	GPIO digital control line
7	GND	Ground
8	RF4	RF4 port
9	RF3	RF3 port
10	RFC	Common RF



Package Information

Table 10: Mechanical Data

Parameter	Symbol	Value	Unit
X-Dimension	X	1.1 ± 0.05	mm
Y-Dimension	Y	1.5 ± 0.05	mm
Size	Size	2.25	mm²
Height	Н	0.375 +0.025/-0.015	mm

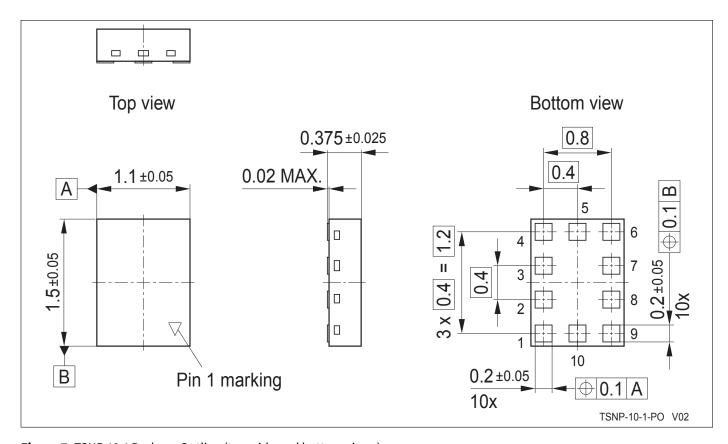


Figure 7: TSNP-10-1 Package Outline (top, side and bottom views)



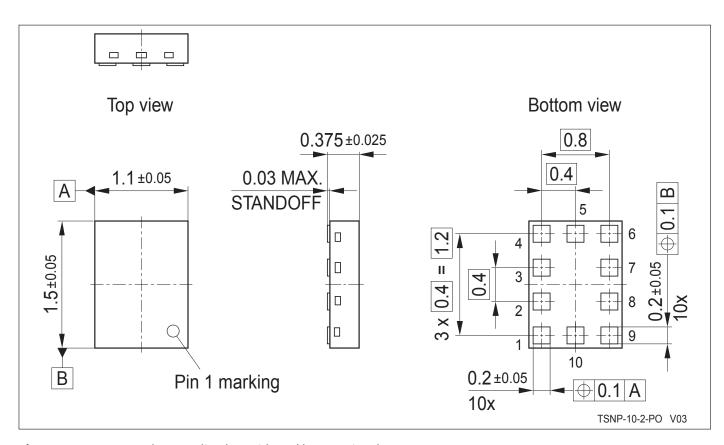


Figure 8: TSNP-10-2 Package Outline (top, side and bottom views)

Single-Pole Quad Throw Antenna Tuning Switch



Table 11: Year date code marking - digit "Y"

			U	_	
Year	"Y"	Year	"Y"	Year	"Y"
2010	0	2020	0	2030	0
2011	1	2021	1	2031	1
2012	2	2022	2	2032	2
2013	3	2023	3	2033	3
2014	4	2024	4	2034	4
2015	5	2025	5	2035	5
2016	6	2026	6	2036	6
2017	7	2027	7	2037	7
2018	8	2028	8	2038	8
2019	9	2029	9	2039	9

Table 12: Week date code marking - digit "W"

			•	•					
Week	"W"								
1	Α	12	N	23	4	34	h	45	V
2	В	13	Р	24	5	35	j	46	x
3	С	14	Q	25	6	36	k	47	у
4	D	15	R	26	7	37	l	48	z
5	E	16	S	27	a	38	n	49	8
6	F	17	T	28	b	39	р	50	9
7	G	18	U	29	С	40	q	51	2
8	Н	19	V	30	d	41	r	52	3
9	J	20	W	31	e	42	S	53	М
10	К	21	Υ	32	f	43	t		
11	L	22	Z	33	g	44	u		

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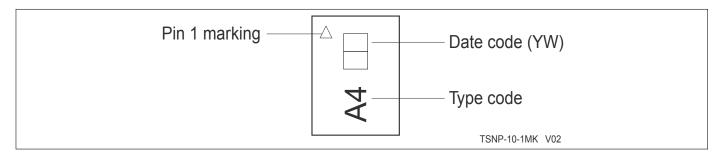


Figure 9: TSNP10-1 Marking Specification (top view): Date code digits Y and W defined in Table 11/12

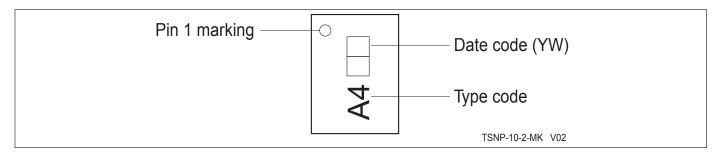


Figure 10: TSNP10-2 Marking Specification (top view): Date code digits Y and W defined in Table 11/12

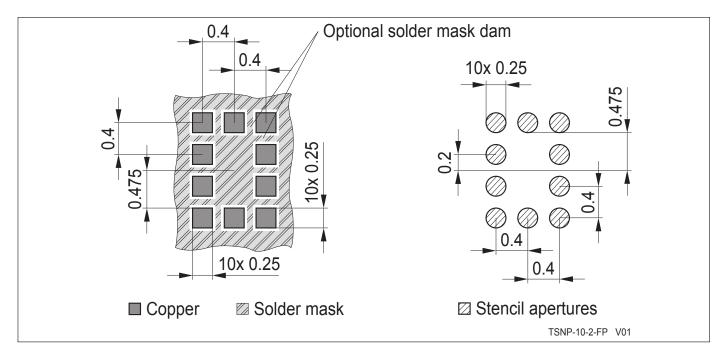


Figure 11: Land pattern and stencil mask (TSNP-10-1/-2)



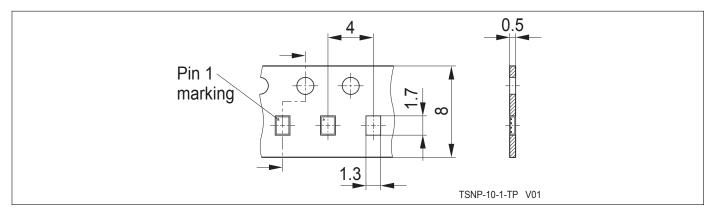


Figure 12: Carrier Tape (TSNP-10-1)

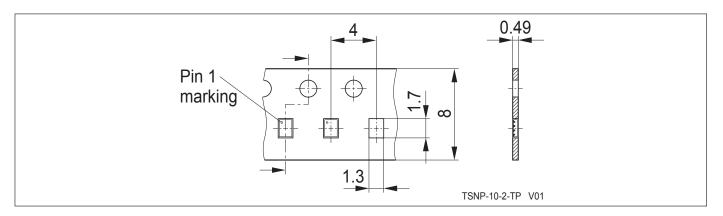


Figure 13: Carrier Tape (TSNP-10-2)

Revision History				
Creation of document Revision 3.1, 2020-07-08				
Page or Item	Subjects (major changes since previous revision)			
5	Typo at max. control current high corrected			

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