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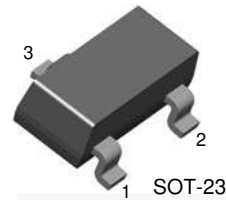
November 2014



BC807 / BC808 PNP Epitaxial Silicon Transistor

Features

- Switching and Amplifier Applications
- Suitable for AF-Driver Stages and Low Power Output Stages
- Complement to BC817 / BC818



1. Base 2. Emitter 3. Collector

Ordering Information

Part Number	Marking	Package	Packing Method
BC80716MTF	9FA	SOT-23 3L	Tape and Reel
BC80725MTF	9FB	SOT-23 3L	Tape and Reel
BC80740MTF	9FC	SOT-23 3L	Tape and Reel
BC80840MTF	9GC	SOT-23 3L	Tape and Reel

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter		Value	Unit
V_{CES}	Collector-Emitter Voltage	BC807	-50	V
		BC808	-30	
V_{CEO}	Collector-Emitter Voltage	BC807	-45	V
		BC808	-25	
V_{EBO}	Emitter-Base Voltage		-5	V
I_C	Collector Current (DC)		-800	mA
T_J	Junction Temperature		150	$^\circ\text{C}$
T_{STG}	Storage Temperature		-65 to +150	$^\circ\text{C}$

BC807 / BC808 — PNP Epitaxial Silicon Transistor

Thermal Characteristics⁽¹⁾

Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Value	Unit
P_D	Power Dissipation	310	mW
	Derate Above 25°C	2.48	mW/ $^\circ\text{C}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	403	$^\circ\text{C}/\text{W}$

Note:

1. PCB size: FR-4, 76 mm x 114 mm x 1.57 mm (3.0 inch x 4.5 inch x 0.062 inch) with minimum land pattern size.

Electrical Characteristics

Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit	
BV_{CEO}	Collector-Emitter Breakdown Voltage	BC807	$I_C = -10\text{ mA}, I_B = 0$	-45			V
		BC808		-25			
BV_{CES}	Collector-Emitter Breakdown Voltage	BC807	$I_C = -0.1\text{ mA}, V_{BE} = 0$	-50			V
		BC808		-30			
BV_{EBO}	Emitter-Base Breakdown Voltage	$I_E = -0.1\text{ mA}, I_C = 0$	-5			V	
I_{CES}	Collector Cut-Off Current	$V_{CE} = -25\text{ V}, V_{BE} = 0$			-100	nA	
I_{EBO}	Emitter Cut-Off Current	$V_{EB} = -4\text{ V}, I_C = 0$			-100	nA	
h_{FE1}	DC Current Gain	$V_{CE} = -1\text{ V}, I_C = -100\text{ mA}$	100		630		
h_{FE2}		$V_{CE} = -1\text{ V}, I_C = -300\text{ mA}$	60				
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$I_C = -500\text{ mA}, I_B = -50\text{ mA}$			-0.7	V	
$V_{BE(on)}$	Base-Emitter On Voltage	$V_{CE} = -1\text{ V}, I_C = -300\text{ mA}$			-1.2	V	
f_T	Current Gain Bandwidth Product	$V_{CE} = -5\text{ V}, I_C = -10\text{ mA}, f = 50\text{ MHz}$		100		MHz	
C_{ob}	Output Capacitance	$V_{CB} = -10\text{ V}, f = 1\text{ MHz}$			12	pF	

h_{FE} Classification

Classification	16	25	40
h_{FE1}	100 ~ 250	160 ~ 400	250 ~ 630
h_{FE2}	60 ~	100 ~	170 ~

Typical Performance Characteristics

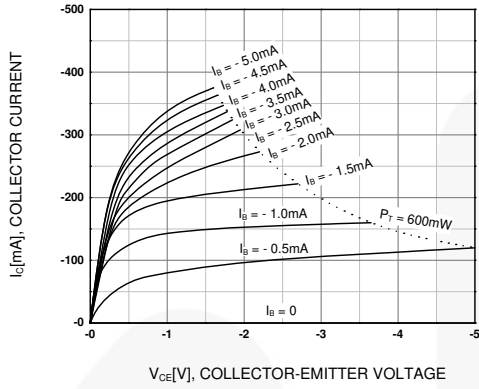


Figure 1. Static Characteristic

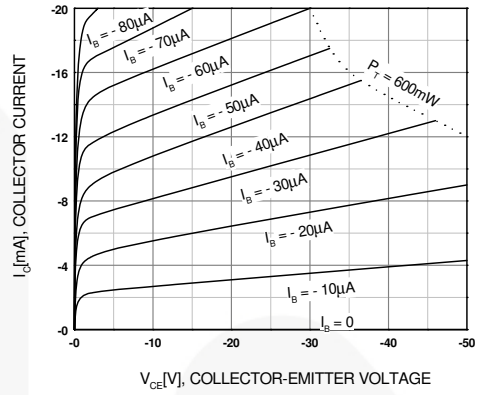


Figure 2. Static Characteristic

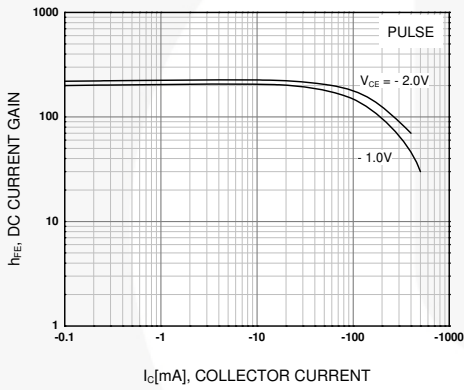


Figure 3. DC Current Gain

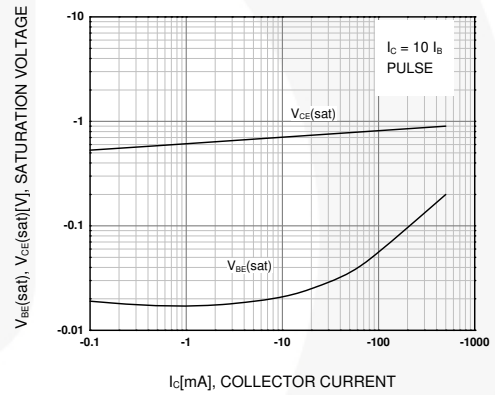


Figure 4. Base-Emitter Saturation Voltage and Collector-Emitter Saturation Voltage

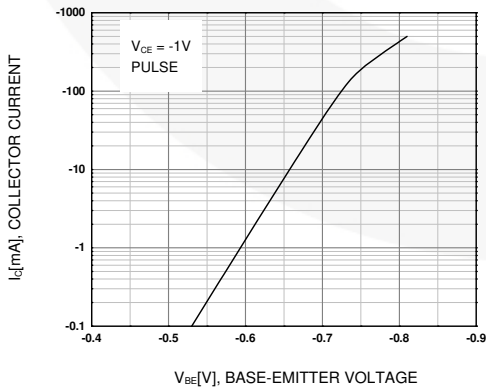


Figure 5. Base-Emitter On Voltage

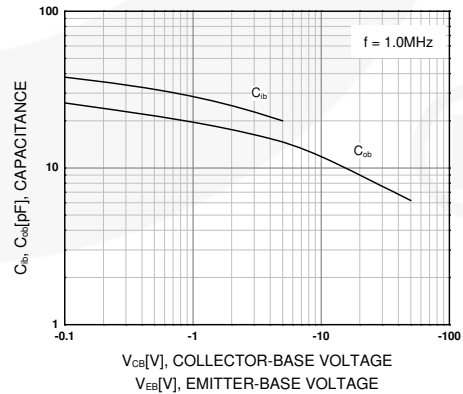


Figure 6. Input Output Capacitance

Typical Performance Characteristics (Continued)

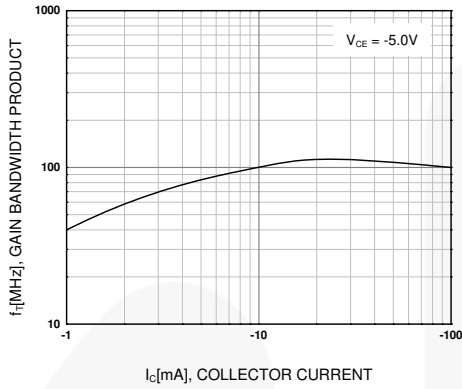
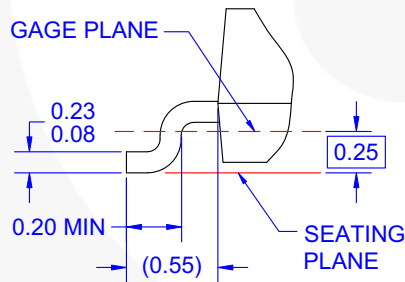
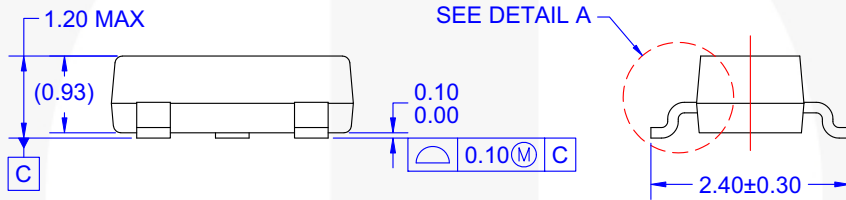
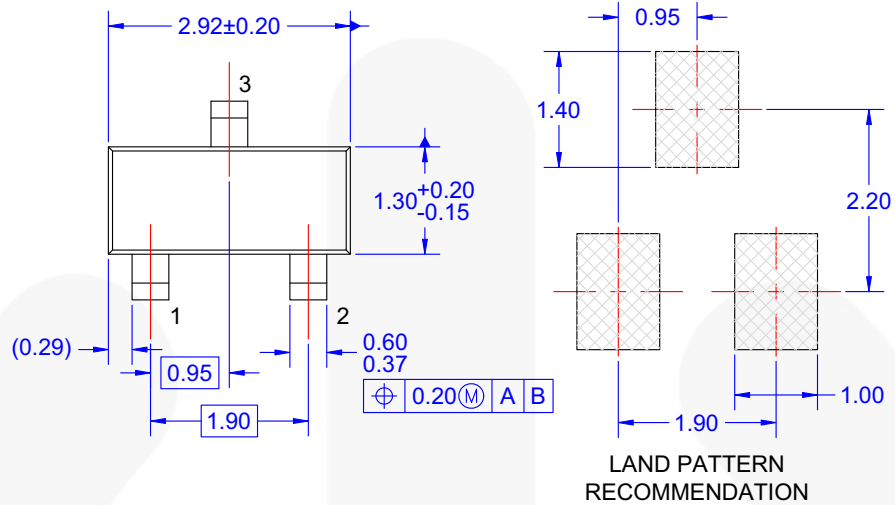


Figure 7. Current Gain Bandwidth Product



Physical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

- A) REFERENCE JEDEC REGISTRATION TO-236, VARIATION AB, ISSUE H.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS ARE INCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M - 1994.
- E) DRAWING FILE NAME: MA03DREV10






DETAIL A
SCALE: 2X

Figure 8. 3-LEAD, SOT23, JEDEC TO-236, LOW PROFILE



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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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