IS31AP4088D

DUAL 2.6W STEREO AUDIO AMPLIFIER

September 2021

GENERAL DESCRIPTION

The IS31AP4088D is a dual bridge-connected audio power amplifier which, when connected to a 5V supply, will deliver 2.6W to a 4Ω load.

The IS31AP4088D features a low-power consumption shutdown mode and thermal shutdown protection. It also utilizes circuitry to reduce “clicks-and-pop” during device turn-on.

APPLICATIONS

- Cell phones, PDA, MP4,PMP
- Portable and desktop computers
- Desktops audio system
- Multimedia monitors

KEY SPECIFICATIONS

- P_O at 1% THD+N, V_{CC} = 5V
  R_L = 4Ω ---------- 2.1W (Typ.)
  R_L = 8Ω---------- 1.3W (Typ.)
- P_O at 10% THD+N, V_{CC} = 5V
  R_L = 4Ω ---------- 2.6W (Typ.)
  R_L = 8Ω ---------- 1.6W (Typ.)
- P_O at 1% THD+N, V_{CC} = 4V
  R_L = 4Ω ---------- 1.4W (Typ.)
  R_L = 8Ω ---------- 0.81W (Typ.)
- Shutdown current ---------- 0.1μA (Typ.)
- Supply voltage range ---------- 2.7V ~ 5.5V
- QFN-16 (4mm × 4mm) package

FEATURES

- Suppress “click-and-pop”
- Thermal shutdown protection circuitry
- Micro power shutdown mode

TYPICAL APPLICATION CIRCUIT

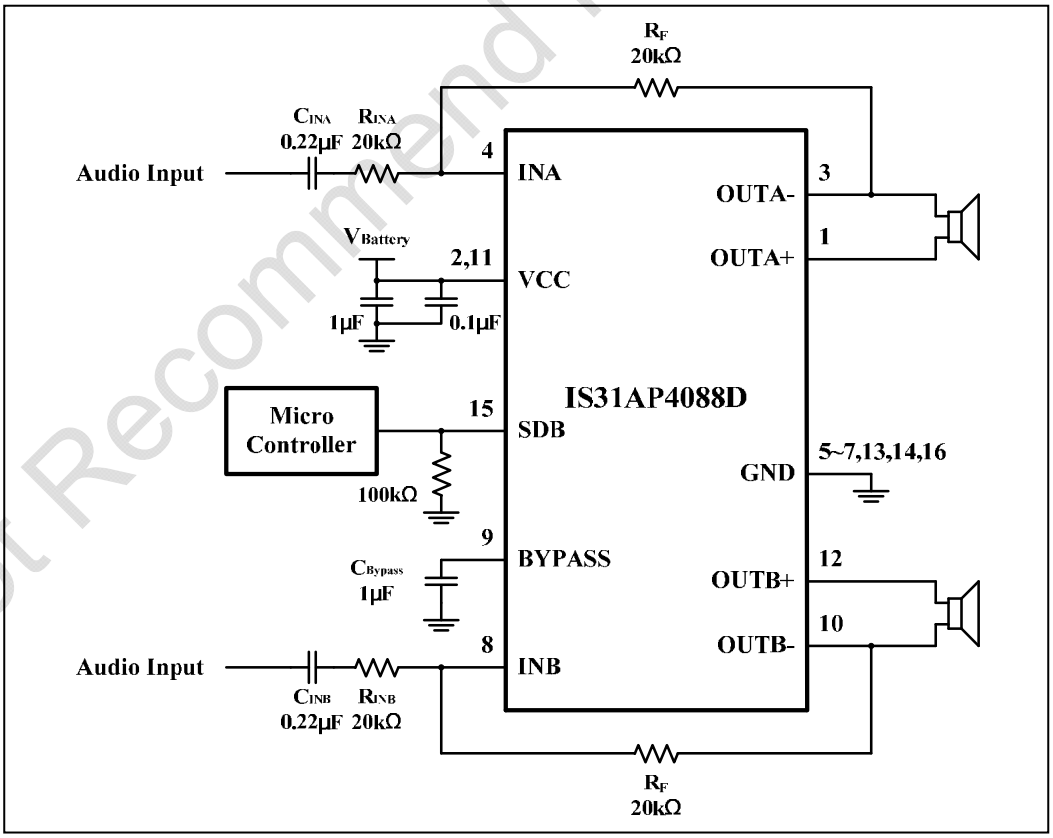
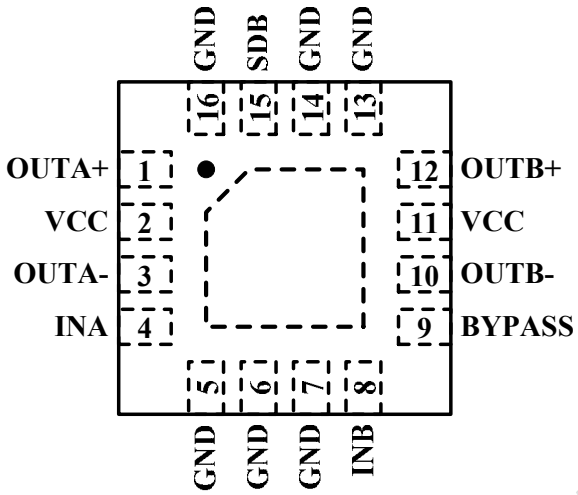


Figure 1 Typical Audio Amplifier Application Circuit

PIN CONFIGURATION

Package	Pin Configuration (Top View)
QFN-16	

PIN DESCRIPTION

No.	Pin	Description
1	OUTA+	Left channel +output.
2,11	VCC	Supply voltage.
3	OUTA-	Left channel –output.
4	INA	Left channel input.
5~7,13,14,16	GND	Ground.
8	INB	Right channel input.
9	BYPASS	Bypass capacitor which provides the common mode voltage.
10	OUTB-	Right channel –output.
12	OUTB+	Right channel +output.
15	SDB	Shut down control, hold low for shutdown mode.
	Thermal Pad	Connect to GND.

ORDERING INFORMATION

Industrial Range: -40°C to +85°C

Order Part No.	Package	QTY/Reel
IS31AP4088D-QFLS2-TR	QFN-16, Lead-free	2500

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	-0.3V ~ +6.0V
Voltage at any input pin	-0.3V ~ V_{CC}+0.3V
Maximum junction temperature, T_{JMAX}	+150°C
Storage temperature range, T_{STG}	-65°C ~ +150°C
Operating temperature range, T_A	-40°C ~ +85°C
ESD (HBM) ESD (CDM)	±1kV ±1kV

Note: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

The following specifications apply for V_{CC} = 5V, unless otherwise noted. Limits apply for T_A = 25°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		2.7		5.5	V
I_{CC}	Quiescent power supply current	V_{IN} = 0V, I_O = 0A		4.5	10.5	mA
I_{SD}	Shutdown current	GND applied to the shutdown pin		0.1	2.5	μA
V_{IH}	Shutdown input voltage high		1.4			V
V_{IL}	Shutdown input voltage low				0.4	V
t_{WU}	Turn on time	C_{Bypass} = 1μF		120		ms

ELECTRICAL CHARACTERISTICS OPERATION

The following specifications apply for V_{CC} = 5V, unless otherwise noted. Limits apply for T_A = 25°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{OS}	Output offset voltage	V_{IN} = 0V		5	25	mV
P_O	Output power	THD+N = 1%, f = 1kHz, R_L= 8Ω	1.15	1.3		W
		THD+N = 10%, f = 1kHz, R_L = 8Ω	1.45	1.6		W
		THD+N = 1%, f = 1kHz, R_L = 4Ω	1.95	2.1		W
		THD+N = 10%, f = 1kHz, R_L = 4Ω	2.45	2.6		W
THD+N	Total harmonic distortion +noise	f = 1kHz, A_V = 2, R_L = 8Ω, P_O = 1W		0.1		%
PSRR	Power supply rejection ratio	Input floating, 217Hz, V_{Ripple} = 200mV_{p-p} C_{Bypass} = 1μF, R_L = 8Ω		80		dB
		Input floating 1kHz, V_{Ripple} = 200mV_{p-p} C_{Bypass} = 1μF, R_L = 8Ω		70		dB
		Input GND 217Hz, V_{Ripple} = 200mV_{p-p} C_{Bypass} = 1μF, R_L =8Ω		60		dB
		Input GND 1kHz V_{Ripple} = 200mV_{p-p} C_{Bypass} = 1μF, R_L = 8Ω		60		dB
X_{Talk}	Channel separation	f = 1kHz, C_{Bypass} = 1μF	-100			dB
V_{NO}	Output noise voltage	1kHz, A-weighted		7		μV

ELECTRICAL CHARACTERISTICS

The following specifications apply for V_{CC} = 3V, unless otherwise noted. Limits apply for T_A = 25°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{CC}	Quiescent power supply current	V_{IN} = 0V, I_O = 0A		3.8		mA
I_{SD}	Shutdown current	GND applied to the shutdown pin		0.1		μA
V_{IH}	Shutdown input voltage high		1.1			V
V_{IL}	Shutdown input voltage low				0.4	V
t_{WU}	Turn on time	C_{Bypass} = 1μF		110		ms

ELECTRICAL CHARACTERISTICS OPERATION

The following specifications apply for V_{CC} = 3V, unless otherwise noted. Limits apply for T_A = 25°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{OS}	Output offset voltage	V_{IN} = 0V		2.5		mV
Po	Output power	THD+N = 1%, f = 1kHz, R_L= 8Ω		0.45		W
		THD+N = 10%, f = 1kHz, R_L = 8Ω		0.56		W
		THD+N = 1%, f = 1kHz, R_L = 4Ω		0.74		W
		THD+N = 10%, f = 1kHz, R_L = 4Ω		0.9		W
THD+N	Total harmonic distortion+noise	f = 1kHz, A_V = 2, R_L = 8Ω, P_O = 0.3W		0.18		%
PSRR	Power supply rejection ratio	Input floating, 217Hz, V_{Ripple} = 200mV_{p-p} C_{Bypass} = 1μF, R_L = 8Ω		75		dB
		Input floating 1kHz, V_{Ripple} = 200mV_{p-p} C_{Bypass} = 1μF, R_L = 8Ω		70		dB
		Input GND 217Hz, V_{Ripple} = 200mV_{p-p} C_{Bypass} = 1μF, R_L =8Ω		60		dB
		Input GND 1kHz V_{Ripple} = 200mV_{p-p} C_{Bypass} = 1μF, R_L = 8Ω		62		dB
X_{Talk}	Channel separation	f = 1kHz, C_{Bypass} = 1μF		-100		dB
V_{NO}	Output noise voltage	1kHz, A-weighted		7		μV

TYPICAL PERFORMANCE CHARACTERISTICS

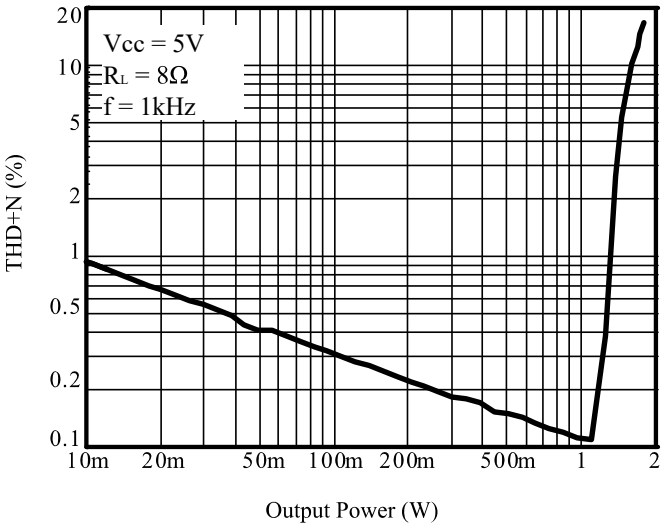


Figure 2 THD+N vs. Output Power

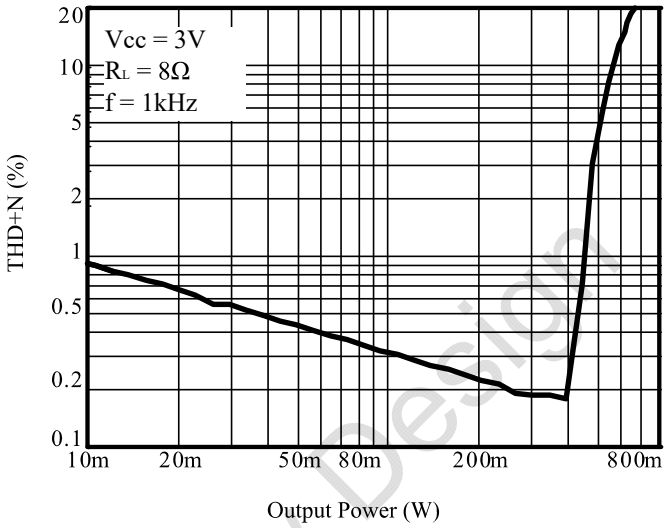


Figure 3 THD+N vs. Output Power

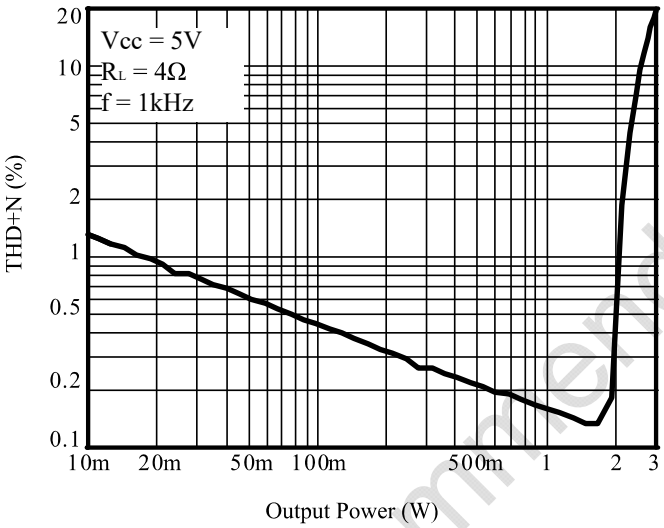


Figure 4 THD+N vs. Output Power

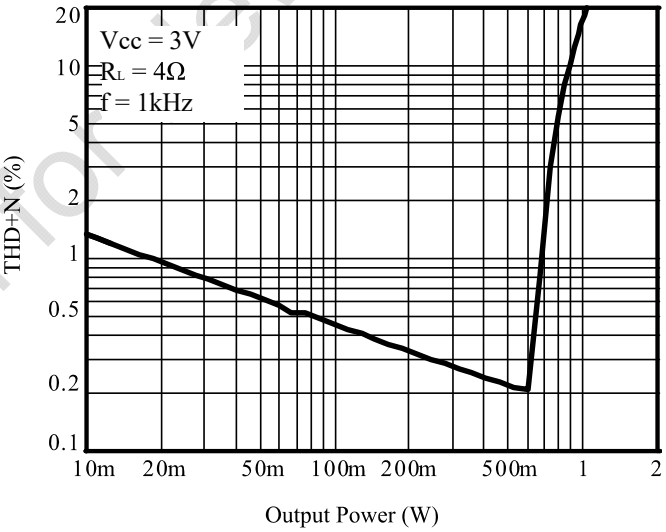


Figure 5 THD+N vs. Output Power

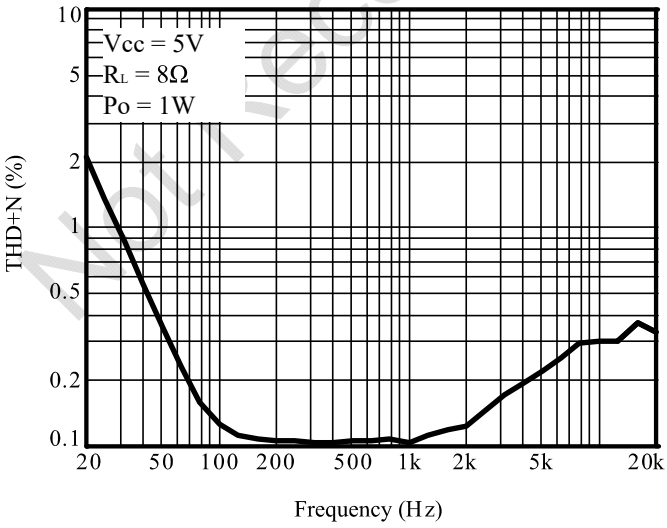


Figure 6 THD+N vs. Frequency

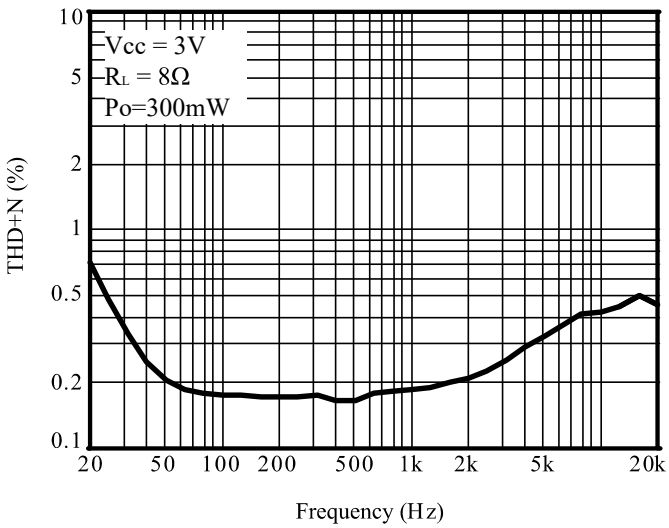


Figure 7 THD+N vs. Frequency

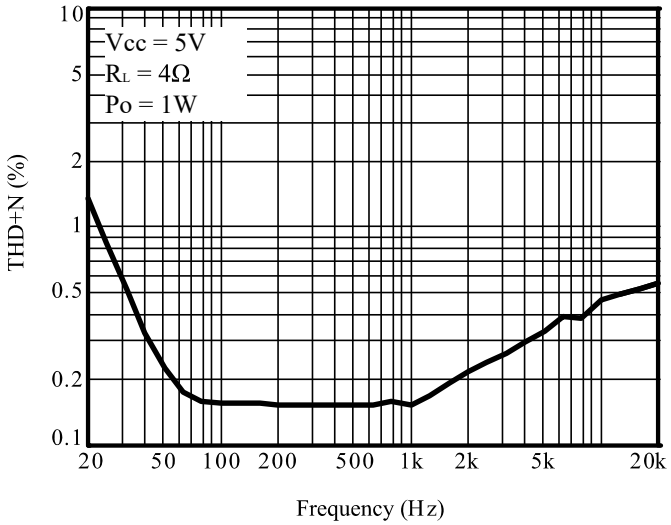


Figure 8 THD+N vs. Frequency

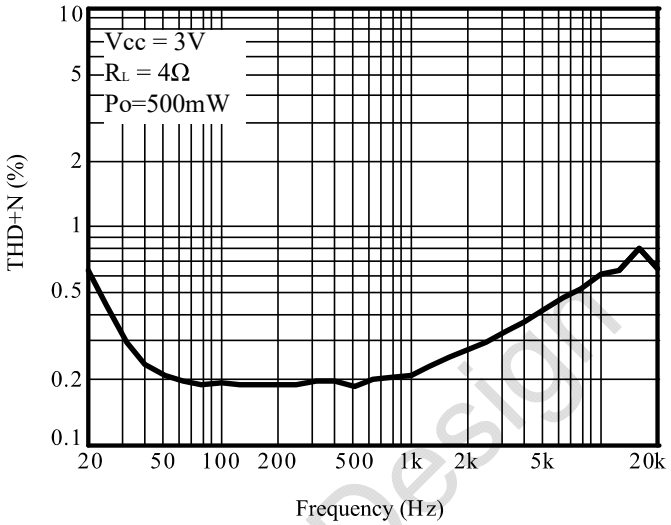


Figure 9 THD+N vs. Frequency

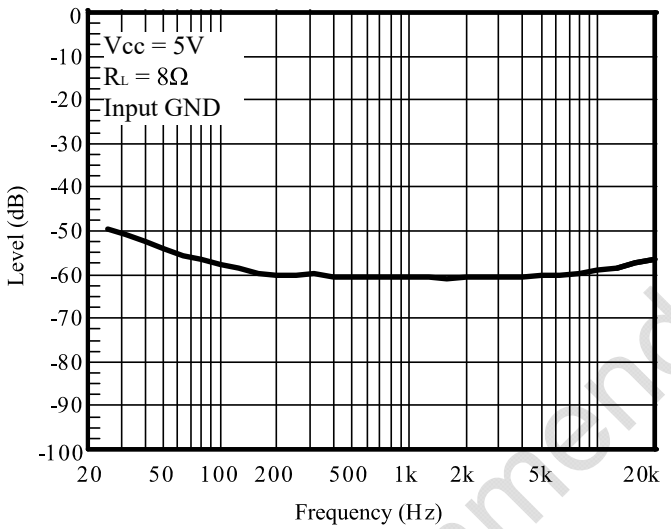


Figure 10 PSRR vs. Frequency

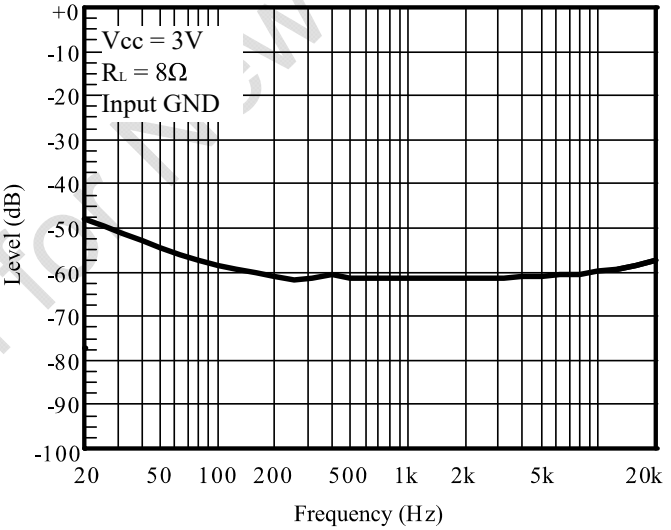


Figure 11 PSRR vs. Frequency

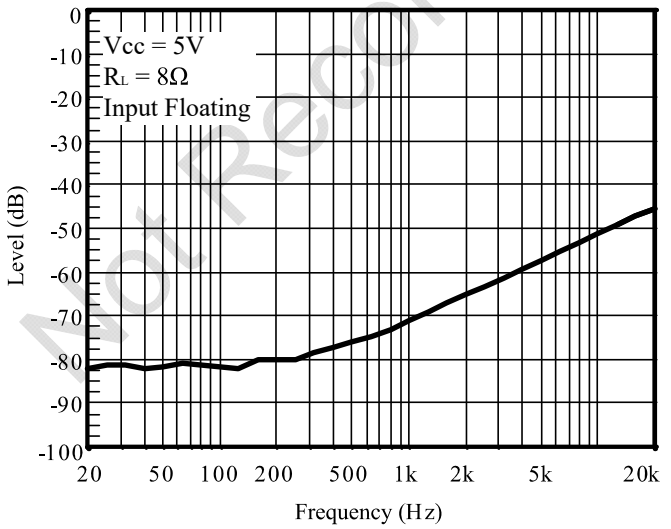


Figure 12 PSRR vs. Frequency

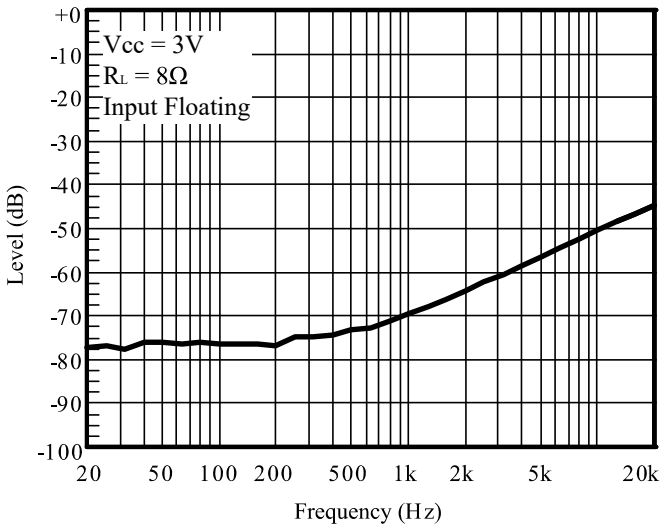


Figure 13 PSRR vs. Frequency

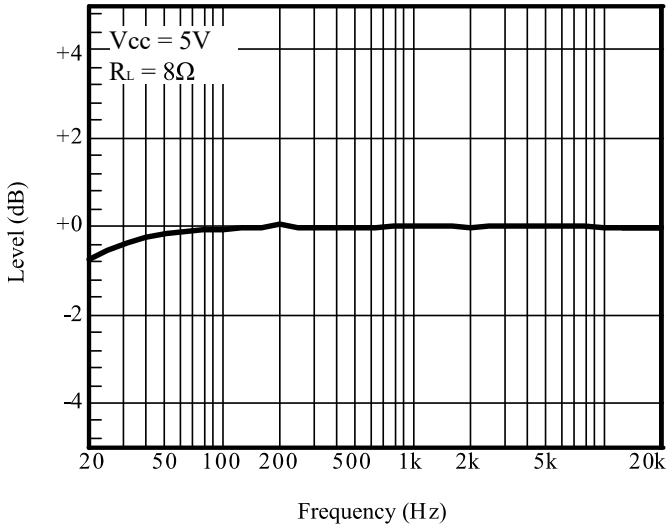


Figure 14 Frequency Response

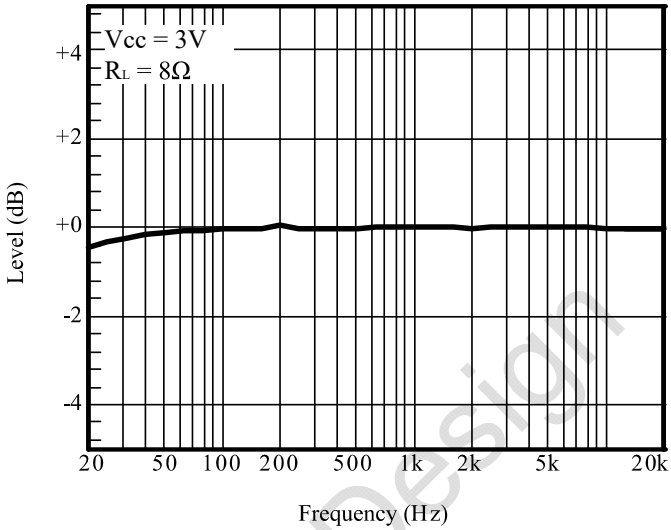


Figure 15 Frequency Response

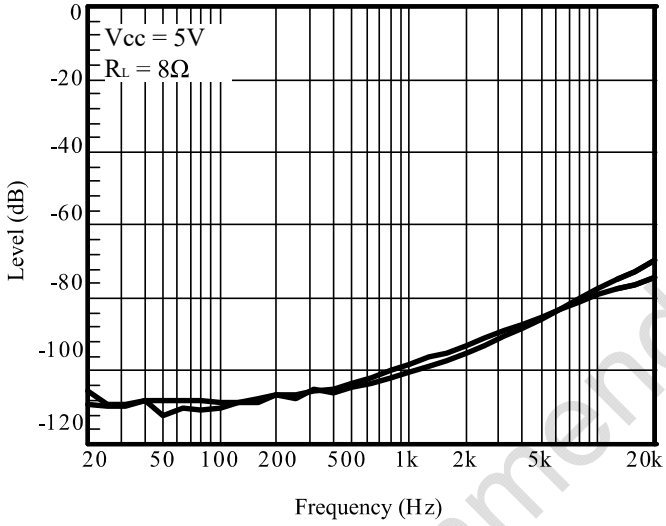


Figure 16 Crosstalk vs. Frequency

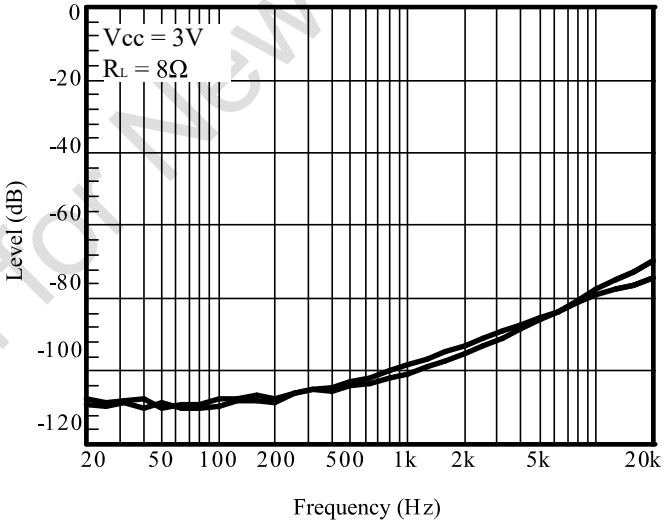


Figure 17 Crosstalk vs. Frequency

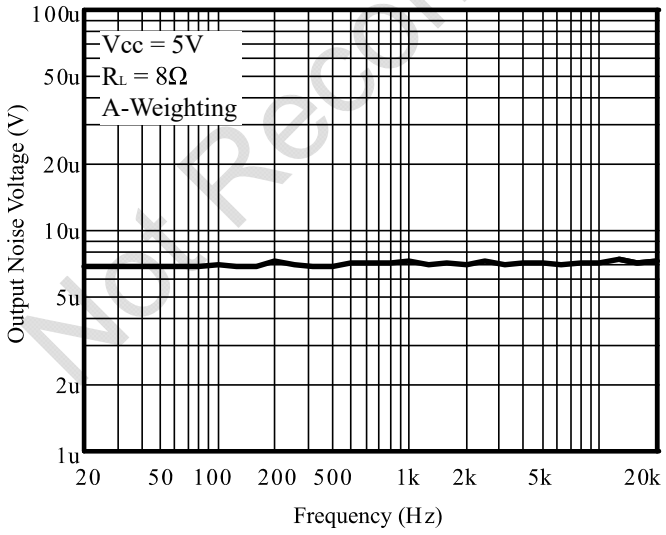


Figure 18 Noise Floor

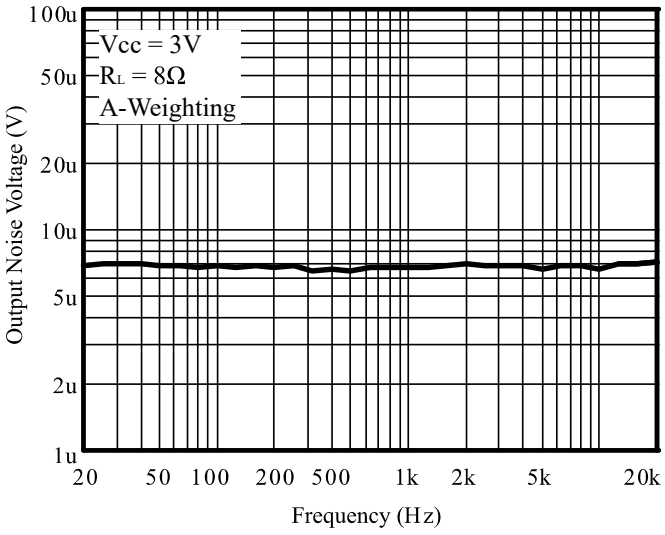


Figure 19 Noise Floor

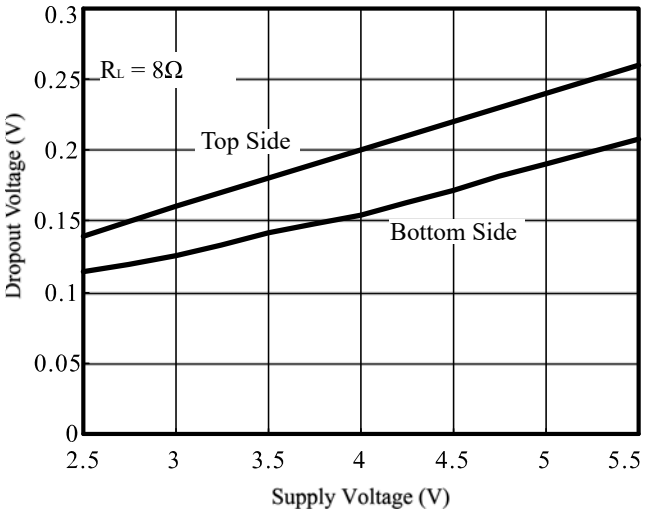


Figure 20 Dropout Voltage vs. Supply Voltage

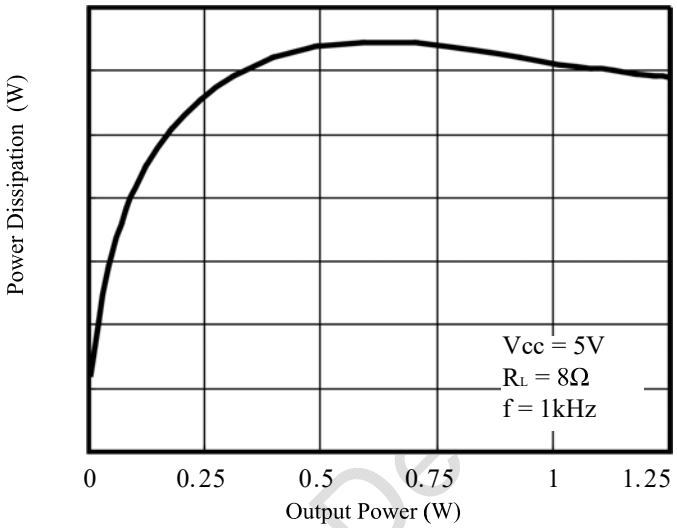


Figure 21 Power Dissipation vs. Output Power

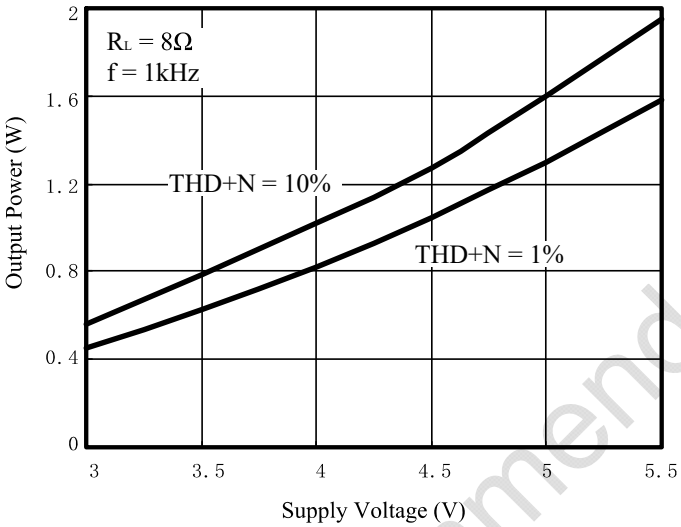
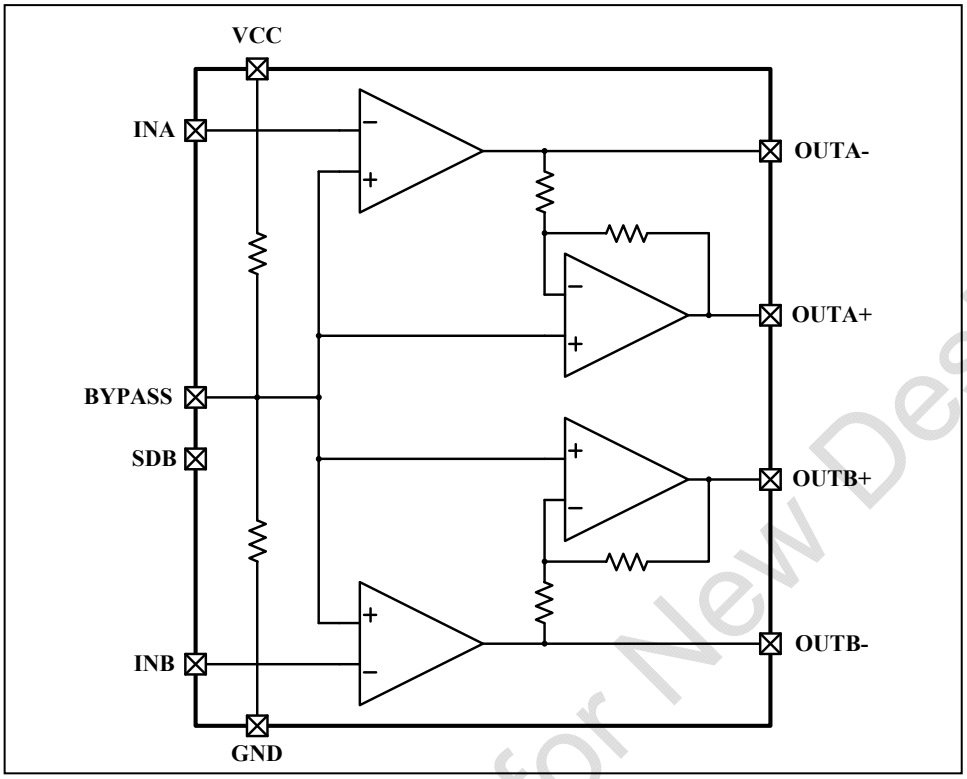


Figure 22 Output Power vs. Supply Voltage

FUNCTIONAL BLOCK DIAGRAM



APPLICATION INFORMATION

EXPOSED-DAP PACKAGE PCB MOUNTING CONSIDERATIONS

The IS31AP4088D's QFN (die attach paddle) package provides a low thermal resistance between the die and the PCB to which the part is mounted and soldered. This allows rapid heat transfer from the die to the surrounding PCB copper traces, ground plane and, finally, surrounding air.

The QFN package must have it's DAP soldered to a copper pad on the PCB. The DAP's PCB copper pad is connected to a large plane of continuous unbroken copper. This plane forms a thermal mass and heat sink and radiation area. Place the heat sink area on either outside plane in the case of a two-sided PCB, or on an inner layer of a board with more than two layers.

BRIDGE CONFIGURATION EXPLANATION

As shown in Figure 1, the IS31AP4088D consists of two pairs of operational amplifiers, forming a two-channel (Channel A and Channel B) stereo amplifier. External feedback resistors R_F and input resistors R_{IN} set the closed-loop gain of Amp A (OUT-) and Amp B (OUT-) whereas two internal 20kΩ resistors set Amp A's (OUT+) and Amp B's (OUT+) gain at 1. The IS31AP4088D drives a load, such speaker, connected between the two amplifier outputs, OUTA− and OUTA+.

Figure 1 shows that Amp A's (OUT-) output serves as Amp A's (OUT+) input. This results in both amplifiers producing signals identical in magnitude, but 180° out of phase. Taking advantage of this phase difference, a load is placed between OUTA− and OUTA+ and driven differentially (commonly referred to as "bridge mode"). This results in a differential gain of

$$A_V = 2\times(R_F/R_{IN}) \quad (1)$$

Bridge mode amplifiers are different from single-ended amplifiers that drive loads connected between a single amplifier's output and ground. For a given supply voltage, bridge mode has a distinct advantage over the single-ended configuration: its differential output doubles the voltage swing across the load. This produces four times the output power when compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited

Another advantage of the differential bridge output is no net DC voltage across the load. This is accomplished by biasing Channel A's and Channel B's outputs at half-supply. This eliminates the coupling capacitor that single supply, single ended amplifiers require. Eliminating an output coupling capacitor in a single-ended configuration forces a single-supply amplifier's half-supply bias voltage across the load. This increases internal IC power dissipation and may permanently damage loads such as speakers.

POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. Applications that employ a 5V regulator typically use a 10μF in parallel with a 0.1μF filter capacitor to stabilize the regulator's output, reduce noise on the supply line, and improve the supply's transient response. However, their presence does not eliminate the need for a local 1.0μF tantalum bypass capacitance connected between the IS31AP4088D's supply pins and ground. Keep the length of leads and traces that connect capacitors between the IS31AP4088D's power supply pin and ground as short as possible.

MICRO-POWER SHUTDOWN

The voltage applied to the SDB pin controls the IS31AP4088D's shutdown function. Activate micro-power shutdown by applying GND to the SDB pin. When active, the IS31AP4088D's micro-power shutdown feature turns off the amplifier's bias circuitry, reducing the supply current. The low 0.1μA typical shutdown current is achieved by applying a voltage that is as near as GND as possible to the SDB pin.

There are a few ways to control the micro-power shutdown. These include using a single-pole, single-throw switch, a microprocessor, or a microcontroller. When use a switch, connect an external 100kΩ resistor between the SDB pin and GND. Select normal amplifier operation by closing the switch. Opening the switch sets the SDB pin to ground through the 100kΩ resistor, which activates the micro power shutdown. The switch and resistor guarantee that the SDB pin will not float. This prevents unwanted state changes. In a system with a microprocessor or a microcontroller, use a digital output to apply the control voltage to the SDB pin. Driving the SDB pin with active circuitry eliminates the pull up resistor.

SELECTING PROPER EXTERNAL COMPONENTS

Optimizing the IS31AP4088D's performance requires properly selecting external components. Though the IS31AP4088D operates well when using external components with wide tolerances, best performance is achieved by optimizing component values.

The IS31AP4088D is unity-gain stable, giving a designer maximum design flexibility. The gain should be set to no more than a given application requires. This allows the amplifier to achieve minimum THD+N and maximum signal-to-noise ratio. These parameters are compromised as the closed-loop gain increases. However, low gain demands input signals with greater voltage swings to achieve maximum output power. Fortunately, many signal sources such as audio CODECs have outputs of 1VRMS (2.83V_{P-P}). Please refer to the Audio Power Amplifier Design section for

more information on selecting the proper gain.

INPUT CAPACITOR VALUE SELECTION

Amplifying the lowest audio frequencies requires high value input coupling capacitors (C_{IN}) in Figure 1. A high value capacitor can be expensive and may compromise space efficiency in portable designs. In many cases, however, the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 150Hz. Applications using speakers with this limited frequency response reap little improvement by using large input capacitor.

Besides effecting system cost and size, C_{IN} have an effect on the IS31AP4088D's click-and-pop performance. When the supply voltage is first applied, a transient (pop) is created as the charge on the input capacitor changes from zero to a quiescent state. The magnitude of the pop is directly proportional to the input capacitor's size. Higher value capacitors need more time to reach a quiescent DC voltage (usually $V_{CC}/2$) when charged with a fixed current. The amplifier's output charges the input capacitor through the feedback resistors, R_F. Thus, pops can be minimized by selecting an input capacitor value that is no higher than necessary to meet the desired −3dB frequency.

A shown in Figure 1, the input resistors (R_{IN}) and the input capacitors (C_{IN}) produce a −3dB high pass filter cutoff frequency that is found using Equation (2).

$$f_{-3dB} = 1/2\pi R_{IN}C_{IN} \quad (2)$$

As an example when using a speaker with a low frequency limit of 150Hz, C_{INA}, using Equation (2) is 0.053μF. The 0.33μF C_{INA} allows the IS31AP4088D to drive high efficiency, full range speaker whose response extends below 30Hz.

BYPASS CAPACITOR VALUE SELECTION

Besides minimizing the input capacitor size, careful consideration should be paid to value of C_{Bypass}, the capacitor connected to the BYPASS pin. Since C_{Bypass} determines how fast the IS31AP4088D settles to quiescent operation, its value is critical when minimizing turn-on pops. The slower the IS31AP4088D's outputs ramp to their quiescent DC voltage (nominally 1/2 V_{CC}), the smaller the turn-on pop. Choosing C_{Bypass} equal to 1.0μF along with a small value of C_{IN} (in the range of 0.1μF to 0.39μF), produces a click-less and pop-less shutdown function. As discussed above, choosing C_{IN} no larger than necessary for the desired band with helps minimize click-and-pop. Connecting a 1μF capacitor, C_{Bypass}, between the BYPASS pin and ground improves the internal bias voltage's stability and improves the amplifier's PSRR.

OPTIMIZING CLICK-AND-POP REDUCTION PERFORMANCE

The IS31AP4088D contains circuitry that minimizes turn-on and shutdown transients or "click-and-pop". For this discussion, turn-on refers to either applying the power supply voltage or when the shutdown mode is deactivated. When the part is turned on, an internal current source changes the voltage of the BYPASS pin in a controlled, linear manner. Ideally, the input and outputs track the voltage applied to the BYPASS pin. The gain of the internal amplifiers remains unity until the voltage on the bypass pin reaches $1/2V_{CC}$. As soon as the voltage on the bypass pin is stable, the device becomes fully operational. Although the BYPASS pin current cannot be modified, changing the size of C_{Bypass} alters the device's turn-on time and the magnitude of "click-and-pop". Increasing the value of C_{Bypass} reduces the magnitude of turn-on pops. However, this presents a tradeoff: as the size of C_{Bypass} increases, the turn-on time increases. There is a linear relationship between the size of C_{Bypass} and the turn-on time. Here are some typical turn-on times for various values of C_{Bypass} (all tested at V_{CC} = 5V).

C_{Bypass}	t_{ON}
0.01μF	13ms
0.1μF	26ms
0.22μF	44ms
0.47μF	68ms
1.0μF	120 ms

In order eliminate "click-and-pop"; all capacitors must be discharged before turn-on. Rapidly switching V_{CC} on and off may not allow the capacitors to fully discharge, which may cause "click-and-pop".

AUDIO POWER AMPLIFIER DESIGN

AUDIO AMPLIFIER DESIGN: DRIVING 1W INTO AN 8Ω LOAD

The following are the desired operational parameters:

Power Output: $1W_{RMS}$

Load Impedance: 8Ω

Input Level: $1V_{RMS}$

Input Impedance: 20kΩ

Bandwidth: 100Hz~20kHz ± 0.25dB

The design begins by specifying the minimum supply voltage necessary to obtain the specified output power. One way to find the minimum supply voltage is to use the Output Power vs. Supply Voltage curve in the Typical Performance Characteristics section. Another way, using Equation (3), is to calculate the peak output voltage necessary to achieve the desired output power for a given load impedance. To account for the amplifier's dropout voltage, two additional voltages, based on the Dropout Voltage vs. Supply Voltage in the Typical Performance Characteristics curves, must be added to the result obtained by Equation (3). The

result is in Equation (4).

$$V_{OUTPECK} = \sqrt{2R_L P_O} \qquad (3)$$

$$V_{CC} \geq V_{OUTPEAK} + (V_{ODTOP} + V_{ODBOT}) \qquad (4)$$

The Output Power vs. Supply Voltage graph for an 8Ω load indicates a minimum supply voltage of 4.35V for a 1W output at 1% THD+N. This is easily met by the commonly used 5V supply voltage. The additional voltage creates the benefit of headroom, allowing the IS31AP4088D to produce peak output power in excess of 1.2W at 5V of V_{CC} and 1% THD+N without clipping or other audible distortion. The choice of supply voltage must also not create a situation that violates maximum power dissipation.

After satisfying the IS31AP4088D's power dissipation requirements, the minimum differential gain needed to achieve 1W dissipation in an 8Ω load is found using Equation (5).

$$A_V = \sqrt{P_O R_L} / V_{IN} = V_{orms}/V_{inrms} \qquad (5)$$

Thus, a minimum gain of 2.83 allows the IS31AP4088D's to reach full output swing and maintain low noise and THD+N performance. For this example, let A_V = 3.

The amplifier's overall gain is set using the input, R_{IN}, and feedback resistors, R_F. With the desired input impedance set at 20kΩ, the feedback resistor is found using Equation (6).

$$R_F/R_{IN} = A_V/2 \qquad (6)$$

The value of R_F is 30kΩ.

The last step in this design example is setting the amplifier's −3dB frequency bandwidth. To achieve the desired ±0.25dB pass band magnitude variation limit, the low frequency response must extend to at least one-fifth the lower bandwidth limit and the high frequency response must extend to at least five times the upper bandwidth limit. The gain variation for both response limits is 0.17dB, well within the ±0.25dB desired limit. The results are an

f_L = 100Hz/5 = 20Hz

and an

f_H = 20kHz×5 = 100kHz.

As mentioned in the External Components section, R_{IN} and C_{IN} create a high pass filter that sets the amplifier's lower band pass frequency limit. Find the coupling capacitor's value using Equation (7).

$$C_{IN} \geq 1/(2\Pi r_{In} f_L) \qquad (7)$$

The result is

1/(2π×20kΩ×20Hz) = 0.398μF

Use a 0.39μF capacitor, the closest standard value.

The product of the desired high frequency cut off (100kHz in this example) and the differential gain, A_V, determines the upper pass band response limit. With A_V = 3 and f_H = 100kHz, the closed-loop gain bandwidth product (GBWP) is 300kHz. With this margin, the amplifier can be used in designs that require more differential gain while avoiding performance-restricting bandwidth limitations.

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

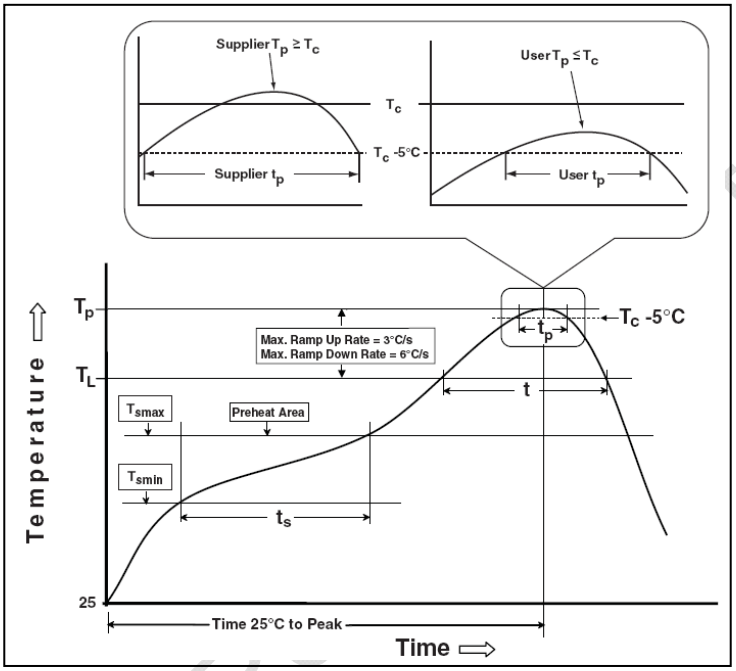
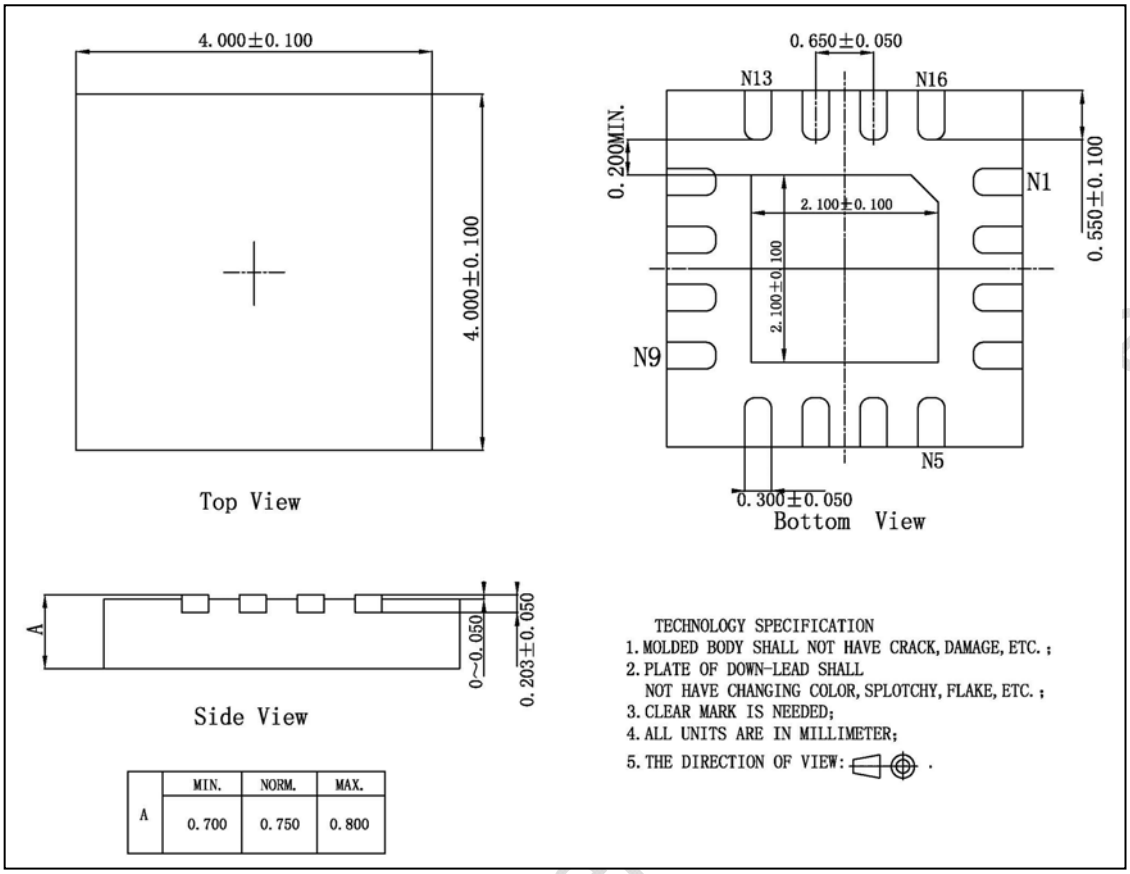


Figure 23 Classification Profile

PACKAGE INFORMATION

QFN-16



	MIN.	NORM.	MAX.
A	0.700	0.750	0.800

Note: All dimensions in millimeters unless otherwise stated.

REVISION HISTORY

Revision	Detail Information	Date
A	Initial release	2011.12.13
B	1. Add ESD(HBM/CDM) 2. Add function block	2014.01.06
C	Add NRND watermark	2021.09.07