User's Guide

TPS7H3302EVM (LP085)

ABSTRACT

This user's guide describes operational use of the TPS7H3302EVM evaluation module (EVM) as a reference design for engineering demonstration and evaluation of the TPS7H3302-SEP, a 3-A sink and source DDR termination LDO regulator. This user's guide provides details about the EVM, the configuration, schematics, and bill of materials (BOM).

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Trademarks

1 Introduction

The TPS7H3302EVM-SEP (LP085) evaluation board is designed to evaluate the performance and characteristics of TI's radiation tolerant DDR/DDR2/DDR3/DDR3L/DDR4 termination regulator, the TPS7H3302-SEP.

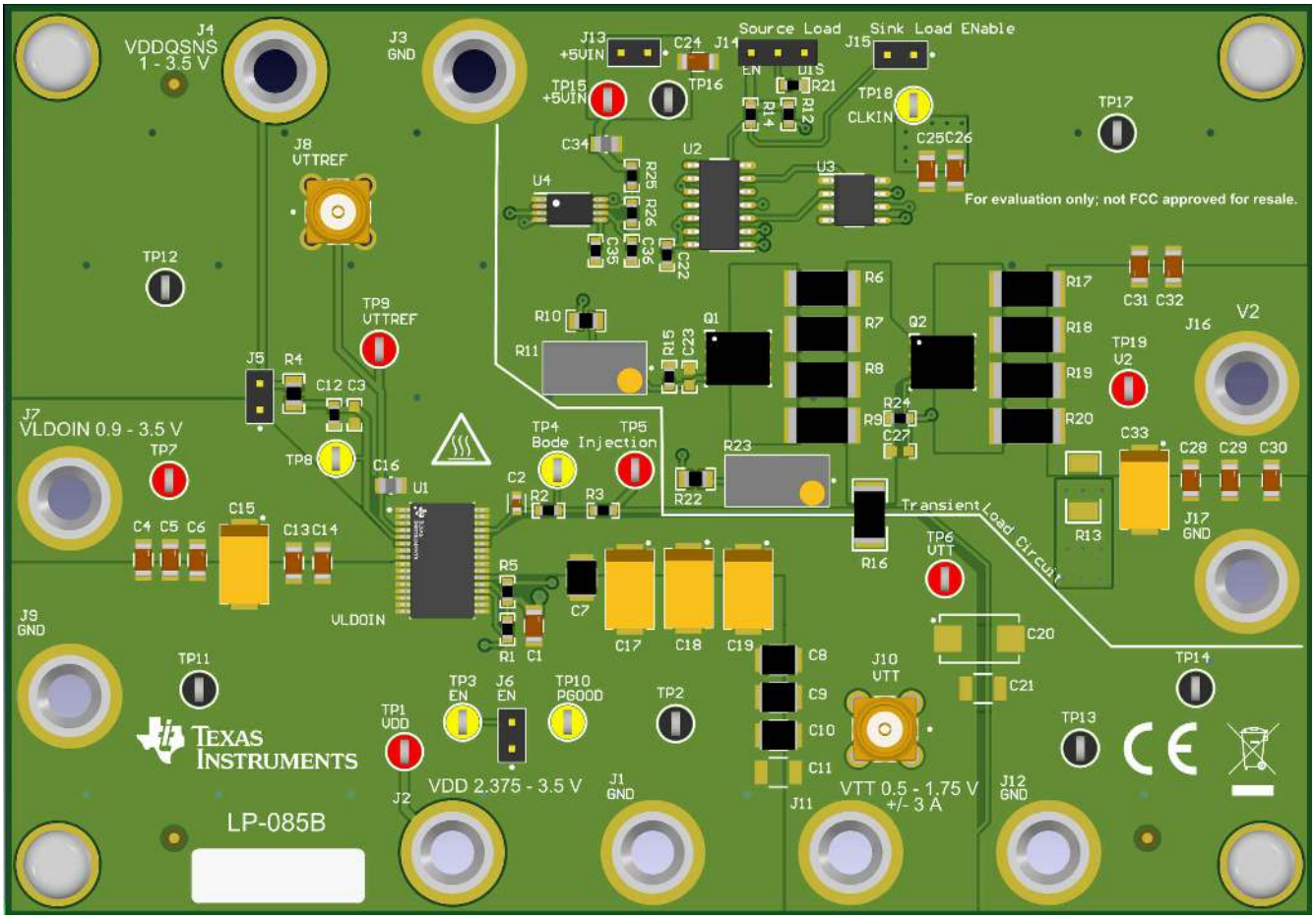

Figure 1-1. TPS7H3302EVM Board (Top View)

2 Description

The TPS7H3302-SEP is a radiation-tolerant double data rate (DDR) ±3 A termination regulator with built-in VTTREF buffer. The regulator is specifically designed to provide a complete, compact, low-noise device for space DDR termination applications such as single board computers, solid state recorders, and payload processing.

The TPS7H3302-SEP supports DDR VTT termination applications using DDR, DDR2, DDR3, and DDR4. The fast transient response of the TPS7H3302-SEP VTT regulator allows for a very stable supply during read and write conditions. During transients, the fast tracking feature of the VTTREF supply minimizes any voltage offset between VTT and VTTREF. To enable simple power sequencing, both an enable input and a power-good output (PGOOD) have been integrated into the TPS7H3302-SEP. The open-drain output of the PGOOD terminal is compatible with being tied to other open-drain outputs, which facilitates the monitoring of a group supplies; such that a solitary GPIO pin can detect when all supplies are in regulation. The enable signal also discharges VTT during suspend to RAM (S3) power down mode.

2.1 Related Information

- TPS7H3302-SEP data sheet (SLVSGX6)

2.2 Typical Applications

The EVM is used in the following applications:

- Radiation-tolerant DDR power applications
- Memory termination regulator for DDR, DDR2, DDR3, and DDR4

2.3 Features

This EVM has the following features:

- Input core voltage VDD supports 2.5-V rail and 3.3-V rail
- V_{LDOIN}, V_{DDQ} voltage range: 0.9 V–3.5 V
- Dynamic performance evaluation features:
  - Sink and source integrated load switches for transient load step emulation
  - Configurable load step and slew rate control by on-board resistors

> **CAUTION**
> The default EVM configuration using the built-in transient test circuit supports testing the DDR4 at ±1.5 A, DDR3 at ±1.875 A, DDR2 at ±2.25 A. To evaluate the DDR node, or different currents for DDR2, DDR3, DDR3L, and DDR4 the total resistance of resistors R6-R9, and R17-R20 needs to be changed to not exceed device maximum ratings.

- Jumper J14 (pins 1 and 2) for device enable. (enabled without J14 installed)
- Convenient test points for probing PGOOD, CLK_IN, and loop response testing
- Optional placeholders for VDDQSNS to VLDOIN filter when not using independent VDDQSNS source

2.4 Performance Specification Summary

Table 2-1 lists the EVM performance specifications. See data sheet (SLVSGX6) for complete specifications.

Table 2-1. Performance Specification Summary

Specification	Test Conditions	MIN	TYP	MAX	Unit
Input voltage range, (V_{VIN})		2.375	3.3	3.5	V
VDDQSNS voltage range ($V_{VDDQSNS}$)		1		3.5	
VLDOIN voltage range (V_{VLDOIN})		0.9		3.5	
VTT Termination Voltage					
DDR	VTT		1.25		
	VTTREF		1.25		
DDR2	VTT		0.9		
	VTTREF		0.9		
DDR3	VTT		0.75		
	VTTREF		0.75		
DDR4	VTT		0.6		
	VTTREF		0.6		
Termination current (I_{VTT})		–3		3	A
Reference current (I_{VTTREF})		–10		10	mA

3 Test Setup

3.1 Equipment

3.1.1 Power Supplies

Power supply #1 (PS#1): a power supply capable of supplying up to 3.5 V at > 3 A is required for VLODIN.

Power supply #2 (PS#2): a power supply capable of supplying up to 2.5 V at 100 mA is required for VDDQSNS. Only required if not using VLDOIN for VDDQSNS.

Power supply #3 (PS#3): a power supply capable of supplying up to 3.5 V at 100 mA is required for VIN.

Power supply #4 (PS#4): a power supply capable of supplying up to 5 V at 100 mA is required to power transient circuit.

Power supply #5 (PS#5): a power supply capable of supplying up to 3.5 V at > 3 A is required for V2 source for transient circuit.

3.1.2 Load #1

Electronic load capable of testing desired DC sink or source load current (up to 3 A).

3.2 EVM Connectors and Test Points

Section 3.2 lists the EVM connectors and test points.

Table 3-1. Connectors and Test Points

Reference Designator	Function
J1	Ground (GND)
J2	Input voltage VDD. V_{IN} range is from 2.375 V to 3.5 V
J3	Ground (GND) for VDD
J4	VDDQSNS voltage range 1.2 V – 2.5 V.
J5	Jumper to connect VDDQSNS to VLDOIN
J6	Jumper to disable device. No jumper = enabled.
J7	VLDOIN
J8	SMA VTTREF
J9	Ground (GND)
J10	SMA VTT
J11	VTT
J12	Ground (GND) for VTT
J13	Transient circuit 5 V 2-pin input header
J14	Source load selector: Jumper (pins 1 and 2) part of transient circuit
J15	Sink load selector Jumper (pins 1 and 2) part of transient circuit
J16	V2 voltage for DDR sink – transient test
J17	Ground (GND) for V2
TP1	Test point for the input voltage node. VDD
TP2	Ground (GND)
TP3	Test point for EN signal
TP4	Test point for Bode signal injection
TP5	Test point for Bode signal injection
TP6	Test point for output voltage node VTT
TP7	Test point for input voltage node VLDOIN
TP8	Test point for input voltage node VLDOIN
TP9	Test point for output voltage VTTREF
TP10	Test point for PGOOD signal
TP11	Test point Ground (GND)
TP12	Test point Ground (GND)
TP13	Test point Ground (GND)
TP14	Test point Ground (GND)
TP15	Test point or voltage input for 5 V transient circuit
TP16	Test point Ground (GND)
TP17	Test point Ground (GND)
TP18	Test point Clock
TP19	Test point for voltage source V2

3.3 Testing Procedure

Use these steps for testing the EVM with a static DC external load:

1. Verify all supplies are off prior to connecting the EVM.
2. Verify proper polarity of power supply and load connections.
3. Remove jumper on J6 to set device to enable.
4. Place a jumper on J5 (pins 1 and 2), connecting VDDQSNS to VLDOIN.
   a. Alternatively a separate voltage source can be used for VLDOIN and a separate voltage source of VDDQSNS, thus isolating the two. This method isolates the transients introduced on VLDOIN from impacting VDDQSNS. Additionally, this method allows for reduced internal power dissipation. VLDOIN can be reduced to VTT + VDO.
5. Set the load to sink desired current up to 3 A.
6. Connect a power supply VDD using J2/J1, or test points TP1 and TP2. Vin current is less than 100 mA.
7. Connect power supply to J7/J9 - VLDOIN. VLDOIN current can be up to 3 A and possibly higher during startup.
8. Connect VTT voltmeter (+) terminal to TP6 and (–) terminal to TP13, or J10.
9. Connect the load (+) to J11 and (–) to J12. If desired, connect a current meter in series to test VTT sourcing current. Alternatively, connect isolated load (+) from J7 VLDOIN and (-) to J11 to test VTT sinking.
10. Set the power supply for VLDOIN to 1.5 V.
11. Set the power supply for VIN to 3 V.
12. Enable both VIN and VLDOIN supplies.
13. Connect a scope or voltmeter monitoring VTTREF to TP9 and GND TP, or using SMA J8.
14. The voltmeter monitoring VTTREF reads approximately 0.75 V
15. The voltmeter monitoring VTT reads approximately 0.75 V
16. Enable the VTT load to observed Sink or Source effect on VTT.
17. Place jumper on J6 to disable the device.
18. The voltmeter monitoring VTT reads near zero volts, as VTT is discharged when disabled.
19. The voltmeter monitoring VTTREF still reads approximately 0.75 V as VTTREF is still active when disabled.
20. Disable supplies to complete the DC static loading test.

Table 3-2 displays the input voltage and output voltage measurement test points. Using the following connection points, monitor VTT and VTTREF regulation overline and overload.

Table 3-2. I/O Voltage Measurement Test Points

EVM	Input / Output Voltage		Test point
TPS7H3302EVM-SEP	VIN	2.375 V ≤ VIN ≤ 3.5 V	TP15 (+) TP16(–)
	VLDOIN	0.9 V ≤ VLDOIN ≤ 3.5 V	TP7(+) TP11(–)
	VDDQSNS	1.2 V ≤ VDDQSNS ≤ 3.5 V	J4 or (Pin2 J5)(+) TP12(–)
	VTT	½ VDDQSNS	TP6(+) TP13(–)
	VTTREF	½ VDDQSNS	TP9(+) TP11(–)

3.3.1 EVM Bode Plot Measurement Setup

The setup for EVM bode plot measurement is as follows:

1. Use a Bode 100 loop analyzer or equivalent equipment.
2. Remove jumper on J5 to isolate VDDQSNS from VLDOIN. To test with VLDOIN tied to single VDDQ along with VDDQSNS, use the optional filter. See note below.
3. Connect the oscillator output across R3 = 51 Ω resistor. Connect the output of oscillator to TP4 (VTTSNS).
4. Connect Channel 2 of the analyzer at TP5 and connect ground to TP2
5. Connect Channel 1 of the analyzer at TP4 and connect ground to TP2.
6. Power EVM with desired conditions for VLDOIN, VIN, VDDQSNS, and VTT load.
7. With the EVM loaded to the required load, run bode plot over desired frequency range.

To verify stability across loads and rated operating temperature, implement a quantity of four 4.7 uF ceramic output capacitors in the application circuit.

> All of the bode measurements presented, VDDQSNS is provided from an independent supply from VLDOIN. If VDDQSNS and VLDOIN inputs are connected to same supply, then use the isolation filter on the EVM to isolate the load effects on VLDOIN from VDDQSNS. The filter can be used by replacing components for R4, and C3.

Figure 3-1 through Figure 3-3 show bode plots for this EVM. All plots generated using default C_{IN} and C_{OUT} capacitances populated on EVM. C_{IN} = 150 µF tantalum // 5-10 µF ceramic, C_{OUT} = 3-150 µF tantalum // 4-4.7 µF ceramic.

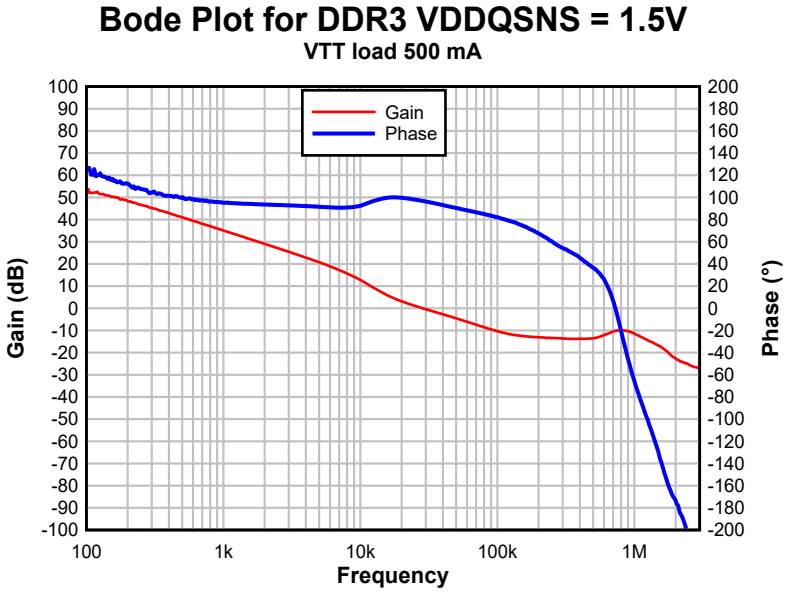

Figure 3-1. DDR3 Bode Plot Iload = 500 mA

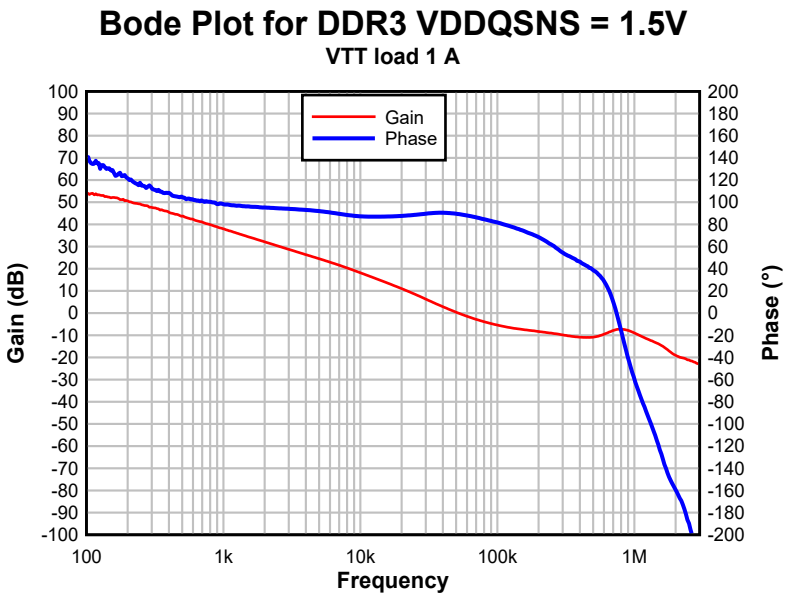

Figure 3-2. DDR3 Bode Plot Iload = 1 A

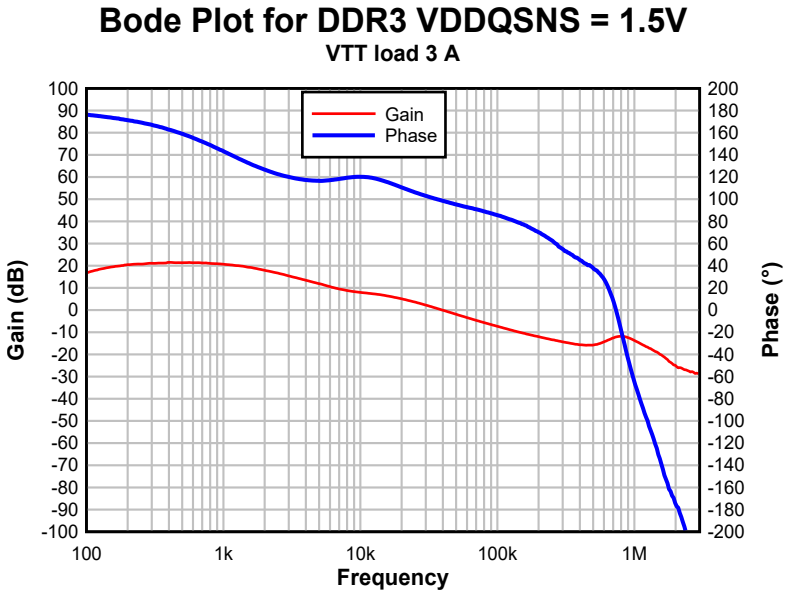

Figure 3-3. DDR3 Bode Plot Iload = 3 A

TI recommends that VLDOIN and VDDQSNS be isolated from each other. If isolating VLDOIN and VDDQSNS is not possible, then add an external input filter between VLDOIN and VDDQSNS. Adding an RC filter between VLDOIN and VDDQSNS results in some loss of dynamic tracking of VTT and VTTREF to VDDQSNS.

3.3.2 EVM Transient Test

A transient test setup circuit is incorporated as part of the EVM.

The built-in transient load switches (with both sinking and sourcing capability) are available to emulate the sink or source transient behavior to evaluate the dynamic performance. For ease of use, both load step and transient timing can be modified by on-board resistors. The EVM has two sets of four parallel 1.6 Ω resistors connected for transient load for both the VTT to GND, and VTT to V2 to accommodate both sourcing and sinking evaluation. Optionally, resistor R13 can be populated with zero Ω resistor to utilize VLDOIN as source for sinking transients. This method can cause a poor response due to transients introduced on VLDOIN, especially if VDDQSNS is tied to VLDOIN.

CAUTION

The default EVM configuration using the built-in transient test circuit supports testing the DDR4 at ±1.5 A, DDR3 at ±1.875 A, and DDR2 at ±2.25 A. To evaluate the DDR node, or different loads for DDR2, DDR3, DDR3L, and DDR4 the total resistance of resistors R6-R9 and R17-R20 needs to be changed to not exceed device maximum ratings.

1. Remove any external loads.
2. Place jumper J14 (pins 2 and 3) source load selector (labeled "EN").
3. Place jumper J15 (pins 1 and 2) sink load selector.
4. Remove jumper J5 to isolate VDDQSNS from VLDOIN.
5. Apply 2.5 V to VIN.
6. Apply 1.5 V to J7/J9 VLDOIN.
7. Apply 1.5 V to J16/J17 V2 (this is the source for the sinking transients).
8. Apply 1.5 V to J4/J3 VDDQSNS. If testing with VDDQSNS is not isolated from VLDOIN, install J10, and only apply to VLDOIN (with reduced performance).
9. Monitor VTT to verify VTT voltage is present. VTT is approximately 750 mV.
10. Apply 5 V to J13 (pin 2 [+], pin 1 [–]) (or by TP15, TP16), providing power to the transient load setup.
11. Monitor VTT at J10 using a scope to see transient results.

The following plots show the results of using the transient circuit configured for DDR3 voltages. All the plots have VTT and VTTREF shown with 750 mV offset applied. In addition to VTT and VTTREF, the plots include the clock signal (CLK), the math function of the difference of VTTREF - VTT, and the current measurements of V2. Note, that V2 only represents the current when the device is sinking. Thus, during the sourcing, this current is zero. During sourcing, a near identical current is present through VLDOIN.

Figure 3-5 shows the response of the circuit with both sinking and sourcing enabled.

Figure 3-5 shows the response of the circuit with only sinking transients applied. This method can be tested by only having shunt on J15 and no shunt on J14.

Figure 3-6 shows the response of the circuit with only sourcing transients applied. This method can be tested by only having shunt on EN pins of J14, and no shunt on J15.

Figure 3-7 shows the transient response with VDDQSNS not isolated from VLDOIN with both sinking and sourcing enabled. Transients on VLDOIN also influences VDDQSNS and cause undesirable disturbances. Transient response can be improved with implementation of a filter on VDDQSNS from VLDOIN. The filter can be implemented by replacing components for R4, and C3. Note the large fluctuation on VTTREF due to VLDOIN and hence VDDQSNS transients.

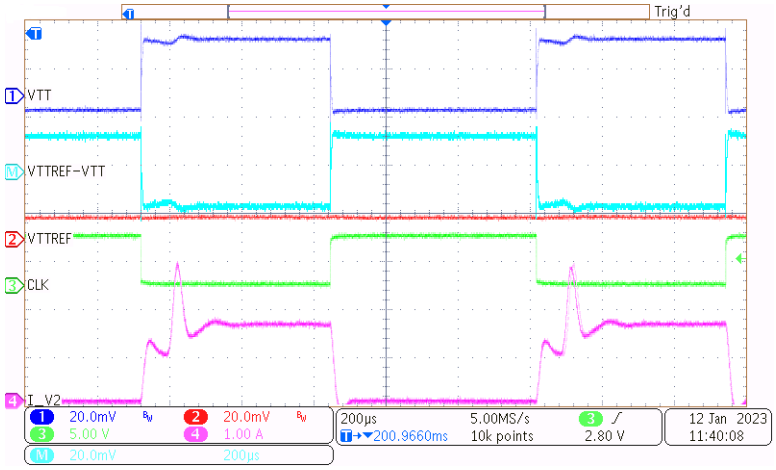

Figure 3-4. DDR3 Scope Plot Response With Both Sinking and Sourcing Enabled and VDDQSNS Isolated.

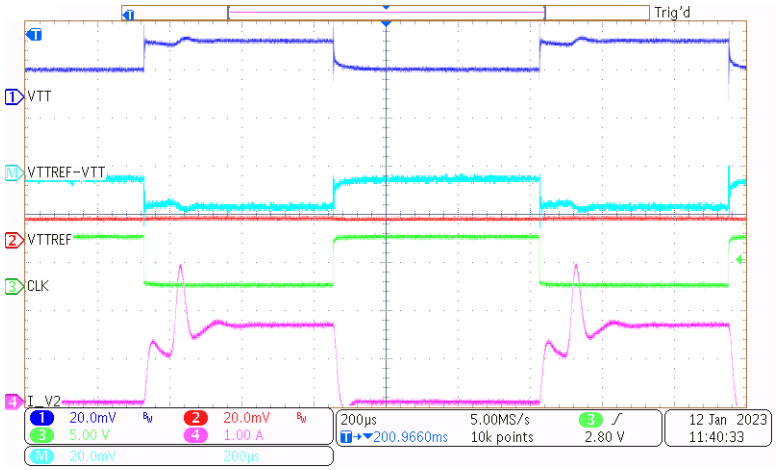

Figure 3-5. DDR3 Scope Plot of Response with 1.875 A Sinking Only with Isolated VDDQSNS

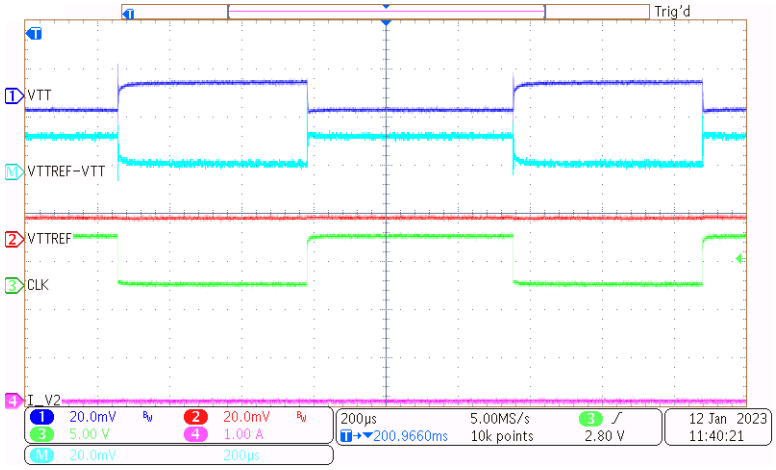

Figure 3-6. DDR3 Scope Plot of Response with 1.875 A Sourcing Only with Isolated VDDQSNS

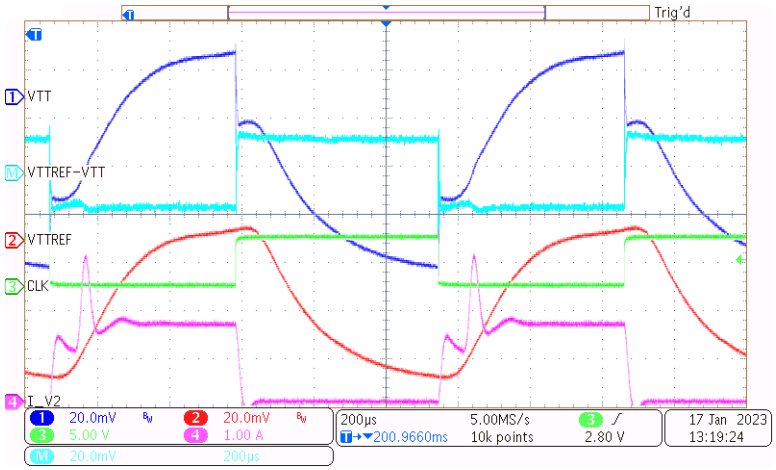

Figure 3-7. DDR3 Scope Plot of Response With 1.875 A Sinking and Sourcing With Non-Isolated VDDQSNS

4 Board Layout

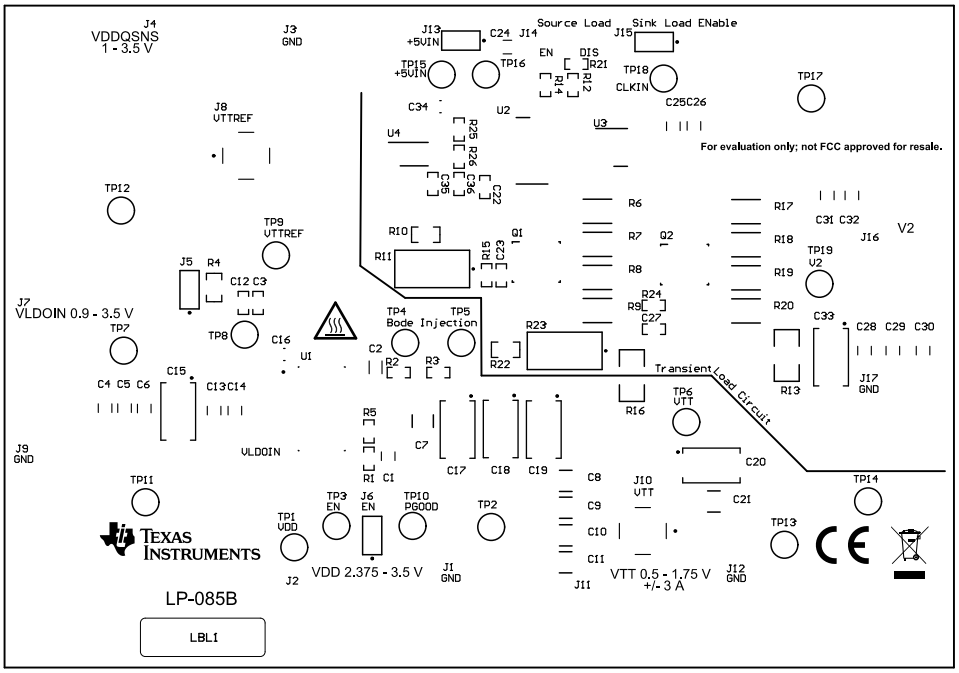

Figure 4-1. Top Overlay

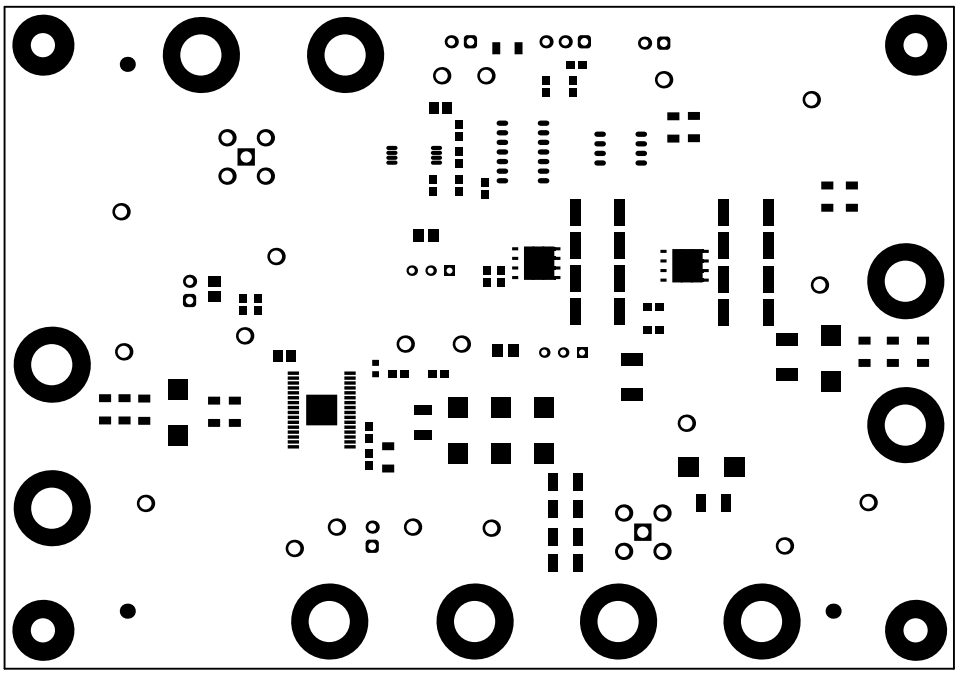

Figure 4-2. Top Solder

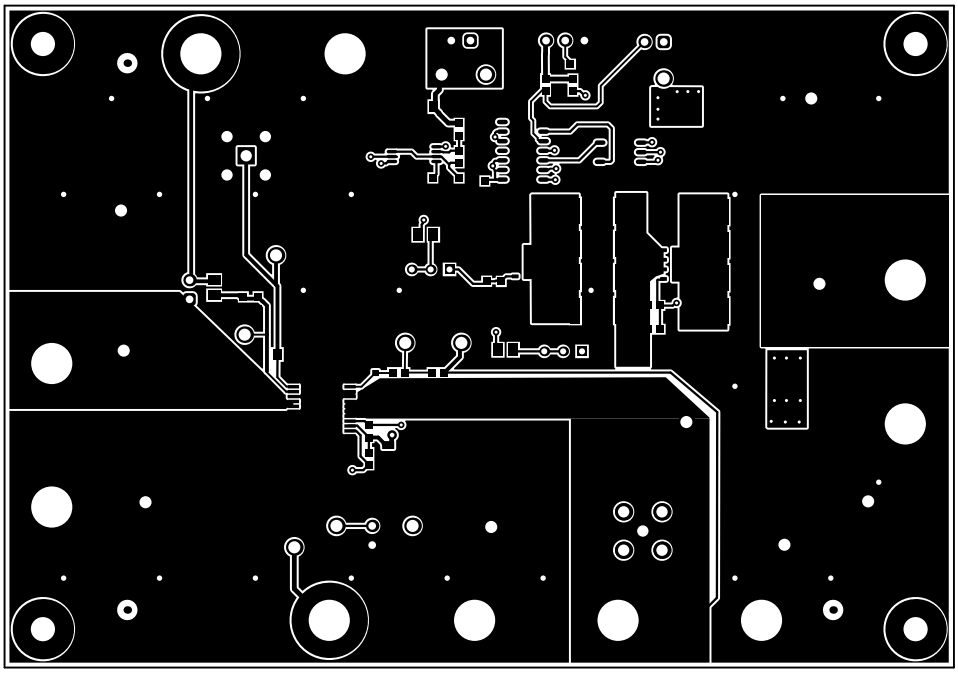

Figure 4-3. Top Layer

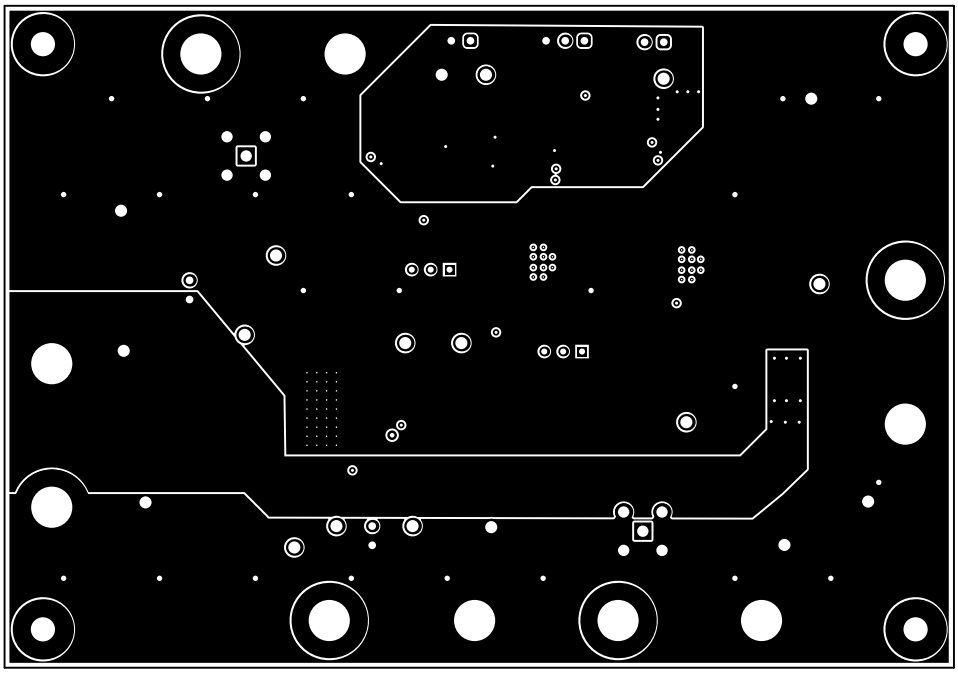

Figure 4-4. Signal and Power Layer 1

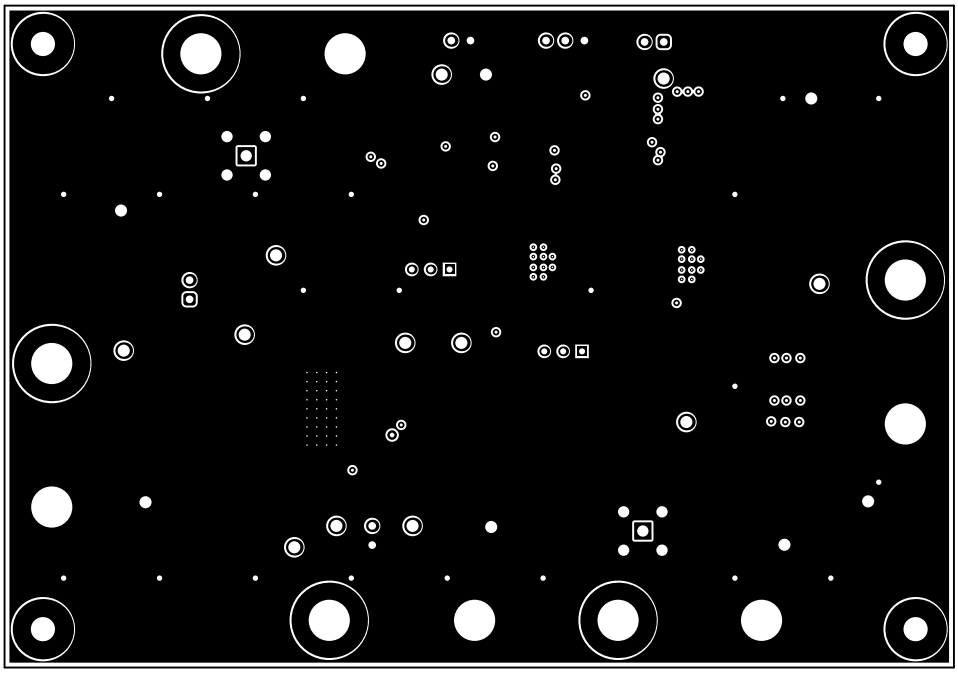

Figure 4-5. Signal and Power Layer 2

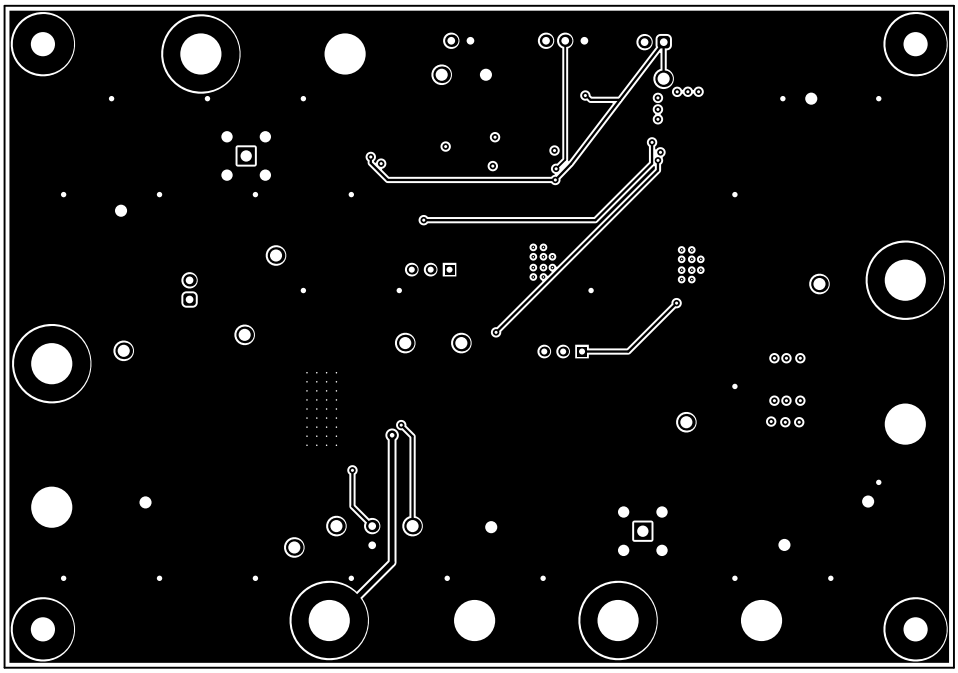

Figure 4-6. Bottom Layer

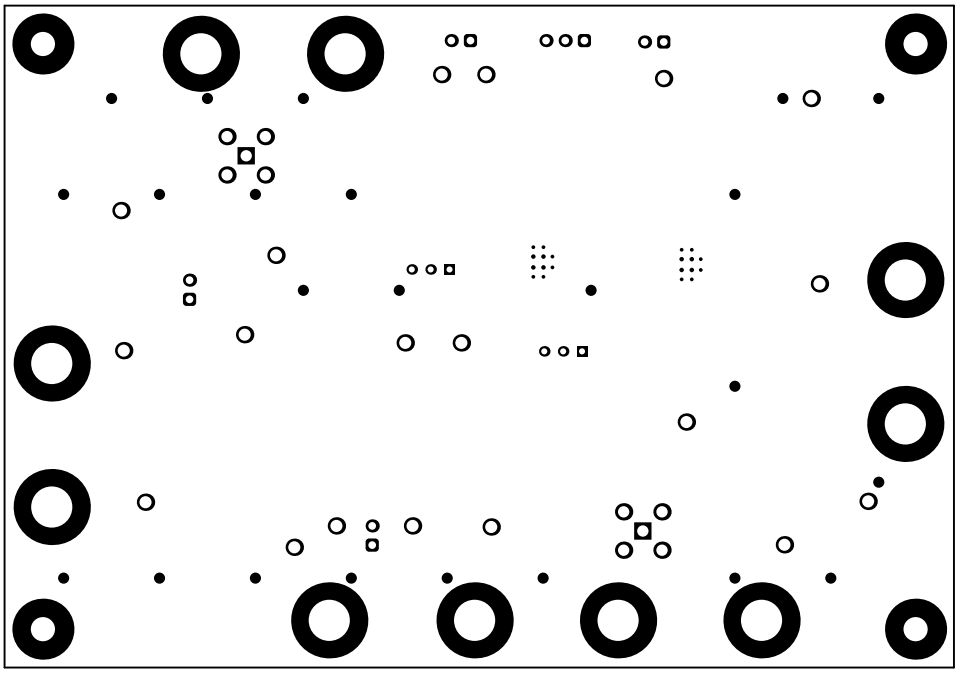

Figure 4-7. Bottom Solder

5 Schematic

Figure 5-1 illustrates the TPS7H3302EVM-SEP schematics.

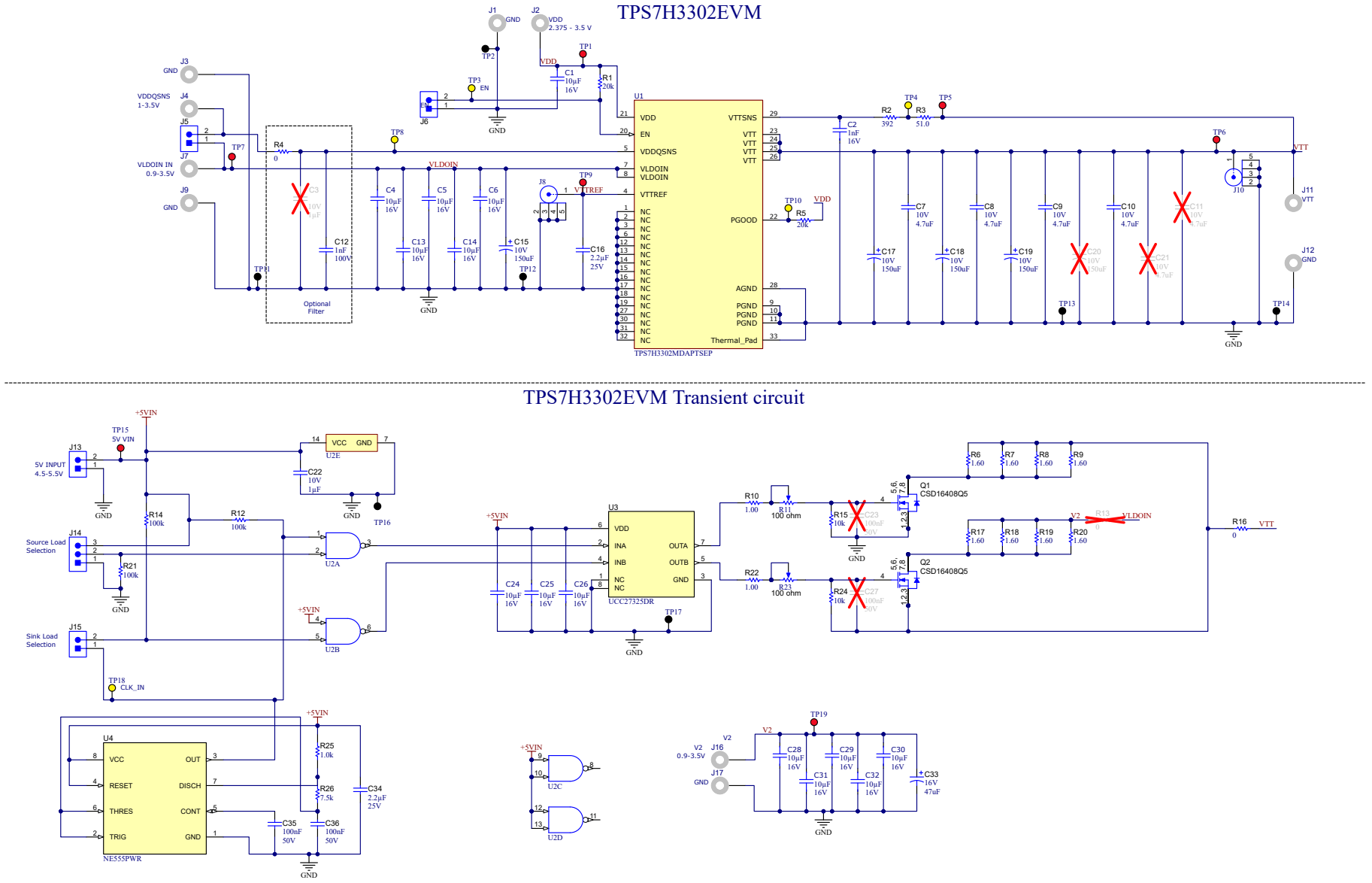

Figure 5-1. LP085B Schematic

6 Bill of Materials

Table 6-1 lists the EVM BOM.

Table 6-1. Bill of Materials

Designator	Quantity	Description	PartNumber	Manufacturer
C1, C4, C5, C6, C13, C14, C24, C25, C26, C28, C29, C30, C31, C32	14	Ceramic capacitor for automotive 10 µF, ±10%, 16VDC, X7R 1206 embossed T/R, 1206	GCM31CR71C106KA64K	Murata
C2	1	Ceramic capacitor, 1000 pF, ±10%, 16 V, X7R, 603	CC0603KRX7R7BB102	YAGEO
C7, C8, C9, C10	4	Ceramic capacitor, 4.7 µF, 10 V, ±10%, X7R, 1210	1210ZC475KAT2A	AVX
C12	1	Ceramic capacitor, 1000 pF, 100 V, ±10%, X7R, 0603	06031C102KAT2A	AVX
C15, C17, C18, C19	4	Capacitor, tantalum polymer, 150 µF, 10 V, ±20%, 0.005 ohm, 7343-31 SMD	T530D157M010ATE005	Kemet
C16, C34	2	Ceramic capacitor, 2.2 µF, 25 V, ±10%, X7R, 0805	08053C225KAT2A	AVX
C22	1	Ceramic capacitor, 1 µF, 10 V, ±10%, X7R, 0603	0603ZC105KAT4A	AVX
C33	1	Capacitor, TA, 47 µF, 16 V, ±20%, 0.15 ohm, SMD	TPSD476M016R0150	AVX
C35, C36	2	Ceramic capacitor, 0.1 µF, 50 V, ±5%, X7R, 0603	06035C104JAT2A	AVX
J1, J2, J3, J4, J7, J9, J11, J12, J16, J17	10	Standard banana jack, uninsulated, 5.5 mm	575-4	Keystone
J5, J6, J13, J15	4	Header, 100 mil, 2x1, gold, TH	TSW-102-07-G-S	Samtec
J8, J10	2	SMA connector receptacle, female socket 50 Ω, PTH_RF_CONN	733910060	Molex
J14	1	Header, 100 mil, 3x1, gold, TH	TSW-103-07-G-S	Samtec
Q1, Q2	2	MOSFET, N-channel, 25 V, 113 A, DQH0008A (VSON-CLIP-8)	CSD16408Q5	Texas Instruments
R1, R5	2	Resistor, 20 kΩ, 5%, 0.1 W, 0603	RC0603JR-0720KL	Yageo
R2	1	Resistor, 392 Ω, 1%, 0.1 W, 0603	RC0603FR-07392RL	Yageo
R3	1	Resistor, 51.0 Ω, 1%, 0.1 W, 0603	RC0603FR-0751RL	Yageo
R4	1	Resistor, 0 Ω, 5%, 0.125 W, 0805	RC0805JR-070RL	Yageo America
R6, R7, R8, R9, R17, R18, R19, R20	8	Resistor, 1.60 Ω, 1%, 1 W, 2512	ERJ-1TRQF1R6U	Panasonic
R10, R22	2	Resistor, 1.00 Ω, 1%, 0.125 W, 0805	RC0805FR-071RL	Yageo America
R11, R23	2	Trimmer, 100 Ω, 0.5W, TH, potentiometer, 953 x 12.36 x 4.95 mm	67WR100LF	TT-Electronics-BI-Technologies
R12, R14, R21	3	Resistor, 100 kΩ, 5%, 0.1 W, 0603	CRCW0603100KJNEAC	Vishay-Dale
R15, R24	2	Resistor, 10 kΩ, 5%, 0.1 W, 0603	RC0603JR-0710KL	Yageo
R16	1	Resistor, 0 Ω, 5%, 0.75 W, AEC-Q200 grade 0, 2010	CRCW20100000Z0EF	Vishay-Dale
R25	1	Resistor, 1.0 kΩ, 5%, 0.25 W, AEC-Q200 grade 0, 0603	ESR03EZPJ102	Rohm
R26	1	Resistor, 7.5 kΩ, 5%, 0.1 W, 0603	RC0603JR-077K5L	Yageo
SH-J1,SH-J2,SH-J3	3	Shunt, 100 mil, gold plated, black	SNT-100-BK-G	Samtec

Table 6-1. Bill of Materials (continued)

Designator	Quantity	Description	PartNumber	Manufacturer
TP1, TP5, TP6, TP7, TP8, TP9, TP15, TP19	8	Test point, multipurpose, red, TH	5010	Keystone Electronics
TP2, TP11, TP12, TP13, TP14, TP16, TP17	7	Test point, multipurpose, black, TH	5011	Keystone Electronics
TP3, TP4, TP10, TP18	4	Test point, multipurpose, yellow, TH	5014	Keystone Electronics
U1	1	Radiation-tolerant 3-A DDR termination regulator, HTSSOP32	TPS7H3302MDAPTSEP	Texas Instruments
U2	1	Quadruple 2-input positive-NAND gates, D0014A, LARGE T&R		Texas Instruments
U3	1	Dual 4-A Peak High Speed Low-Side Power MOSFET Drivers, D0008A (SOIC-8)	UCC27325DR	Texas Instruments
U4	1	Single Precision Timer, PW0008A (TSSOP-8)	NE555PWR	Texas Instruments
C3	0	Ceramic capacitor, 1 µF, 10 V, ± 10%, X7R, 0603	0603ZC105KAT4A	AVX
C11, C21	0	Ceramic capacitor, 4.7 µF, 10 V, ±10%, X7R, 1210	1210ZC475KAT2A	AVX
C20	0	Capacitor, tantalum polymer, 150 µF, 10 V, ±20%, 0.005 Ω, 7343-31	T530D157M010ATE005	Kemet
C23, C27	0	Ceramic capacitor, 0.1 µF, 50 V,±5%, X7R, 0603	06035C104JAT2A	AVX
R13	0	Resistor, 0 Ω, 5%, 0.75 W, AEC-Q200 Grade 0, 2010	CRCW20100000Z0EF	Vishay-Dale

7 Related Documentation

Texas Instruments, Standard Terms for Evaluation Modules

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (August 2022) to Revision A (April 2023) **Page**

- Deleted notes pertaining to revision A board....7
- Changed board plots to LP085B.... 12
- Changed schematic to LP085B.... 16
- Change *Bill of Materials* to LP085B....17

STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

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