IS32LT3125/3125A

SINGLE CHANNEL 250mA LED DRIVER WITH FAULT DETECTION

June 2022

GENERAL DESCRIPTION

The IS32LT3125/3125A is a linear programmable current regulator consisting of a single output channel capable of 250mA. It features an EN pin to enable and disable the output channel's current source. It supports PWM dimming via EN pin or power supply modulation (PSM). The UV pin can be used to set external VCC undervoltage lockout threshold via a resistor divider. An external resistor programs the current level for the channel current source. In addition, IS32LT3125/3125A integrates fault protection for LED open/short, ISET pin open/short and over temperature condition for robust operation. Detection of these failures is reported by the FAULTB pin. When a fault is detected the device will disable itself and output an open drain low signal. Multiple devices can have their FAULTB pins connected to create a "one-fail-all-fail" condition. Under a fault condition, the IS32LT3125 will sink 30mA I_{CC} current, while the IS32LT3125A will sink a lower 2mA (Max.) I_{CC}.

The IS32LT3125/3125A is targeted at the automotive market with end applications to include interior and exterior lighting. For 12V automotive applications the low dropout driver can support one to several LEDs on the output channel.

Both devices are offered in a small thermally enhanced SOP-8-EP package.

FEATURES

- Single channel, sources up to 250mA
- 5.0V to 28V input supply voltage range
  - Withstand 42V load dump
- External resister sets source current
- Programmable VCC undervoltage lockout to match the LED stack for High Side PWM operation
- Shared fault flag for multiple devices operation
- Fault protection with flag output:
  - LED string open/short
  - OUT pin short to VCC/GND
  - ISET pin open/short
  - Thermal shutdown
- - I_{CC} set to 30mA under fault condition (IS32LT3125 only)
- External C_{STOR} capacitor keeps fault status during start/stop operation
- SOP-8-EP package
- AEC-Q100 Qualified
- Operating temperature range from -40°C ~ +125°C

APPLICATIONS

- Automotive interior/exterior lighting:
  - Turn signal light
  - Tail/stop light
  - Position light
  - Dome light

TYPICAL APPLICATION CIRCUIT

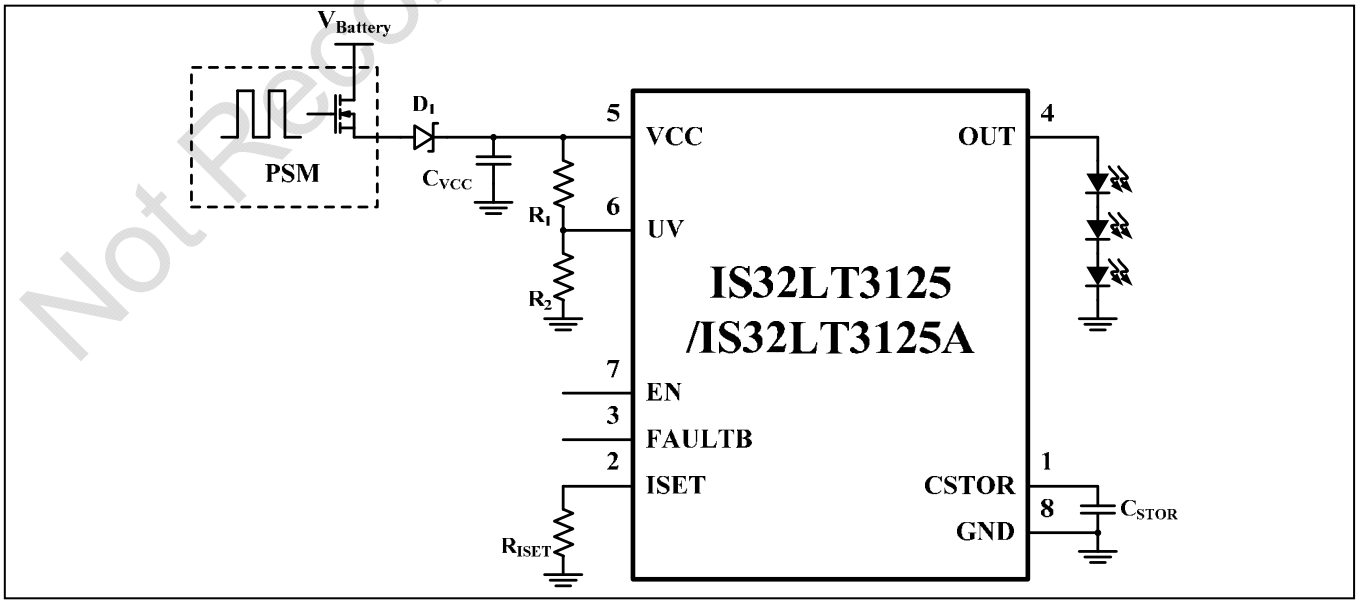


Figure 1 Typical Application Circuit

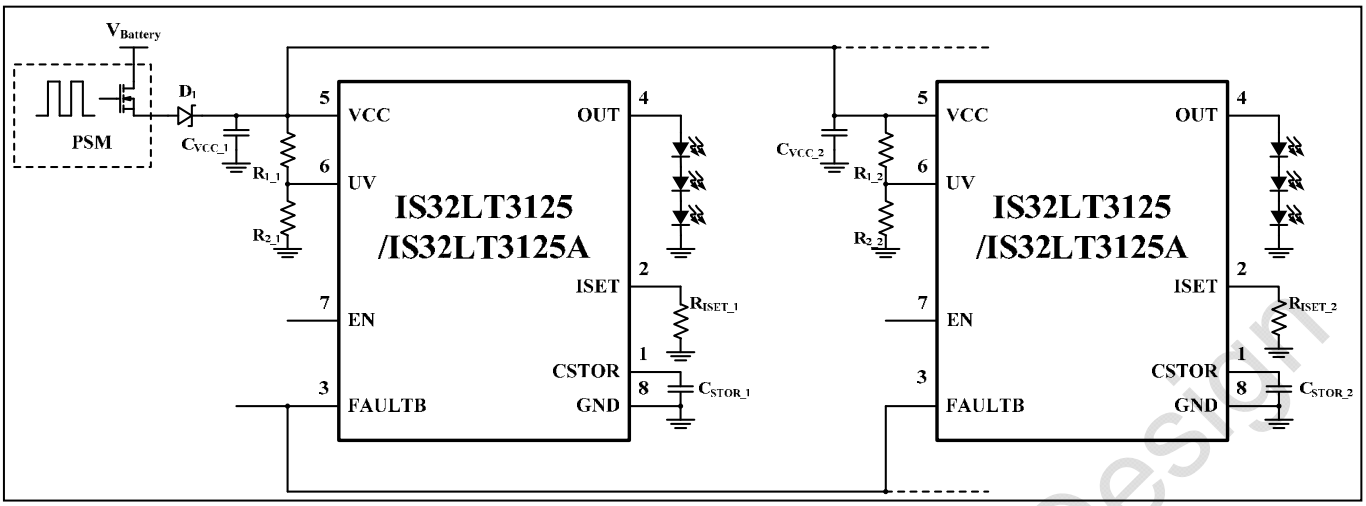
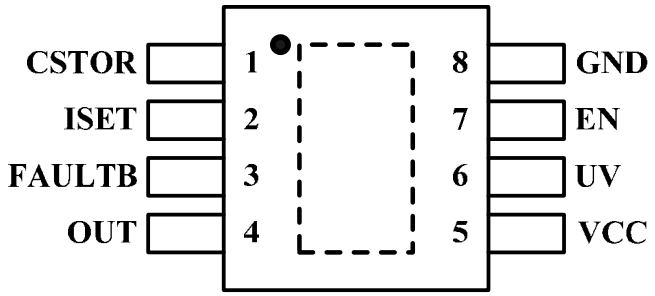


Figure 2 Typical Application Circuit (Several Devices in Parallel with FAULTB Interconnection)

Note 1: For PSM dimming application, high C_{VCC} capacitor value will affect the dimming accuracy. To get better dimming performance, recommend 0.1μF for it.

PIN CONFIGURATION

Package	Pin Configuration (Top view)
SOP-8-EP	

PIN DESCRIPTION

No.	Pin	Description
1	CSTOR	Keep-alive capacitor to maintain the deglitch timer and fault latch status with collapsing VCC.
2	ISET	Output current setting for channel. Connect a resistor between this pin and GND to set the maximum output current.
3	FAULTB	Open drain output with internal pull up to 4.5V. Active low to indicate the fault conditions. This pin is also an input pin. Pulling this pin low will shutdown the device.
4	OUT	Output current source channel.
5	VCC	Power supply input pin.
6	UV	External under voltage lockout threshold detection pin.
7	EN	Enable pin. It can be used for LED PWM dimming or device ON/OFF.
8	GND	Ground.
	Thermal Pad	Must be electrically connected to GND plane for better thermal dissipation.

ORDERING INFORMATION
Automotive Range: -40°C to +125°C

Order Part No.	Package	QTY/Reel
IS32LT3125-GRLA3-TR IS32LT3125A-GRLA3-TR	SOP-8-EP, Lead-free	2500

ABSOLUTE MAXIMUM RATINGS

VCC, OUT, EN, UV	-0.3V ~ +45V
ISET, FAULTB, CSTOR	-0.3V ~ +7.0V
Operating temperature, T_A=T_J	-40°C ~ +150°C
Storage temperature range, T_{STG}	-65°C ~ +150°C
Package thermal resistance, junction to ambient (4-layer standard test PCB based on JESD 51-2A), θ_{JA}	43.3°C/W
Package thermal resistance, junction to thermal PAD (4-layer standard test PCB based on JESD 51-8), θ_{JP}	1.39°C/W
Maximum power dissipation, P_{DMAX}	2.31W
ESD (HBM) ESD (CDM)	±2kV ±750V

Note 2: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

T_J = -40°C ~ +125°C, V_{CC}=12V, the detail refers to each condition description. Typical values are at T_J = 25°C.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
Power Up Parameter							
V_{CC}	Supply voltage range			5		28	V
V_{UVLO}	VCC under voltage lockout threshold voltage	VCC falling		4.2	4.5	4.8	V
V_{UVLO_HY}	VCC under voltage lockout voltage hysteresis				0.15		V
I_{CC}	VCC supply current	R_{ISET}=20kΩ, V_{EN} =high, No Fault condition.			2.5	3.5	mA
I_{SD}	Quiescent supply current	In shutdown mode (OUT turned off), V_{EN} = low			0.7		mA
I_{SD_FLT}	Supply current during LED string short or open	R_{ISET}=20kΩ, V_{EN}=high. OUT connected to GND (in fault master mode)	IS32LT3125	20	30	40	mA
			IS32LT3125A		1	2	
		R_{ISET}=20kΩ, V_{EN}= high, V_{FAULTB}= low (in fault slave mode).			1	2	
t_{SD}	EN low time for IC power shutdown			40	48	55	ms
t_{ON}	EN high time for IC power up	I_{OUT}= -100mA, V_{CC}= 12V, V_{EN}= High				40	μs
Channel Parameter							
V_{ISET}	ISET pin voltage	R_{ISET}= 20kΩ			1		V
I_{OUT}	Output current (Note 3)	R_{ISET}= 20kΩ, V_{HR}= 1V		-106	-100	-94	mA

ELECTRICAL CHARACTERISTICS (CONTINUE)

T_J = -40°C ~ +125°C, V_{CC}=12V, the detail refers to each condition description. Typical values are at T_J = 25°C.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{HR}	Minimum headroom voltage	V_{CC} – V_{OUT}, I_{OUT}= -250mA			1500	mV
		V_{CC} – V_{OUT}, I_{OUT}= -100mA			700	
I_{OUT_R}	Channel output current range	R_{ISET}= 80kΩ, I_{OUT}=-25mA R_{ISET}= 8kΩ, I_{OUT}=-250mA	-250		-25	mA
I_{OUT_L}	Output limit current	R_{ISET}=5kΩ	-350	-300	-260	mA
I_{LEAK}	Channel leakage current	V_{EN}=Low, V_{OUT}=0V, V_{CC}=28V			1	μA
t_{SL}	Current slew time	Enabled by EN pin, current rise/fall between 0%~100%		4		μs
Fault Protect Parameter						
t_{FD}	Fault deglitch time	Fault must be present at least this long to trigger the fault detect		25		μs
V_{FAULTB}	FAULTB pin voltage	Sink current = 20mA		0.2	0.4	V
R_{FAULTB}	FAULTB pin pull up resistor			200	300	KΩ
V_{FAULTB_IH}	FAULTB pin input high enable threshold				2	V
V_{FAULTB_IL}	FAULTB pin input low disable threshold		0.8			V
V_{SCD}	OUT pin short to GND threshold	Measured at OUT	1.0	1.2	1.5	V
V_{SCD_HY}	OUT pin short to GND hysteresis	Measured at OUT		220		mV
V_{OCD}	OUT pin open threshold	Measured at (V_{CC}-V_{OUT})	150		300	mV
V_{OC_HY}	OUT pin open hysteresis	Measured at (V_{CC}-V_{OUT})		100		mV
I_{CST}	CSTOR leakage current	V_{CSTOR} = 5.5V		4.6	10	μA
T_{SD}	Thermal shutdown threshold	(Note 4)		165		°C
T_{HY}	Over-temperature hysteresis	(Note 4)		25		°C
Logic Input						
V_{EN}	EN input voltage threshold	Voltage rising	1.18	1.23	1.28	V
V_{ENHY}	EN input hysteresis			40		mV
f_{PWM}	PWM frequency to EN	(Note 4)			1	kHz
V_{UV}	UV input voltage threshold	Voltage rising	1.18	1.23	1.28	V
V_{UVHY}	UV input hysteresis			40		mV

Note 3: Output current accuracy is not intended to be guaranteed at output voltages less than 1.8V.

Note 4: Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

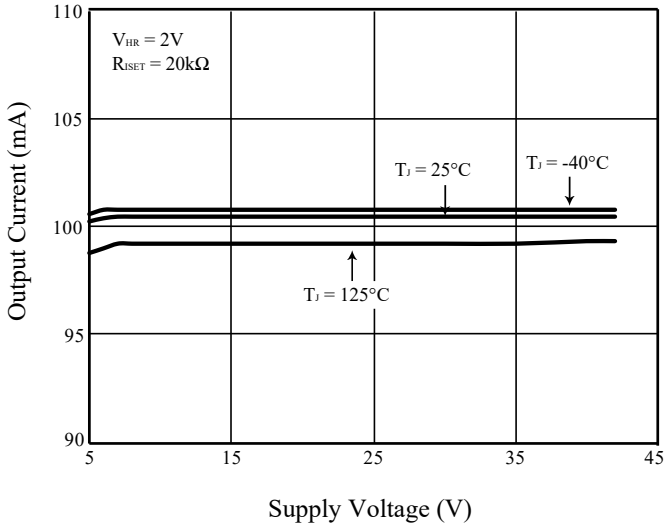


Figure 3 I_{OUT} vs. V_{CC}

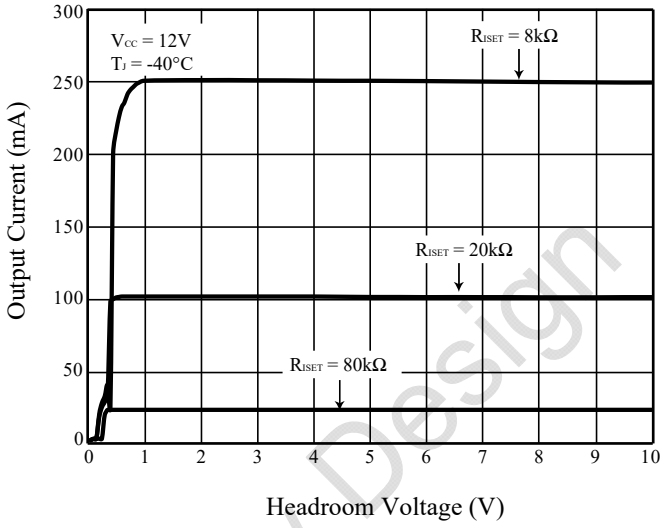


Figure 4 I_{OUT} vs. V_{HR}

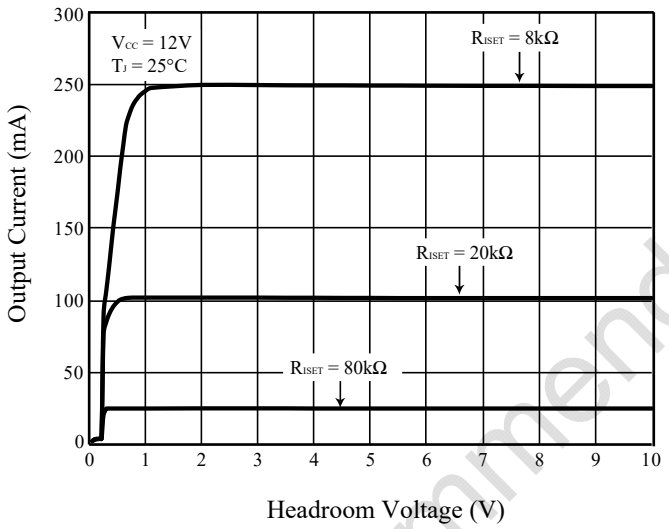


Figure 5 I_{OUT} vs. V_{HR}

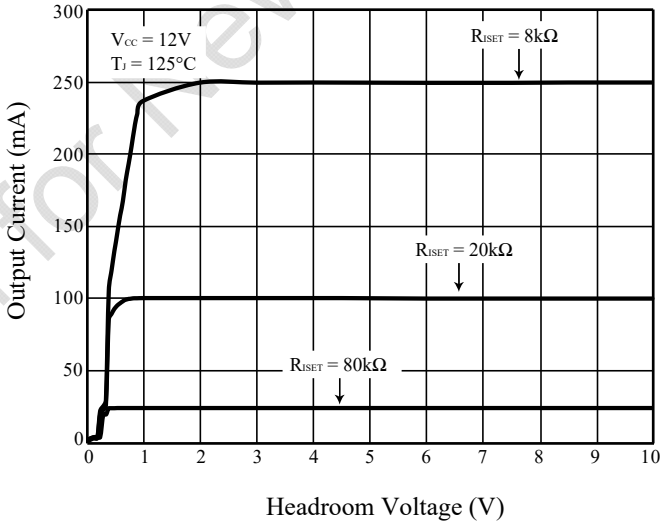


Figure 6 I_{OUT} vs. V_{HR}

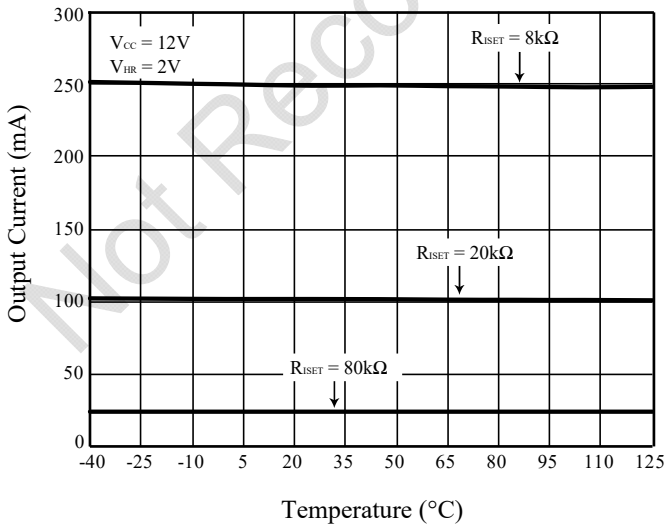


Figure 7 I_{OUT} vs. T_J

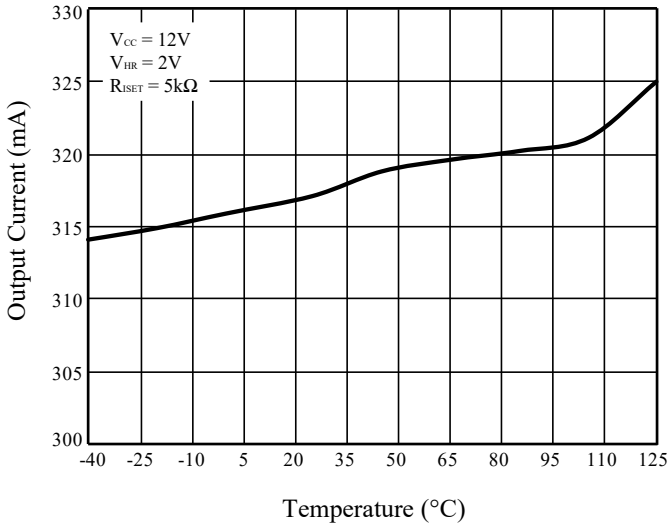


Figure 8 I_{OUT_L} vs. T_J

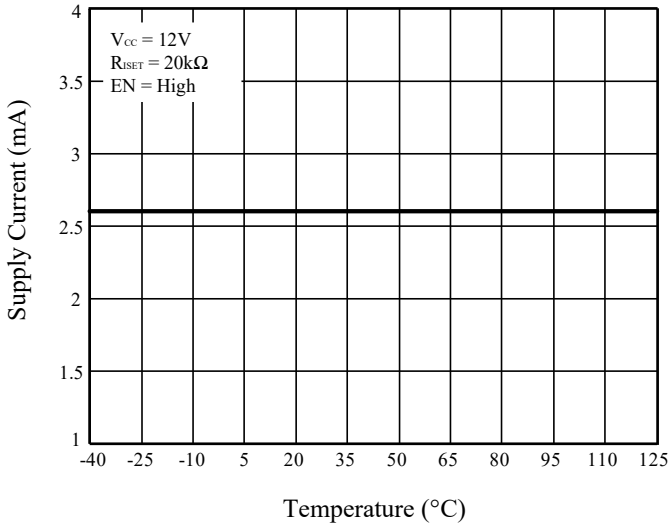


Figure 9 I_{CC} vs. T_J

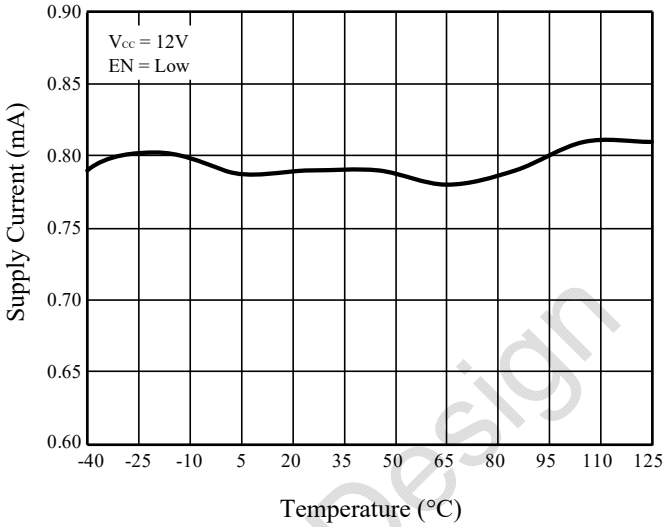


Figure 10 I_{SD} vs. T_J

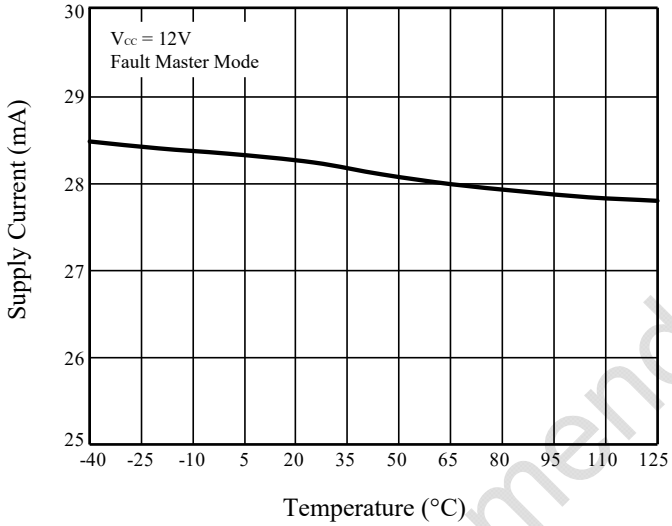


Figure 11 I_{SD_FLT} vs. T_J For IS32LT3125

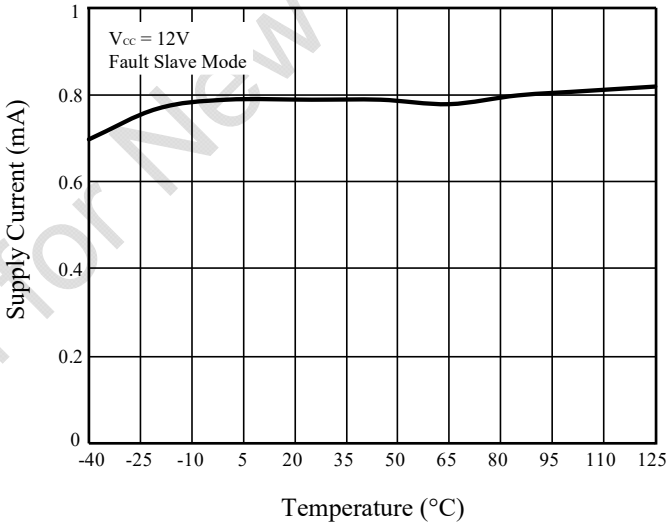


Figure 12 I_{SD_FLT} vs. T_J

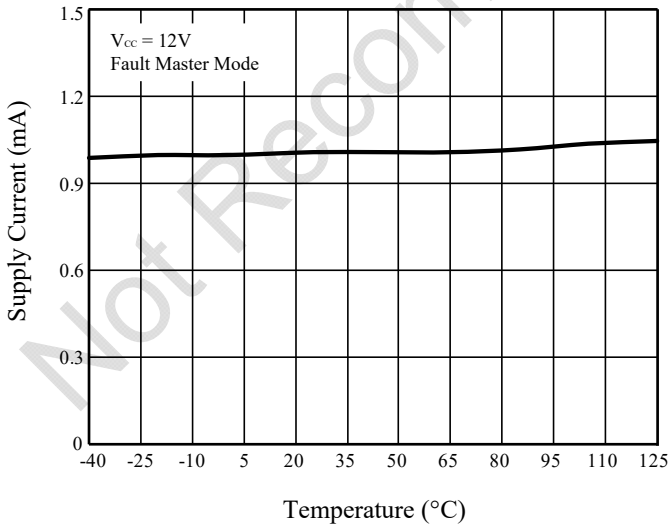


Figure 13 I_{SD_FLT} vs. T_J for IS32LT3125A

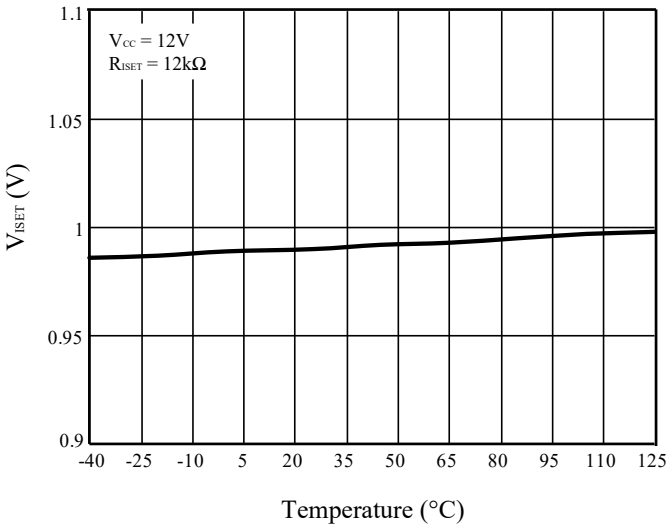


Figure 14 V_{ISET} vs. T_J

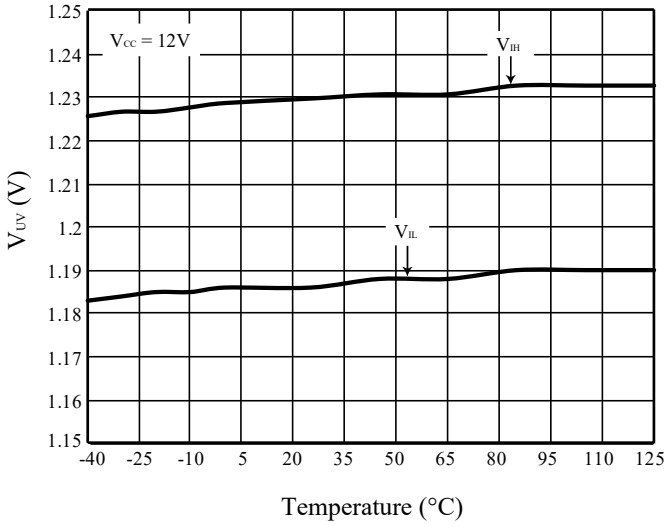


Figure 15 V_{UV} vs. T_J

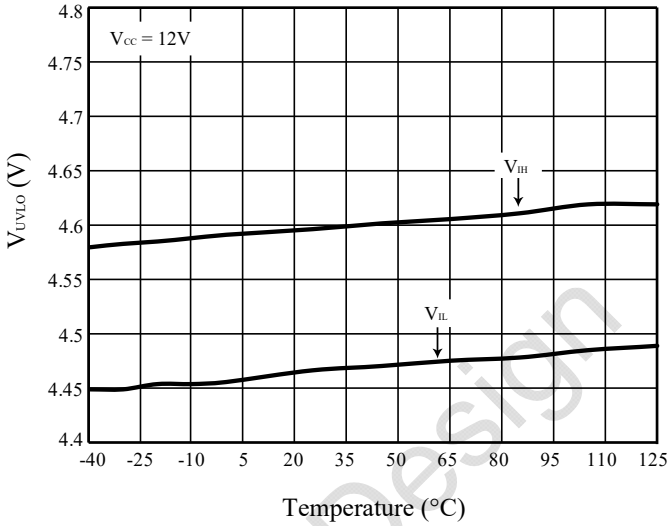


Figure 16 V_{UVLO} vs. T_J

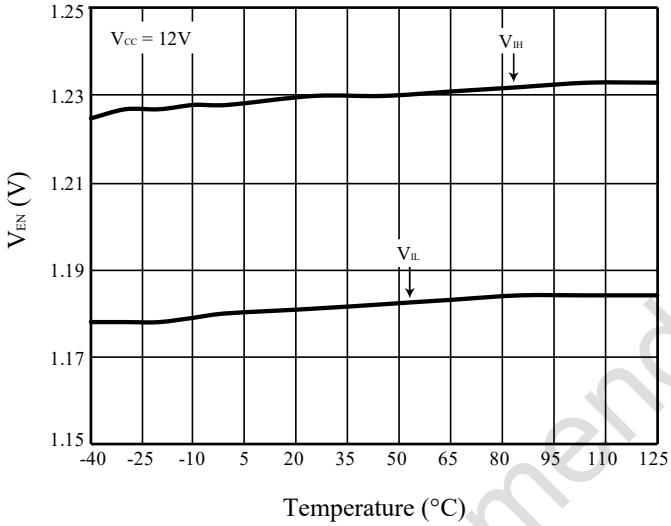


Figure 17 V_{EN} vs. T_J

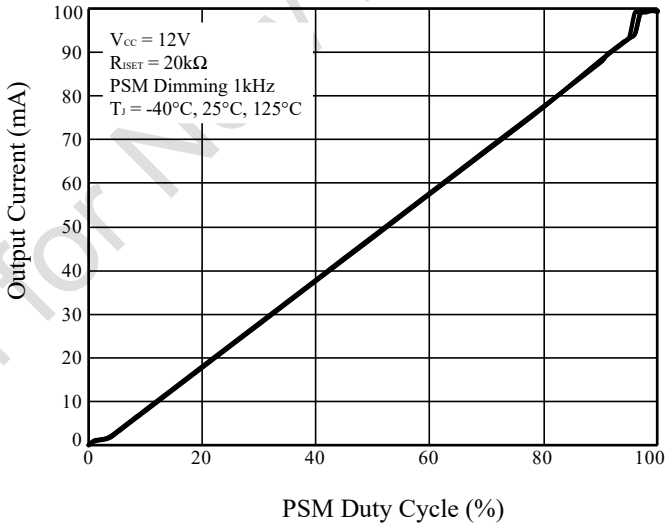


Figure 18 PSM Dimming at 1kHz

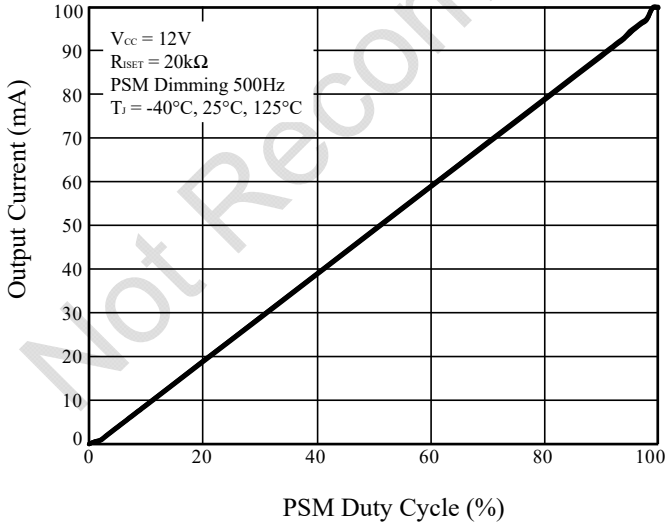


Figure 19 PSM Dimming at 500Hz

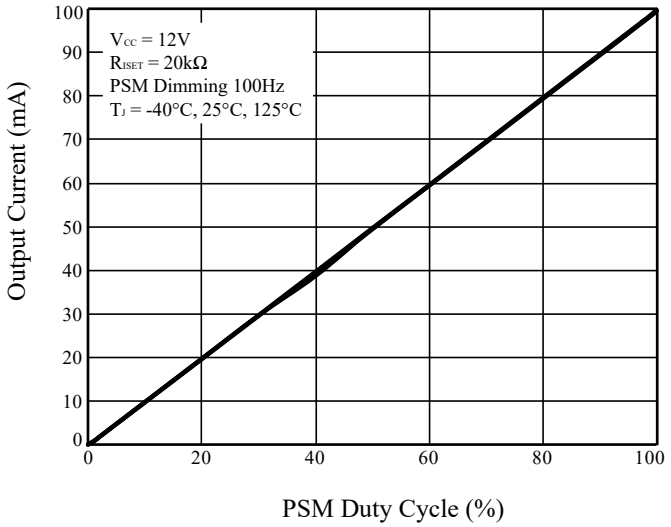


Figure 20 PSM Dimming at 100Hz

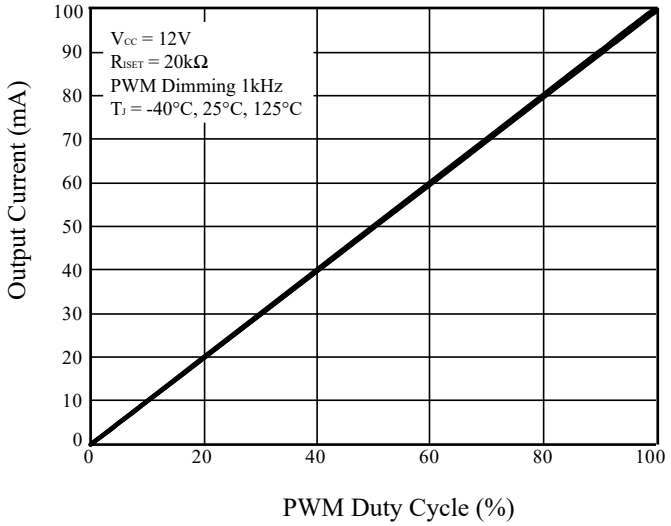


Figure 21 PWM Dimming at 1kHz

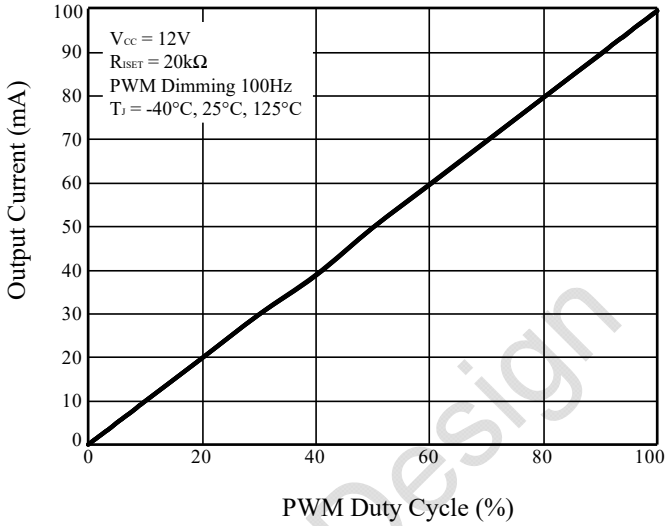


Figure 22 PWM Dimming at 100Hz

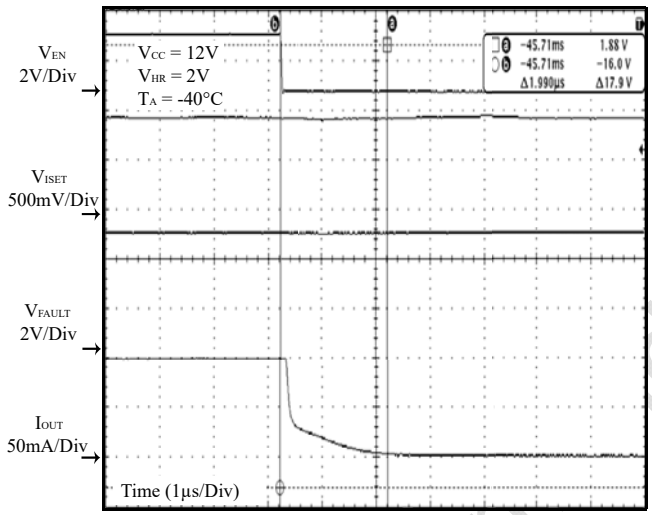


Figure 23 EN Off

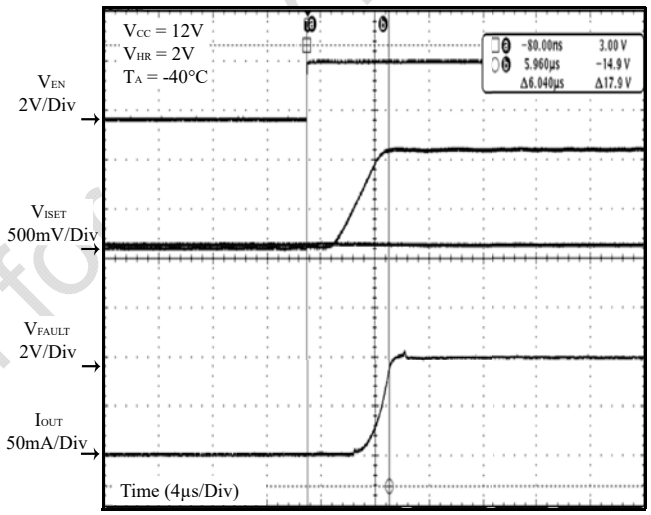


Figure 24 EN On

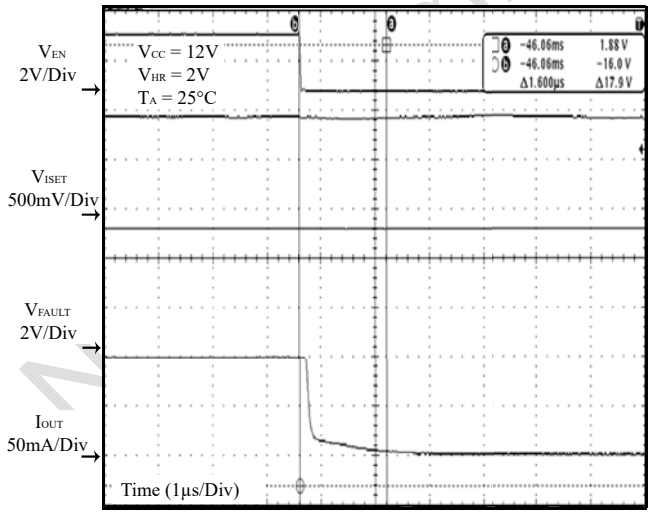


Figure 25 EN Off

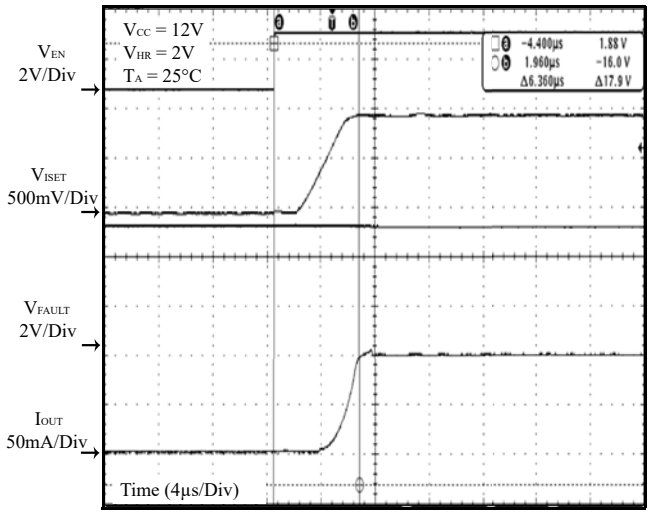


Figure 26 EN On

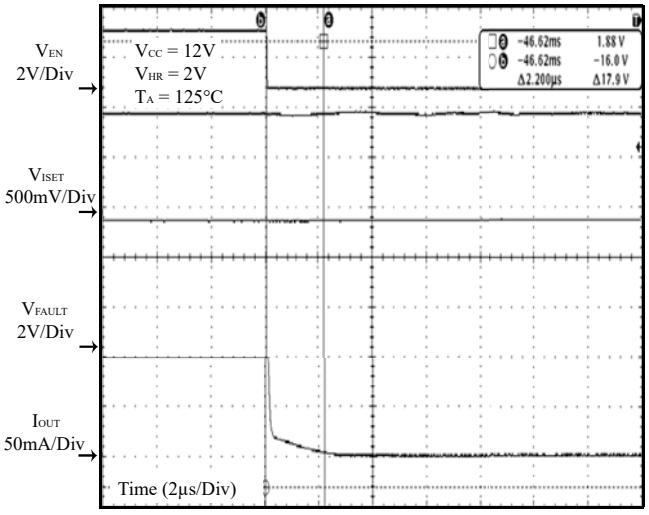


Figure 27 EN Off

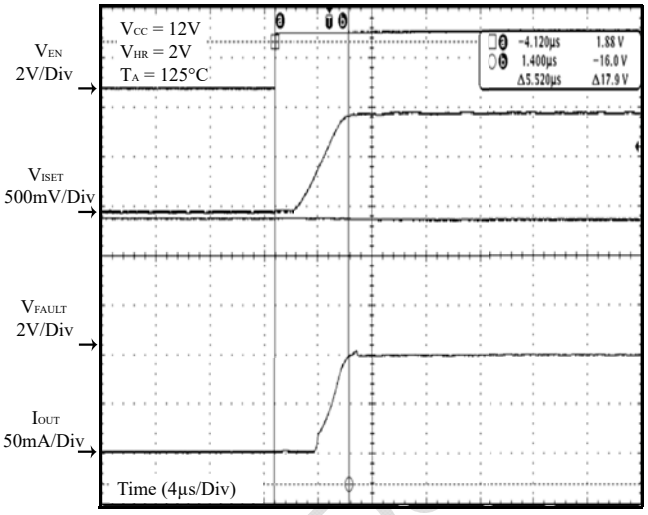


Figure 28 EN On

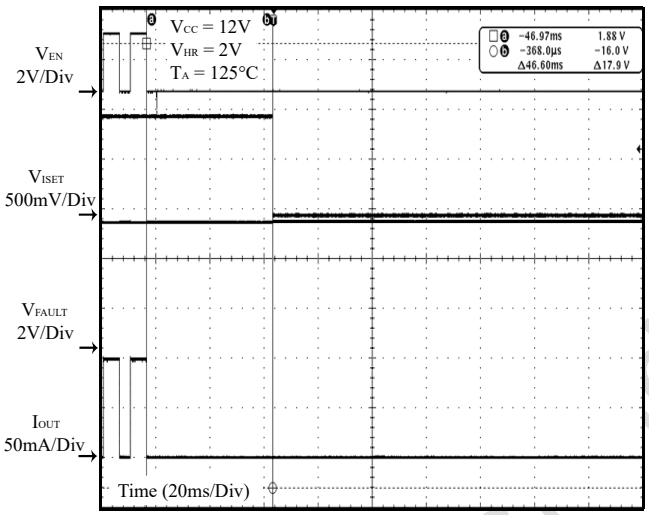


Figure 29 t_{SD}

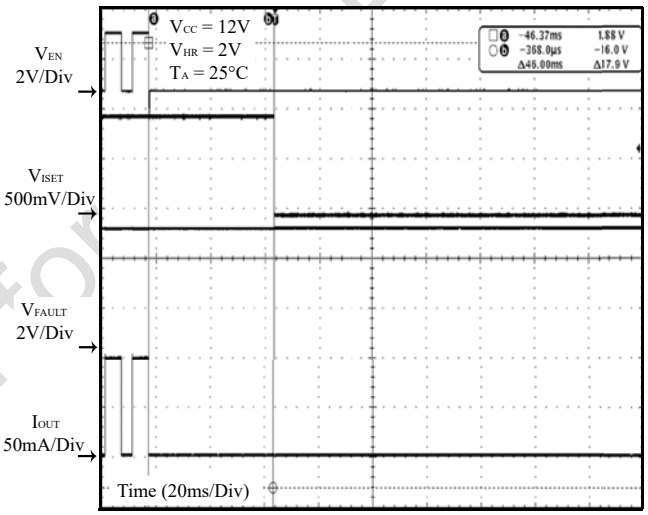


Figure 30 t_{SD}

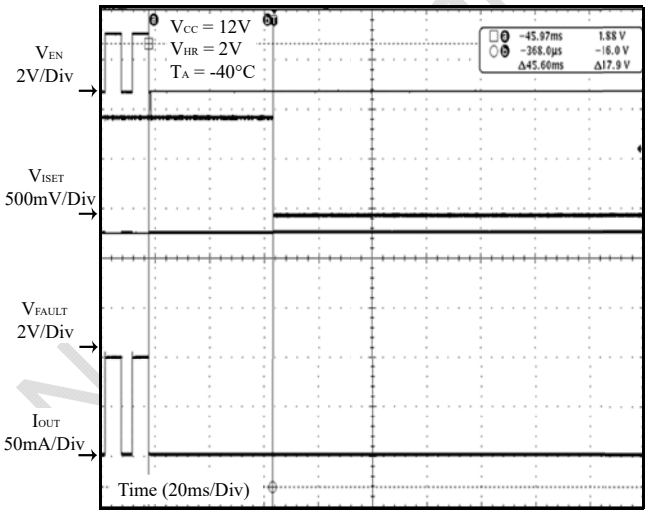
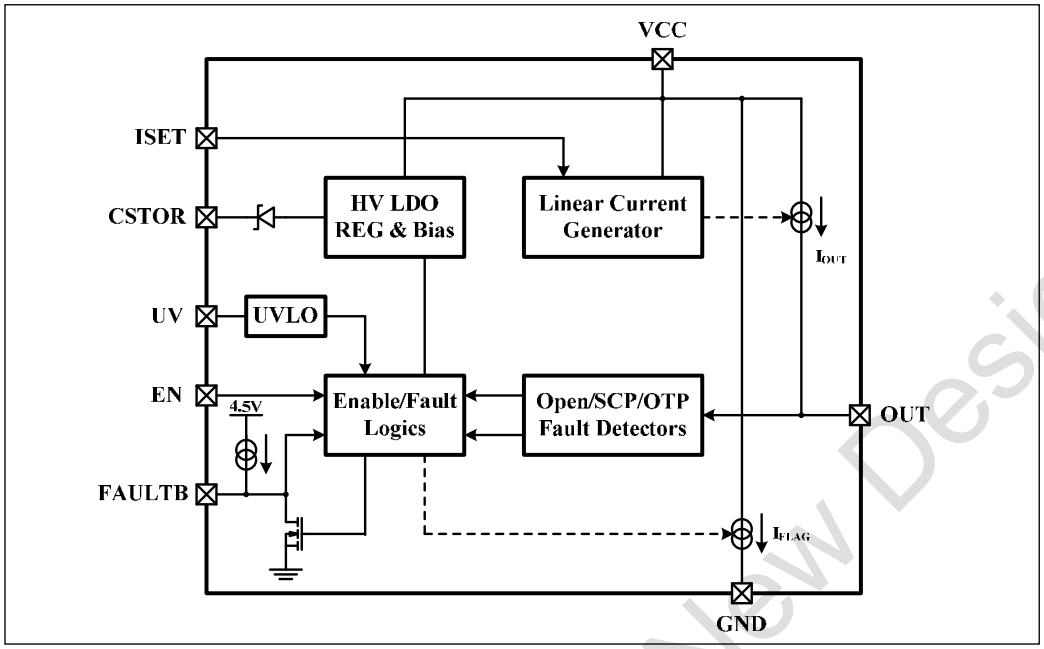


Figure 31 t_{SD}

FUNCTIONAL BLOCK DIAGRAM



APPLICATION INFORMATION

The IS32LT3125/3125A is a single channel linear current driver optimized to drive automotive interior or exterior LED light which can be dimmed via Power Supply Modulation (PSM) or by digitally driving the EN pin. The output current is set by a single reference resistor (R_{ISET}) and capable of 250mA.

OUTPUT CURRENT SETTING

A single resistor (R_{ISET}) controls the maximum output current for the channel. The resistor value for a specific current level is calculated using the following Equation (1):

$$R_{ISET} = \frac{2000}{I_{SET}} \qquad (1)$$

($8k\Omega \le R_{ISET} \le 80k\Omega$)

R_{ISET} need to be chosen 1% accuracy resistor with good temperature characteristic to ensure stable output current.

The device is protected from an output overcurrent condition caused by a too low value R_{ISET}, by internally limiting the maximum current to 300mA (Typ.). If ISET pin is open, the output will be off and FAULTB will be pulled low.

POWER SUPPLY MODULATION DIMMING

The IS32LT3125/3125A can operate with Power Supply Modulation (PSM) where the device's power supply is pulse width modulated to achieve LED dimming. The IS32LT3125/3125A stability is not affected by operation with PSM. To get better dimming linearity, the recommended PSM frequency can be in the range of 100Hz to 300Hz, (200Hz Typ.) and input capacitor, C_{VCC}, should be low value (0.1uF typical) to ensure rapid discharge during PSM low period.

CSTOR OPERATION

To keep the IC operating normally during condition of PSM when V_{CC} goes to zero, C_{STOR} capacitor provides the keep-alive current needed to power the digital counter and the fault flag circuits. A capacitor value of 2.2μF is recommended. The keep-alive time could be roughly calculated by the following Equation (2):

$$t_{alive} = \frac{2.5V \times C_{STOR}}{I_{CST}} \qquad (2)$$

EN PIN OPERATION

The voltage at the EN pin must be higher than V_{EN} to enable the IC and below (V_{EN}-V_{ENHY}) to disable the IC. The EN pin of the IS32LT3125/3125A can accept a PWM signal to implement LED dimming. LED average current may be computed using the following Equation (3).

$$I_{LED} = I_{MAX} \times D_{PWM} \qquad (3)$$

I_{MAX} is computed using Equation (1) and D_{PWM} is the duty cycle. To guarantee a reasonably good dimming effect, recommend PWM frequency in the range of 100Hz ~ 1kHz. Driving the EN pin with a PWM signal can effectively adjust the LED intensity. The PWM signal voltage levels must meet the EN pin input voltage levels, V_{EN}. Pull up to VCC via a 10KΩ resister when EN pin is unused; do not leave it floating.

UNDER VOLTAGE PIN OPERATION

The IC has an internal VCC UVLO (Under Voltage Lock Out) set at V_{UVLO}. However, it may be desirable to externally set an UVLO to track the number of LED's used in the string. For PSM dimming application, the higher UVLO will track the PSM off time to a pre-determined VCC level. In addition, it is necessary to prevent false LED open detection due to the LED string losing its headroom voltage, such as when VCC rises up from zero during power up or PSM dimming. The UV pin can be used to set a VCC under voltage lockout threshold via a resistor divider.

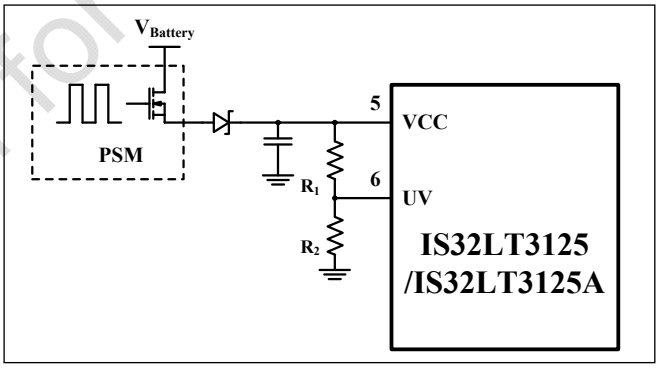


Figure 32 UV Pin Operation

This external UVLO threshold voltage can be computed using the following Equation (4):

$$V_{CC\_UVLO} = V_{UV} \times \frac{R_1 + R_2}{R_2} \qquad (4)$$

Pull up to VCC using a 10kΩ resister when UV pin is unused; do not leave it floating.

To prevent false open detection, the external UVLO threshold voltage should be set at Equation (5):

$$V_{CC\_UVLO} > V_{LED\_MAX} + V_{OCD} \qquad (5)$$

Where V_{LED_MAX} is the maximum LED string forward voltage on the output channel.

OUTPUT STATE DETECTION AND FAULT DIAGNOSTIC

IS32LT3125/3125A offers a fault diagnostic function. LED string open/short, output shorted to GND/VCC,

ISET pin short/open or thermal shutdown will trigger this function.

An output shorted to GND or VCC is detected as a fault if the OUT pin voltage drops below the short detect voltage threshold V_{SCD} or VCC to OUT drop voltage is lower than V_{OCD} and remains below the threshold for t_{FD}. Then the channel will change to source a 4mA current for recovery detection. The FAULTB pin will be pulled low and the V_{CC} standby current will increase to I_{SD_FLT} (typical, 30mA for IS32LT3125, 1mA for IS32LT3125A) to indicate the fault condition. This state will recover after the fault condition is removed.

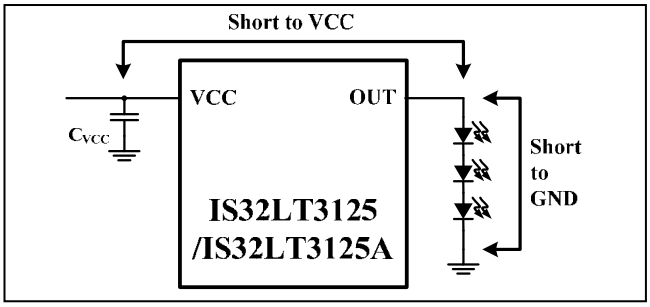


Figure 33 OUT Pin Shorted Operation

In the event the LED channel is open circuited, the OUT pin voltage will go up close to V_{CC}. If VCC to OUT drop voltage remains below the threshold V_{OCD} for t_{FD}, the channel will change to source a 4mA current for recovery detection. The FAULTB pin will be pulled low and the V_{CC} standby current will increase to I_{SD_FLT} (typical, 30mA for IS32LT3125, 1mA for IS32LT3125A) to indicate the fault condition. The state will recover after the open condition is removed.

If the ISET pin is either shorted or open for t_{FD} deglitch time, the channel will turn off. The FAULTB pin will pull low and the V_{CC} standby current will increase to I_{SD_FLT} (typical, 30mA for IS32LT3125, 1mA for IS32LT3125A) to indicate the fault condition. The state will recover after the fault condition is removed.

FAULTB PARALLEL INTERCONNECTION

For LED lighting systems which require the complete lighting system be shut down when a fault is detected, the FAULTB pin can be used in a parallel connection with multiple IS32LT3125/3125A devices as shown in Figure 2. A detected fault output by one device (fault master device) will pull low the FAULTB pins of the other parallel connected devices (fault slave devices) and simultaneously turn them off. This satisfies the "One-Fail-All-Fail" operating requirement. For IS32LT3125, only the fault master device has 30mA V_{CC} standby current indication.

THERMAL SHUTDOWN

To protect the IC from damage due to high power dissipation, the temperature of the die is monitored. In the event that the die temperature exceeds 165°C, the device will go into shutdown mode. The channel (OUT) will turn off. The FAULTB pin will pull low and the V_{CC} standby current will increase to I_{SD_FLT} (typical, 30mA for IS32LT3125, 1mA for IS32LT3125A) to indicate the fault condition. At this point, the IC begins to cool off. Any attempt to enable the channel back to the source condition before the IC cooled to T_J<140°c will be blocked and the IC will not be allowed to restart. The device will not resume operation until the junction temperature goes below 140°C.

Table 1 Fault Table

Fault Type	Fault Condition	Output Channel	VCC Current	FAULTB	Recovery
ISET open	ISET pin current close to zero	Off	IS32LT3125: typical 30mA IS32LT3125A: typical 1mA	Low	ISET pin current goes back normal
ISET short	ISET pin voltage close to zero	Off			ISET pin voltage goes back normal
LED string open (OUT shorted to VCC)	$(V_{CC}-V_{OUT})<V_{OCD}$	4mA for recovery detection			$(V_{CC}-V_{OUT})>(V_{OCD}+V_{OCD\_HY})$
Thermal shutdown	$T_J>T_{SD}$	Off			$T_J<(T_{SD}-T_{HY})$
LED string shorted (OUT shorted to GND)	$V_{OUT}<V_{SCD}$	4mA for recovery detection	IS32LT3125: typical 30mA IS32LT3125A: typical 5mA		$V_{OUT}>(V_{SCD}+V_{SCD\_HY})$
One-Fail-All-Fail (FAULTB parallel interconnection)	$V_{FAULTB}<V_{FAULTB\_IL}$	Off	IS32LT3125 master: typical 30mA IS32LT3125 slave: typical 1mA	Externally pulled low	$V_{FAULTB}>V_{FAULTB\_IH}$
			IS32LT3125A: typical 1mA		

THERMAL CONSIDERATIONS

The package thermal resistance, $R_{\theta JA}$, determines the amount of heat that can pass from the silicon die to the surrounding ambient environment. The $R_{\theta JA}$ is a measure of the temperature rise created by power dissipation and is usually measured in degree Celsius per watt (°C/W). The junction temperature, T_J, can be calculated by the rise of the silicon temperature, ΔT, the power dissipation, P_D, and the package thermal resistance, $R_{\theta JA}$, as in Equation (6) and (7):

$$P_D = V_{CC} \times I_{CC} + (V_{CC} - V_{OUT}) \times I_{OUT} \quad (6)$$

and,

$$T_J = T_A + \Delta T = T_A + P_D \times R_{\theta JA} \qquad (7)$$

Where V_{CC} is the supply voltage, V_{OUT} is the OUT pin voltage and T_A is the ambient temperature.

When operating the chip at high ambient temperatures, or when driving maximum load current, care must be taken to avoid exceeding the package power dissipation limits. The maximum power dissipation can be calculated using the following Equation (8):

$$P_{D(MAX)} = \frac{125°C - 25°C}{\theta_{JA}} \qquad (8)$$

So,

$$P_{D(MAX)} = \frac{125°C - 25°C}{43.3°C/W} \approx 2.31W$$

Figure 34 shows the power derating of the IS32LT3125/3125A on a JEDEC boards (in accordance with JESD 51-5 and JESD 51-7) standing in still air.

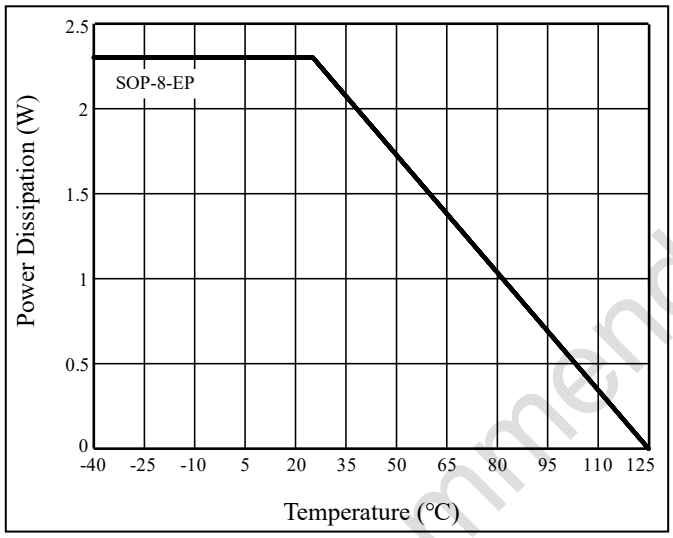


Figure 34 Dissipation Curve (SOP-8-EP)

The thermal resistance is achieved by mounting the IS32LT3125/3125A on a standard FR4 double-sided printed circuit board (PCB) with a copper area of a few square inches on each side of the board under the IS32LT3125/3125A. Multiple thermal vias, as shown in Figure 35, help to conduct the heat from the exposed pad of the IS32LT3125/3125A to the copper on each side of the board. The thermal resistance can be reduced by using a metal substrate or by adding a heatsink.

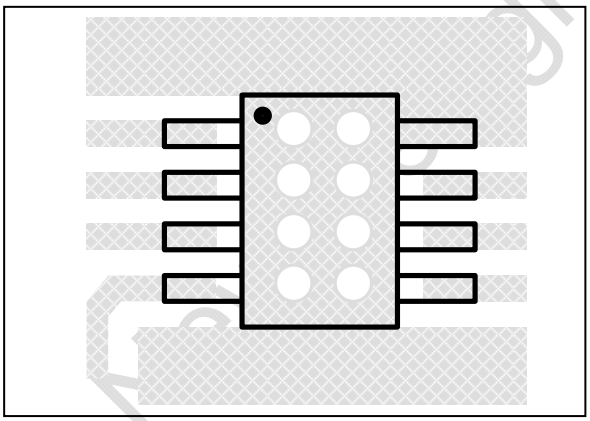


Figure 35 Board Via Layout For Thermal Dissipation

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

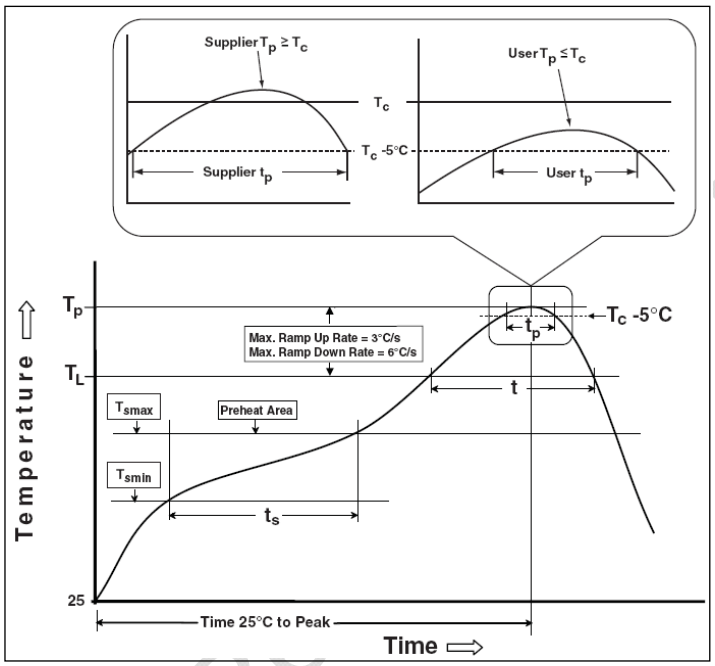
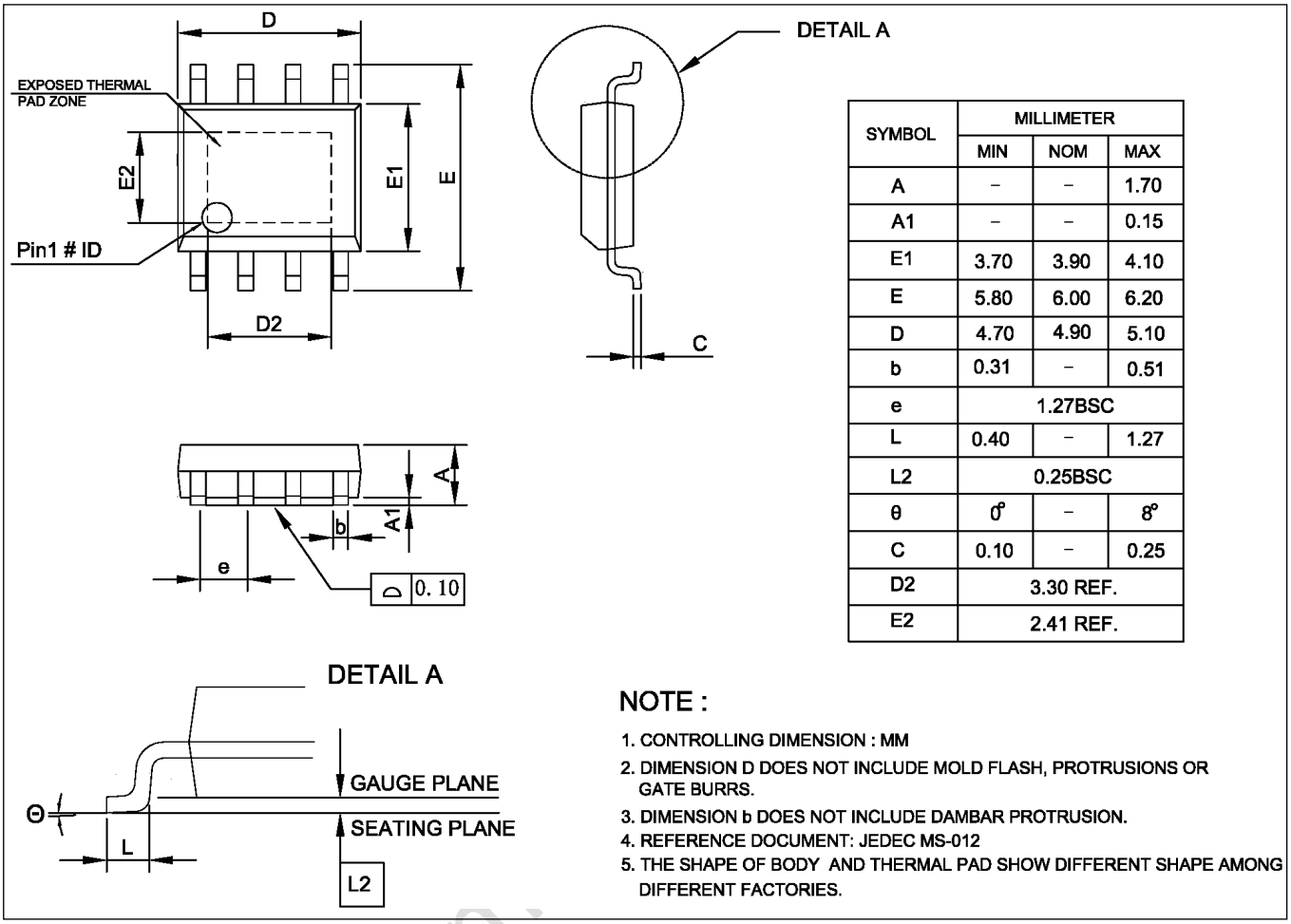


Figure 36 Classification Profile

PACKAGE INFORMATION

SOP-8-EP



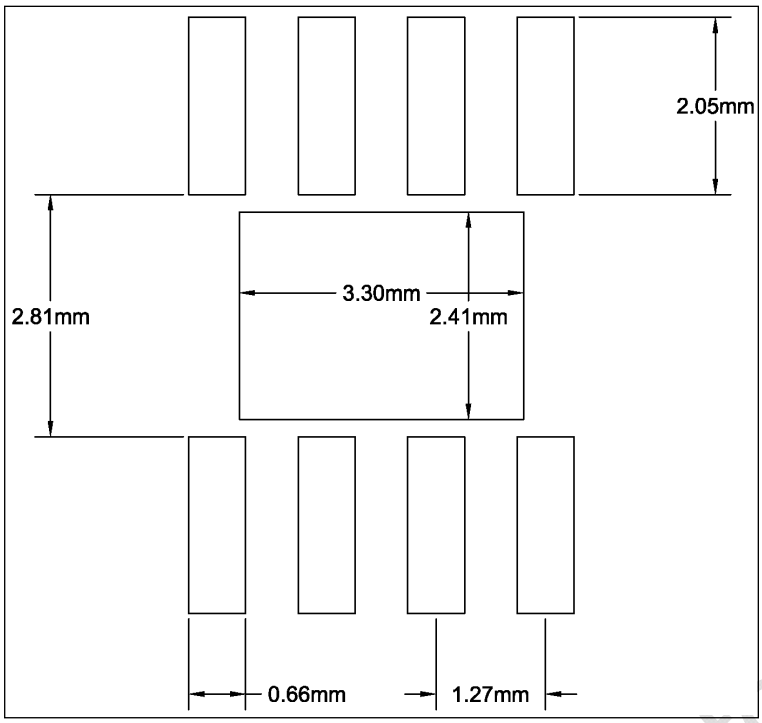
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	–	–	1.70
A1	–	–	0.15
E1	3.70	3.90	4.10
E	5.80	6.00	6.20
D	4.70	4.90	5.10
b	0.31	–	0.51
e	1.27BSC		
L	0.40	–	1.27
L2	0.25BSC		
θ	0°	–	8°
C	0.10	–	0.25
D2	3.30 REF.		
E2	2.41 REF.		

NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.
4. REFERENCE DOCUMENT: JEDEC MS-012
5. THE SHAPE OF BODY AND THERMAL PAD SHOW DIFFERENT SHAPE AMONG DIFFERENT FACTORIES.

RECOMMENDED LAND PATTERN

SOP-8-EP



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. user's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
0A	Initial release	2017.10.23
0B	Update curves and detail description	2018.01.05
A	Update EC parameters, POD and LP	2020.06.08
B	Add NRND watermark	2022.06.14