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ON Semiconductor®

# FDP085N10A

# N-Channel PowerTrench<sup>®</sup> MOSFET 100 V, 96 A, 8.5 m $\Omega$

#### **Features**

- $R_{DS(on)}$  = 7.35 m $\Omega$  (Typ.) @  $V_{GS}$  = 10 V,  $I_D$  = 96 A
- · Fast Switching Speed
- Low Gate Charge, Q<sub>G</sub> = 31 nC (Typ.)
- High Performance Trench Technology for Extremely Low  $R_{\mbox{\footnotesize{DS}}(\mbox{\footnotesize{on}})}$
- · High Power and Current Handling Capability
- · RoHS Compliant

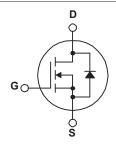
## **Description**

This N-Channel MOSFET is produced using ON Semiconductor's PowerTrench® process that has been tailored to minimize the on-state resistance while maintaining superior switching performance.

### **Applications**

- Synchronous Rectification for ATX / Server / Telecom PSU
- · Battery Protection Circuit
- · Motor Drives and Uninterruptible Power Supplies





## **MOSFET Maximum Ratings** $T_C = 25^{\circ}C$ unless otherwise noted.

Symbol		FDP085N10A-F102	Unit	
$V_{DSS}$	Drain to Source Voltage	100	V	
$V_{GSS}$	Gate to Source Voltage		±20	V
I-	Drain Current	- Continuous (T <sub>C</sub> = 25°C)	96	Α
ID	Diam Current	- Continuous (T <sub>C</sub> = 100°C)	68	
I <sub>DM</sub>	Drain Current	- Pulsed (Note	1) 384	Α
E <sub>AS</sub>	Single Pulsed Avalanche E	nergy (Note	2) 269	mJ
dv/dt	Peak Diode Recovery dv/dt	: (Note	3) 6.0	V/ns
P <sub>D</sub>	Power Dissipation	$(T_C = 25^{\circ}C)$	188	W
' D	- Derate Above 25°C		1.25	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Ten	-55 to +175	°C	
$T_L$	Maximum Lead Temperatur	re for Soldering, 1/8" from Case for 5 Seconds	300	°C

#### **Thermal Characteristics**

Symbol	Parameter	FDP085N10A-F102	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.8	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	C/VV

# **Package Marking and Ordering Information**

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDP085N10A-F102	FDP085N10A	TO-220	Tube	N/A	N/A	50 units

# **Electrical Characteristics** $T_C = 25^{\circ}C$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Off Charac	cteristics					
BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V, T_C = 25^{\circ} C$	100	-	-	V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	$I_D$ = 250 $\mu$ A, Referenced to 25°C	-	0.07	-	V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 80 V, V <sub>GS</sub> = 0 V	-	-	1	μА
		$V_{DS} = 80 \text{ V}, T_{C} = 150^{\circ}\text{C}$	-	-	500	μΑ
I <sub>GSS</sub>	Gate to Body Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	-	-	±100	nA

#### **On Characteristics**

V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$	2.0	-	4.0	V
R <sub>DS(on)</sub>	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 96 \text{ A}$	-	7.35	8.5	mΩ
9 <sub>FS</sub>	Forward Transconductance	$V_{DS} = 10 \text{ V}, I_{D} = 96 \text{ A}$	-	72	-	S

## **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	.,		-	2025	2695	pF
C <sub>oss</sub>	Output Capacitance	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1  MHz		-	468	620	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	1 - 1 1/11/12		-	20	-	pF
C <sub>oss(er)</sub>	Energy Releted Output Capacitance	V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 0 V		-	752	-	pF
Q <sub>g(tot)</sub>	Total Gate Charge at 10V			-	31	40	nC
$Q_{gs}$	Gate to Source Gate Charge	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 50 V,		-	9.7	-	nC
Q <sub>gs2</sub>	Gate Charge Threshoid to Plateau	I <sub>D</sub> = 96 A		-	5.0	-	nC
Q <sub>gd</sub>	Gate to Drain "Miller" Charge	(No	te 4)	-	7.5	-	nC
ESR	Equivalent Series Resistance (G-S)	f = 1 MHz		-	0.97	-	Ω

## **Switching Characteristics**

t <sub>d(on)</sub>	Turn-On Delay Time		-	18	46	ns
t <sub>r</sub>		$V_{DD} = 50 \text{ V}, I_{D} = 96 \text{ A},$	-	22	54	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	$V_{GS} = 10 \text{ V}, R_G = 4.7 \Omega$	-	29	68	ns
t <sub>f</sub>	Turn-Off Fall Time	(Note 4)	-	8	26	ns

#### **Drain-Source Diode Characteristics**

I <sub>S</sub>	Maximum Continuous Drain to Source Diode Forward Current			-	96	Α
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode Forward Current			-	384	Α
$V_{SD}$	Drain to Source Diode Forward Voltage V <sub>GS</sub> = 0 V, I <sub>SD</sub> = 96 A		-	-	1.3	V
t <sub>rr</sub>	Reverse Recovery Time	$V_{DD} = 50 \text{ V}, V_{GS} = 0 \text{ V}, I_{SD} = 96 \text{ A},$	-	59	-	ns
Q <sub>rr</sub>	Reverse Recovery Charge	$dI_F/dt = 100 A/\mu s$	-	80	-	nC

#### Notes

- 1. Repetitive rating: pulse-width limited by maximum junction temperature.
- 2. L = 3 mH, I<sub>AS</sub> = 13.4 A, R<sub>G</sub> = 25  $\Omega$ , starting T<sub>J</sub> = 25°C.
- 3.  $I_{SD} \le 96$  A, di/dt  $\le 200$  A/ $\mu$ s,  $V_{DD} \le BV_{DSS}$ , starting  $T_J = 25^{\circ}C$ .
- 4. Essentially independent of operating temperature typical characteristics.

## **Typical Performance Characteristics**

Figure 1. On-Region Characteristics

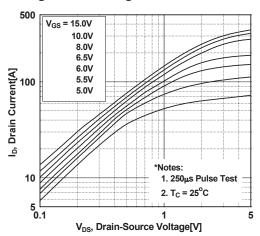
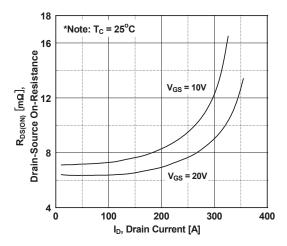


Figure 3. On-Resistance Variation vs.

Drain Current and Gate Voltage



**Figure 5. Capacitance Characteristics** 

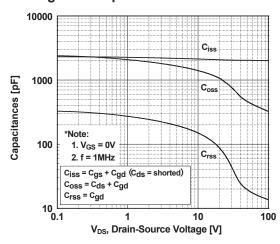


Figure 2. Transfer Characteristics

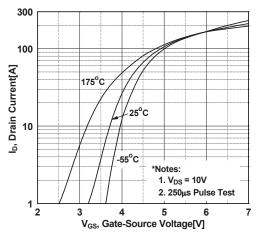


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

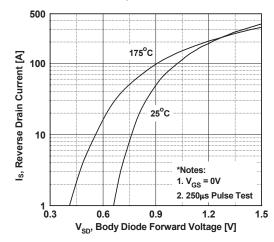
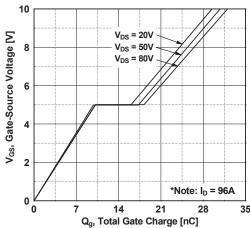


Figure 6. Gate Charge Characteristics



## **Typical Performance Characteristics** (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

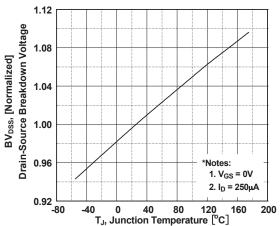


Figure 9. Maximum Safe Operating Area

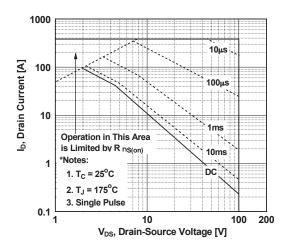


Figure 11. Eoss vs. Drain to Source Voltage

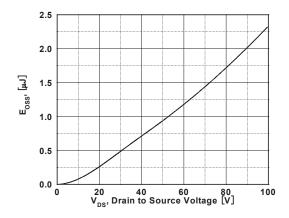


Figure 8. On-Resistance Variation vs. Temperature

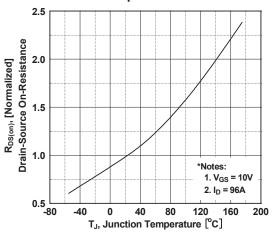


Figure 10. Maximum Drain Current vs. Case Temperature

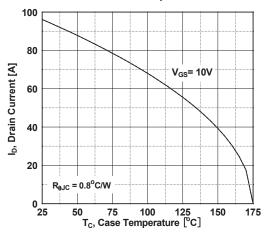
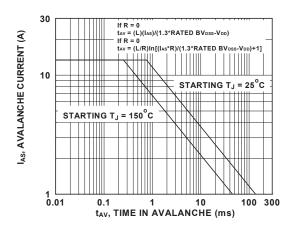
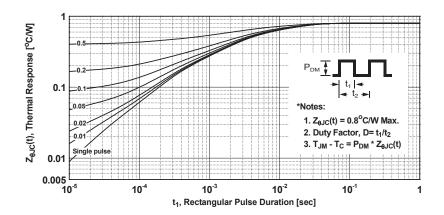


Figure 12. Unclamped Inductive Switching Capability



# **Typical Performance Characteristics** (Continued)

Figure 13. Transient Thermal Response Curve



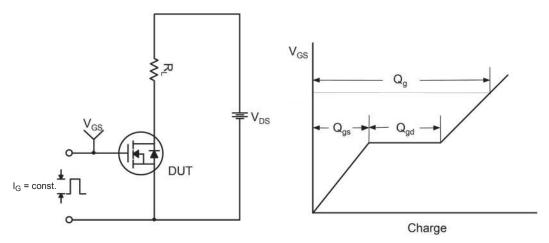


Figure 14. Gate Charge Test Circuit & Waveform

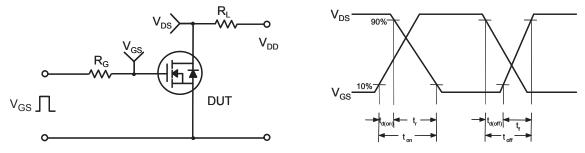


Figure 15. Resistive Switching Test Circuit & Waveforms

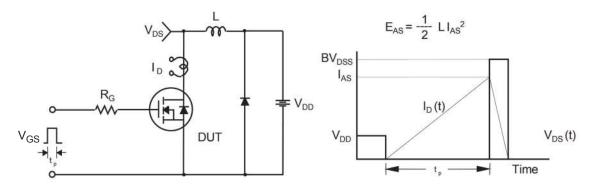
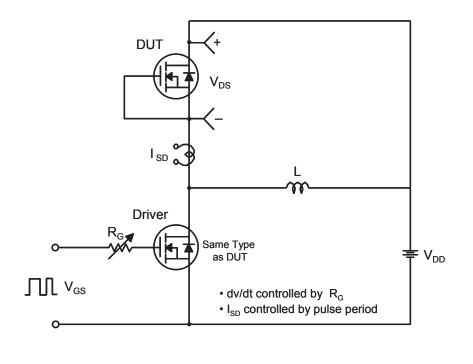


Figure 16. Unclamped Inductive Switching Test Circuit & Waveforms



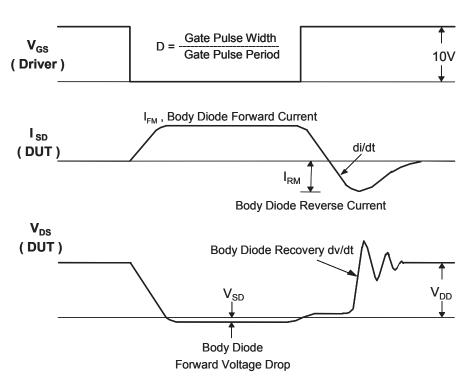
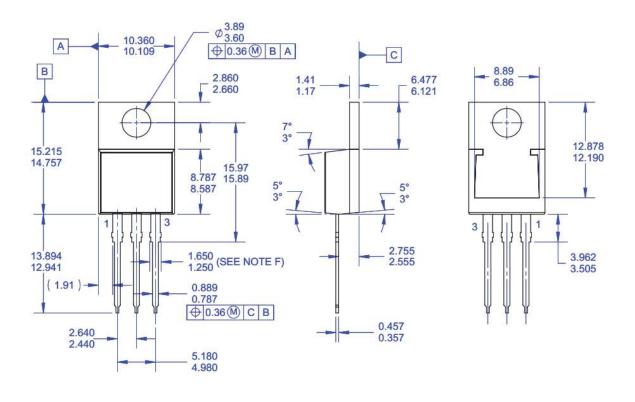
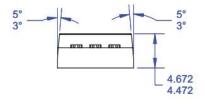


Figure 17. Peak Diode Recovery dv/dt Test Circuit & Waveforms

#### **Mechanical Dimensions**





#### NOTES:

- A. PACKAGE REFERENCE: JEDEC TO220 **VARIATION AB**
- B. ALL DIMENSIONS ARE IN MILLIMETERS. C. DIMENSION AND TOLERANCE AS PER ASME
- Y14.5-1994. D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS. E. THIS PACKAGE IS FSZZ INTERNAL PRODUCTION
- AND INTENDED FOR DELTA CUSTOMER ONLY.
- F. MAX WIDTH FOR F102 DEVICE = 1.35mm. G. DRAWING FILE NAME: TO220T03REV3

Figure 18. TO-220, Molded, 3-Lead, Jedec Variation AB (Delta)

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