BUK9Y09-40B

N-channel TrenchMOS logic level FET

Rev. 04 — 7 April 2010 **Product data sheet**

1. Product profile

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Q101 compliant
- Suitable for logic level gate drive sources
- Suitable for thermally demanding environments due to 175 °C rating

1.3 Applications

- 12 V loads
- Automotive systems
- General purpose power switching
- Motors, lamps and solenoids

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C	-	-	40	V
I_D	drain current	$V_{GS} = 5$ V; $T_{mb} = 25$ °C; see Figure 1; see Figure 4	-	-	75	A
P_{tot}	total power dissipation	$T_{mb} = 25$ °C; see Figure 2	-	-	105.3	W
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 5$ V; $I_D = 25$ A; $T_j = 25$ °C; see Figure 11; see Figure 12	-	6.9	9	mΩ
		$V_{GS} = 10$ V; $I_D = 25$ A; $T_j = 25$ °C	-	5.8	8	mΩ

Table 1. Quick reference data *...continued*

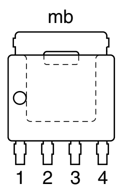
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 75 A; V_{sup} ≤ 40 V; R_{GS} = 50 Ω; V_{GS} = 5 V; $T_{j(init)}$ = 25 °C; unclamped	-	-	146	mJ
Dynamic characteristics						
Q_{GD}	gate-drain charge	V_{GS} = 5 V; I_D = 25 A; V_{DS} = 32 V; see Figure 13	-	11	-	nC

2. Pinning information

Table 2. Pinning information

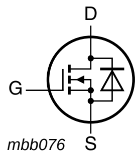
Pin	Symbol	Description
1	S	source
2	S	source
3	S	source
4	G	gate
mb	D	mounting base; connected to drain

Simplified outline



SOT669 (LFPAK)

Graphic symbol



3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9Y09-40B	LFPAK	plastic single-ended surface-mounted package (LFPAK); 4 leads	SOT669

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C		-	-	40	V
V_{DGR}	drain-gate voltage	R_{GS} = 20 kΩ		-	-	40	V
V_{GS}	gate-source voltage			-15	-	15	V
I_D	drain current	T_{mb} = 25 °C; V_{GS} = 5 V; see Figure 1; see Figure 4		-	-	75	A
		T_{mb} = 100 °C; V_{GS} = 5 V; see Figure 1		-	-	53	A
I_{DM}	peak drain current	T_{mb} = 25 °C; $t_p \leq 10$ µs; pulsed; see Figure 4		-	-	300	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; see Figure 2		-	-	105.3	W
T_{stg}	storage temperature			-55	-	175	°C
T_j	junction temperature			-55	-	175	°C
Source-drain diode							
I_S	source current	T_{mb} = 25 °C		-	-	75	A
I_{SM}	peak source current	$t_p \leq 10$ µs; pulsed; T_{mb} = 25 °C		-	-	300	A
Avalanche ruggedness							
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 75 A; $V_{sup} \leq 40$ V; R_{GS} = 50 Ω; V_{GS} = 5 V; $T_{j(init)}$ = 25 °C; unclamped		-	-	146	mJ
$E_{DS(AL)R}$	repetitive drain-source avalanche energy	see Figure 3	[1][2][3][4]	-	-	-	J

[1] Maximum value not quoted. Repetitive rating defined in avalanche rating figure.

[2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.

[3] Repetitive avalanche rating limited by an average junction temperature of 170 °C.

[4] Refer to application note AN10273 for further information.

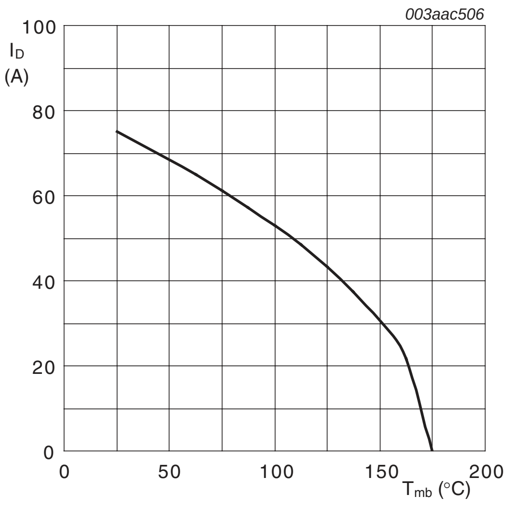
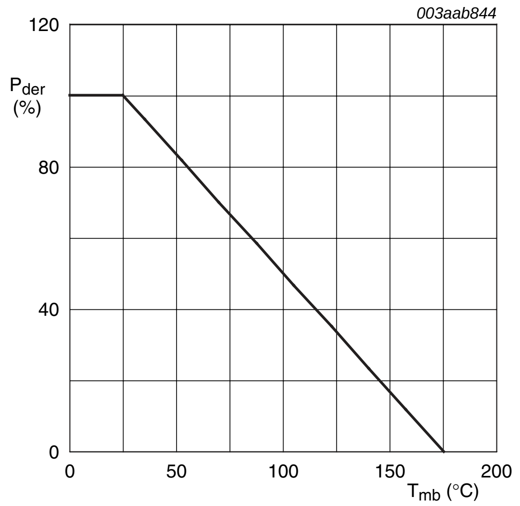


Fig 1. Continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100\,\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature

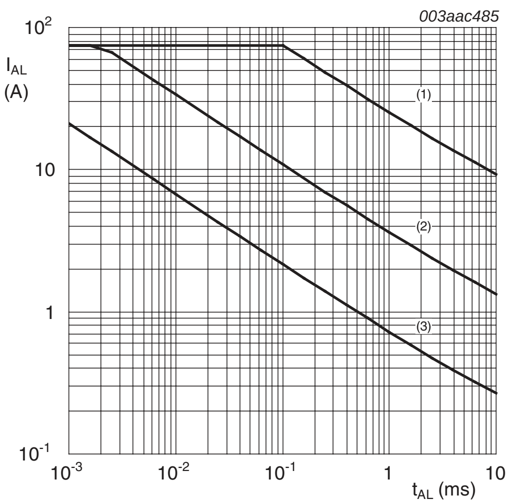
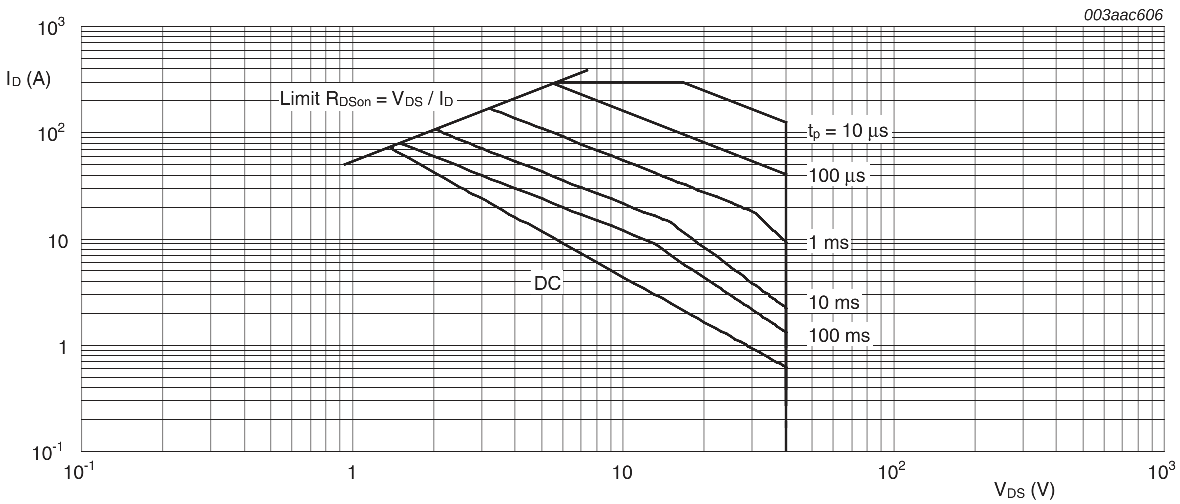


Fig 3. Single-pulse and repetitive avalanche rating; avalanche current as a function of avalanche time



$T_{mb} = 25\,°C; I_{DM}$ is single pulse

Fig 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 5	-	-	1.42	K/W

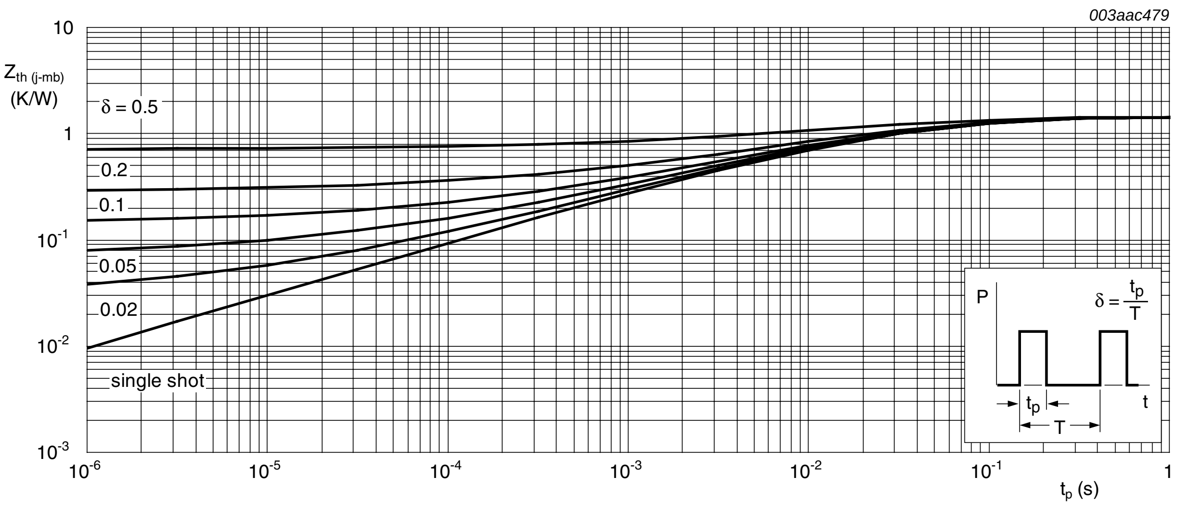
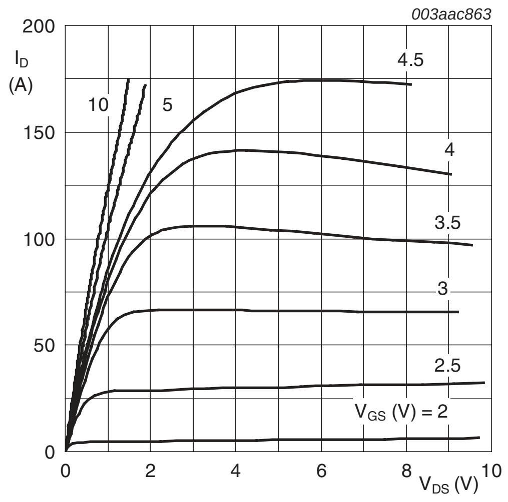


Fig 5. Transient thermal impedance from junction to mounting base as a function of pulse duration.

6. Characteristics

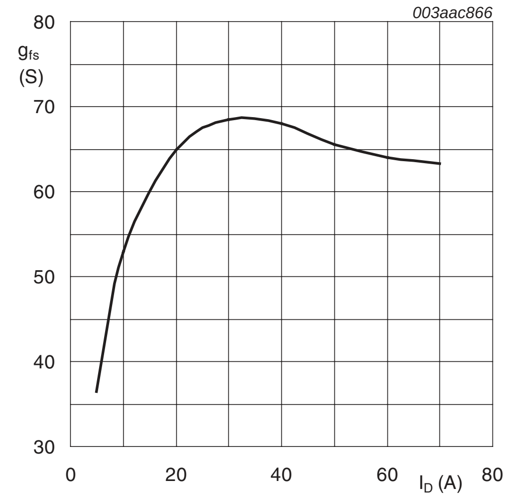
Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 0.25 mA; V_{GS} = 0 V; T_j = -55 °C	36	-	-	V
		I_D = 0.25 mA; V_{GS} = 0 V; T_j = 25 °C	40	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C; see Figure 9; see Figure 10	1.25	1.65	2.15	V
V_{GSth}	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 175 °C; see Figure 9; see Figure 10	0.5	-	-	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 °C; see Figure 9; see Figure 10	-	-	2.45	V
I_{DSS}	drain leakage current	V_{DS} = 40 V; V_{GS} = 0 V; T_j = 25 °C	-	0.02	1	µA
		V_{DS} = 40 V; V_{GS} = 0 V; T_j = 175 °C	-	-	500	µA
I_{GSS}	gate leakage current	V_{DS} = 0 V; V_{GS} = 15 V; T_j = 25 °C	-	2	100	nA
		V_{DS} = 0 V; V_{GS} = -15 V; T_j = 25 °C	-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 5 V; I_D = 25 A; T_j = 25 °C; see Figure 11; see Figure 12	-	6.9	9	mΩ
		V_{GS} = 4.5 V; I_D = 25 A; T_j = 25 °C	-	-	10	mΩ
		V_{GS} = 5 V; I_D = 25 A; T_j = 175 °C; see Figure 12	-	-	19	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C	-	5.8	8	mΩ
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 32 V; V_{GS} = 5 V; see Figure 13	-	30	-	nC
Q_{GS}	gate-source charge		-	6.5	-	nC
Q_{GD}	gate-drain charge		-	11	-	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; T_j = 25 °C; see Figure 14	-	2150	2866	pF
C_{oss}	output capacitance		-	378	454	pF
C_{rss}	reverse transfer capacitance		-	194	266	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 30 V; R_L = 1.2 Ω; V_{GS} = 5 V; $R_{G(ext)}$ = 10 Ω	-	29	-	ns
t_r	rise time		-	92	-	ns
$t_{d(off)}$	turn-off delay time		-	97	-	ns
t_f	fall time		-	83	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C; see Figure 15	-	0.85	1.2	V
t_{rr}	reverse recovery time	I_S = 20 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 30 V	-	40	-	ns
Q_r	recovered charge		-	66	-	nC



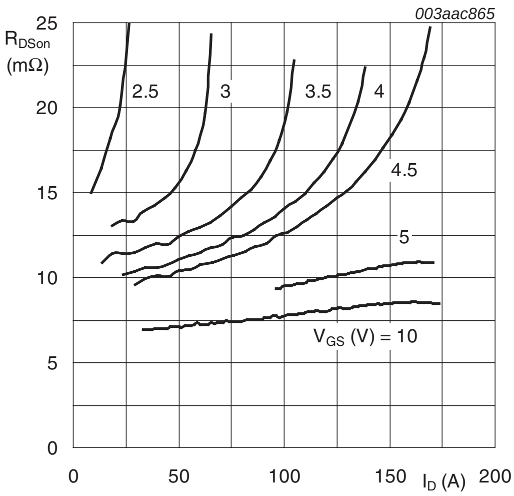
$T_j = 25\,°C$

Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values.



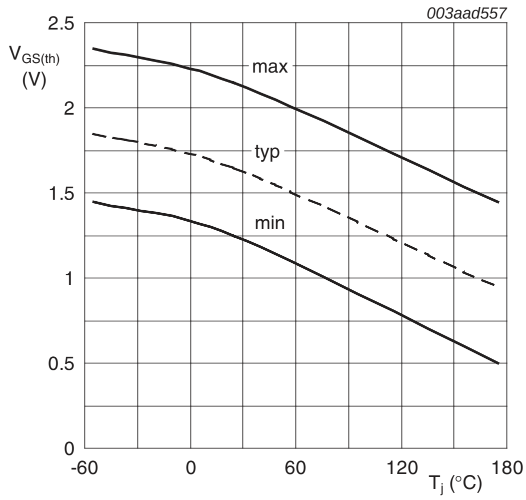
$T_j = 25\,°C; V_{DS} = 25\,V$

Fig 7. Forward transconductance as a function of drain current; typical values.



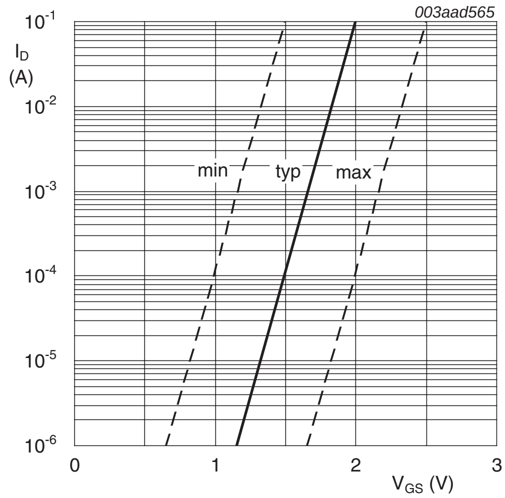
$T_j = 25\,°C$

Fig 8. Drain-source on-state resistance as a function of drain current; typical values.



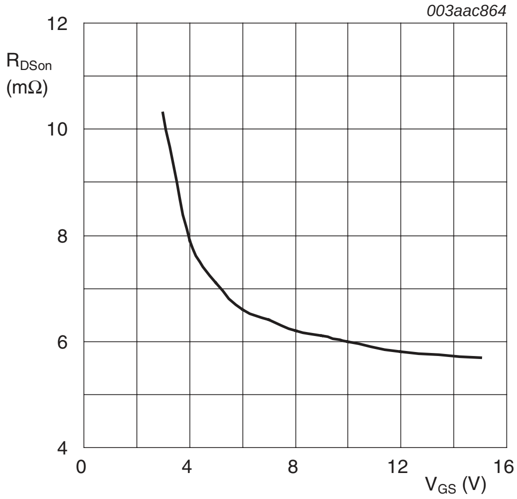
$I_D = 1\,mA; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature



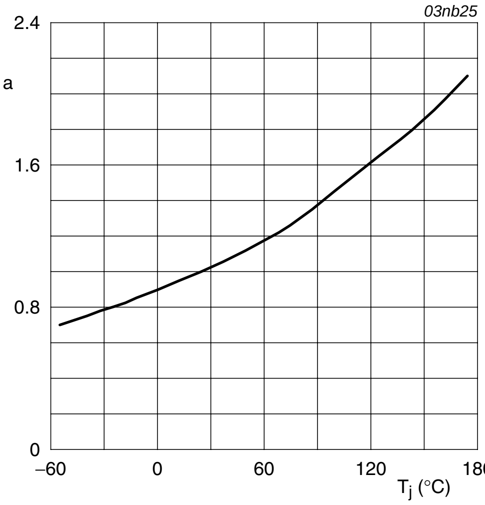
$$T_j = 25\,°C; V_{DS} = V_{GS}$$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



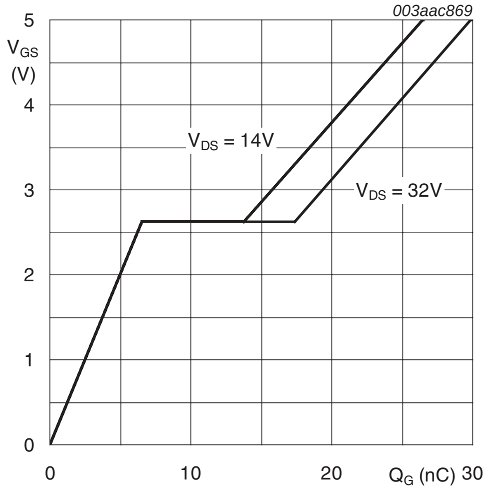
$$T_j = 25\,°C; I_D = 25A$$

Fig 11. Drain-source on-state resistance as a function of gate-source voltage; typical values.



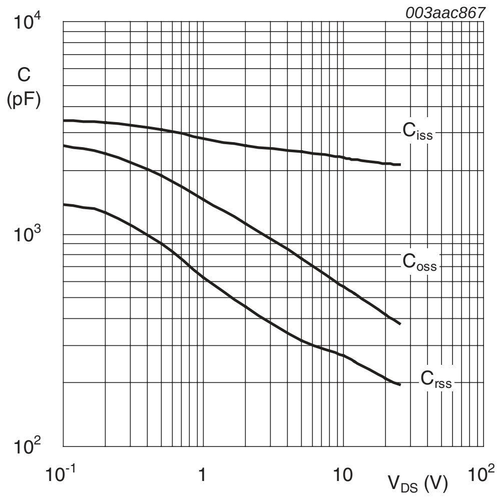
$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature



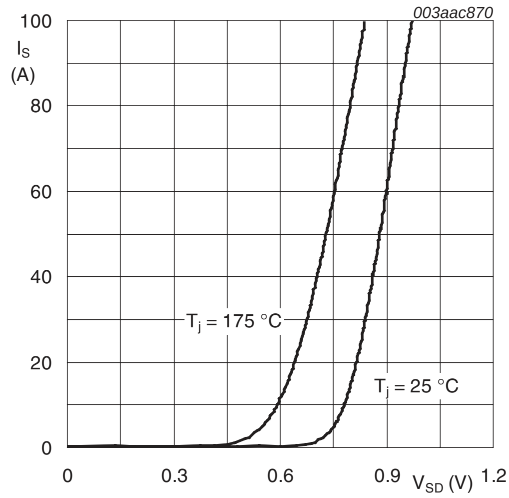
$$T_j = 25\,°C; I_D = 25A$$

Fig 13. Gate-source voltage as a function of turn-on gate charge; typical values.



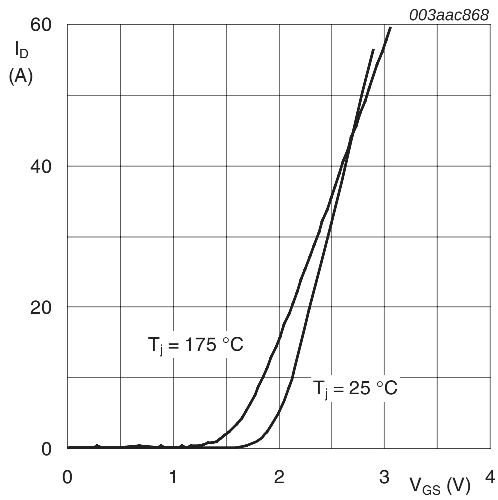
$V_{GS} = 0V; f = 1MHz$

Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



$V_{GS} = 0V$

Fig 15. Reverse diode current as a function of reverse diode voltage; typical values.

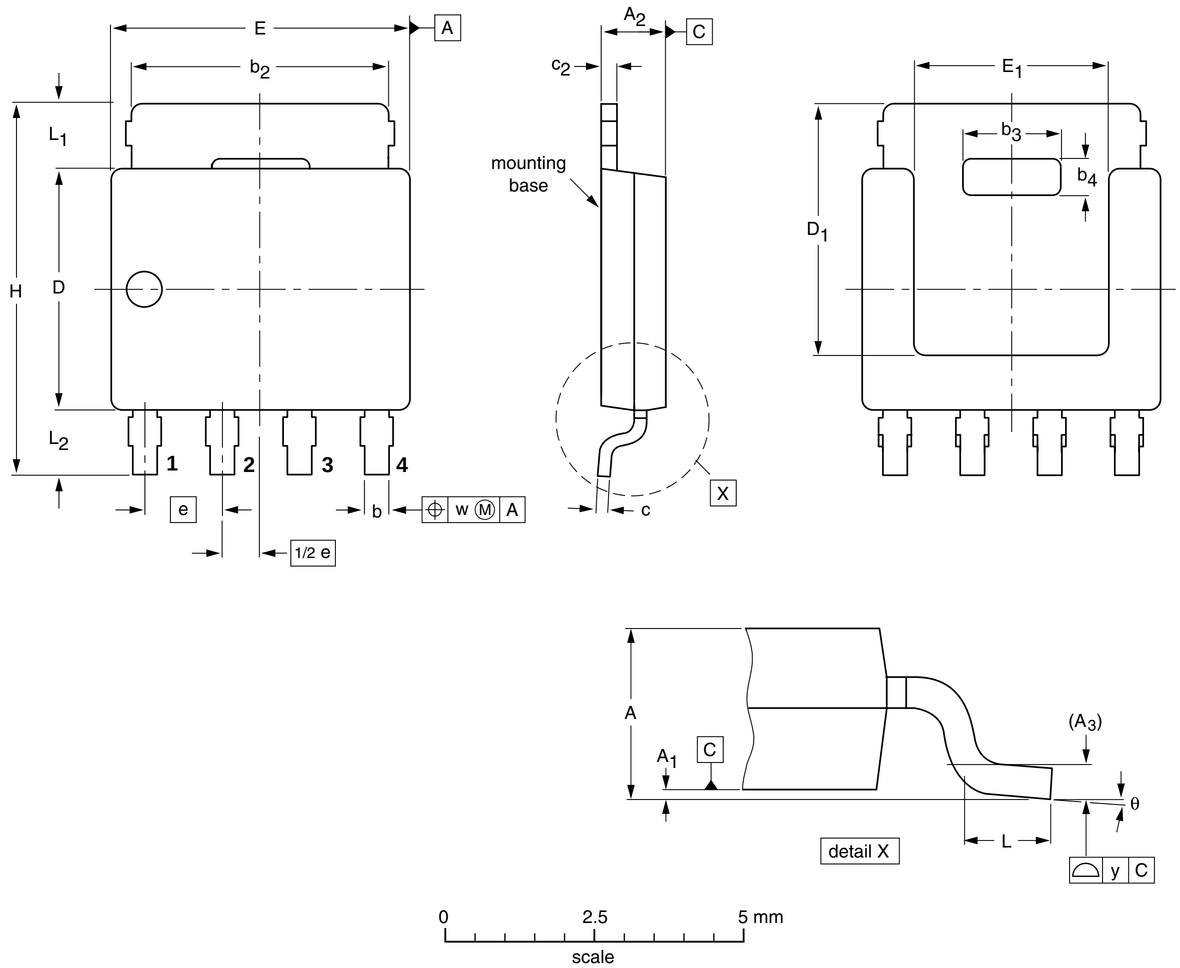


$V_{DS} = 25V$

Fig 16. Transfer characteristics: drain current as a function of gate-source voltage; typical values.

7. Package outline

Plastic single-ended surface-mounted package (LFPAK); 4 leads **SOT669**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	A_2	A_3	b	b_2	b_3	b_4	c	c_2	D(1)	D_1(1) max	E(1)	E_1(1)	e	H	L	L_1	L_2	w	y	θ
mm	1.20 1.01	0.15 0.00	1.10 0.95	0.25	0.50 0.35	4.41 3.62	2.2 2.0	0.9 0.7	0.25 0.19	0.30 0.24	4.10 3.80	4.20	5.0 4.8	3.3 3.1	1.27	6.2 5.8	0.85 0.40	1.3 0.8	1.3 0.8	0.25	0.1	8° 0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT669		MO-235				~~04-10-13~~ 06-03-16

Fig 17. Package outline SOT669 (LFPAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK9Y09-40B_4	20100407	Product data sheet	-	BUK9Y09-40B_3
Modifications:	• Status changed from objective to product.			
BUK9Y09-40B_3	20100215	Objective data sheet	-	BUK9Y09-40B_2

9. Legal information

9.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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11. Contents

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