

TWR-KL43Z Tower Module

User's Guide

1 TWR-KL43Z

The TWR-KL43Z microcontroller module is designed to work either in standalone mode or as part of the Freescale Tower System, a modular development platform that enables rapid prototyping and tool re-use through reconfigurable hardware. Take your design to the next level and begin constructing your Tower System today by visiting Freescale.com/Tower for additional Tower System MCU modules and compatible peripherals. For TWR-KL43Z specific information and updates, visit Freescale.com/TWR-KL43Z.

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Figure 1. Freescale Tower system overview

2 Contents

The TWR-KL43Z module includes:

- TWR-KL43Z board assembly
- Three-foot A to micro-B USB cable for debug interface and power
- Three-foot A to micro-B USB cable for MKL43Z256VLH4 USB interface
- Quick Start Guide
- TWRPI-sLCD

3 TWR-KL43Z features

- Tower compatible microcontroller module
- MKL43Z256VLH4 MCU (48 MHz, 256 KB Flash, 32 KB RAM, 16 KB ROM (Kibble), segment LCD low-power, 64 LQFP package)
- Dual role USB interface with Micro-AB USB connector
- Touch Tower plug-in/sLCD socket
- General purpose Tower plug-in (TWRPI) socket
- On-board debug circuit MK20 openSDA serial debug interface with virtual serial port and mass storage device bootloader
- 6-axis Xtrinsic sensor with integrated linear accelerometer and magnetometer (FXOS8700CQ)
- Four user-controllable LEDs
- Two (2) user pushbutton switch
- Infrared transmit and receive

- GPIO header for prototyping
- Potentiometer for ADC measurements
- 32.768 clock for RTC operation
- Power selectable 3.3V/1.8V

4 Get to know the TWR-KL43Z



Figure 2. Front side of TWR-KL43Z48M module (TWRPI device not attached)

5 Reference documents

Reference the documents listed below for more information on the Kinetis family, Tower System, and MCU modules. These can be found in the documentation section at Freescale.com/TWR-KL43Z or Freescale.com/Kinetis.

- TWR-KL43Z48M_QSG: Quick Start Guide
- TWR- KL43Z48M_SCH: Schematics
- TWR KL43Z48M_PWB: Design Package
- MKL43Z256VLH4 Reference Manual
- Tower Configuration Tool
- Tower Mechanical Drawing

6 Hardware description

The TWR-KL43Z is a Tower MCU Module featuring the MKL43Z256VLH4 — a Kinetis microcontroller with USB 2.0 full-speed device controllers in a 64-LQFP package. It is intended for use in the Freescale Tower System but can operate standalone. An on-board OpenSDA debug circuit provides a SWD interface and a power supply input through a single USB mini-AB connector.

The block diagram of the TWR-KL43Z board is presented in [Figure 3](#).

6.1 Block diagram

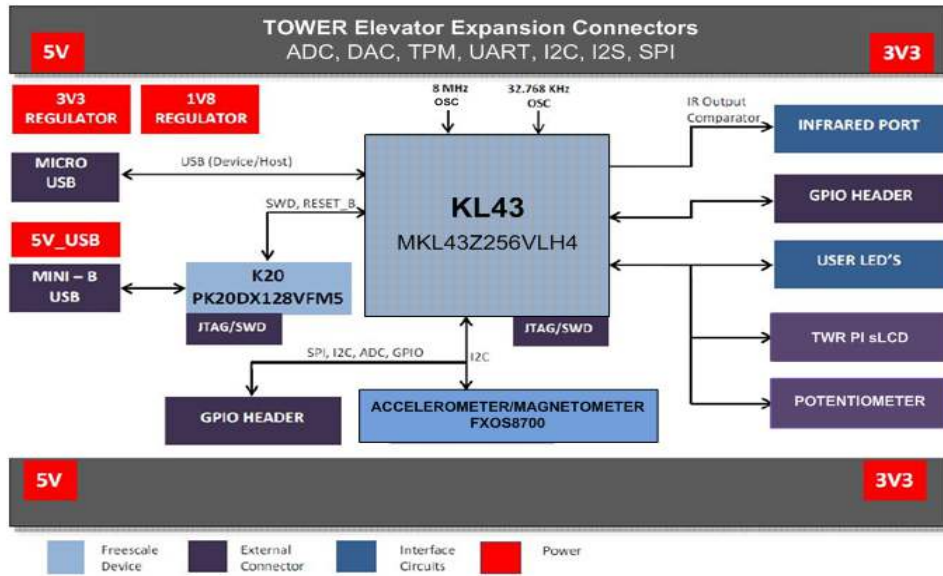


Figure 3. Block diagram of TWR-KL43Z

6.2 Microcontroller

The TWR-KL43Z is a Tower MCU module featuring the MKL43Z256VLH4 — a Kinetis microcontroller with USB 2.0 full-speed device controller and segment LCD controller in a 64 LQFP package. It is intended for use in the Freescale Tower System but can operate standalone. An on-board debug circuit, OpenSDA, provides a SWD interface and a power supply input through a single USB mini-AB connector, as well as serial to USB and CDC class compliant UART interface.

Table 1. Features of MKL43Z256VLH4

Feature	Description
Ultra-low-power	<ul style="list-style-type: none"> - 10 low-power modes with power and clock gating for optimal peripheral activity and recovery times. Stop currents of <190 nA (VLLS0), run currents of <280 uA/MHz, 4 s wake-up from Stop mode - Full memory and analog operation down to 1.71V for extended battery life - Low-leakage wake-up unit with up to eight internal modules and eight pins as wake-up sources in low-leakage stop (LLS)/very low-leakage stop (VLLS) modes - Low-power timer for continual system operation in reduced power states

Table 1. Features of MKL43Z256VLH4

Flash, SRAM, ROM	<ul style="list-style-type: none"> - 256 KB flash featuring fast access times, high reliability, and four levels of security protection. No user or system intervention to complete programming and erase functions and full operation down to 1.71V. - 32 KB of SRAM - 16 KB of ROM with Kinetis bootloader included (UART, SPI, I²C, USB)
Mixed-signal capability	<ul style="list-style-type: none"> - SAR 16-bit analog-to-digital converter (ADC) - High-speed comparator (CMP) with internal 6-bit digital-to-analog converter (DAC) - 12-bit digital-to-analog converter (DAC) - VREF module 1,2V output
Performance	<ul style="list-style-type: none"> - 48 MHz ARM Cortex-M0+ core - Up to four channel DMA for peripheral and memory servicing with reduced CPU loading and faster system throughput - Cross bar switch enables concurrent multi-master bus accesses, increasing bus bandwidth - Independent flash banks allowing concurrent code execution and firmware updating with no performance degradation or complex coding routines - Bit manipulation engine (BME) allows execution of single-instruction atomic bit-modify-write operations on the peripheral address space
Timing and control	<ul style="list-style-type: none"> - Three timer/PWM modules – one with six channel, and two with two channels - Low-power timer - Real-time clock - Two-channel 32-bit periodic interrupt timer provides time base for RTOS task scheduler or trigger source for ADC conversion, provides lifetime timer capability
Human-machine interface	<ul style="list-style-type: none"> - Segment LCD controller up to 4x32 or 8x28 segments - General-purpose input/output up to 54
Connectivity and communications	<ul style="list-style-type: none"> - USB full-speed slave controller with on-chip transceiver and 5V to 3.3V regulator, supporting crystal-less recovery - USB low-voltage regulator supplies up to 120 mA off chip at 3.3 volts to power external components from 5-volt input - Two 16-bit SPI modules - One UART module supporting ISO7816 - Two LPUART modules - Two I²C modules supporting up to 1 Mbit/s - One I²S (SAI) module - One FlexIO module

6.3 Clocking

The Kinetis MCUs start up to the default reset clock for core/system clock, which is 8 MHz from IRC8M. Software can enable the main external oscillator (EXTAL0/XTAL0), or to high frequency internal reference (HIRC) 48 MHz if desired. The external oscillator/resonator can range from 32.768 KHz up to a 32 MHz. An 8 MHz crystal is the default external source for the MCG lite oscillator inputs (XTAL/EXTAL). A 32.768 KHz oscillator is connected to the real-time clock in input.

6.4 System power

When installed into a Tower System, the TWR-KL43Z can be powered from either an on-board source or from another source in the assembled Tower System.

In standalone operation, the main power source (5.0V) for the TWR-KL43Z48M module is derived from either the OpenSDA USB micro-AB connector or the KL43 USB micro-AB connector (J5). Two low-dropout regulators provide 3.3V and 1.8V supplies from the 5.0V input voltage. Additionally, the 3.3V regulator built into the KL43 can be selected to power the 3.3V bus. All the user selectable options can be configured using two headers, J35, J25 or J28.

6.5 Real-time clock (RTC)

Y1 is a 32.768 kHz oscillator that can be connected to RTC_CLKIN via selection header J31. By enabling the external clock input option in the RTC, it can be used as a highly precise time reference.

6.6 Debug interface

There are two debug interface options provided: the on-board OpenSDA circuit and an external ARM SWD connector.

6.6.1 OpenSDA

An on-board MK20-OpenSDA circuit provides an SWD debug interface to the MKL43Z256. A standard USB A male to micro-AB male cable (provided) can be used for debugging via the USB connector, J8. The OpenSDA interface also provides a USB to serial bridge.

6.6.2 Cortex Debug SWD connector

The Cortex Debug SWD connector is a standard 2x5-pin (0.05") connector providing an external debugger cable with access to the SWD interface of the MKL43Z256.

Table 2. Cortex Debug connector

Pin	Function	TWR-KL43Z Connection
1	VTref	3.3V MCU supply (V_BRD)
2	SWDIO	PTA3/I2C1_SCL/FTM0_CH0/SWD_DIO
3	GND	GND
4	SWCLK	PTA0/ FTM0_CH5 /SWD_CLK
5	GND	GND
6	NC	
7	NC	
8	NC	
9	NC	
10	nRESET	PTA20/RESET

6.7 UART

UART2 can be connected to OpenSDA or TWR-Elevators through jumpers J3 and J5.

J3 UART2_TX_TGTMCU – PTE22/UART2_TX

J3 UART2_RX_TGTMCU – PTE23/UART2_RX

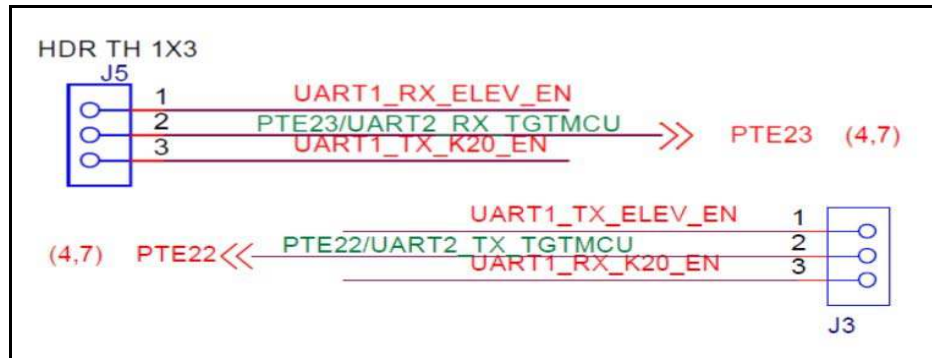


Figure 4. UART2 connection to OpenSDA CDC serial/elevator

6.8 Infrared port

An infrared transmit and receive interface is implemented as shown in Figure 5. The LPUART0_TX (PTE20/ ADC0_DP0/LPUART0_TX) pin directly drives an infrared diode. The receiver uses an infrared phototransistor connected to LPUART0_RX (PTE21/ ADC0_DM0/ UART0_RX) through a low-pass filter.

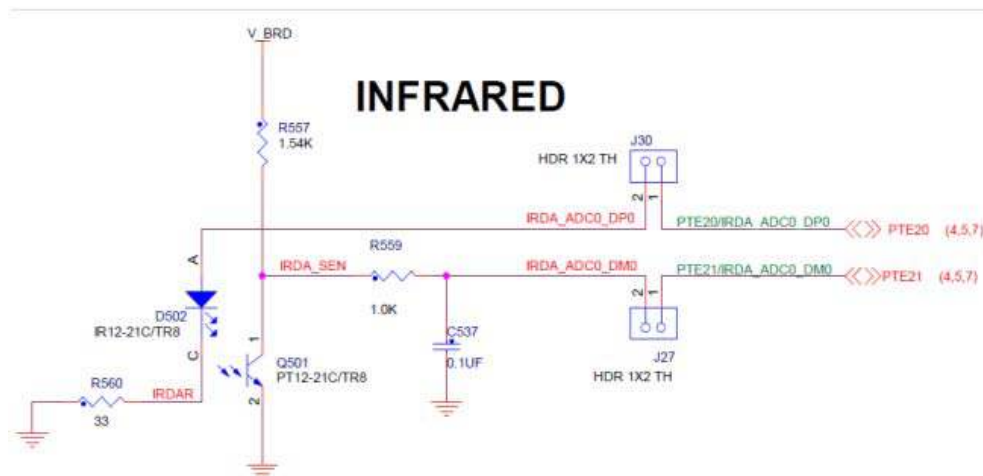


Figure 5. Infrared circuit

6.9 Accelerometer

An FXOS8700CQ 6-Axis Xtrinsic sensor with integrated linear accelerometer and magnetometer is connected to the MKL43Z256VLH4 MCU through I²C module, I²C1, and GPIO/IRQ signals, PTD6 and PTD7. The device can be configured to generate inertial wake-up interrupt signals from any combination of the configurable embedded functions allowing the FXOS8700CQ to monitor events and remain in a

low-power mode during periods of inactivity. For more information on the FXOS8700CQ, visit the FXOS8700CQ Product Summary Page at Freescale.com/FXOS8700CQ.

6.10 General Purpose Tower Plug-in (TWRPI) socket

The TWR-KL43Z features a socket (J22 and J14) that can accept a variety of different Tower Plug-in modules featuring sensors, RF transceivers, and more. The General Purpose TWRPI socket provides access to I²C, SPI, IRQs, GPIOs, timers, analog conversion signals, TWRPI ID signals, reset, and voltage supplies. The pinout for the TWRPI socket is defined in [Table 3](#).

Table 3. General Purpose TWRPI socket pinout

J22		J14	
Pin	Description	Pin	Description
1	5V VCC	1	GND
2	3.3 V VCC	2	GND
3	GND	3	I ² C: SCL
4	3.3V VDDA	4	I ² C: SDA
5	VSS (Analog GND)	5	GND
6	VSS (Analog GND)	6	GND
7	VSS (Analog GND)	7	GND
8	ADC: Analog 0	8	GND
9	ADC: Analog 1	9	SPI: MISO
10	VSS (Analog GND)	10	SPI: MOSI
11	VSS (Analog GND)	11	SPI: SS
12	ADC: Analog 2	12	SPI: CLK
13	VSS (Analog GND)	13	GND
14	VSS (Analog GND)	14	GND
15	GND	15	GPIO: GPIO0/IRQ
16	GND	16	GPIO: GPIO1/IRQ
17	ADC: TWRPI ID 0	17	GPIO: GPIO2
18	ADC: TWRPI ID 1	18	GPIO: GPIO3
19	GND	19	GPIO: GPIO4/Timer
20	Reset	20	GPIO: GPIO5/Timer

6.11 Potentiometer, pushbuttons, LEDs

The TWR-KL43Z features two pushbutton switches connected to GPIO/interrupt signals, one pushbutton connected to the master reset signal, four user-controllable LEDs, and a potentiometer connected to an ADC input signal. Refer to [Table 5](#) for information about which port pins are connected to these features.

6.12 SLCD TWRPI interface

[Table 4](#) shows TWRPI/TWRPI-SLCD pin-out and corresponding connection to GD-6363P LCD. TWRPI-SLCD connector is also compatible with other TWRPIs. It can accept touch TWRPI daughter cards that may feature keypads, rotary dials, sliders, etc. As MKL43Z256 MCU does not support TSI the only software GPIO method provided in TSS can be used for touch events detection.

Table 4. SLCD TWRPI socket pinout

Pin	TWRPI	LCD_n	KL43	Module pin	Module signal
1	P5V_TRG_USB				
2	V_BRD				
3	PTB16/LCD_P12	LCD_P12	PTB16	1	COM0
4	VDDA				
5	PTB17/LCD_P13	LCD_P13	PTB17	2	COM1
6	VSSA				
7	PTB18/LCD_P14	LCD_P14	PTB18	3	COM2
8	PTB19/LCD_P15	LCD_P15	PTB19	4	COM3
9	PTC3/LCD_P23	LCD_P23	PTC3	5	3A/3B/3C/3D
10	PTB0/LCD_P0	LCD_P0	PTB0	6	T2/T3/AM/PM
11	PTB1/LCD_P1	LCD_P1	PTB1	7	3F/3G/3E/T1
12	PTB2/LCD_P2	LCD_P2	PTB2		
13	PTB3/LCD_P3	LCD_P3	PTB3	8	2A/2B/2C/2D
14	PTC0/LCD_P20	LCD_P20	PTC0	9	2F/2G/2E/COL
15	PTC2/LCD_P22	LCD_P22	PTC2	10	1A/1B/1C/1D
16	PTC4/LCD_P24	LCD_P24	PTC4	11	1F/1G/1E/P1
17	PTD3/LCD_P43-ID0	LCD_P43	PTD3		
18	PTD2/LCD_P42-ID1	LCD_P42	PTD2		
19	GND				
20	RST_TGT_MCU				

6.13 USB

The MKL43Z256 features USB full-speed slave controller with on-chip transceiver and 5 V to 3.3 V regulator, supporting crystal-less recovery. The TWR-KL43Z routes the USB D+ and D- signals from the KL43Z256 MCU directly to the on-board USB connector (J21).

7 TWR-KL43Z jumper options

NOTE:

Default configuration for power is OpenSDA USB with 3.3V voltage selection.

Table 5. Jumper options

Jumper Function	Jumper	Default Position	Jumper Option	KL43 Pin Name
Board power selection	J28	1-2	1-2 P5V_TRG_USB 2-3 VBUS_ELEV	
	J25	Open	1-2 P5V_KL43_USB	
VREG input power selection	J16	1-2	1-2 P5V_TRG_USB 2-3 VBUS_ELEV	P5V_VREGIN_K L43
	J19	Open	1-2 P5V_KL43_USB	P5V_VREGIN_K L44
Voltage level selection	J35	1-2	1-2 3.3V 2-3 1.8V	
VREFH isolation (when onchip VREF module enabled)	J38	Open	1-2 VREFH to VDDA	VREFH
Digital part of MCU power	J12	1-2	Open - VDD isolated from MCU_POWER	VDD1, VDD2
Analog part of MCU power	J10	1-2	Open - VDDA_HDR isolated from MCU_POWER	VDDA
Isolation between board and MCU power	J17	1-2	Open - V_BRD isolated from MCU_POWER	
Isolation between MCU VOUT33 and MCU power	J11	Open	1-2 VOUT_3V3 to MCU_POWER	
VLL3 to VDD enable	J36	Open	1-2 VLL3 to VDD enable	VLL3

Table 6. Connectors and pin usage

Jumper Function	Jumper	Default Position	Jumper Option	KL43 Pin Name
Reset selection	J1	1-2	1-2 RESET_B 2-3 RST_TGTMCU_B	
RTC clock input	J31	1-2	1-2 RTC_CLKIN 2-3 ELEV_IRQ_C	PTC1
switch button SW2	J24	1-2	Open - PTA4 isolated	PTA4
switch button SW3	J33	1-2	Open - PTA5 isolated	PTA5
LED D7	J23	1-2	Open - LED Green PTA12 isolated	PTA12
LED D5	J18	1-2	Open - LED Red PTA13 isolated	PTA13
LED D4	J13	1-2	Open - LED Green PTB0 isolated	PTB0
LED D3	J7	1-2	Open - LED Red PTB19 isolated	PTB19
IRDA TX isolation	J30	Open	1-2 PTE20 to IRDA (Tx)	PTE20
IRDA RX isolation	J27	Open	1-2 TPE21 to IRDA (Rx)	PTE21
Accelerometer SCL isolation	J26	Open	1-2 PTE1 to ACCEL SCL Enable	PTE1 I2C1_SCL
Accelerometer SDA isolation	J29	Open	1-2 PTE0 to ACCEL SDA Enable	PTE0 I2C1_SDA
Accelerometer INT1 isolation	J32	Open	1-2 PTD6 to ACCEL INT1 Enable	PTD6/ACC_INT1
Accelerometer INT2 isolation	J34	Open	1-2 PTD7 to ACCEL INT2 Enable	PTD7/ACC_INT2
Accelerometer reset	J37	Open	1-2 ACCEL RST to P3V3_REG enable	
UART2 TX selection	J3	2-3	2-3 UART2 Tx- OpenSDA 2-1 UART2 Tx Elevator	PTE22
UART2 RX selection	J5	2-3	2-3 UART2 Rx- OpenSDA 2-1 UART2 Rx- Elevator	PTE23
Potentiometer isolation	J2	1-2	Open - PTE20 isolated from potentiometer	PTE29/POT_ADC0_SE4B

8 Useful links

- freescale.com/TWR-KL43Z
- freescale.com
- iar.com/freescale
- pemicro.com
- segger.com

9 Revision history

Table 7. Revision history

Revision	Date	Description
1	May, 2014	Initial release

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