

# ***DSP-Codec Development Platform***

## *User's Guide*

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It is important to operate this EVM within the input voltage range of 3.3 V described in the EVM User's Guide.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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# Read This First

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### ***About This Manual***

This user's guide describes the operation and use of the DSP-codec development platform. A complete circuit description as well as schematic diagram and bill of materials are also included.

### ***How to Use This Manual***

This document contains the following chapters:

- Chapter 1 – Introduction and EVM Overview
- Chapter 2 – Digital Interface
- Chapter 3 – Support Functions
- Chapter 4 – EVM Bill of Materials and Schematic

### ***Related Documentation From Texas Instruments***

To obtain a copy of any of the following TI documents, call the Texas Instruments literature response center at (800) 477-8924 or the product information center (PIC) at (972) 644-5580. When ordering, please identify this booklet by its title and literature number. Updated documents can also be obtained through the TI website at [www.ti.com](http://www.ti.com).

**Data Sheets:**

SN74LVC1G08DBVR  
SN74LVC74ADR  
TPS70151PWP

**Literature Number:**

SCES217J  
SCAS287M  
SLVS222A

**FCC Warning**

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

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# **Introduction and EVM Overview**

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This chapter provides a brief overview of the DSP-codec development platform.

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## 1.1 Features

- Provides all necessary voltages for device under test
- Provides bit clock for codecs
- Flexible interface to popular TI DSPs
- General codec requirements are addressed

## 1.2 Introduction

The DSP-codec development platform provides all the supplementary control signals necessary to interface a range of TI codecs to TI DSP starter kits (DSKs).

The platform supports the following devices

- TLV320AIC1103
- TLV320AIC1106
- TLV320AIC1107
- TLV320AIC1109
- TLV320AIC1110
- TLV320AIC12
- TLV320AIC13
- TLV320AIC14
- TLV320AIC15
- TLV320AIC20
- TLV320AIC21
- TLV320AIC22
- TLV320AIC24

# Digital Interface

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This chapter describes the digital interface of the DSP-codec development platform.

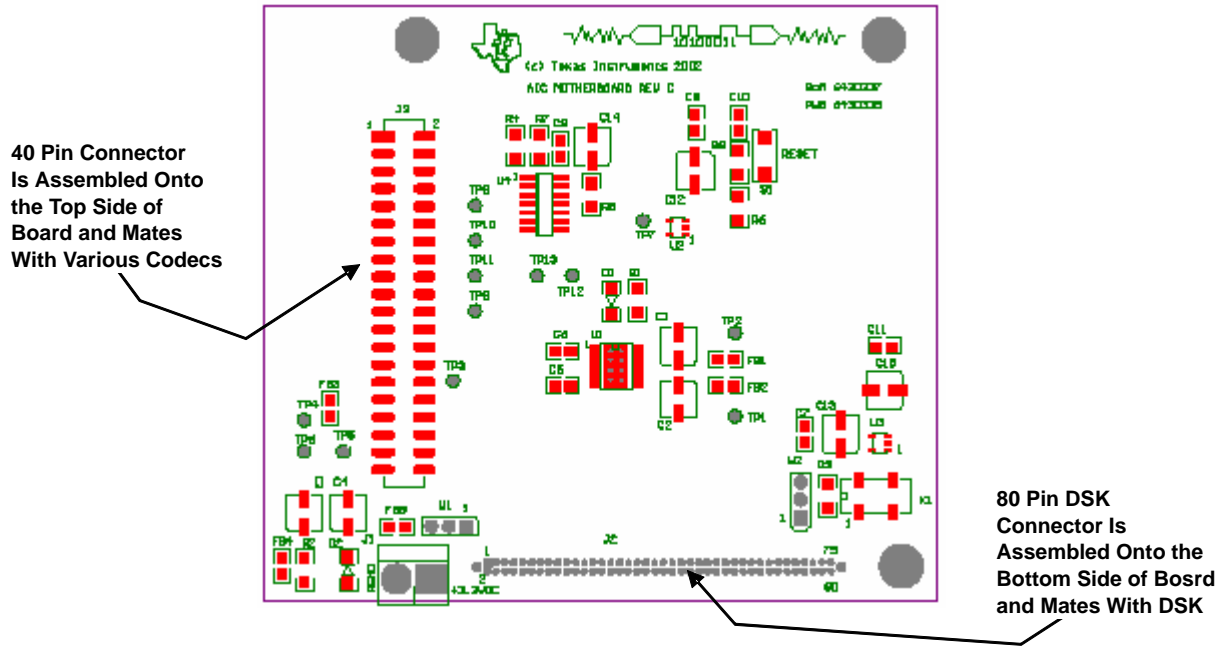
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## 2.1 Introduciton

There are two sections within the digital interface of the development platform:

- DSP-to-platform
- Platform-to-codec

Figure 2-1. DSP-Codec Development Platform



## 2.2 DSP-to-Platform

The development platform mates with TI DSKs via the 80-pin Samtec connector located at J2. Consult the schematic for pinout details.

## 2.3 Platform-to-Codec

Codec EVMs mate with the development platform via a 40-pin Samtec connector located at J3. The mating connector (Samtec part number, SSW-120-22-F-D-VS-K) is used on the EVM board to provide the electrical connections necessary for various codec EVMs. Consult Samtec at [www.samtec.com](http://www.samtec.com) or 1-800-SAMTEC-9 for more information.

The pinout for the 40-pin connector is given in Table 2-1.

Table 2-1. J2 Connector Pinouts

| Pin Number | Signal                    | Description                       |
|------------|---------------------------|-----------------------------------|
| J2.1       | MCLK                      | Master clock                      |
| J2.2       | DGND                      | Digital ground                    |
| J2.3       | SCLK                      | Serial data clock                 |
| J2.4       | DGND                      | Digital ground                    |
| J2.5       | DIN                       | Data in                           |
| J2.6       | DGND                      | Digital ground                    |
| J2.7       | DOUT                      | Data out                          |
| J2.8       | Reserved                  | Reserved for future use           |
| J2.9       | FS                        | Frame sync                        |
| J2.10      | Reserved                  | Reserved for future use           |
| J2.11      | CLKX                      | Transmit clock                    |
| J2.12      | Reserved                  | Reserved for future use           |
| J2.13      | FSX                       | Frame sync transmit               |
| J2.14      | Reserved                  | Reserved for future use           |
| J2.15      | DX                        | Data transmit                     |
| J2.16      | DR                        | Data receive                      |
| J2.17      | $\overline{\text{RESET}}$ | Global reset for all devices      |
| J2.18      | FSR                       | Frame sync receive                |
| J2.19      | PWDN                      | Global power down for all devices |
| J2.20      | CLKR                      | Receive clock                     |
| J2.21      | CNTLb                     | GPIO pin                          |
| J2.22      | CNTLa                     | GPIO pin                          |
| J2.23      | STATb                     | Status pin                        |
| J2.24      | STATa                     | Status pin                        |
| J2.25      | 3.3V_D                    | Digital 3.3 V                     |
| J2.26      | Reserved                  | Reserved for future use           |
| J2.27      | 3.3V_D                    | Digital 3.3 V                     |
| J2.28      | DGND                      | Digital ground                    |
| J2.29      | 1.8V_D                    | Digital 1.8 V                     |
| J2.30      | DGND                      | Digital ground                    |
| J2.31      | 1.8V_D                    | Digital 1.8 V                     |

Table 2-1. J2 Connector Pinouts (Continued)

| Pin Number | Signal     | Description                |
|------------|------------|----------------------------|
| J2.32      | DGND       | Digital ground             |
| J2.33      | 3.3V_A_DRV | Output driver supply 3.3 V |
| J2.34      | AGND       | Analog ground              |
| J2.35      | 3.3V_A_DRV | Output driver supply 3.3 V |
| J2.36      | AGND       | Analog ground              |
| J2.37      | 3.3V_A     | Analog 3.3 V               |
| J2.38      | AGND       | Analog ground              |
| J2.39      | 3.3V_A     | Analog 3.3 V               |
| J2.40      | AGND       | Analog ground              |

# Support Functions

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This chapter provides a description of the codec support functions.

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### 3.1 Introduction

The development platform supports a number of functions required by the codecs:

- MCLK generation
- Reset generation
- Power options

Alternatives for each function are described below.

#### 3.1.1 MCLK Generation

MCLK is the clock required by the Sigma Delta converter. All other timing is derived from MCLK. The DSK provides a clock that can be used as MCLK for the codecs. Alternatively, a 100 MHz clock is available on the development platform. Jumper W2 selects the clock source.

*Table 3-1. Jumper W2 Function*

| Position | Function  |
|----------|---|
| 1-2      | DSP Clock is selected                               |
| 2-3      | 100 MHz clock from development platform is selected |

#### 3.1.2 Reset Generation

Reset may be generated by either the DSK via software, or manually by momentarily pressing SW1. Either of these options is valid and generates a **RESET** signal that is asynchronous to MCLK.

#### 3.1.3 Power Options

System power may be supplied from either the DSK via connector J2, or an external source via connector J1. If an external source is used to supply system power, switch the position of jumper W1.

*Table 3-2. Jumper W1 Function*

| Position | W1 Function                                  |
|----------|--|
| 1-2      | 3.3 V is supplied via the DSK                |
| 2-3      | 3.3 V is supplied via the J1 screw terminals |



## 3.2 Key Signal Synchronization

The reset and power-down signals must be synchronized to MCLK before being applied to any codec. As mentioned previously,  $\overline{\text{RESET}}$  is generated by the DSK or the user, and is asynchronous to the MCLK. Synchronization is achieved by D-type flip-flop. Similarly, the  $\overline{\text{PWDN}}$  signal is generated by the user's software, and is asynchronous to the MCLK signal. Synchronization of  $\overline{\text{PWDN}}$  is also achieved by D-type flip-flop.



# **EVM Bill of Materials and Schematic**

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The development platform bill of materials and schematic are provided in this chapter.

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## 4.1 EVM Bill of Materials

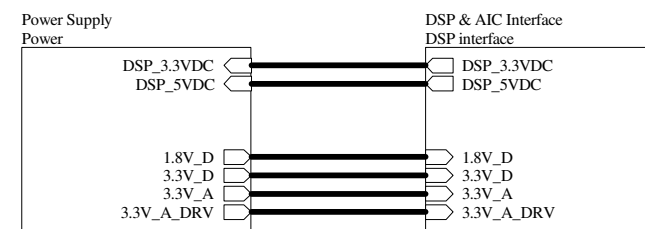
The following table contains a complete bill of materials for the DSP-codec development platform. The schematic diagram is also provided for reference. Contact the product information center, or e-mail [dataconvapps@list.ti.com](mailto:dataconvapps@list.ti.com) if you have questions regarding this EVM.

| Ref Des   | Description                                    | Vendor                     | Part number       |
|---|--|----------------------------|-------------------|
| C7, C8, C9, C10, C11  | Capacitor, 0.1 $\mu$ F 50 V, ceramic X7R 0805  | Panasonic                  | ECJ-2YB1H104K     |
| C5, C6  | Capacitor, .22 $\mu$ F 16 V ceramic X7R 0805   | Panasonic                  | ECJ-2VB1C224K     |
| C12, C13, C14, C15  | Capacitor, 10 $\mu$ F 16 V VS electrolytic SMD | Panasonic                  | ECE-V1CA100SR     |
| C1, C2, C3, C4  | Capacitor, 33 $\mu$ F 10 V VS electrolytic SMD | Panasonic                  | ECE-V1AA330SR     |
| FB1, FB2, FB3, FB4, FB5   | Ferrite bead inductor                          | FairRite                   | 2744044447        |
| R1, R2  | RES 270 $\Omega$ 1/8 W 5%, 1206 SMD            | Panasonic                  | ERJ-8GEYJ271V     |
| R8  | RES 1.0 k $\Omega$ 1/8 W,5%, 1206 SMD          | Panasonic                  | ERJ-8GEYJ102V     |
| R3, R4, R5  | Resistor 10 k $\Omega$ , 1/8 W 5%, 1206 SMD    | Panasonic                  | ERJ-8GEYJ103V     |
| R7  |  |                            |                   |
| R6  | Resistor 130 k $\Omega$ , 1/8 W 5% 1206 SMD    | Panasonic                  | ERJ-8GEYJ134V     |
| D1, D2  | LED, green, clear 1206 SMD                     | Chicago Miniature Lamp Inc | CMD5-21VGC/TR8    |
| X1  | 100 MHz Oscillator                             | Epson                      | SG-8002JC100M-PCC |
|   | TLV320 AIC motherboard                         |                            | 6430339           |
|   | TLV320 AIC motherboard DDB                     | Texas Instruments          | 6430338           |
| U2, U3  | Single 2-input positive-AND gate               | Texas Instruments          | SN74LVC1G08DBVR   |
| U4  | IC, dual D-type flip-flop 14-SOP               | Texas Instruments          | SN74LVC74ADR      |
| U1  | IC, dual 3.3/1.8 LDO Reg. 20 HTSSOP            | Texas Instruments          | TPS70151PWP       |
| J1  | 2-Terminal screw connector                     | Lumberg                    | KRMZ2             |
| W1, W2  | 3-position jumper                              | Samtec                     | TSW-103-07-L-S    |
| J3  | 40-PIN SMT plug                                | Samtec                     | TSM-120-01-T-DV-P |
| J2  | 80-Pin 0.05" center                            | Samtec                     | TFM-140-31-S-D-A  |
| S1  | Switch, light touch 6X3.5 240 GF SMD           | Panasonic                  | EVQ-PJU04K        |
| TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13 | Test point                                     | Keystone                   | 5000              |

## 4.2 EVM Schematic

The full DSP-codec EVM schematic is on the following pages.

| Revision History |            |          |
|------------------|------------|----------|
| REV              | ECN Number | Approved |
|                  |            |          |
|                  |            |          |
|                  |            |          |



|   |                           |                        |
|---|---------------------------|------------------------|
| 12500 TI Boulevard. Dallas, Texas 75243 |                           |                        |
| Title: DSP / CODEC Development Platform |                           |                        |
| Engineer:                               | DOCUMENTCONTROL # 6430338 | REV: C                 |
| Drawn By:                               | DATE: 9-Jul-2002          | SIZE: 6 SHEET: 1 OF: 3 |

|                                |  |
|--------------------------------|--|
| Engineer:                      |  |
| Drawn By:                      |  |
| FILE: CODEC Development system |  |

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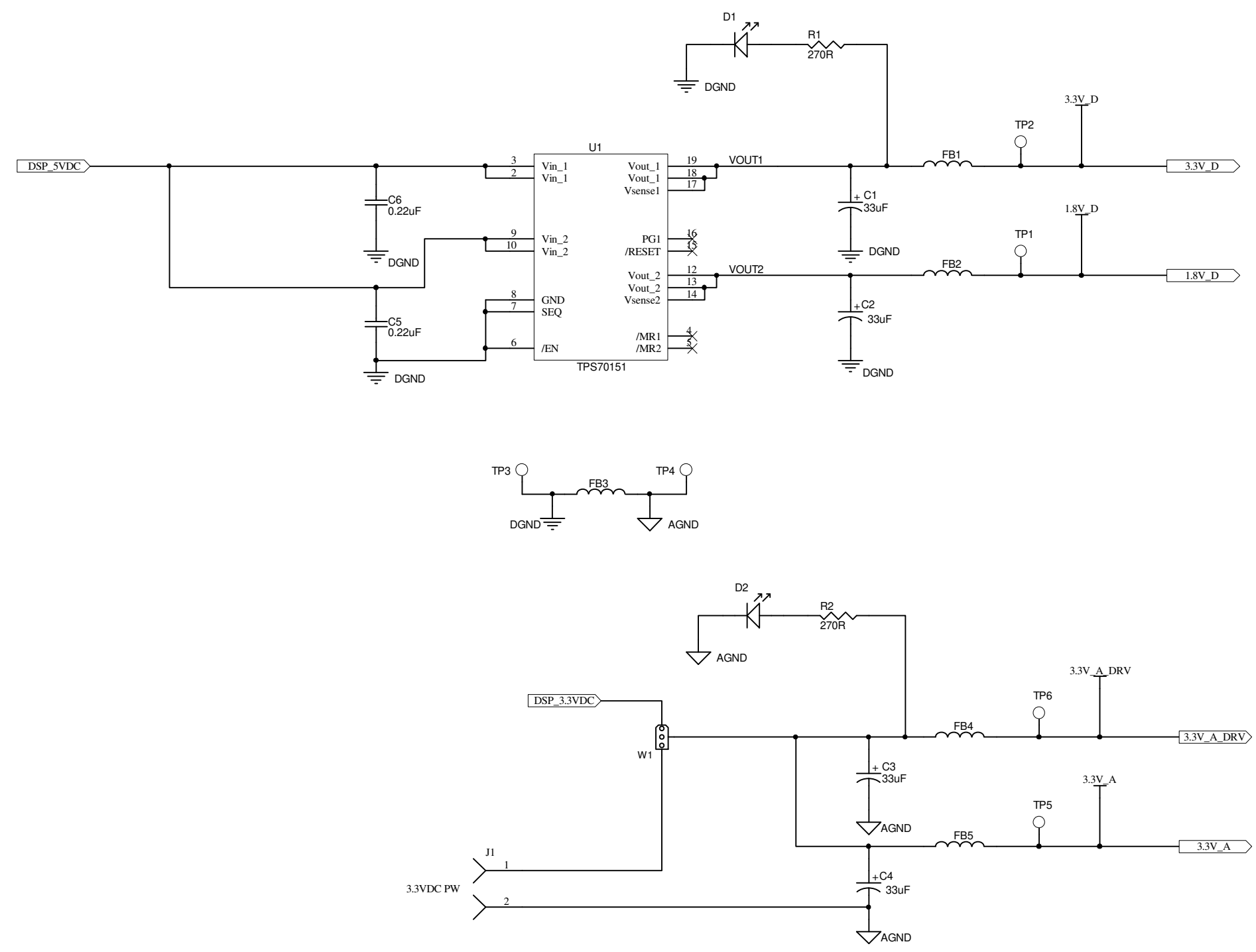
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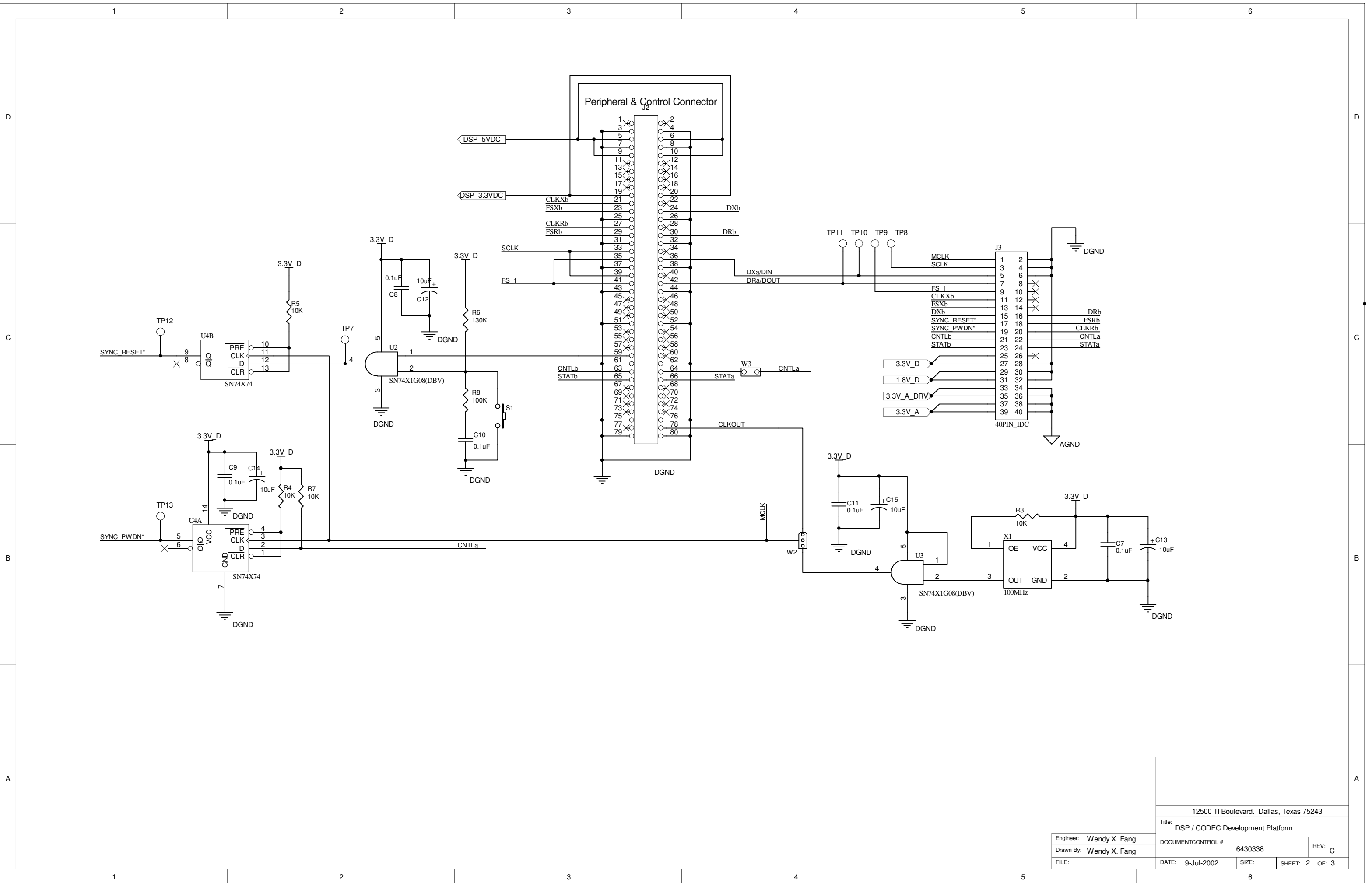
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| REV              | ECN Number | Approved |
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| Drawn By: Wendy X. Fang                 | DATE: 9-Jul-2002          | SIZE: 6 SHEET: 3 OF: 3 |
| FILE: Power                             |                           |                        |



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| Drawn By: Wendy X. Fang                 | DATE: 9-Jul-2002          | SIZE:  | SHEET: 2 OF: 3 |