Triple Buck Regulator Integrated Power Solution

Data Sheet

ADP5055

FEATURES

- Wide input voltage range: 2.75 V to 18 V
- Bias input voltage range: 4.5 V to 18 V
- Operation up to 150°C junction temperature
- PMBus-compatible interface with configurable address
- FB1 voltage accuracy (default): −0.62% to +0.69% (−40°C ≤ T_J ≤ +125°C)
- Channel 1 and Channel 2: 7 A synchronous buck regulator (9.4 A minimum valley current-limit threshold)
- Channel 1 and Channel 2: 14 A output in parallel operation
- Channel 3: 3 A synchronous buck regulator (4.2 A minimum valley current-limit threshold)
- 8-bit precision DAC for DVS
  - Adjustable feedback voltage range: 408 mV to 790.5 mV per 1.5 mV step
  - Upper and lower threshold limit setting
- 250 kHz to 2500 kHz adjustable switching frequency range
- External compensation for fast load transient response
- Precision enable pin with 0.615 V accurate threshold
- Programmable power-up and power-down sequence
- Selective active output discharge switch
- Selective FPWM/PSM mode selection
- Frequency synchronization input or output
- Power-good flag on selective channels
- UVLO, overcurrent protection, and TSD protection
- 43-terminal, 5.00 mm × 5.50 mm LGA package

APPLICATIONS

- Small cell base stations
- Field programmable gate array (FPGA) and processor applications
- Security and surveillance
- Medical applications

GENERAL DESCRIPTION

The ADP5055 combines three high performance buck regulators in a 43-terminal land grid array (LGA) package that meets the demanding performance and board space requirements. The device enables direct connection to high input voltages up to 18 V with no preregulators.

All channels integrate both high-side and low-side power metal-oxide semiconductor field effect transistors (MOSFETs) to achieve an efficiency optimized solution. Channel 1 and Channel 2 deliver a programmable output current of 3.5 A or 7 A or provide a single output with up to 14 A of current in parallel operation. Channel 3 delivers a programmable output current of 1.5 A or 3 A.

TYPICAL APPLICATION CIRCUIT

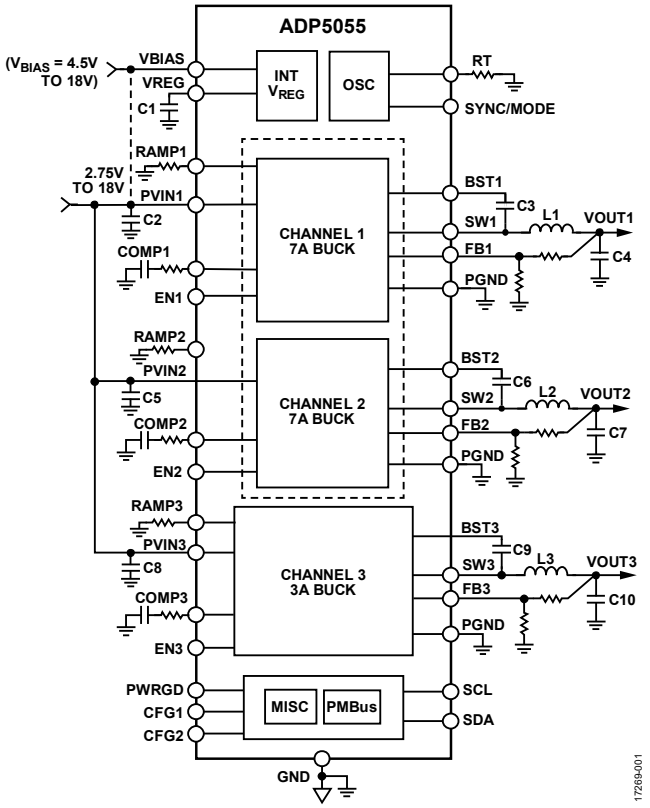

Figure 1.

The switching frequency of the ADP5055 can be programmed or synchronized to an external clock. The ADP5055 contains an enable pin (ENx) on each channel for simple power-up sequencing or adjustable undervoltage lockout (UVLO) threshold.

The ADP5055 integrates a high precision 8-bit digital-to-analog converter (DAC) to enable the output voltage dynamic voltage scaling (DVS) via the PMBus®-compatible, 2-wire interface. The PMBus interface provides other flexible configurations, such as start-up and shutdown sequence control, individual forced pulse-width modulation or power saving mode (FPWM or PSM) selection, an output discharge switch, and a power-good signal.

The ADP5055 is rated at −40°C to +150°C junction temperature.

Note that throughout this data sheet, multifunction pins, such as SYNC/MODE, are referred to either by the entire pin name or by a single function of the pin, for example, SYNC, when only that function is relevant.

Rev. 0 Document Feedback

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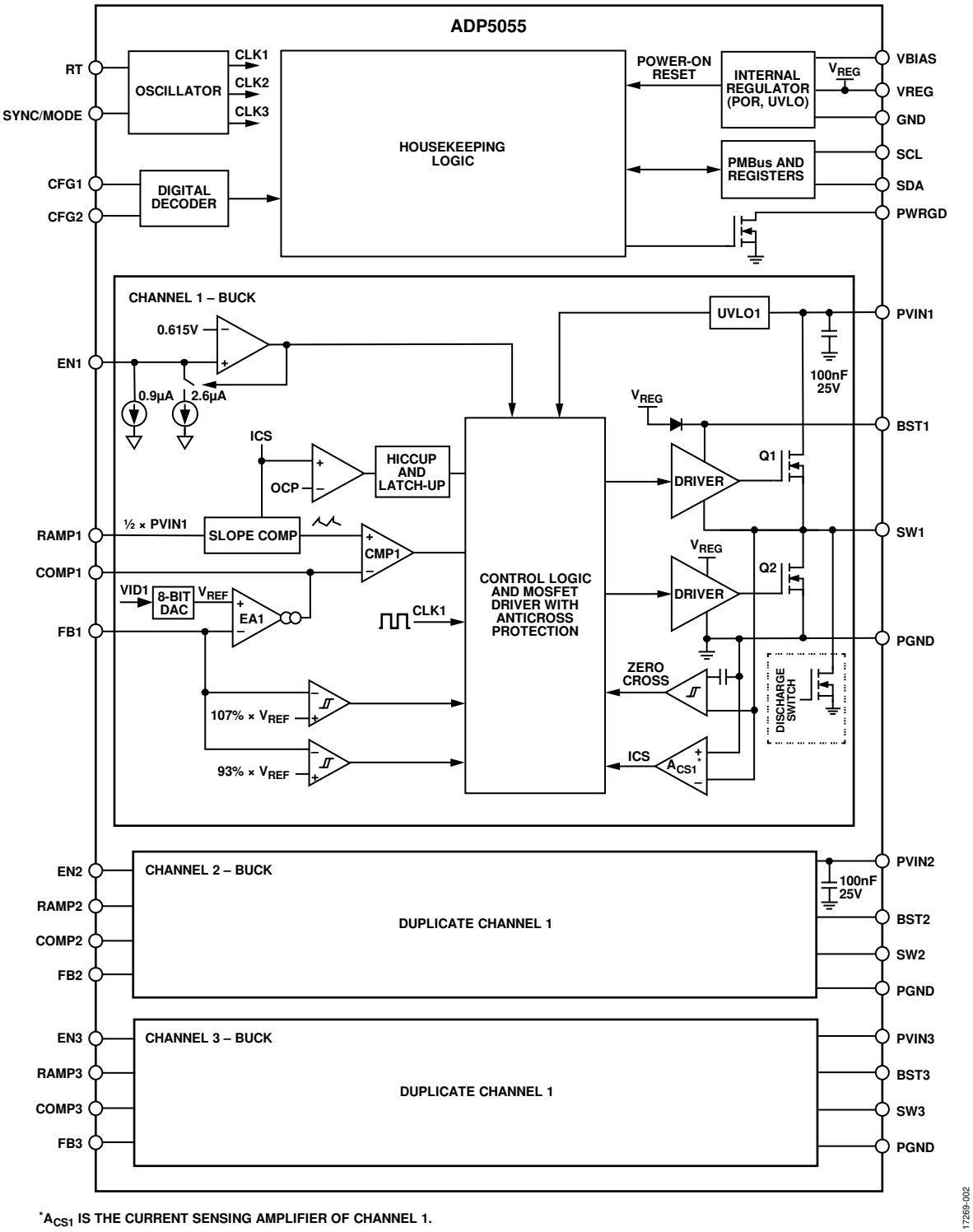
REVISION HISTORY

1/2022—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM



*A_{CS1} IS THE CURRENT SENSING AMPLIFIER OF CHANNEL 1.

Figure 2.

SPECIFICATIONS

Input voltage (V_{IN}) = bias input voltage (V_{BIAS}) = 12 V, VREG voltage (V_{REG}) = 4.8 V, T_J = −40°C to + 150°C for minimum and maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
WIDE INPUT VOLTAGE RANGE	V_{IN}	2.75		18	V	PVIN1, PVIN2, and PVIN3 pins
BIAS INPUT VOLTAGE RANGE	V_{BIAS}	4.5		18	V	VBIAS pin
QUIESCENT CURRENT						VBIAS pin
Operating Quiescent Current	$I_{Q(3\text{-}BUCKS)}$		6.2	7.5	mA	No switching, all ENx pins high
Shutdown Current of Three Channels	$I_{SHDN(3\text{-}BUCKS)}$		42	80	µA	All ENx pins low
UNDERVOLTAGE LOCKOUT						
Power Input	$UVLO_{PVINx}$					PVIN1, PVIN2, and PVIN3 pins
Rising Threshold	$V_{UVLO1\text{-}RISING}$		2.60	2.75	V	
Falling Threshold	$V_{UVLO1\text{-}FALLING}$		2.30		V	
Hysteresis	V_{HYS1}		0.30		V	
Bias Input Voltage	$UVLO_{VBIAS}$					VBIAS pin
Rising Threshold	$V_{UVLO2\text{-}RISING}$		4.20	4.50	V	
Falling Threshold	$V_{UVLO2\text{-}FALLING}$	3.60	3.80		V	
Hysteresis	V_{HYS2}		0.40		V	
OSCILLATOR CIRCUIT						
Switching Frequency	f_{SW}	530	600	630	kHz	The resistor connected between RT and ground (R_T) = 280 kΩ
		1140	1200	1250	kHz	R_T = 140 kΩ
		1700	1800	1900	kHz	R_T = 94.2 kΩ
Switching Frequency Range		250		2500	kHz	
Synchronization Input						
Input Clock Range	f_{SYNC}	250		2500	kHz	
Input Clock Pulse Width						
Minimum On Time	$t_{SYNC\_MIN\_ON}$	100			ns	
Minimum Off Time	$t_{SYNC\_MIN\_OFF}$	100			ns	
Input Clock High Voltage	$V_{H(SYNC)}$	2.65			V	
Input Clock Low Voltage	$V_{L(SYNC)}$			1.25	V	
Synchronization Output						
Clock Frequency	f_{CLK}		f_{SW}		kHz	
Positive Pulse Duty Cycle	$t_{CLK\_PULSE\_DUTY}$		50		%	
Rise or Fall Time	$t_{CLK\_RISE\_FALL}$		2		ns	
High Level Voltage	$V_{H(SYNC\_OUT)}$		V_{REG}		V	
PRECISION ENABLING						EN1, EN2, and EN3 pins
Enable Voltage Range	V_{EN_RANGE}	0		18	V	
High Level Threshold	$V_{TH\_H(EN)}$		0.615	0.67	V	
Low Level Threshold	$V_{TH\_L(EN)}$	0.52	0.575		V	
Source Current (High Level)	$I_{TH\_H(EN)}$	0.48	0.9	1.55	µA	Above the rising threshold
Source Current (Low Level)	$I_{TH\_L(EN)}$	2.0	3.5	6.0	µA	Below the falling threshold
POWER GOOD						
Rising High Threshold	$V_{PWRGD(RISE\_H)}$		105		%	
Rising Low Threshold	$V_{PWRGD(RISE\_L)}$		95		%	
Falling High Threshold	$V_{PWRGD(FALL\_H)}$		107		%	
Falling Low Threshold	$V_{PWRGD(FALL\_L)}$		93		%	
Internal Power-Good Hysteresis	$V_{PWRGD(HYS)}$		2		%	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Falling Delay for PWRGD Pin[1]	$t_{PWRGD\_FALL\_DLY}$		$4 \times t_{SW}$		ms	
Rising Delay for PWRGD Pin[2]	$t_{PWRGD\_RISE\_DLY}$		0 or t_{SET}		ms	2.6 ms when the CFG2 resistor value (R_{CFG2}) = 0 Ω
Leakage Current for PWRGD Pin	$I_{PWRGD\_LEAKAGE}$		0.1	1	µA	
Output Low Voltage for PWRGD Pin	V_{PWRGD_LOW}		10	150	mV	PWRGD current (I_{PWRGD}) = 1 mA
PMBUS INTERFACE						SCL and SDA pins
High Level Threshold	V_{IH}	1.4			V	
Low Level Threshold	V_{IL}			0.4	V	
LOGIC OUTPUTS						
Low Level Output Voltage	V_{SDA_LOW}			0.4	V	SDA pin, PMBus supply voltage (V_{DDIO}) = 3.3 V, SDA current (I_{SDA}) = 3 mA
THERMAL SHUTDOWN (TSD)						
Threshold	T_{SHDN}		175		°C	
Hysteresis	T_{HYS}		15		°C	

[1] t_{SW} is the switching period.
[2] t_{SET} is the setting time programmed by CFG2.

BUCK REGULATOR SPECIFICATIONS

V_{IN} = 12 V, V_{REG} = 4.8 V, f_{SW} = 600 kHz for all channels, T_J = −40°C to +150°C for minimum and maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
CHANNEL 1 SYNCHRONOUS BUCK REGULATOR						
Continuous Output Current	I_O		7		A	Determined by the CFG1 pin configuration (see Table 11), CFG1 resistor (R_{CFG1}) = 0 Ω
			3.5		A	Determined by the CFG1 pin configuration (see Table 11), R_{CFG1} = open
FB1 Pin						
Voltage Range	V_{FB1}	408		790.5	mV	Via PMBus interface
Voltage Adjustment LSB			1.5		mV	
Voltage (Default)			600		mV	
Voltage Accuracy (Default)	$V_{FB1\_DEFAULT}$					$V_{FB1\_DEFAULT}$ = 600 mV (VID1 code = 128)
		−0.25		+0.25	%	T_J = 25°C
		−0.62		+0.69	%	−40°C ≤ T_J ≤ +125°C
		−0.62		+0.83	%	−40°C ≤ T_J ≤ +150°C
Voltage Accuracy (Set by VID1 Register Value)	V_{FB1_VID}					−40°C ≤ T_J ≤ +150°C
Adjustable V_{FB1_VID} During DVS Function		−1.19		+1.44	%	V_{FB1} = 408 mV (VID1 code = 0)
		−0.68		+0.86	%	V_{FB1} = 504 mV (VID1 code = 64)
		−0.52		+0.68	%	V_{FB1} = 696 mV (VID1 code = 192)
		−0.69		+0.79	%	V_{FB1} = 790.5 mV (VID1 code = 255)
Bias Current	I_{FB1}			0.1	µA	Adjustable voltage

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SW1 Pin						
High-Side Power Field Effect Transistor (FET) On Resistance	$R_{DSON\_HS(1)}$		25		mΩ	Pin to pin measurement
Low-Side Power FET On Resistance	$R_{DSON\_LS(1)}$		12		mΩ	Pin to pin measurement
Valley Current-Limit Threshold	$I_{TH(ILIM1)}$	9.4			A	Current limit of Channel 1 (I_{LIM1}) = 7 A, T_J = 25°C
		4.4			A	I_{LIM1} = 3.5 A, T_J = 25°C
Negative Current-Limit Threshold	$I_{TH(ILIM1-NEG)}$		−5.0		A	
Minimum On Time	t_{MIN_ON1}		35	55	ns	f_{SW} = 250 kHz to 2500 kHz
Minimum Off Time	t_{MIN_OFF1}		120	150	ns	f_{SW} = 250 kHz to 2500 kHz
Error Amplifier for the COMP1 Pin						
Transconductance	g_{m1}	330	350	365	µS	
Soft Start Time	t_{SS1}		0.83 × t_{SET}		ms	t_{SET} = 2.6 ms when R_{CFG2} = 0 Ω
Hiccup Time	$t_{HICCUP1}$		7 × t_{SET}		ms	
Output Capacitor (C_{OUT}) Discharge Switch On Resistance	R_{DIS1}		75		Ω	
CHANNEL 2 SYNCHRONOUS BUCK REGULATOR						
Continuous Output Current	I_O		7		A	Determined by the CFG1 pin configuration (see Table 11), R_{CFG1} = 0 Ω
			3.5		A	Determined by CFG1 pin configuration (see Table 11), R_{CFG1} = open
FB2 Pin						
Voltage Range	V_{FB2}	408		790.5	mV	Via PMBus interface
Voltage Adjustment LSB			1.5		mV	
Voltage (Default)			600		mV	
Voltage Accuracy (Default)	$V_{FB2\_DEFAULT}$	−0.25		+0.25	%	T_J = 25°C
		−0.62		+0.69	%	−40°C ≤ T_J ≤ +125°C
		−0.62		+0.83		−40°C ≤ T_J ≤ +150°C
Voltage Accuracy (Set by VID2 Register Value)	V_{FB2_VID}					−40°C ≤ T_J ≤ +150°C
Adjustable V_{FB2_VID} During DVS Function		−1.19		+1.47	%	V_{FB2} = 408 mV (VID2 code = 0)
		−0.67		+0.86	%	V_{FB2} = 504 mV (VID2 code = 64)
		−0.50		+0.65	%	V_{FB2} = 696 mV (VID2 code = 192)
		−0.68		+0.77	%	V_{FB2} = 790.5 mV (VID2 code = 255)
Bias Current	I_{FB2}			0.1	µA	Adjustable voltage
SW2 Pin						
High-Side Power FET On Resistance	$R_{DSON\_HS(2)}$		25		mΩ	Pin to pin measurement
Low-Side Power FET On Resistance	$R_{DSON\_LS(2)}$		12		mΩ	Pin to pin measurement
Valley Current-Limit Threshold	$I_{TH(ILIM2)}$	9.4			A	Current limit of Channel 2 (I_{LIM2}) = 7 A, T_J = 25°C
		4.4			A	I_{LIM2} = 3.5 A, T_J = 25°C
Negative Current-Limit Threshold	$I_{TH(ILIM2-NEG)}$		−5.0		A	
Minimum On Time	t_{MIN_ON2}		35	55	ns	f_{SW} = 250 kHz to 2500 kHz
Minimum Off Time	t_{MIN_OFF2}		120	150	ns	f_{SW} = 250 kHz to 2500 kHz
Error Amplifier for the COMP2 Pin						
Transconductance	g_{m2}	330	350	365	µS	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Soft Start Time	t_{SS2}		$0.83 \times t_{SET}$		ms	t_{SET} = 2.6 ms when R_{CFG2} = 0 Ω
Hiccup Time	$t_{HICCUP2}$		$7 \times t_{SET}$		ms	
C_{OUT} Discharge Switch On Resistance	R_{DIS2}		75		Ω	
CHANNEL 3 SYNCHRONOUS BUCK REGULATOR						
Continuous Output Current	I_O		7		A	Determined by the CFG1 pin configuration (see Table 11), R_{CFG1} = 0 Ω
			3.5		A	Determined by the CFG1 pin configuration (see Table 11), R_{CFG1} = open
FB3 Pin						
Voltage Range	V_{FB3}	408		790.5	mV	Via PMBus interface
Voltage Adjustment LSB			1.5		mV	
Voltage (Default)			600		mV	
Voltage Accuracy (Default)	$V_{FB3\_DEFAULT}$	−0.25		+0.25	%	T_J = 25°C
		−0.62		+0.69	%	−40°C ≤ T_J ≤ +125°C
		−0.62		+0.83		−40°C ≤ T_J ≤ +150°C
Voltage Accuracy (Set by VID3 Register Value)	V_{FB3_VID}					−40°C ≤ T_J ≤ +150°C
Adjustable V_{FB3_VID} During DVS Function		−1.14		+1.37	%	V_{FB3} = 408 mV (VID3 code = 0)
		−0.67		+0.79	%	V_{FB3} = 504 mV (VID3code = 64)
		−0.51		+0.60	%	V_{FB3} = 696 mV (VID3 code = 192)
		−0.68		+0.71	%	V_{FB3} = 790.5 mV (VID3 code = 255)
Bias Current	I_{FB3}			0.1	µA	Adjustable voltage
SW3 Pin						
High-Side Power FET On Resistance	$R_{DSON\_HS(3)}$		85		mΩ	Pin to pin measurement
Low-Side Power FET On Resistance	$R_{DSON\_LS(3)}$		45		mΩ	Pin to pin measurement
Valley Current-Limit Threshold	$I_{TH(ILIM3)}$	4.2			A	Current limit of Channel 3 (I_{LIM3}) = 3 A, T_J = 25°C
		2.1			A	I_{LIM3} = 1.5 A, T_J = 25°C
Negative Current-Limit Threshold	$I_{TH(ILIM3-NEG)}$		−2.5		A	
Minimum On Time	t_{MIN_ON3}		35	55	ns	f_{SW} = 250 kHz to 2500 kHz
Minimum Off Time	t_{MIN_OFF3}		120	150	ns	f_{SW} = 250 kHz to 2500 kHz
Error Amplifier for the COMP3 Pin						
Transconductance	g_{m3}	330	350	365	µS	
Soft Start Time	t_{SS3}		$0.83 \times t_{SET}$		ms	t_{SET} = 2.6 ms when R_{CFG2} = 0 Ω
Hiccup Time	$t_{HICCUP3}$		$7 \times t_{SET}$		ms	
C_{OUT} Discharge Switch On Resistance	R_{DIS3}		75		Ω	

PMBus INTERFACE TIMING SPECIFICATIONS

T_A = 25°C and V_{DDIO} = 3.3 V, unless otherwise noted.

Table 3.

Parameter	Min	Typ	Max	Unit	Description
f_{SCL}	10		400	kHz	SCL clock frequency
t_{HIGH}	0.6		50	µs	SCL high time
t_{LOW}	1.3			µs	SCL low time
$t_{SU;DAT}$	100			ns	Data setup time
$t_{HD;DAT}$	300			ns	Data hold time[1]
$t_{TIMEOUT,SCL}$	25		35	ms	SCL low timeout (not shown in Figure 3)
$t_{TIMEOUT,SDA}$	25		35	ms	SDA low timeout (not shown in Figure 3)
$t_{SU;STA}$	0.6			µs	Setup time for a repeated start condition
$t_{HD;STA}$	0.6			µs	Hold time for a start or repeated start condition
t_{BUF}	1.3			µs	Bus free time between a stop condition and a start condition
$t_{SU;STO}$	0.6			µs	Setup time for a stop condition
t_R	20		300	ns	Rise time of SCL and SDA
t_F	20		300	ns	Fall time of SCL and SDA
t_{SP}			50	ns	Pulse width of suppressed spike (not shown in Figure 3)
C_B[2]			400	pF	Capacitive load for each bus line

[1] A master device must provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IH} minimum of the SCL signal) to bridge the undefined region of the SCL falling edge.

[2] C_B is the total capacitance of one bus line in picofarads (pF).

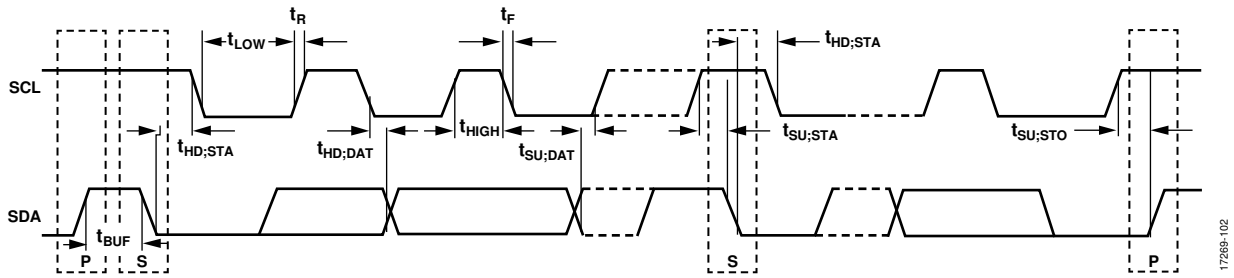


Figure 3. Serial Bus Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
VBIAS to GND	−0.3 V to +21 V
PVINx to PGND	−0.3 V to +21 V
SWx to PGND	−0.3 V to +21 V
RAMPx to GND	−0.3 V to +21 V
PGND to GND	−0.3 V to +0.3 V
BST1 to SW1	−0.3 V to +6.5 V
BST2 to SW2	−0.3 V to +6.5 V
BST3 to SW3	−0.3 V to +6.5 V
CFG1 and CFG2 to GND	−0.3 V to +6.5 V
ENx to GND	−0.3 V to +21 V
VREG to GND	−0.3 V to +6.5 V
SYNC/MODE to GND	−0.3 V to +6.5 V
RT to GND	−0.3 V to +6.5 V
PWRGD to GND	−0.3 V to +6.5 V
FB1, FB2, and FB3 to GND	−0.3 V to +6.5 V
COMPx to GND	−0.3 V to +6.5 V
SCL and SDA to GND	−0.3 V to +6.5 V
Temperature Range	
Storage	−65°C to +150°C
Operational Junction	−40°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Thermal resistance values specified in Table 5 are simulated based on JEDEC specifications (unless specified otherwise) and are used in compliance with JESD51-12. Using enhanced heat removal (PCB, heat sink, and airflow) techniques improve thermal resistance values.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}[1]	θ_{JB}	Ψ_{JT}	Ψ_{JB}	Unit
CC-43-1	26.0	14.3	9.3	0.2	9.0	°C/W

[1] For the θ_{JC} test, 100 µm thermal interface material (TIM) was used. TIM is assumed to have 3.6 W/mK.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

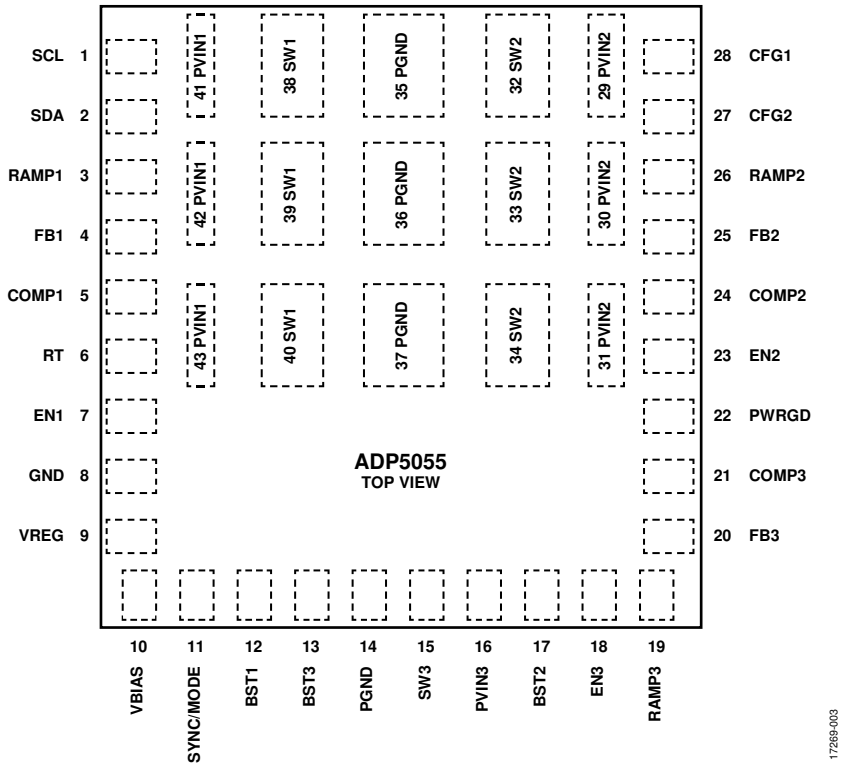


Figure 4. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	SCL	Clock Input for the PMBus Interface.
2	SDA	Data Input and Output for the PMBus Interface. Open-drain input and output port.
3	RAMP1	Slope Compensation Setting for Channel 1. Connect a resistor from RAMP1 to ground to set the slope compensation.
4	FB1	Feedback Sensing Input for Channel 1.
5	COMP1	Error Amplifier Output for Channel 1. Connect an RC network from COMP1 to ground.
6	RT	Frequency Setting (RT). Connect a resistor (R_{RT}) from RT to ground to program the switching frequency.
7	EN1	Enable Input for Channel 1.
8	GND	Analog Ground.
9	VREG	Output of the Internal 4.8 V Regulator. The control circuitry is powered from the VREG voltage. Place a 4.7 µF ceramic capacitor (X7R or X5R) between VREG and GND.
10	VBIAS	Bias Input Voltage Pin to the Supply Internal Regulator.
11	SYNC/MODE	Synchronization Input and Output (SYNC). To synchronize the switching frequency of the device to an external clock, connect SYNC to an external clock with a frequency from 250 kHz to 2500 kHz. SYNC can also be configured as a synchronization clock output via the CFG1 pin configuration. FPWM or Automatic PWM/PSM Selection Pin (MODE). When MODE is logic high, each channel works in FPWM mode. When MODE is logic low, all channels operate in automatic PWM/PSM mode.
12	BST1	Supply Rail for the High-Side Gate Drive in Channel 1. Place a 0.1 µF capacitor (X7R or X5R) between SW1 and BST1.
13	BST3	Supply Rail for the High-Side Gate Drive in Channel 3. Place a 0.1 µF capacitor (X7R or X5R) between SW3 and BST3.
14	PGND	Power Ground for All Channels.
15	SW3	Switching Node Output for Channel 3.
16	PVIN3	Power Input for Channel 3.
17	BST2	Supply Rail for the High-Side Gate Drive in Channel 2. Place a 0.1 µF capacitor (X7R or X5R) between SW2 and BST2.

Pin No.	Mnemonic	Description
18	EN3	Enable Input for Channel 3.
19	RAMP3	Slope Compensation Setting for Channel 3. Connect a resistor from RAMP3 to ground to set the slope compensation.
20	FB3	Feedback Sensing Input for Channel 3.
21	COMP3	Error Amplifier Output for Channel 3. Connect an RC network from COMP3 to ground.
22	PWRGD	Power Good Output for Selective Channels.
23	EN2	Enable Input for Channel 2.
24	COMP2	Error Amplifier Output for Channel 2. Connect an RC network from COMP2 to ground.
25	FB2	Feedback Sensing Input for Channel 2.
26	RAMP2	Slope Compensation Setting for Channel 2. Connect a resistor from RAMP2 to ground to set the slope compensation.
27	CFG2	System Configuration Pin 2. Connect a resistor from CFG2 to ground to program the t_{SET} timer, fast transient mode, and PMBus address settings.
28	CFG1	System Configuration Pin 1. Connect a resistor from CFG1 to ground to program the current-limit, parallel operation, and clock output settings.
29 to 31	PVIN2	Power Input for Channel 2.
32 to 34	SW2	Switching Node Output for Channel 2.
35 to 37	PGND	Power Ground for All Channels.
38 to 40	SW1	Switching Node Output for Channel 1.
41 to 43	PVIN1	Power Input for Channel 1.

TYPICAL PERFORMANCE CHARACTERISTICS

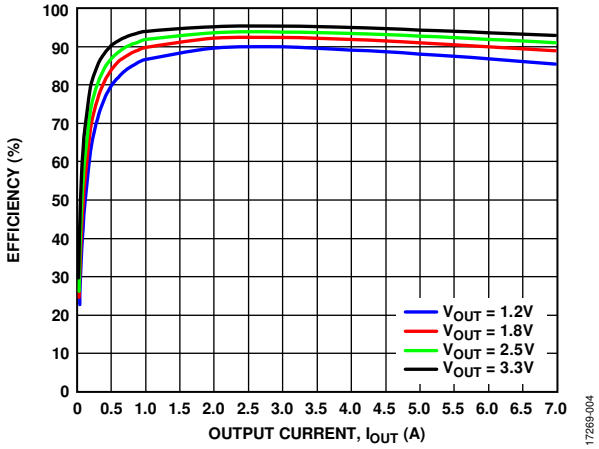


Figure 5. Channel 1/Channel 2 Efficiency Curve, V_{IN} = 5 V, f_{SW} = 600 kHz, FPWM Mode (V_{OUT} Is the Output Voltage)

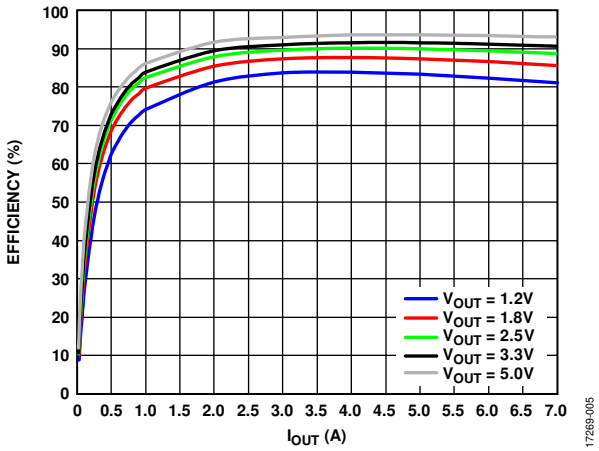


Figure 6. Channel 1/Channel 2 Efficiency Curve, V_{IN} = 12 V, f_{SW} = 600 kHz, FPWM Mode

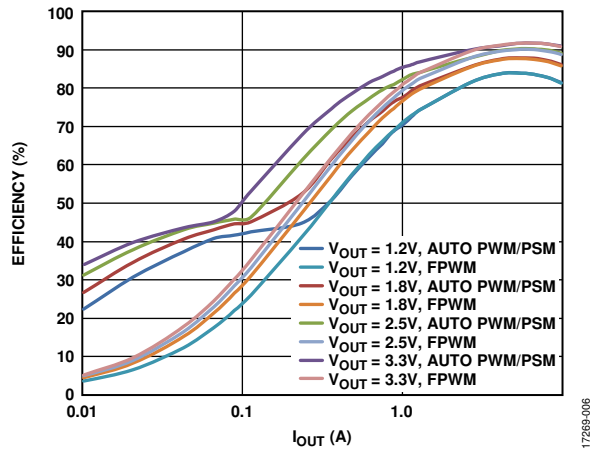


Figure 7. Channel 1/Channel 2 Efficiency Curve, V_{IN} = 12 V, f_{SW} = 600 kHz, FPWM and Automatic PWM/PSM Modes

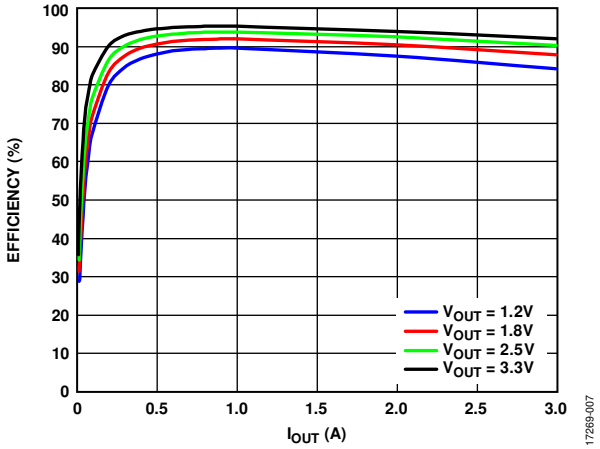


Figure 8. Channel 3 Efficiency Curve, V_{IN} = 5 V, f_{SW} = 600 kHz, FPWM Mode

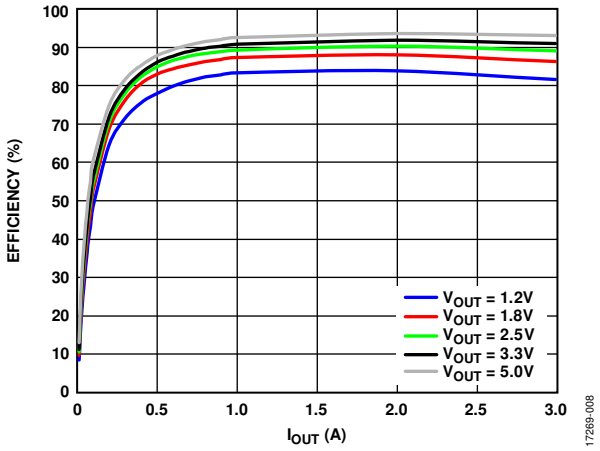


Figure 9. Channel 3 Efficiency Curve, V_{IN} = 12 V, f_{SW} = 600 kHz, FPWM Mode

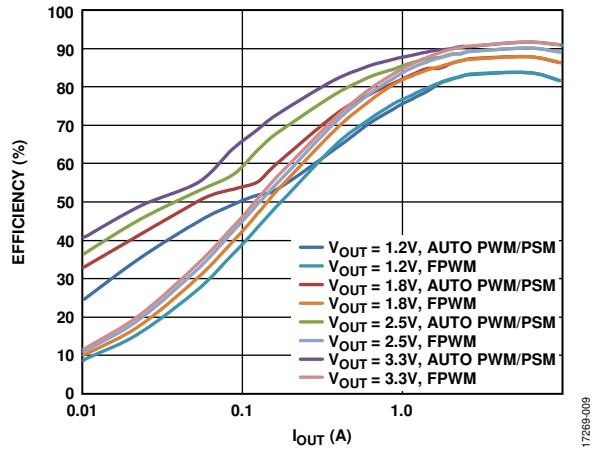


Figure 10. Channel 3 Efficiency Curve, V_{IN} = 12 V, f_{SW} = 600 kHz, FPWM Mode and Automatic PWM/PSM Modes

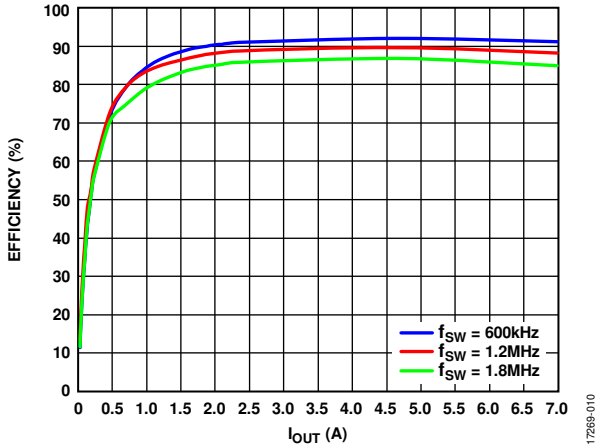


Figure 11. Channel 1/Channel 2 Efficiency Curve, V_{IN} = 12 V, V_{OUT} = 3.3 V, FPWM Mode (600 kHz, 1.2 MHz, 1.8 MHz)

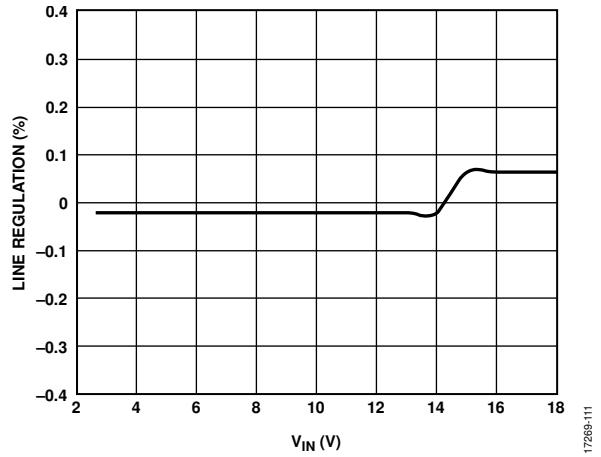


Figure 12. Channel 1/Channel 2 Line Regulation, V_{OUT} = 1.2 V, I_{OUT} = 7 A, f_{SW} = 600 kHz, FPWM Mode

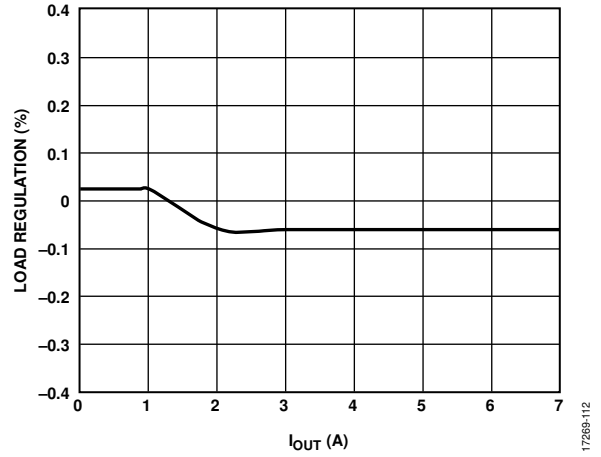


Figure 13. Channel 1/Channel 2 Load Regulation, V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 600 kHz, FPWM Mode

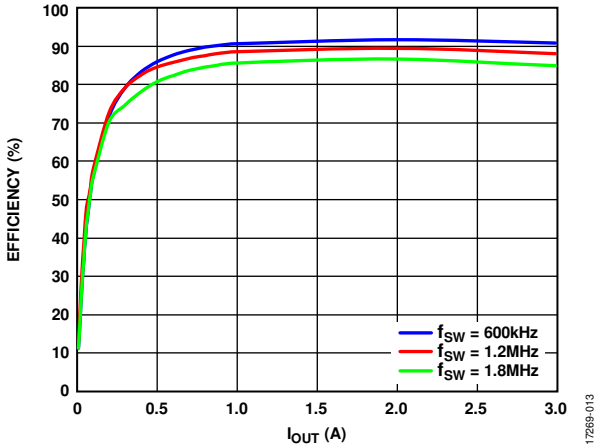


Figure 14. Channel 3 Efficiency Curve, V_{IN} = 12 V, V_{OUT} = 3.3 V, FPWM Mode (600 kHz, 1.2 MHz, 1.8 MHz)

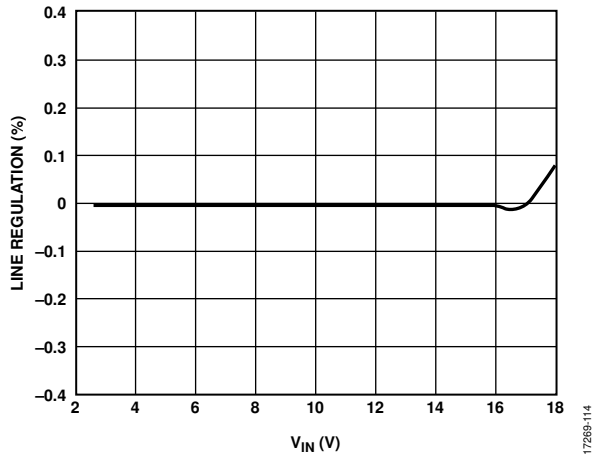


Figure 15. Channel 3 Line Regulation, V_{OUT} = 1.2 V, I_{OUT} = 3 A, f_{SW} = 600 kHz, FPWM Mode

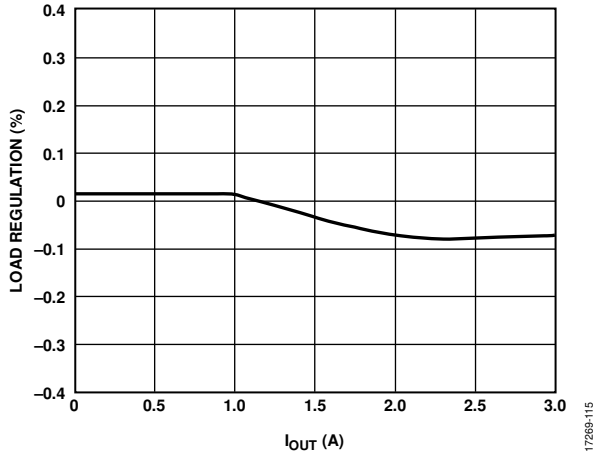


Figure 16. Channel 3 Load Regulation, V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 600 kHz, FPWM Mode

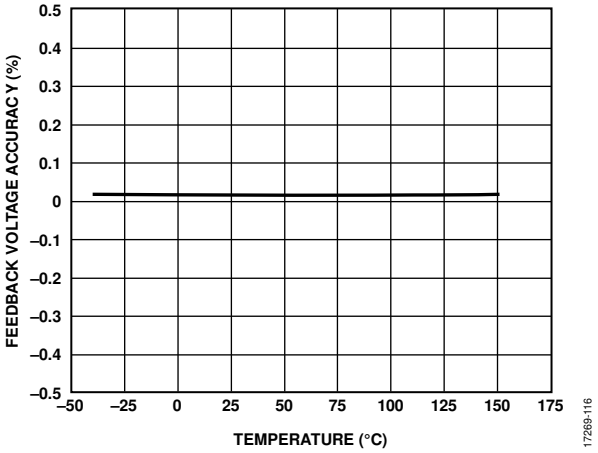


Figure 17. Feedback Voltage Accuracy vs. Temperature for Channel 1

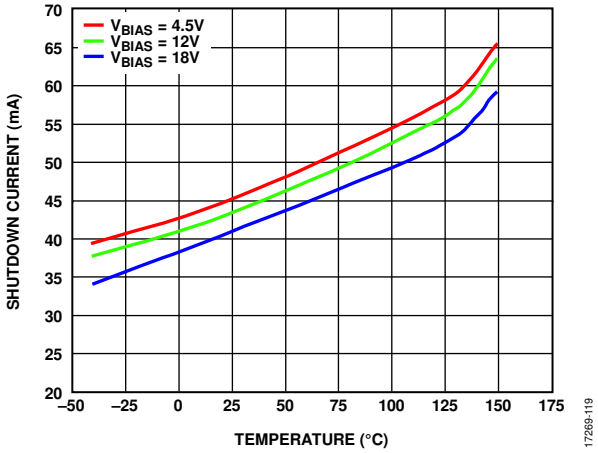


Figure 20. Shutdown Current vs. Temperature (EN1, EN2, and EN3 Low)

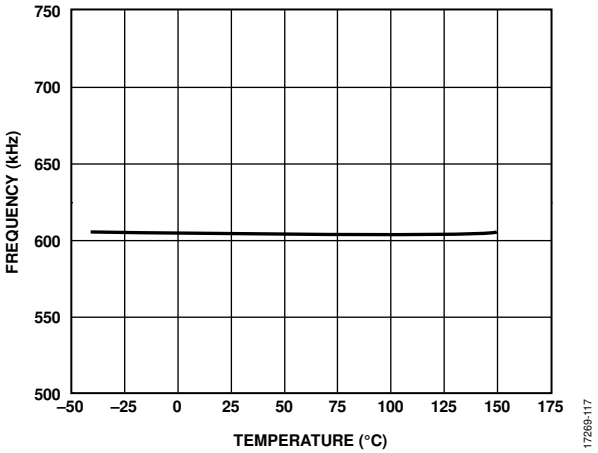


Figure 18. Frequency vs. Temperature, V_{IN} = 12 V

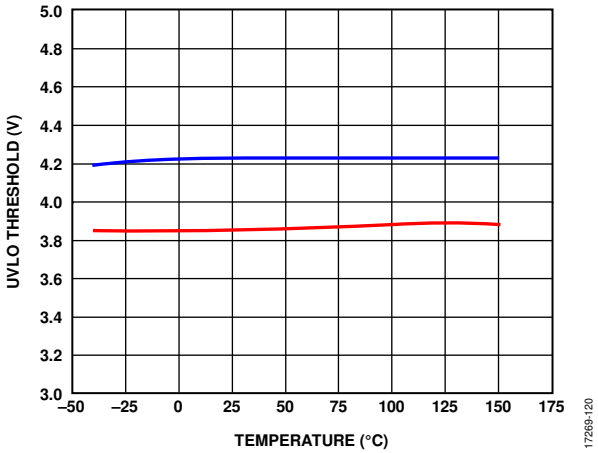


Figure 21. UVLO Threshold vs. Temperature

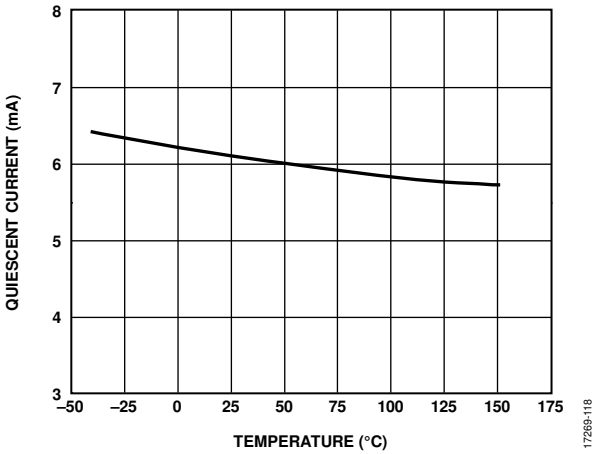


Figure 19. Quiescent Current vs. Temperature (Includes PVIN1, PVIN2, and PVIN3)

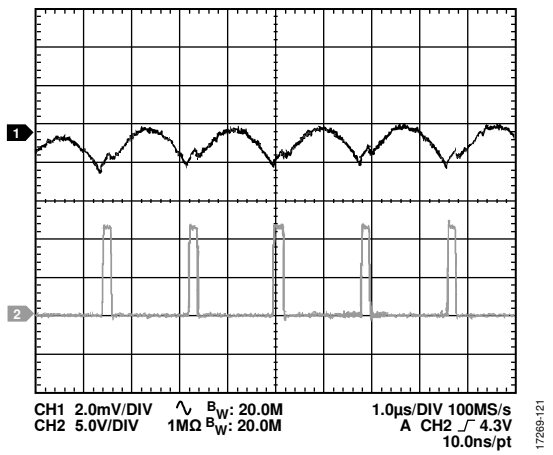


Figure 22. Channel 1/Channel 2 Steady State Waveform, V_{IN} = 12 V, V_{OUT} = 1.2 V, I_{OUT} = 7 A, f_{SW} = 600 kHz, L = 1 µH, C_{OUT} = 47 µF × 6, FPWM Mode, Channel 1 = V_{OUT}, Channel 2 = Switching Point (SW)

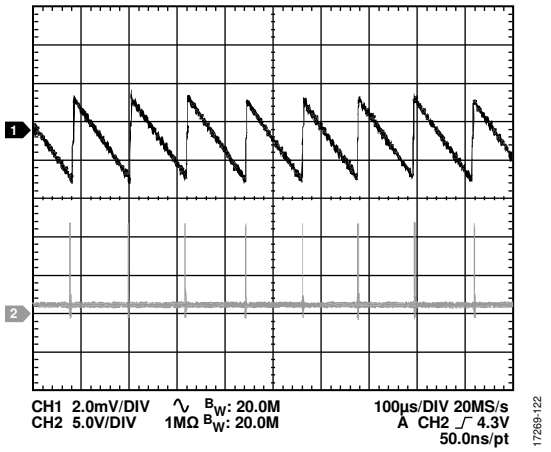


Figure 23. Channel 1/Channel 2 Steady State Waveform, V_{IN} = 12 V, V_{OUT} = 1.2 V, I_{OUT} = 10 mA, f_{SW} = 600 kHz, L = 1 µH, C_{OUT} = 47 µF × 6, Automatic PWM/PSM, Channel 1 = V_{OUT}, Channel 2 = SW

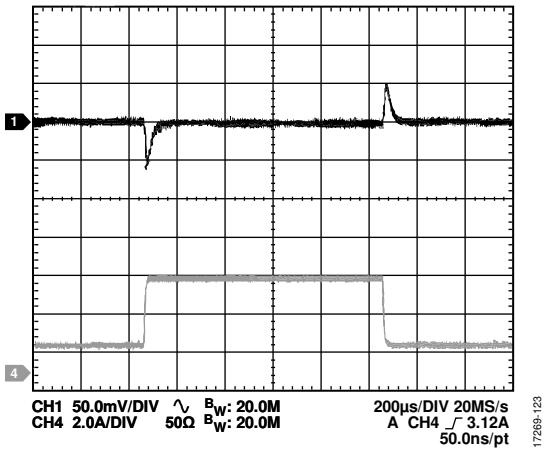


Figure 24. Load Transient, Channel 1/Channel 2 From 1.5 A to 5 A, V_{IN} = 12 V, V_{OUT} = 3.3 V, f_{SW} = 600 kHz, L = 1 µH, C_{OUT} = 47 µF × 6, 1 A/µs, Channel 1 = V_{OUT}, Channel 4 = I_{OUT}

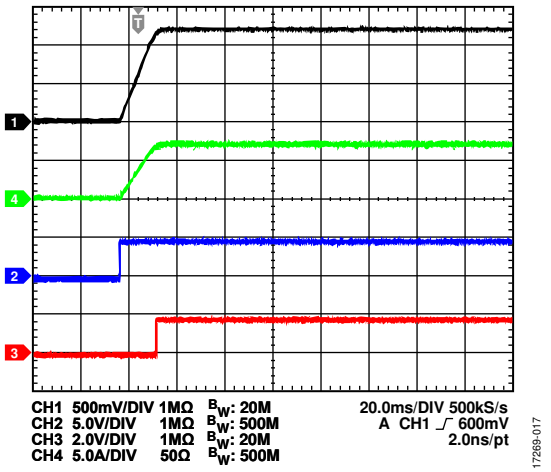


Figure 25. Channel 1/Channel 2 Soft Start with 7 A Resistance Load, V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 600 kHz, L = 1 µH, C_{OUT} = 47 µF × 6, Channel 1 = V_{OUT}, Channel 2 = EN, Channel 3 = PWRGD, Channel 4 = I_{OUT}

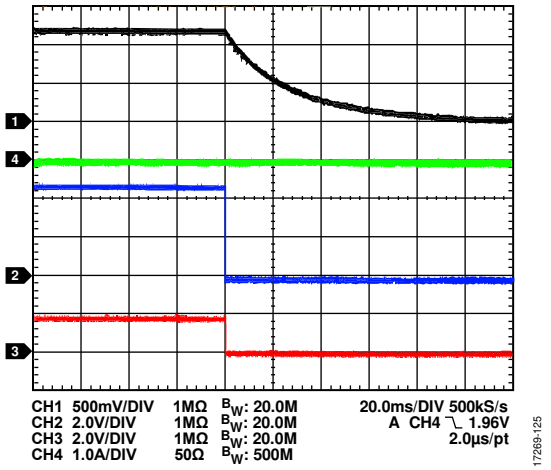


Figure 26. Channel 1/Channel 2 Shutdown with Active Output Discharge, V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 600 kHz, L = 1 µH, C_{OUT} = 47 µF × 6, Channel 1 = V_{OUT}, Channel 2 = EN, Channel 3 = PWRGD, Channel 4 = I_{OUT}

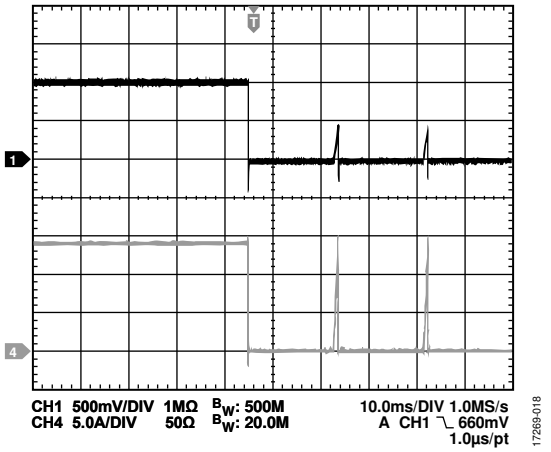


Figure 27. Channel 1/Channel 2 Short-Circuit Protection Entry, V_{IN} = 12 V, V_{OUT} = 1.0 V, f_{SW} = 600 kHz, L = 1 µH, C_{OUT} = 47 µF × 6, Channel 1 = V_{OUT}, Channel 4 = I_{OUT}

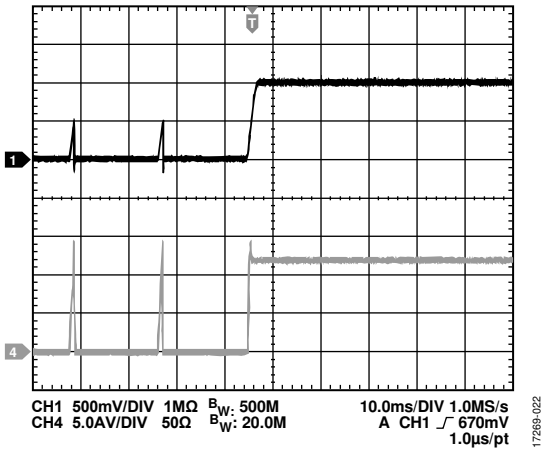


Figure 28. Channel 1/Channel 2 Short-Circuit Protection Recovery, V_{IN} = 12 V, V_{OUT} = 1.0 V, f_{SW} = 600 kHz, L = 1 µH, C_{OUT} = 47 µF × 6, Channel 1 = V_{OUT}, Channel 4 = I_{OUT}

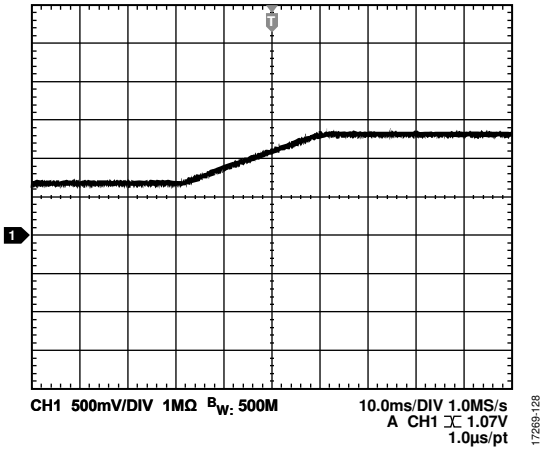


Figure 29. Channel 1/Channel 2 DVS from 0.62 V to 1.24 V, 12 mV/ms, V_{IN} = 12 V, I_{OUT} = 7 A

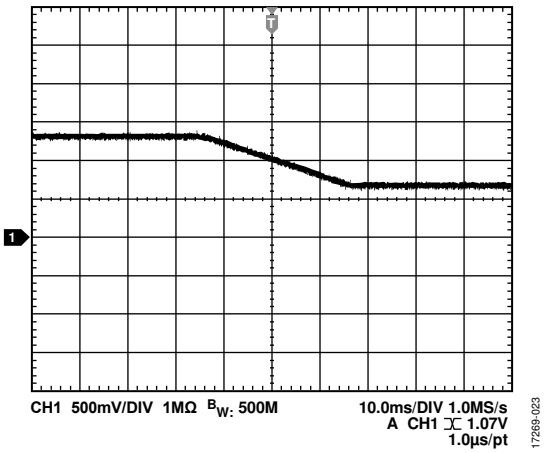


Figure 30. Channel 1/Channel 2 DVS from 1.24 V to 0.62 V, 12 mV/ms, V_{IN} = 12 V, I_{OUT} = 7 A

THEORY OF OPERATION

The ADP5055 is a power management unit that combines three high performance buck regulators with a PMBus interface in a 43-terminal LGA package to meet demanding performance and board space requirements. The device enables direct connection to high input voltages up to 18 V with no preregulators to make applications simpler and more efficient.

BUCK REGULATOR OPERATIONAL MODES

PWM Mode

In PWM mode, the buck regulators in the ADP5055 operate at a fixed frequency. An internal oscillator programmed by the RT pin sets this frequency. The ADP5055 uses the low-side MOSFET current for the PWM control as shown in Figure 31. The valley current information is captured at the end of the off period and combines with the slope ramp to form the emulated current ramp voltage. The resistor from the RAMPx pin to ground controls the slope ramp voltage. At the start of each oscillator cycle, the high-side MOSFET turns on, and the inductor current increases until the emulated current ramp voltage crosses the COMPx voltage. When the current ramp voltage crosses the COMPx voltage, it turns off the high-side MOSFET and turns on the low-side MOSFET, which in turn places a negative voltage across the inductor, causing a reduction in the inductor current. The low-side MOSFET stays on for the remainder of the cycle.

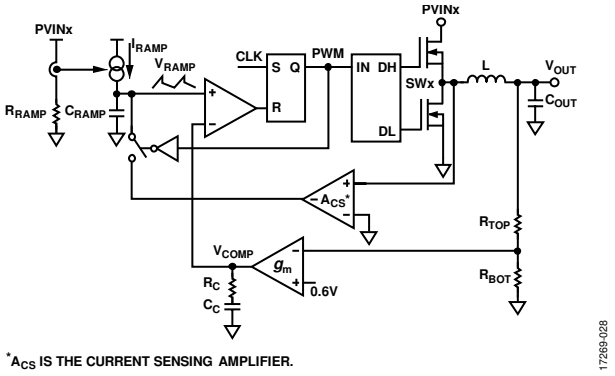


Figure 31. FlexMode™ PWM Control Architecture

PSM Mode

To achieve higher efficiency at light loads, the buck regulators in the ADP5055 smoothly transition to variable frequency PSM operation when the output load falls below the PSM current threshold. When V_{OUT} falls below regulation, the buck regulator enters PWM mode for a few oscillator cycles until the voltage increases to within regulation. During the idle time between bursts, the MOSFET turns off, and the output capacitor supplies all the output current.

The PSM comparator monitors the COMPx node, which represents the emulated current ramp. The average PSM current threshold depends on the V_{IN}, the V_{OUT}, the inductor, and the output capacitor. Because the output voltage occasionally falls below regulation and then recovers, the output voltage ripple in PSM operation is larger than the ripple in the FPWM mode of operation under light load conditions.

FPWM and Automatic PWM/PSM Modes

The buck regulators can be configured to always operate in FPWM mode using the SYNC/MODE pin and the PMBus interface. In FPWM mode, the regulator continues to operate at a fixed frequency even when the output current is below the PWM/PSM threshold. In FPWM mode, efficiency is lower compared to PSM mode under light load conditions. The low-side MOSFET remains on when the inductor current falls to less than 0 A, causing the ADP5055 to enter continuous conduction mode (CCM).

The buck regulators can be configured to operate in automatic PWM/PSM mode using the SYNC/MODE pin and the PMBus interface. In automatic PWM/PSM mode, the buck regulators operate in either PWM mode or PSM mode, depending on the output current. When the average output current falls below the PWM/PSM threshold, the buck regulator enters PSM mode operation. In PSM mode, the regulator operates with a reduced switching frequency to maintain high efficiency. The low-side MOSFET turns off when the inductor current reaches 0 A, causing the regulator to operate in discontinuous mode (DCM).

The user can alternate between FPWM mode and automatic PWM/PSM mode during operation. The flexible configuration capability during operation of the device enables efficient power management.

When a logic high level is applied to the SYNC/MODE pin (or when SYNC/MODE is configured as a clock input or output), the operational mode of each channel is set by the PSMx_ON bit in Register 0xD4, CTRL_MODE2. A value of 0 for the PSMx_ON bit configures the channel for FPWM mode. A value of 1 configures the channel for automatic PWM/PSM mode.

When a logic low level is applied to the SYNC/MODE pin, the operational mode of all three buck regulators is automatic PWM/PSM mode, and the settings of the PSMx_ON bits in Register 0xD4, CTRL_MODE2 are ignored.

Table 7 describes the function of the SYNC/MODE pin when a logic high level is applied to the SYNC/MODE pin in setting the operational mode of the device.

Table 7. Configuring the Mode of Operation Using the SYNC/MODE Pin

SYNC/MODE Pin	Mode of Operation for Each Channel
High	Specified by the PSMx_ON bit setting in Register 0xD4, CTRL_MODE2 (0 = FPWM mode, and 1 = automatic PWM/PSM mode)
Clock Input/Output	Via CFG1
Low	Automatic PWM/PSM mode (PSMx_ON bit settings in Register 0xD4, CTRL_MODE2 are ignored)

For example, with the SYNC/MODE pin high, write 1 to the PSM3_ON bit in Register 0xD4 to configure automatic PWM/PSM mode operation for Channel 3 and write 0 to the PSM1_ON and PSM2_ON bits to configure FPWM mode for Channel 1 and Channel 2.

ADJUSTABLE OUTPUT VOLTAGES

The ADP5055 provides an adjustable output voltage via an external resistor divider. For the adjustable output settings, use an external resistor divider to set the desired output voltage via the feedback reference voltage. The default reference voltage on each feedback (FBx) pin is 600 mV for each channel.

DYNAMIC VOLTAGE SCALING (DVS)

The ADP5055 provides a DVS function for Channel 1 to Channel 3. These reference voltages can be programmed in real time via the PMBus interface in Register 0xD8 to Register 0xDA. The DVS_INTVALx bits in Register 0xDB are used to set the step interval during the transition for individual channel. Table 8 lists the adjustable output voltage ranges configured by the VIDx bits. The default output voltage can also be programmed by factory fuse. If a different default output voltage is required, contact a local Analog Devices, Inc., sales or distribution representative.

During the DVS transition, the device generates a blanking period, which is a DVS transition period combined with a 128-cycle delay timer (see Figure 32). During this DVS blanking period, the regulator is forced into FPWM mode operation (regardless of PSM setting) to provide both current source and sink capability. Hiccup protection is masked as well, if Register 0xD4, Bit 7, OCP_BLANKING, is set. Make sure to use appropriate DVS slew rate and reasonable output capacitors to enable the output voltage to track VIDx changes and maintain PWRGD signal during DVS transition period.

Both the upper and lower thresholds are configured by the VIDx_HIGH bits and VIDx_LOW bits in Register 0xDC to Register 0xDE to limit the DVS voltage adjustment range in each channel. This limit provides extra safety against the accidently programmable VIDx code, which can cause system failures.

INTERNAL REGULATOR (VREG)

The internal VREG regulator in the ADP5055 provides a stable 4.8 V power supply for the internal circuitry. Connect a 4.7 µF (X5R or X7R) ceramic capacitor between VREG and ground. The internal VREG regulator is always active as long as the VBIAS voltage is available. The current-limit circuit is included in the VREG regulator to protect the circuit when the device is heavily loaded.

SEPARATE SUPPLY APPLICATIONS

The ADP5055 supports separate input voltages for the triple buck regulators so that the input voltages for the triple buck regulators can connect to different supply voltages. The ADP5055 integrates each 100 nF, 25 V, X8L ceramic capacitor to provide local decoupling from PVIN1 and PVIN2 to power ground in Channel 1 and Channel 2.

The VBIAS voltage provides the power supply for the internal regulators and the control circuitry. Therefore, if the user plans to use separate supply voltages for the buck regulators, the VBIAS voltage must be greater than the UVLO threshold before the other channels can operate.

Precision enabling can monitor the voltages of the PVIN1, PVIN2, and PVIN3 pins and to delay the startup of the outputs to ensure that the voltages of the PVIN1, PVIN2, and PVIN3 pins are high enough to support the outputs in regulation. For more information, see the Precision Enabling section.

Table 8. Reference Voltage Ranges Set by the VIDx Bits

Channel	Default (mV)	Register	Adjustable Reference Voltage Range Set by the VIDx Bits
Channel 1	600	0xD8, VID1	408 mV to 790.5 mV per 1.5 mV step
Channel 2	600	0xD9, VID2	408 mV to 790.5 mV per 1.5 mV step
Channel 3	600	0xDA, VID3	408 mV to 790.5 mV per 1.5 mV step

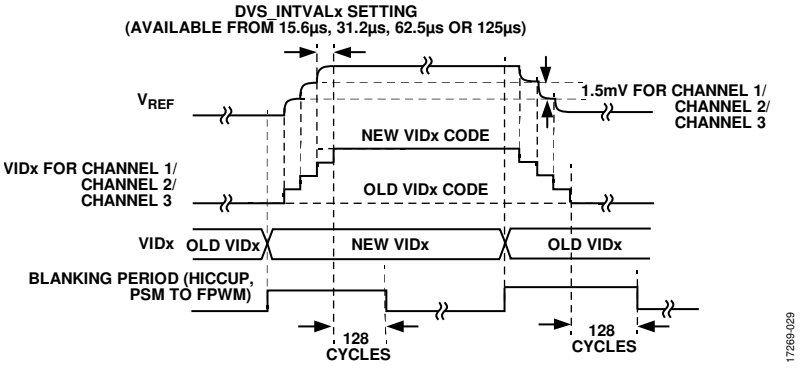


Figure 32. Dynamic Voltage Scaling

The ADP5055 supports cascading supply operation for the triple buck regulators. As shown in Figure 33, PVIN2 and PVIN3 are powered from the Channel 1 output. In this configuration, the Channel 1 output voltage must be higher than the UVLO threshold for PVIN2 and PVIN3.

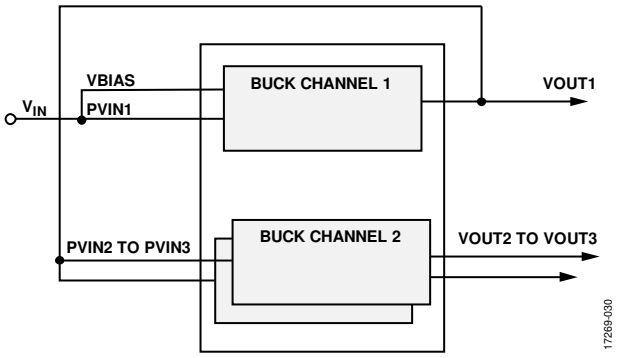


Figure 33. Cascading Supply Application

BOOTSTRAP CIRCUITRY

Each buck regulator in the ADP5055 has an integrated bootstrap regulator. The bootstrap regulator requires a 0.1 µF ceramic capacitor (X5R or X7R) between the BSTx and SWx pins to provide the gate drive voltage for the high-side MOSFET.

ACTIVE OUTPUT DISCHARGE SWITCH

Each buck regulator in the ADP5055 integrates a discharge switch from the switching node to ground. This switch is turned on when the associated regulator is disabled, which helps to discharge the output capacitor quickly. The typical value of the discharge switch is 75 Ω for Channel 1 to Channel 3.

The discharge switch can be programmed individually by the DSCGx_ON bits in Register 0xD4, CTRL_MODE2, via the PMBus interface.

PRECISION ENABLING

The ADP5055 has an enable control pin for each regulator. The enable control pin (ENx) features a precision enable circuit with a 0.615 V reference voltage. When the voltage at the ENx pin is greater than 0.615 V (typical high level threshold), the regulator is enabled. When the ENx pin voltage falls below 0.575 V (typical low level threshold), the regulator is disabled. The ADP5055 turns off the low-side MOSFET only after the inductor current reaches zero.

The precision enable pin has an internal pull-down current source (3.5 µA) that provides a default turn-off when the enable pin is left open. When the enable pin exceeds 0.615 V (typical high level threshold), the regulator is enabled and the internal pull-down current source at the enable pin decreases to 0.9 µA. The precision enabling uses the ratio of the external resistor divider to program the UVLO threshold to monitor either input voltage or output voltage, while using the absolute value of the external resistor divider to program the hysteresis window. For more information, see the Programming the UVLO Input section.

To force the regulator to automatically start up when input power is applied, connect the enable pin (ENx) to the VREG pin.

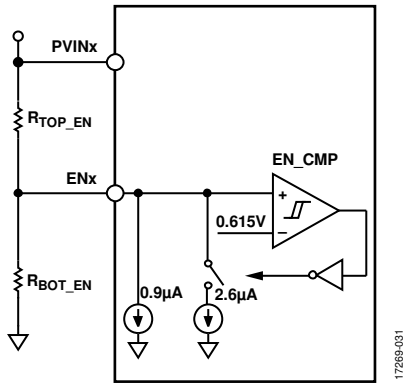


Figure 34. Precision Enable Diagram for One Channel

In addition to the ENx hardware pins, the PMBus interface can also be used to enable and disable each channel. The on and off status of a channel is controlled by the CHx_ON bits in Register 0xD1, Register CTRL123, and the external hardware enable pin (ENx).

The EN_MODE bits (Bit 1 and Bit 0) in Register 0xD3, CTRL_MODE1, are used to configure the different enabling methods of the individual channels. The default setting of the channel enable method by the EN_MODE bits specifies that the channel enable is controlled by the external hardware pin. Table 9 shows the logic for the channel enable control between the hardware pin and the register bits.

If some channels are unused, pull down the corresponding PVINx, ENx, COMPx, and FBx pins to ground and leave SWx, BSTx, and RAMPx floating.

Table 9. Enabling Configuration in the ADP5055

EN_MODE Bits	ENx Pin	CHx_ON Bit	Logic Between ENx Pin and CHx_ON Bit
00 (Default)	Valid	Ignored	Not applicable
01	Ignored	Valid	Not applicable
10	Valid	Valid	AND'ed logic
11	Valid	Valid	OR'ed logic

SEQUENCE MODE

The ADP5055 integrates the sequence control on each channel. When the ENx signal (enable method configured by the EN_MODE bits) goes high, each channel controlled by the sequencer begins a soft start after the delay time specified by the EN_DLYx bits in Register 0xD5 to Register 0xD7 (t_{EN_DLYx}). Similarly, when the ENx signal goes low, the channel turns off after the delay timer specified by the DIS_DLYx bits in Register 0xD5 to Register 0xD7 (t_{DIS_DLYx}). Note that Figure 35 shows the logical states of each channel controlled by the grouped ENx signal, and it does not show soft start and output discharge ramps.

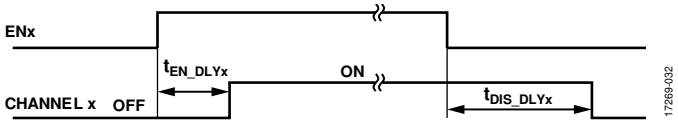


Figure 35. Sequencer Mode

OSCILLATOR

By connecting a resistor from the RT pin to ground, the f_{SW} of the ADP5055 can be set to a value between 250 kHz and 2500 kHz. Calculate the R_T resistor value as follows:

$$R_T\,(\text{k}\Omega) = (167, 305)/(f_{SW}\,(\text{kHz})^{0.098})$$

Figure 36 shows the typical relationship between the f_{SW} and the R_T resistance. The adjustable frequency allows users to make decisions based on the trade-off between efficiency and solution size.

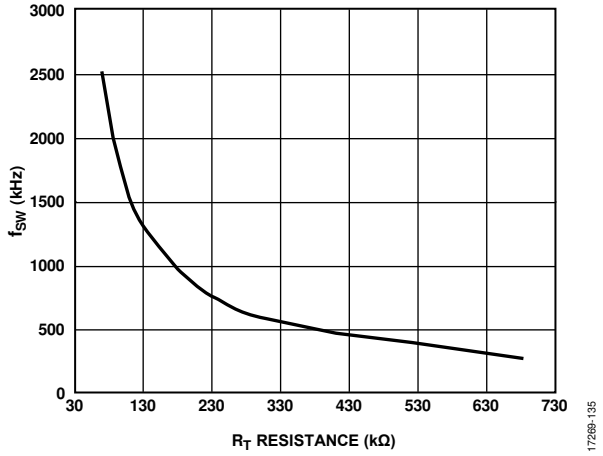


Figure 36. Switching Frequency vs. R_T Resistance

Out of Phase Operation

By default, the phase shift between Channel 1, Channel 2, and Channel 3 is 120°. This value provides the benefits of out-of-phase operation by reducing the input ripple current and lowering the ground noise.

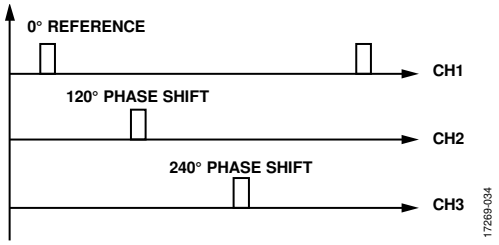


Figure 37. Phase Shift Diagram, Triple Buck Regulators

In the in-phase parallel operation configuration of Channel 1 and Channel 2, both channels operate in the same phase of Channel 1.

In the interleaved parallel operation configuration of Channel 1 and Channel 2, the phase shift between Channel 1, Channel 2, and Channel 3 is 0°, 180°, and 240°.

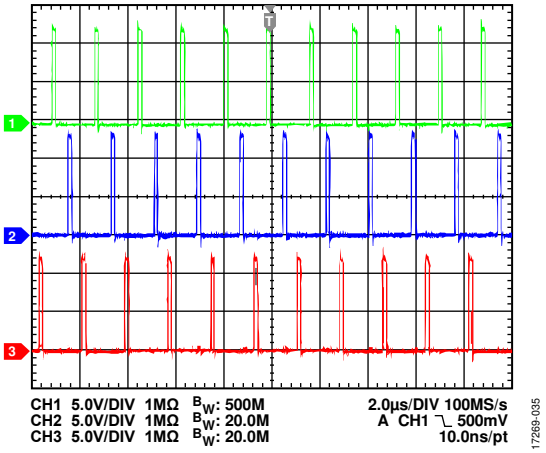


Figure 38. 120° Phase Shift Waveforms, Triple Buck Regulators Channel 1 = SW1, Channel 2 = SW2, Channel 3 = SW3

SYNCHRONIZATION INPUT AND OUTPUT

The switching frequency of the ADP5055 can be synchronized to an external clock with a frequency range from 250 kHz to 2500 kHz. The ADP5055 automatically detects the presence of an external clock applied to the SYNC/MODE pin, and the switching frequency transitions smoothly to the frequency of the external clock. When the external clock signal stops, the device automatically switches back to the internal clock and continues to operate.

Note that the internal switching frequency set by the RT pin must be programmed to a value that is close to the external clock value for successful synchronization. The suggested frequency difference is less than ±15% in typical applications.

The SYNC/MODE pin can be configured as a synchronization clock output by the CFG1 pin (refer to Table 11). A positive clock pulse with a 50% duty cycle and VREG voltage level is generated at the SYNC/MODE pin with a frequency equal to the internal switching frequency set by the RT pin.

Figure 39 shows two ADP5055 devices configured for frequency synchronization mode. One ADP5055 device is configured as the clock output to synchronize another ADP5055 device.

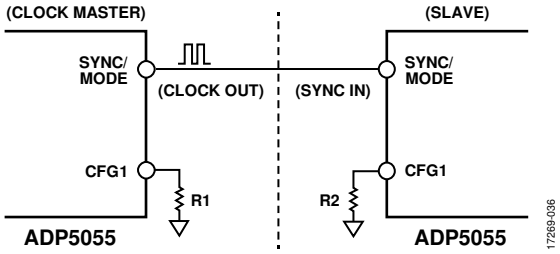


Figure 39. Two ADP5055 Devices Configured for Synchronization Mode

In the configuration shown in Figure 39, the phase shift between Channel 1 of the first ADP5055 device and Channel 1 of the second ADP5055 device is 0° (see Figure 40).

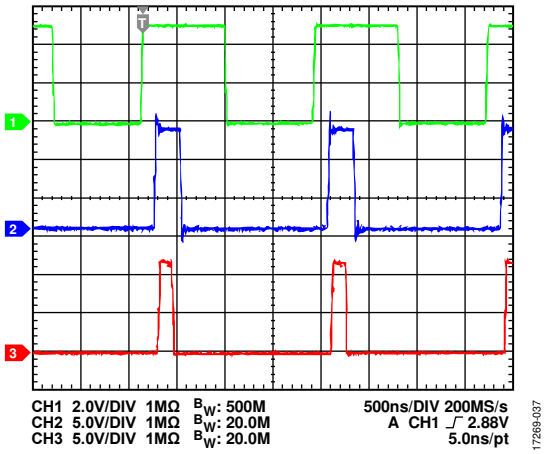


Figure 40. Waveforms of Two ADP5055 Devices Operating in Synchronization Mode, Channel 1 = Synchronization Clock Output, Channel 2 = SW1 of First ADP5055 Device, Channel 3 = SW1 of Second ADP5055 Device

SOFT START

The buck regulators in the ADP5055 include soft start circuitry that ramps the output voltage in a controlled manner during startup, thereby limiting the inrush current. The soft start time for all channels is fixed at 0.83 × t_{SET} timer (2.2 ms or 17.3 ms, depending on R_{CFG2} value, see Table 10).

FUNCTION CONFIGURATIONS (CFG1 AND CFG2)

The ADP5055 includes the CFG1 pin and CFG2 pin to decode the function configurations for all channels. Each pin has 16 logic statuses decoded by connecting one resistor to ground. It is recommended to use ±1% resistor tolerance to achieve accurate decoding.

This decoder circuitry only works in the initiation stage of the ADP5055 when it passes the power-on reset (POR) threshold when the VBIAS voltage is available, therefore, these configurations are latched into internal registers and cannot be changed in operation.

The CFG1 pin can program the SYNC/MODE pin function, the load output capability, and the parallel operation for all channels. Table 11 lists the values of the resistors needed to set different functionality in CFG1 pin.

The CFG2 pin can program the t_{SET} timer (2.6 ms or 20.8 ms), fast transient functionality, and the PMBus address for the ADP5055. Table 10 lists the values of the resistors needed to set the different functionality in the CFG2 pin.

Table 10. Configuration by the CFG2 Pin

R_{CFG2} (kΩ), ±1%	t_{SET} timer (ms)	Fast Transient	PMBus Address
0 (GND)	2.6	Disable	0x70
14.3	2.6	Disable	0x71
16.9	2.6	Disable	0x72
20.0	2.6	Disable	0x73
23.7	2.6	Enable	0x70
32.4	2.6	Enable	0x71
39.2	2.6	Enable	0x73
Open	20.8	Disable	0x70
47.5	20.8	Disable	0x71
57.6	20.8	Disable	0x72
71.5	20.8	Disable	0x73
90.9	20.8	Enable	0x70
127	20.8	Enable	0x71
200	20.8	Enable	0x72
511	20.8	Enable	0x73

Table 11. Configuration by the CFG1 Pin

R_{CFG1} (kΩ), ±1%	GPIO	Output Capability		
		Channel 1	Channel 2	Channel 3
0 (GND)	SYNC/MODE	7 A	7 A	3 A
14.3	SYNC/MODE	7 A	7 A	1.5 A
16.9	SYNC/MODE	7 A	3.5 A	3 A
20.0	SYNC/MODE	7 A	3.5 A	1.5 A
23.7	SYNC/MODE	Interleaved parallel (14 A)	Interleaved parallel (14 A)	3 A
Open	SYNC/MODE	3.5 A	3.5 A	1.5 A
32.4	SYNC/MODE	In phase parallel (14 A)	In phase parallel (14 A)	3 A
39.2	Clock output	7 A	7 A	3 A
47.5	Clock output	7 A	7 A	1.5 A
57.6	Clock output	7 A	3.5 A	3 A
71.5	Clock output	7 A	3.5 A	1.5 A
90.9	Clock output	3.5 A	7 A	3 A
127	Clock output	Interleaved parallel (14 A)	Interleaved parallel (14 A)	3 A
200	Clock output	3.5 A	3.5 A	1.5 A
511	Clock output	In phase parallel (14 A)	In phase parallel (14 A)	3 A

PARALLEL OPERATION

The ADP5055 supports 2-phase parallel operation of Channel 1 and Channel 2 to provide a single output with up to 14 A of current. The ADP5055 includes two different parallel operation modes via the CFG1 pin configuration: in-phase parallel operation and interleaved parallel operation.

In-Phase Parallel Operation

In-phase parallel operation parallels internal MOSFETs and driver circuitry between Channel 1 and Channel 2. This operation treats Channel 1 as the control master, and the Channel 2 control stage is ignored. The in-phase parallel operation mode uses a single inductor for external components and space saving. To configure Channel 1 and Channel 2 as a 2-phase single output in parallel operation, do the following (see Figure 41):

- Use the CFG1 pin to select parallel operation as specified in Table 11.
- Use the COMP1 pin as the compensation network.
- Use the FB1 pin to set the output voltage.
- Use the EN1 pin to enable the channel.
- Connect the FB2 pin to ground (FB2 is ignored).
- Leave the COMP2 pin open (COMP2 is ignored).
- Leave the RAMP2 pin open (RAMP2 is ignored).
- Connect the EN2 pin to ground (EN2 is ignored).

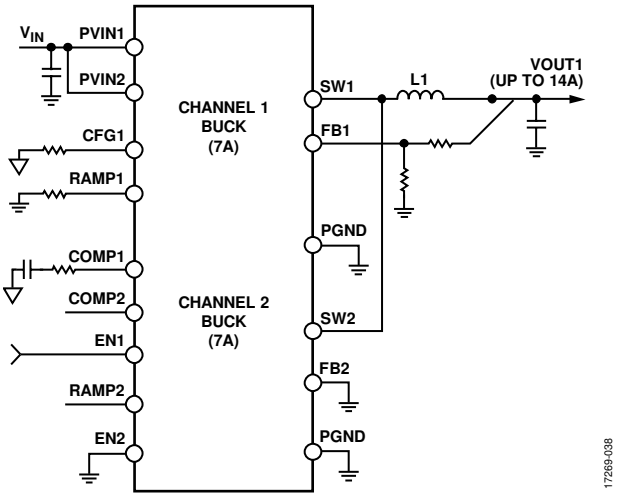


Figure 41. In-Phase Parallel Operation for Channel 1 and Channel 2

Interleaved Parallel Operation

The ADP5055 supports 2-phase interleaved parallel operation of Channel 1 and Channel 2 to provide a single output with up to 14 A of current. In this mode, two channels operate in 180° out-of-phase operation and rely on an individual control loop to achieve current balance between the two channels. The interleaved parallel operation mode uses two inductors with the advantages of ripple current cancellation and higher equivalent switching frequency. To configure a 2-phase interleaved parallel operation, do the following (see Figure 42):

- Use the CFG1 pin to select interleaved parallel operation as specified in in Table 11.
- Use the COMP1 pin as the compensation network.
- Use the same RAMP1 and RAMP2 resistors.
- Use the FB1 pin to set the output voltage.
- Use the EN1 pin to enable the channel.
- Connect the FB2 pin to ground (FB2 is ignored).
- Leave the COMP2 pin open (COMP2 is ignored).
- Connect the EN2 pin to ground (EN2 is ignored).

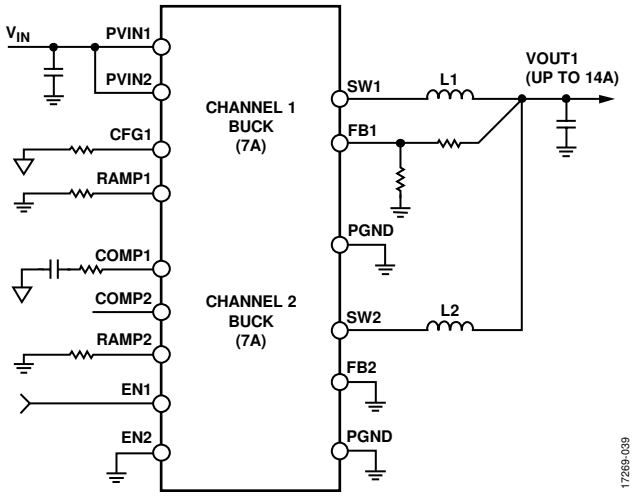


Figure 42. Interleaved Parallel Operation for Channel 1 and Channel 2

The current balance between the two phases can be achieved by careful design of the symmetrical PCB layout. Figure 43 and Figure 44 show the typical steady state waveform and current balance performance of the interleave parallel output configuration.

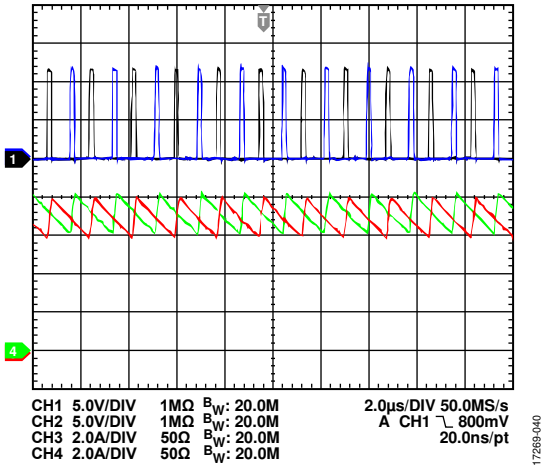


Figure 43. Steady State Waveform in Interleaved Parallel Output Configuration, V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 600 kHz, FPWM Mode, Channel 1 = SW1, Channel 2 = SW2, Channel 3 = Inductor Current of L1 (I_{L1}), Channel 4 = Inductor Current of L2 (I_{L2})

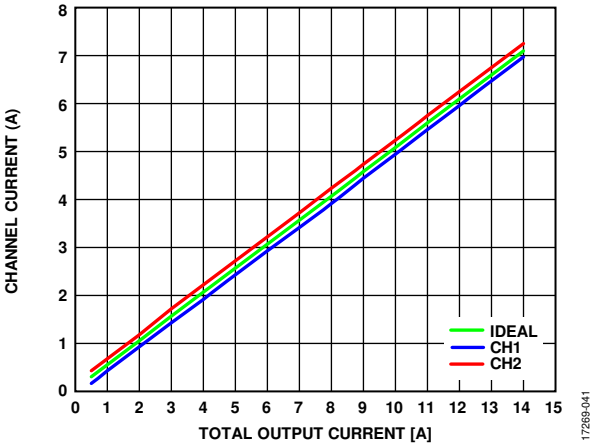


Figure 44. Current Balance in Interleaved Parallel Output Configuration, V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 600 kHz, FPWM Mode

FAST TRANSIENT MODE

The ADP5055 includes the fast transient response for the large load step conditions. The ADP5055 feedback pin (FBx) senses the output voltage to determine if a load step has occurred. When the output voltage falls below the specific threshold, the internal loop gain gradually increases to improve the load transient response speed. The fast transient threshold is programmable at different levels by the FTx_TH bit in Register 0xDF via the PMBus interface.

The CFG2 pin must be programmable to turn on the fast transient mode.

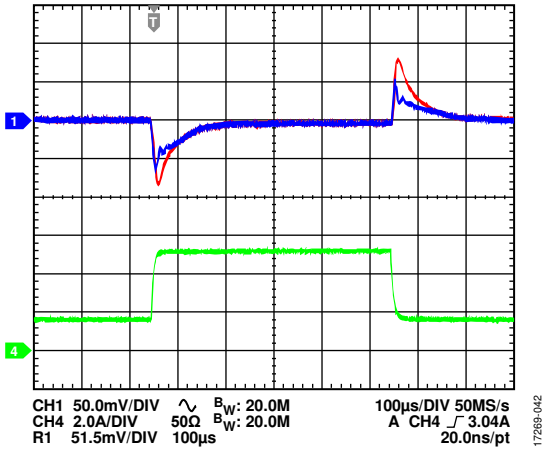


Figure 45. Enable or Disable Fast Transient Mode Load Transient Comparison, V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 600 kHz, FPWM Mode, Channel 1 = V_{OUT} with Fast Transient Mode Enable, Channel 3 = V_{OUT} with Fast Transient Mode Enable, Channel 4 = I_{OUT}

STARTUP WITH PRECHARGED OUTPUT

The buck regulators in the ADP5055 include a precharged start-up feature to protect the low-side FETs from damage during startup. If the output voltage is precharged before the regulator is turned on, the regulator prevents reverse inductor current, which discharges the output capacitor, until the internal soft start reference voltage exceeds the precharged voltage on the feedback (FBx) pin.

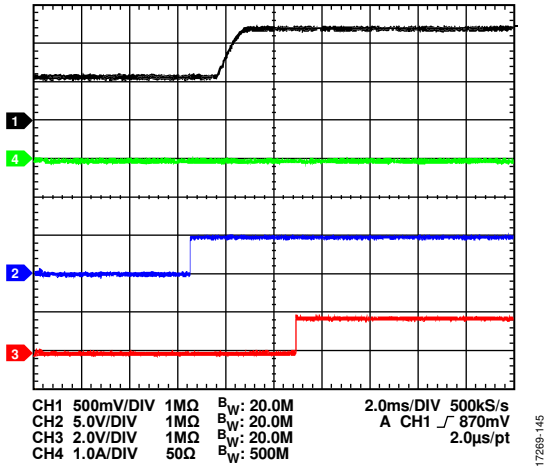


Figure 46. Channel 1 Startup with Precharged Output, V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 600 kHz, FPWM Mode, Channel 1 = V_{OUT}, Channel 2 = EN, Channel 3 = PWRGD, Channel 4 = I_{OUT}

CURRENT-LIMIT PROTECTION

The ADP5055 uses the emulated current ramp voltage for cycle-by-cycle current-limit protection to prevent current runaway. When the emulated current ramp voltage reaches the valley current-limit threshold plus the ramp voltage, the high-side MOSFET turns off, and the low-side MOSFET turns on until the next cycle. If the overcurrent counter reaches 20, the device enters hiccup mode, and the ADP5055 turns off the low-side MOSFET only after the inductor current reaches zero. During hiccup mode, the high-side MOSFET and low-side MOSFET are both turned off. The device remains in this mode for seven soft start cycles and then attempts to restart with soft start. If the current-limit fault is cleared, the device resumes normal operation. Otherwise, the device re-enters hiccup mode.

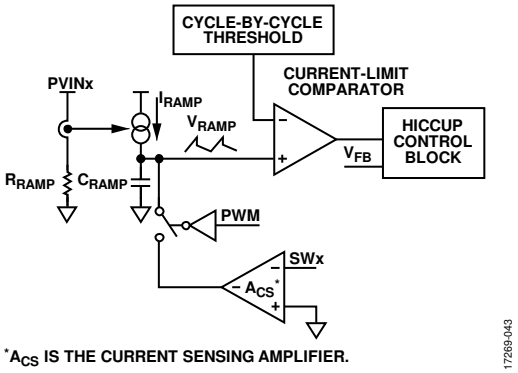


Figure 47. Current-Limit Circuitry

The buck regulators in the ADP5055 include negative current-limit protection circuitry to limit certain amounts of negative current flowing through the low-side MOSFET switch and high-side MOSFET body diode.

UVLO

Undervoltage lockout circuitry monitors both the bias supply input (VBIAS pin) and the power input voltage level (PVINx pin) of each buck regulator in the ADP5055. If the power input voltage falls below 2.30 V (typical falling threshold), the corresponding channel is turned off. After the input voltage rises above 2.60 V (typical rising threshold), the soft start period initiates, and the corresponding channel enables when the ENx pin is high.

If the bias voltage falls below 3.80 V (typical falling threshold), all channels turn off. After the bias voltage rises above 4.20 V (typical rising threshold), a soft start initiates for each enabled channel.

POWER-GOOD FUNCTION

The ADP5055 includes an open-drain, power-good output (PWRGD pin) that becomes active high when the selected buck regulators are operating normally. By default, the PWRGD pin monitors the output voltage on three channels. The specifications that control the PWRGD pin (Channel 1 to Channel 3) can be programmed by the PGx_MASK bits in Register 0xE0 via the PMBus interface.

The power-good status of each channel (PWRGDx bit) can be read back via the PMBus interface (Register 0xE1). A value of 1 for the PWRGDx bit indicates that the regulated output voltage of the buck regulator is above 95% (typical) and below 105% (typical) of the nominal output. When the regulated output voltage of the buck regulator falls below 93% (typical) or rises above 107% (typical) of the nominal output for a deglitched time greater than approximately eight switching cycles, the PWRGDx bit is set to 0.

The output of the PWRGD pin is the logical AND of the internal PWRGD signals on the individual channels. An internal PWRGD signal on an individual channel must be high for a certain validation time before the PWRGD pin goes high. If one internal PWRGD fails, the PWRGD pin goes low with no delay. The PWRGD_DLY bit in Register 0xE0 can be used to configure the validation timer as the t_{SET} timer or 0. This default validation t_{SET} timer can be increased by eight times using the CFG2 pin configuration.

POWER-UP AT HIGH TEMPERATURE

Although the maximum operating junction temperature is 150°C, the ADP5055 has a lower temperature protection limit of 125°C by which the device must be powered up. This 125°C limit protects the internal nonvolatile memory, which is read on this initial power-up. Power-up is the condition of V_{BIAS} rising above $UVLO_{VBIAS}$. If power-up is attempted above 125°C, the device does not allow operation until the temperature drops below 125°C. When this temperature is achieved and stored in the volatile memory, the device is ready for normal operation without the 125°C limit.

THERMAL SHUTDOWN

If the ADP5055 junction temperature exceeds 175°C, the thermal shutdown circuit turns off the IC except for the internal linear regulators. The ADP5055 turns off the low-side MOSFET only after the inductor current reaches zero. Extreme junction temperatures can be the result of high current operation, poor circuit board design, or high ambient temperature. A 15°C hysteresis is included so that the ADP5055 does not return to operation after thermal shutdown until the on-chip temperature falls below 160°C. When the device exits thermal shutdown, a soft start initiates for each enabled channel.

PMBus INTERFACE

The ADP5055 includes a PMBus-compatible serial interface for control of the power management blocks and for reading back of the status of the system (see Figure 48). The PMBus interface operates at clock frequencies of up to 400 kHz.

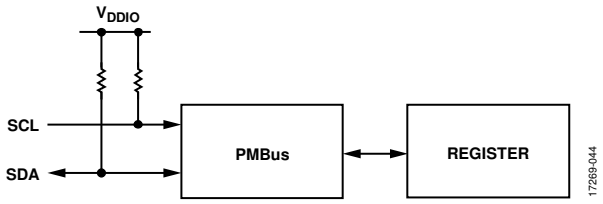


Figure 48. PMBus Interface Block Diagram

The ADP5055 does not respond to general calls. The ADP5055 accepts multiple masters, but if the device is in read mode, access is limited to one master until the data transmission is completed.

The PMBus serial interface can access the internal registers of the ADP5055. For complete information about the ADP5055 registers, see the Register Map section.

SDA AND SCL PINS

The ADP5055 has two dedicated PMBus interface pins, SDA and SCL. SDA is an open-drain line for receiving and transmitting data, and SCL is an input line for receiving the clock signal.

Serial data is transferred on the rising edge of SCL. The read data is generated at the SDA pin in read mode.

PMBus ADDRESSES

The 7-bit PMBus chip addresses for the ADP5055 include the following:

- 0x70 (1110000 in binary)
- 0x71 (1110001 in binary)
- 0x72 (1110010 in binary)
- 0x73 (1110011 in binary)

A different PMBus address can be configured using the CFG2 pin. The CFG2 pin allows the use of two ADP5055 devices on the same PMBus communication bus. Figure 49 shows two ADP5055 devices configured with different PMBus addresses using the CFG2 pin.

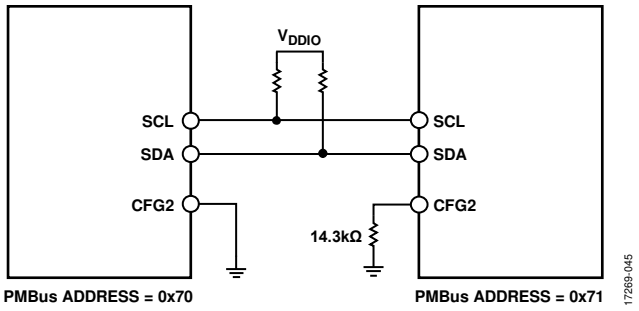


Figure 49. Two ADP5055 Devices Configured with Different PMBus Addresses

PMBus INTERFACE TIMING DIAGRAMS

Figure 50 shows the timing diagram for the PMBus write operation. Figure 51 shows the timing diagram for the PMBus read operation. The subaddress is used to select one of the user registers in the ADP5055. The ADP5055 sends data to and from the register specified by the subaddress.

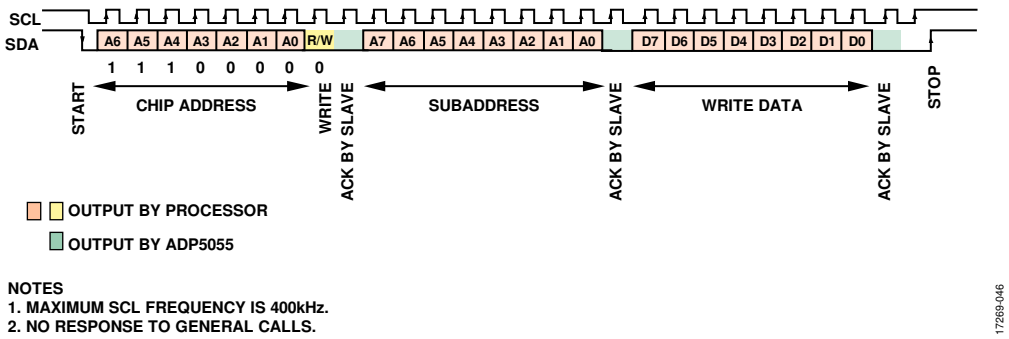


Figure 50. PMBus Write to Register

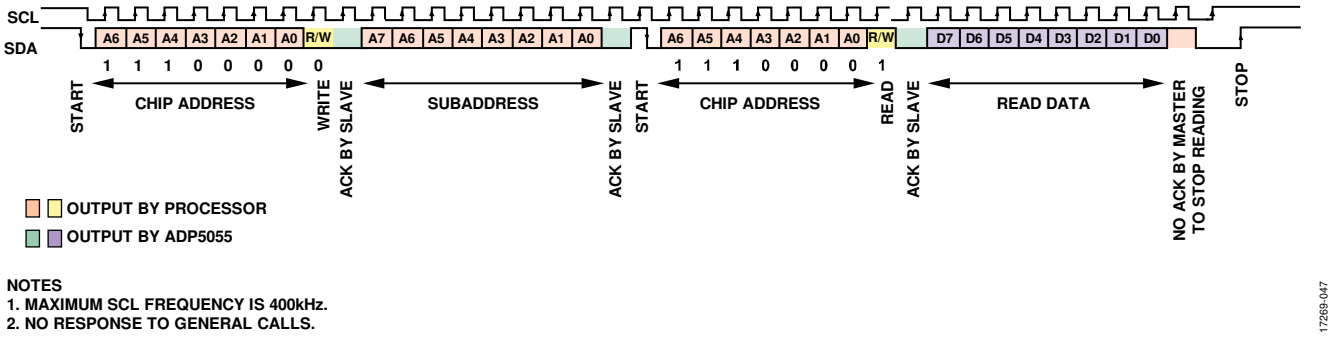


Figure 51. PMBus Read from Register

APPLICATIONS INFORMATION

PROGRAMMING THE ADJUSTABLE OUTPUT VOLTAGE

The V_{OUT} of the ADP5055 is externally set by a resistive voltage divider from the V_{OUT} to the FBx pin. To limit the degradation of the V_{OUT} accuracy due to feedback bias current, ensure that the bottom resistor in the divider is not too large. A value of less than 50 kΩ is recommended.

The V_{OUT} setting equation is as follows:

$$V_{OUT} = V_{REF} \times (1 + (R_{TOP}/R_{BOT}))$$

where:
V_{REF} is the feedback reference voltage, 600 mV for Channel 1 to Channel 3.
R_{TOP} is the feedback resistor from V_{OUT} to FBx.
R_{BOT} is the feedback resistor from FBx to ground.

VOLTAGE CONVERSION LIMITATIONS

For a given input voltage, upper and lower limitations on the V_{OUT} exist due to the minimum on time and the minimum off time.

The minimum on time limits the minimum V_{OUT} for a given input voltage and f_{SW}. The minimum on time for Channel 1 to Channel 3 is 55 ns (maximum).

In FPWM mode, Channel 1 and Channel 2 can skip the switching pulses to maintain the output regulation when the minimum on time limit is exceeded. Careful switching of frequency selection is required to avoid this problem.

To calculate the minimum V_{OUT} in CCM for a given input voltage and f_{SW}, use the following equation:

$$V_{OUT\_MIN} = V_{IN} \times t_{MIN\_ON} \times f_{SW} - (R_{DSON\_HS} - R_{DSON\_LS}) \times I_{OUT\_MIN} \times t_{MIN\_ON} \times f_{SW} - (R_{DSON\_LS} + R_L) \times I_{OUT\_MIN} \quad (1)$$

where:
V_{OUT_MIN} is the minimum output voltage.
t_{MIN_ON} is the minimum on time.
R_{DSON_HS} is the on resistance of the high-side MOSFET.
R_{DSON_LS} is the on resistance of the low-side MOSFET.
R_L is the resistance of the output inductor.
I_{OUT_MIN} is the minimum output current.

The maximum V_{OUT} for a given input voltage and f_{SW} is limited by the minimum off time and the maximum duty cycle.

To calculate the maximum V_{OUT} for a given input voltage and f_{SW}, use the following equation:

$$V_{OUT\_MAX} = V_{IN} \times (1 - t_{MIN\_OFF} \times f_{SW}) - (R_{DSON\_HS} - R_{DSON\_LS}) \times I_{OUT\_MAX} \times (1 - t_{MIN\_OFF} \times f_{SW}) - (R_{DSON\_LS} + R_L) \times I_{OUT\_MAX} \quad (2)$$

where:
V_{OUT_MAX} is the maximum output voltage.
t_{MIN_OFF} is the minimum off time.
I_{OUT_MAX} is the maximum output current.

As shown in Equation 1 and Equation 2, reducing f_{SW} eases the minimum on time and off time limitations.

CURRENT-LIMIT SETTING

The ADP5055 has two selectable current-limit thresholds for Channel 1, Channel 2, and Channel 3. Ensure that the selected current-limit value is larger than the peak current of the inductor (I_{PEAK}) for the current-limit configuration for all channels.

SOFT START SETTING

To set the soft start time to a value of 2.2 ms or 17.3 ms, connect a resistor divider from the CFG2 pin to ground (see the Soft Start section and Table 10).

INDUCTOR SELECTION

The inductor value is determined by f_{SW}, the input voltage, V_{OUT}, and the inductor ripple current. Using a small inductor value yields faster transient response but degrades efficiency due to the larger inductor ripple current. Using a large inductor value yields a smaller ripple current and better efficiency but results in slower transient response. Therefore, a trade-off must be made between transient response and efficiency. As a guideline, the inductor ripple current, ΔI_L, is typically set to a value from 30% to 40% of the maximum load current. Use the following equation to calculate the inductor value:

$$L = ((V_{IN} - V_{OUT}) \times D)/(\Delta I_L \times f_{SW})$$

where:
D is the duty cycle ($D = V_{OUT}/V_{IN}$).
ΔI_L is the inductor ripple current.

The ADP5055 has internal slope compensation in the current loop to prevent subharmonic oscillations when the duty cycle is greater than 50%.

Use the following equation to calculate the peak inductor current (I_{PEAK}):

$$I_{PEAK} = I_{OUT} + (\Delta I_L/2)$$

The saturation current of the inductor must be larger than the peak inductor current. For ferrite core inductors with a fast saturation characteristic, make sure that the saturation current rating of the inductor is higher than the current-limit threshold of the buck regulator to prevent the inductor from becoming saturated.

Calculate the rms current (I_{RMS}) of the inductor by using the following equation:

$$I_{RMS} = \sqrt{I_{OUT}^2 + \frac{\Delta I_L^2}{12}}$$

Shielded ferrite core materials are recommended for low core loss and low electromagnetic interference (EMI). Table 12 lists recommended inductors.

OUTPUT CAPACITOR SELECTION

The selected output capacitor affects both the output voltage ripple and the loop dynamics of the regulator. For example, during load step transients on the output, when the load is suddenly increased, the output capacitor supplies the load until the control loop can ramp up the inductor current, causing an undershoot of V_{OUT}.

To calculate the output capacitance required to meet the undershoot (voltage droop) requirement (C_{OUT_UV}), use the following equation:

$$C_{OUT\_UV} = \frac{K_{UV} \times \Delta I_{STEP}^2 \times L}{2 \times (V_{IN} - V_{OUT}) \times \Delta V_{OUT\_UV}}$$

where:
K_{UV} is a factor (typically set to 2).
ΔI_{STEP} is the load step.
ΔV_{OUT_UV} is the allowable undershoot on the output voltage.

Another example of the effect of the output capacitor on the loop dynamics of the regulator is when the load is suddenly removed from the output and the energy stored in the inductor rushes into the output capacitor, causing an overshoot of V_{OUT}.

To calculate the output capacitance required to meet the overshoot requirement, use the following equation:

$$C_{OUT\_OV} = \frac{K_{OV} \times \Delta I_{STEP}^2 \times L}{(V_{OUT} + \Delta V_{OUT\_OV})^2 - V_{OUT}^2}$$

where:
K_{OV} is a factor (typically set to 2).
ΔV_{OUT_OV} is the allowable overshoot on the output voltage.

The effective series resistance (ESR) of the output capacitor and the capacitance value of the output capacitor determines the output voltage ripple. Use the following equations to select a capacitor that can meet the output ripple requirements (C_{OUT_RIPPLE}):

$$C_{OUT\_RIPPLE} = \frac{\Delta I_L}{8 \times f_{SW} \times \Delta V_{OUT\_RIPPLE}}$$

where:
ΔI_L is the inductor ripple current.
ΔV_{OUT_RIPPLE} is the allowable output voltage ripple.

$$R_{ESR} = \frac{\Delta V_{OUT\_RIPPLE}}{\Delta I_L}$$

where R_{ESR} is the equivalent series resistance of the output capacitor.

Select the largest output capacitance given by C_{OUT_UV}, C_{OUT_OV}, and C_{OUT_RIPPLE} to meet both load transient and output ripple requirements.

The voltage rating of the selected output capacitor must be greater than V_{OUT}. The minimum rms current rating of the output capacitor is determined by the following equation:

$$I_{C_{OUT}\_rms} = \frac{\Delta I_L}{\sqrt{12}}$$

Table 12. Recommended Inductors

Vendor	Device No.	Inductor Value (µH)	Saturated Current, I_{SAT} (A)	I_{RMS} (A)	DC Resistance (mΩ)	Size (mm)
Coilcraft	XAL5030-601	0.6	19.8	17.7	4.11	5.28 × 5.48
	XAL5030-801	0.8	18.5	13.0	5.14	5.28 × 5.48
	XAL5030-102	1.5	14.0	11.1	8.50	5.28 × 5.48
	XAL5030-222	2.2	9.2	9.7	13.2	5.28 × 5.48
Murata	FDUE0650-H-R60M	0.6	12.0	18.0	2.24	6.7 × 7.6
	FDUE0650-H-1R0M	1.0	9.8	16.0	3.45	6.7 × 7.6
Wurth	744393440056	0.56	30.5	16.0	2.9	6.65 × 6.45
	74439344010	1.0	27.5	12.0	5.5	6.65 × 6.45
	74439344012	1.2	26.0	10.3	6.4	6.65 × 6.45
	74439344022	2.2	16.0	8.0	10.5	6.65 × 6.45

INPUT CAPACITOR SELECTION

The input decoupling capacitor attenuates high frequency noise on the input and acts as an energy reservoir. Use a ceramic capacitor and place it near to the PVINx pin. The loop composed of the input capacitor, the high-side MOSFET, and the low-side MOSFET must be kept as small as possible. The voltage rating of the input capacitor must be greater than the maximum input voltage. Make sure that the rms current rating of the input capacitor (I_{CIN_rms}) is larger than the following equation:

$$I_{C_{IN}\_rms} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

PROGRAMMING THE UVLO INPUT

The precision enabling input can program the UVLO threshold of the input voltage, as shown in Figure 34.

The high level threshold is 0.615 V typical, and the low level threshold is 0.575 V typical for precision enabling. Use the following equations to calculate the resistive voltage divider for the programmable V_{IN} turn on voltage and the V_{IN} turn off voltage:

$$V_{IN\_RISING} = (3.5\ \mu A + 0.615\ V/R_{BOT\_EN}) \times R_{TOP\_EN} + 0.615\ V$$

$$V_{IN\_FALLING} = (0.9\ \mu A + 0.575\ V/R_{BOT\_EN}) \times R_{TOP\_EN} + 0.575\ V$$

where:

V_{IN_RISING} is the V_{IN} turn on voltage.
R_{BOT_EN} is the resistor from ENx to ground.
R_{TOP_EN} is the resistor from V_{IN} to ENx.
$V_{IN\_FALLING}$ is the V_{IN} turn off voltage.

SLOPE COMPENSATION SETTING

The slope compensation is necessary in a current mode control architecture to prevent subharmonic oscillation and to maintain a stable output. The ADP5055 uses the emulated current mode, and the slope compensation is implemented by connecting a resistor (R_{RAMPx}) from the RAMPx pin to ground.

Theoretically, an extra slope of $V_{OUT}/(2 \times L)$ is enough to stabilize the system. To guarantee that any noise is decimated in one cycle and the system is stable from subharmonic oscillation, the ADP5055 uses an extra slope of V_{OUT}/L.

Calculate the R_{RAMPx} value by using the following equations:

$$R_{RAMP1}\ (k\Omega) = L1\ (\mu H) \times 500$$

$$R_{RAMP2}\ (k\Omega) = L2\ (\mu H) \times 500$$

$$R_{RAMP3}\ (k\Omega) = L3\ (\mu H) \times 226$$

where Lx is the inductor value in each channel.

COMPENSATION COMPONENTS DESIGN

For the peak current mode control architecture, the power stage can be simplified as a voltage controlled current source that supplies current to the output capacitor and load resistor. The simplified loop is composed of one domain pole and a zero contributed by the output capacitor ESR. The control to output transfer function is shown in the following equations:

$$G_{vd}(s) = \frac{V_{OUT}(s)}{V_{COMP}(s)} = A_{VI} \times R \times \frac{\left(1 + \frac{s}{2 \times \pi \times f_z}\right)}{\left(1 + \frac{s}{2 \times \pi \times f_p}\right)}$$

where:

s is the domain in the control to output transfer function.
A_{VI} = 12.5 A/V for Channel 1 and Channel 2 and 5 A/V for Channel 3.
R is the load resistance.
f_z is the zero frequency.
f_p is the pole frequency.

$$f_z = \frac{1}{2 \times \pi \times R_{ESR} \times C_{OUT}}$$

$$f_p = \frac{1}{2 \times \pi \times (R + R_{ESR}) \times C_{OUT}}$$

where:

R_{ESR} is the equivalent series resistance of the output capacitor.
C_{OUT} is the output capacitance.

The ADP5055 uses a transconductance amplifier as the error amplifier to compensate the system. Figure 52 shows the simplified peak current mode control small signal circuit.

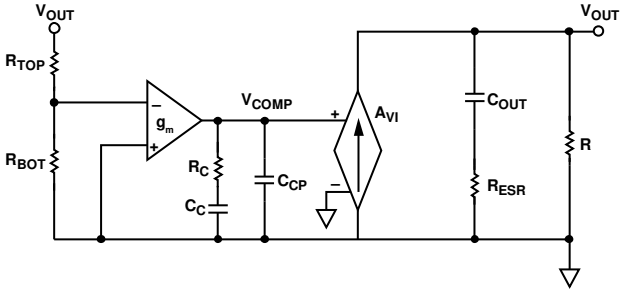


Figure 52. Simplified Peak Current Mode Control Small Signal Circuit

The compensation components, R_C and C_C, contribute a zero. R_C and the optional C_{CP} component contribute an optional pole.

The closed-loop transfer equation (s domain) follows:

$$T_V(s) = \frac{R_{BOT}}{R_{BOT} + R_{TOP}} \times \frac{-g_m}{C_C + C_{CP}} \times \frac{1 + R_C \times C_C \times s}{s \times \left(1 + \frac{R_C \times C_C \times C_{CP}}{C_C + C_{CP}} \times s\right)} \times G_{vd}(s)$$

The following guidelines detail how to select the compensation components (R_C, C_C, and C_{CP}) for ceramic output capacitor applications:

1. Determine the cross frequency (f_C). Generally, f_C is between $f_{SW}/12$ and $f_{SW}/6$.
2. Calculate R_C using the following equation:

$$R_C = \frac{2 \times \pi \times V_{OUT} \times C_{OUT} \times f_C}{0.6 \times g_m \times A_{VI}}$$

3. Place the compensation zero at the domain pole (f_P). Calculate C_C by using the following equation:

$$C_C = \frac{(R + R_{ESR}) \times C_{OUT}}{R_C}$$

4. C_{CP} is optional. It can be used to cancel the zero caused by the ESR of the output capacitor. Calculate C_{CP} by using the following equation:

$$C_{CP} = (R_{ESR} \times C_{OUT})/(R_C)$$

POWER DISSIPATION

The total power dissipation in the ADP5055 simplifies to

$$P_D = P_{BUCK1} + P_{BUCK2} + P_{BUCK3}$$

where:
P_D is the power dissipation in the package.
P_{BUCK1} is the Channel 1 power dissipation.
P_{BUCK2} is the Channel 2 power dissipation.
P_{BUCK3} is the Channel 3 power dissipation.

Buck Regulator Power Dissipation

The power dissipation (P_{LOSS}) for each buck regulator includes power switch conduction losses (P_{COND}), power switching losses (P_{SW}), and power transition losses (P_{TRAN}). Other sources of power dissipation exist, but these sources are generally less significant at the high output currents of the application thermal limit.

Use the following equation to estimate the power dissipation of the buck regulator:

$$P_{LOSS} = P_{COND} + P_{SW} + P_{TRAN}$$

Power Switch Conduction Loss (P_{COND})

Power switch conduction losses are caused by the flow of output current through both the high-side and low-side power switches. Each of these switches has internal on resistance (R_{DSON}).

To estimate the power switch conduction loss, use the following equation:

$$P_{COND} = (R_{DSON\_HS} \times D + R_{DSON\_LS} \times (1 - D)) \times I_{OUT}^2$$

where:
R_{DSON_HS} is the on resistance of the high-side MOSFET.
D is the duty cycle ($D = V_{OUT}/V_{IN}$).
R_{DSON_LS} is the on resistance of the low-side MOSFET.

Power Switching Loss (P_{SW})

Switching losses are associated with the current drawn by the driver to turn the power devices on and off at f_{SW}. Each time a power device gate turns on or off, the driver transfers a charge from the input supply to the gate, and then from the gate to ground. Use the following equation to estimate P_{SW}:

$$P_{SW} = (C_{GATE\_HS} + C_{GATE\_LS}) \times V_{IN}^2 \times f_{SW}$$

where:
C_{GATE_HS} is the gate capacitance of the high-side MOSFET.
C_{GATE_LS} is the gate capacitance of the low-side MOSFET.

Power Transition Loss (P_{TRAN})

Transition losses occur because the high-side MOSFET cannot turn on or off instantaneously. During a switch node transition, the MOSFET provides all the inductor current. The source to drain voltage of the MOSFET is half the input voltage, resulting in power loss. Transition losses increase with both load and input voltage and occur twice for each switching cycle. Use the following equation to estimate the transition loss:

$$P_{TRAN} = 0.5 \times V_{IN} \times I_{OUT} \times (t_R + t_F) \times f_{SW}$$

where:
t_R is the rise time of the switch node.
t_F is the fall time of the switch node.

Thermal Shutdown

The buck regulator stores the value of the inductor current during the on and off time of the internal MOSFETs. Therefore, there is a certain power loss dissipated inside the ADP5055, especially if all three channels run at high current. If the junction temperature exceeds 175°C, the regulator enters thermal shutdown and recovers when the junction temperature falls below 160°C.

JUNCTION TEMPERATURE

The junction temperature of the die is the sum of the ambient temperature of the environment and the temperature rise of the package due to power dissipation, as shown in the following equation:

$$T_J = T_A + T_R$$

where:
T_J is the junction temperature.
T_A is the ambient temperature.
T_R is the rise in temperature of the package due to power dissipation.

The rise in temperature of the package is directly proportional to the power dissipation in the package. The proportionality constant for this relationship is the thermal resistance from the junction of the die to the ambient temperature, as shown in the following equation:

$$T_R = \theta_{JA} \times P_D$$

where:
θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature of the package (see Table 5).

An important factor to consider is that the thermal resistance value is based on a 4-layer, 4 inch × 3 inch PCB with 2.5 oz. of copper, as specified in the JEDEC standard, whereas real-world applications may use PCBs with different dimensions and a different number of layers.

It is important to maximize the amount of copper used to remove heat from the device. Copper exposed to air dissipates heat better than copper used in the inner layers. Connect the exposed pad to the ground plane with several vias.

TYPICAL APPLICATION CIRCUITS

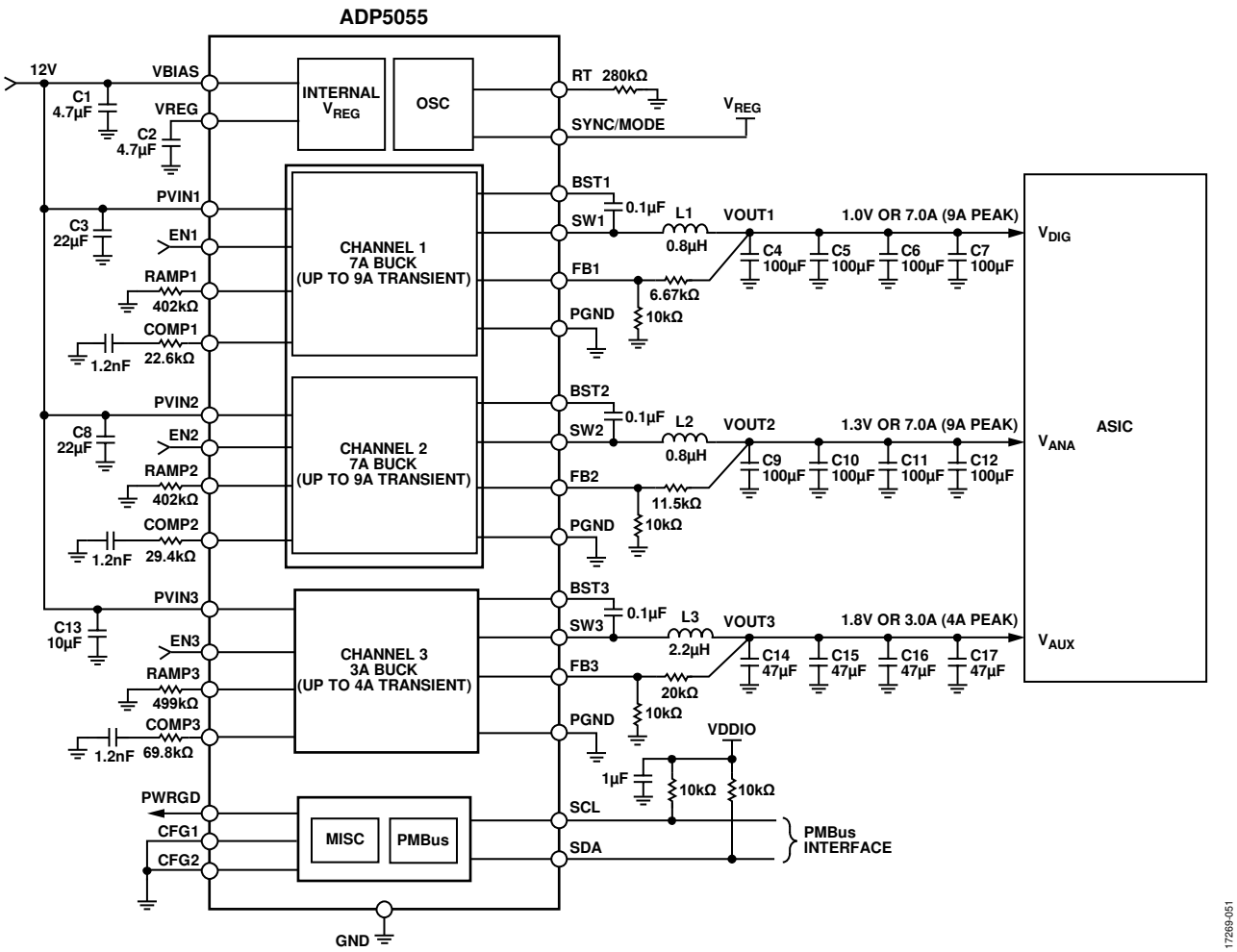


Figure 53. Typical Application, 12 V Input, f_{SW} = 600 kHz, VOUT1 = 1.0 V, VOUT2 = 1.3 V, VOUT3 = 1.8 V

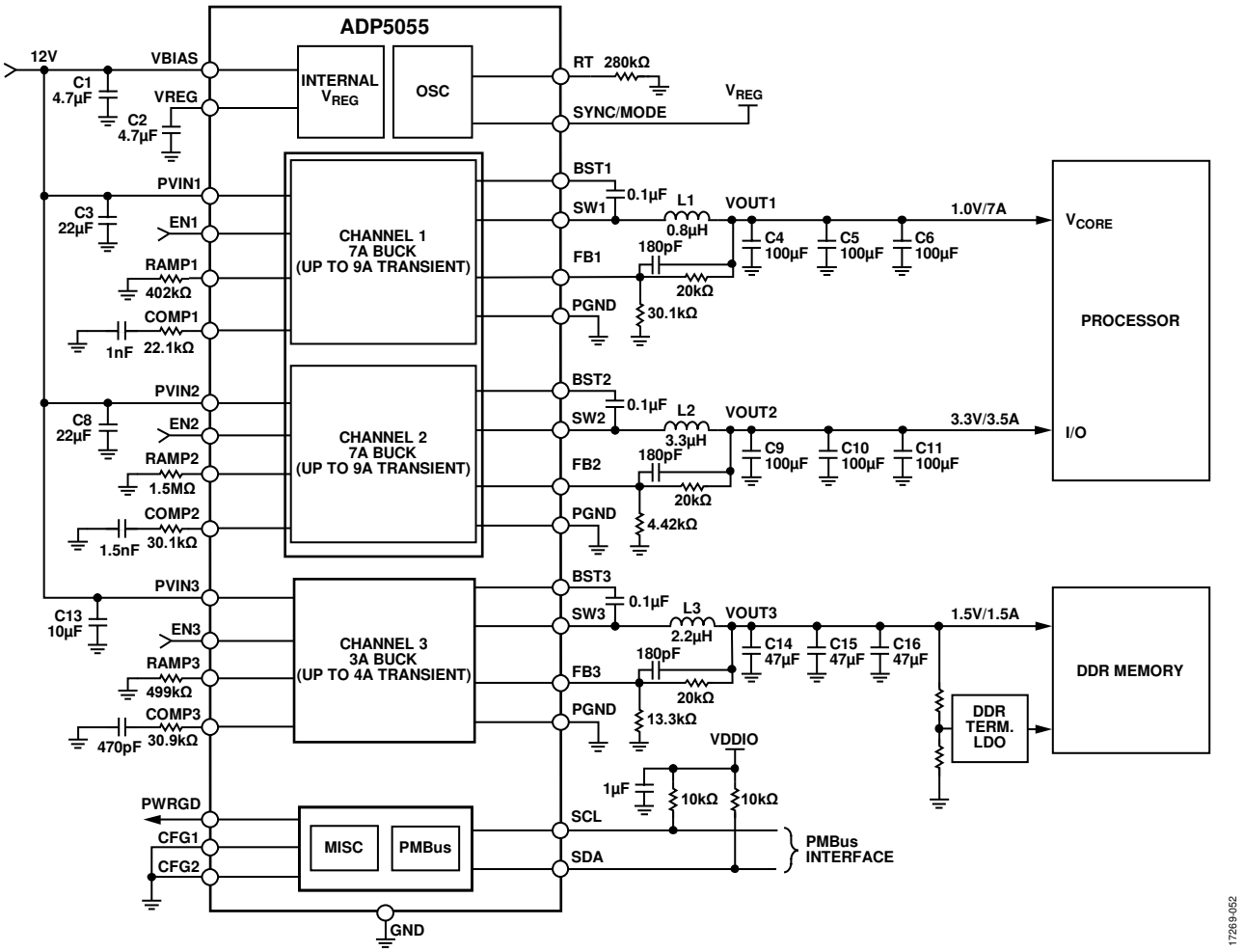


Figure 54. Typical Dynamic Voltage Scaling Application, 12 V Input, f_{SW} = 600 kHz, VOUT1 = 1.0 V to 1.1 V DVS (2.5 mV per Step), VOUT2 = 3.3 V, VOUT3 = 1.5 V

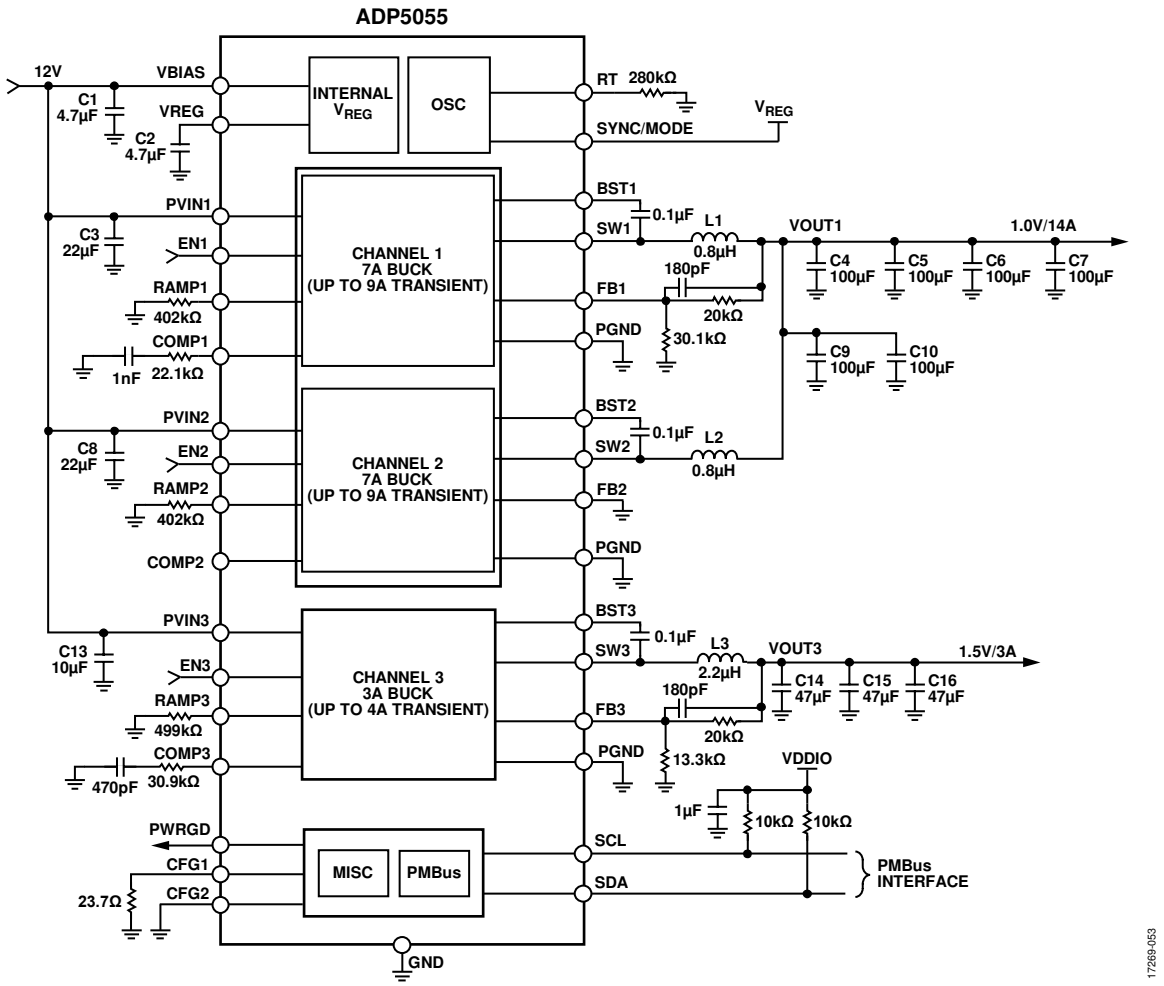


Figure 55. Typical Channel 1 and Channel 2 Interleaved Parallel Application, 12 V Input, f_{SW} = 600 kHz, VOUT1 = 1.0 V, VOUT3 = 1.5 V

DESIGN EXAMPLE

This section provides an example of the step by step design procedures and the external components required for Channel 1. Table 13 lists the design requirements for this example.

Table 13. Example Design Requirements for Channel 1

Parameter	Specification
Input Voltage	V_{PVIN1} = 12 V ± 5%
Output Voltage	VOUT1 = 1.2 V
Output Current	I_{OUT1} = 7 A
Output Ripple	ΔV_{OUT1_RIPPLE} = 12 mV in CCM mode
Load Transient	±5% at 25% to 75% load transient, 1 A/µs

Although this example shows step by step design procedures for Channel 1, the procedures apply to all other buck regulator channels (Channel 1 to Channel 3).

SETTING THE SWITCHING FREQUENCY

The first step is to determine the switching frequency (f_{SW}) for the ADP5055 design. In general, higher f_{SW} produce a smaller solution size due to the lower component values required, whereas lower f_{SW} result in higher conversion efficiency due to lower switching losses.

The f_{SW} of the ADP5055 can be set to a value from 250 kHz to 2500 kHz by connecting a resistor from the RT pin to ground. The selected resistor allows the user to make decisions based on the trade-off between efficiency and solution size.

However, the highest supported f_{SW} must be assessed by checking the voltage conversion limitations enforced by the minimum on time and the minimum off time (see the Voltage Conversion Limitations section).

In this design example, a f_{SW} of 600 kHz is used to achieve a good combination of small solution size and high conversion efficiency. To set f_{SW} to 600 kHz, use the following equation to calculate the resistor value, R_T:

$$f_{SW} = 168{,}000/R_T$$

$$R_T = 280\ \text{k}\Omega$$

Therefore, select 280 kΩ as the standard resistor, R_T.

SETTING THE OUTPUT VOLTAGE

Select a 10 kΩ R_{BOT} and then calculate the top feedback resistor by using the following equation:

$$R_{BOT} = R_{TOP} \times (V_{REF}/(V_{OUT} - V_{REF}))$$

where:
V_{REF} = 600 mV for Channel 1.

To set V_{OUT} to 1.2 V, choose the following resistor values as follows:

- R_{TOP} = 10 kΩ
- R_{BOT} = 10 kΩ

SETTING THE CONFIGUATIONS (CFG1 AND CFG2)

The CFG1 pin can program the load output capability and parallel operation for all channels. For this example, choose R_{CFG1} = 0 Ω (see Table 11).

The CFG2 pin can program the t_{SET} timer (2.6 ms or 20.8 ms), fast transient functionality, and the PMBus address for the ADP5055. For this example, choose R_{CFG2} = 0 Ω (see Table 10).

SELECTING THE INDUCTOR

The peak-to-peak inductor ripple current (ΔI_L) is set to 35% of the maximum output current. Use the following equation to estimate the value of the inductor:

$$L = ((V_{IN} - V_{OUT}) \times D)/(\Delta I_L \times f_{SW})$$

where:
V_{IN} = 12 V.
V_{OUT} = 1.2 V.
D is the duty cycle ($D = V_{OUT}/V_{IN}$ = 0.1).
ΔI_L = 35% × 7 A = 2.45 A.
f_{SW} = 600 kHz.

The resulting value for L is 0.73 µH. The closest standard inductor value is 0.8 µH. Therefore, ΔI_L is 2.25 A.

Calculate the peak inductor current by using the following equation:

$$I_{PEAK} = I_{OUT} + (\Delta I_L/2)$$

The calculated peak current for the inductor is 8.125 A.

Use the following equation to calculate the rms current of the inductor:

$$I_{RMS} = \sqrt{I_{OUT}^2 + \frac{\Delta I_L^2}{12}}$$

The rms current of the inductor is approximately 7.03 A.

Therefore, an inductor with a minimum rms current rating of 7.03 A and a minimum saturation current rating of 8.125 A is required. However, to prevent the inductor from reaching the saturation point in current-limit conditions, it is recommended that the inductor saturation current be higher than the maximum peak current limit, typically 11.65 A, for reliable operation.

Based on these requirements and recommendations, the XAL5030-801, with a dc resistance of 5.14 mΩ, was selected for this design.

SELECTING THE OUTPUT CAPACITOR

The output capacitor must meet the output voltage ripple and load transient requirements. To meet the output voltage ripple requirement, use the following equations to calculate the ESR and capacitance:

$$C_{OUT\_RIPPLE} = \frac{\Delta I_L}{8 \times f_{SW} \times \Delta V_{OUT\_RIPPLE}}$$

$$R_{ESR} = \frac{\Delta V_{OUT\_RIPPLE}}{\Delta I_L}$$

The calculated capacitance, C_{OUT_RIPPLE}, is 39 µF, and the calculated R_{ESR} is 5.3 mΩ.

To meet the ±5% overshoot and undershoot requirements, use the following equations to calculate the capacitance:

$$C_{OUT\_UV} = \frac{K_{UV} \times \Delta I_{STEP}{}^2 \times L}{2 \times \left(V_{IN} - V_{OUT}\right) \times \Delta V_{OUT\_UV}}$$

$$C_{OUT\_OV} = \frac{K_{OV} \times \Delta I_{STEP}{}^2 \times L}{\left(V_{OUT} + \Delta V_{OUT\_OV}\right)^2 - V_{OUT}{}^2}$$

For estimation purposes, use $K_{OV} = K_{UV} = 2$. Therefore, $C_{OUT\_OV} = 133$ µF and $C_{OUT\_UV} = 15.1$ µF.

The ESR of the output capacitor must be less than 11 mΩ, and the output capacitance must be greater than 133 µF. It is recommended that three ceramic capacitors be used (47 µF, X5R, and 6.3 V), such as Murata GRM21BR60J476ME15 with an ESR of 2 mΩ.

DESIGNING THE COMPENSATION NETWORK

For better load transient and stability performance, set f_C to $f_{SW}/10$. In this example, f_{SW} is set to 600 kHz, therefore, f_C is set to 60 kHz.

For the 1.2 V output rail, the 47 µF ceramic output capacitor has a derated value of 40 µF.

Choose $R_C = 24.9$ kΩ and $C_C = 1$ nF for the standard components. Note that, C_{CP} is optional.

Figure 56 shows the Bode plot for the 1.2 V output rail. The cross frequency is 58 kHz, and the phase margin is 63°.

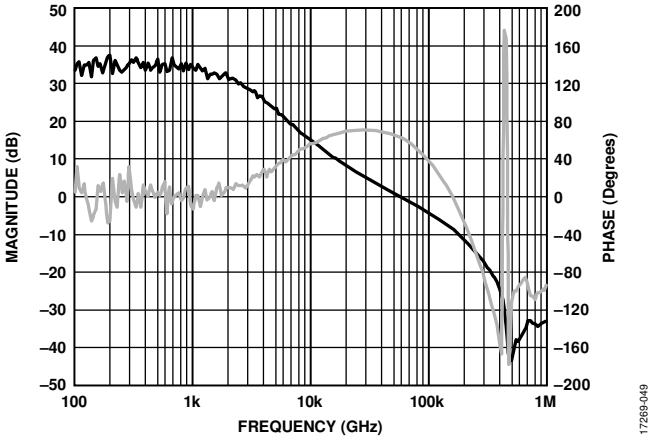


Figure 56. Bode Plot for 1.2 V Output

SELECTING THE INPUT CAPACITOR

For the input capacitor, select a ceramic capacitor with a minimum value of 10 µF. Place the input capacitor near to the PVIN1 pin. In this example, one 10 µF, X5R, 25 V ceramic capacitor is recommended.

PCB LAYOUT RECOMMENDATIONS

Optimal PCB layout is essential to obtain the best performance from the ADP5055 (see Figure 57). Poor layout can affect the regulation and stability of the device, as well as the EMI and electromagnetic compatibility (EMC) performance. Refer to the following guidelines for an optimal PCB layout:

- Place the input capacitor, inductor, output capacitor, and bootstrap capacitor close to the IC.
- Use short, thick traces to connect the input capacitors to the PVINx pins and use a dedicated power ground to connect the input and output capacitor grounds to minimize the connection length.
- Use several high current vias, if required, to connect PVINx, PGND, and SWx to other power planes.
- Use short, thick traces to connect the inductors to the SWx pins and the output capacitors.
- Ensure that the high current loop traces are as short and wide as possible.
- Maximize the amount of ground metal for the exposed pad and use as many vias as possible on the component side to improve thermal dissipation.
- Use a ground plane with several vias connecting to the component side ground to further reduce noise interference on sensitive circuit nodes.
- Place the decoupling capacitors close to the VREG pin.
- Place the frequency setting resistor close to the RT pin.
- Place the feedback resistor divider close to the FBx pin. In addition, keep the FBx traces away from the high current traces and the switch node to avoid noise pickup.
- Use size 0402 or 0603 resistors and capacitors to achieve the smallest possible footprint solution on boards where space is limited.

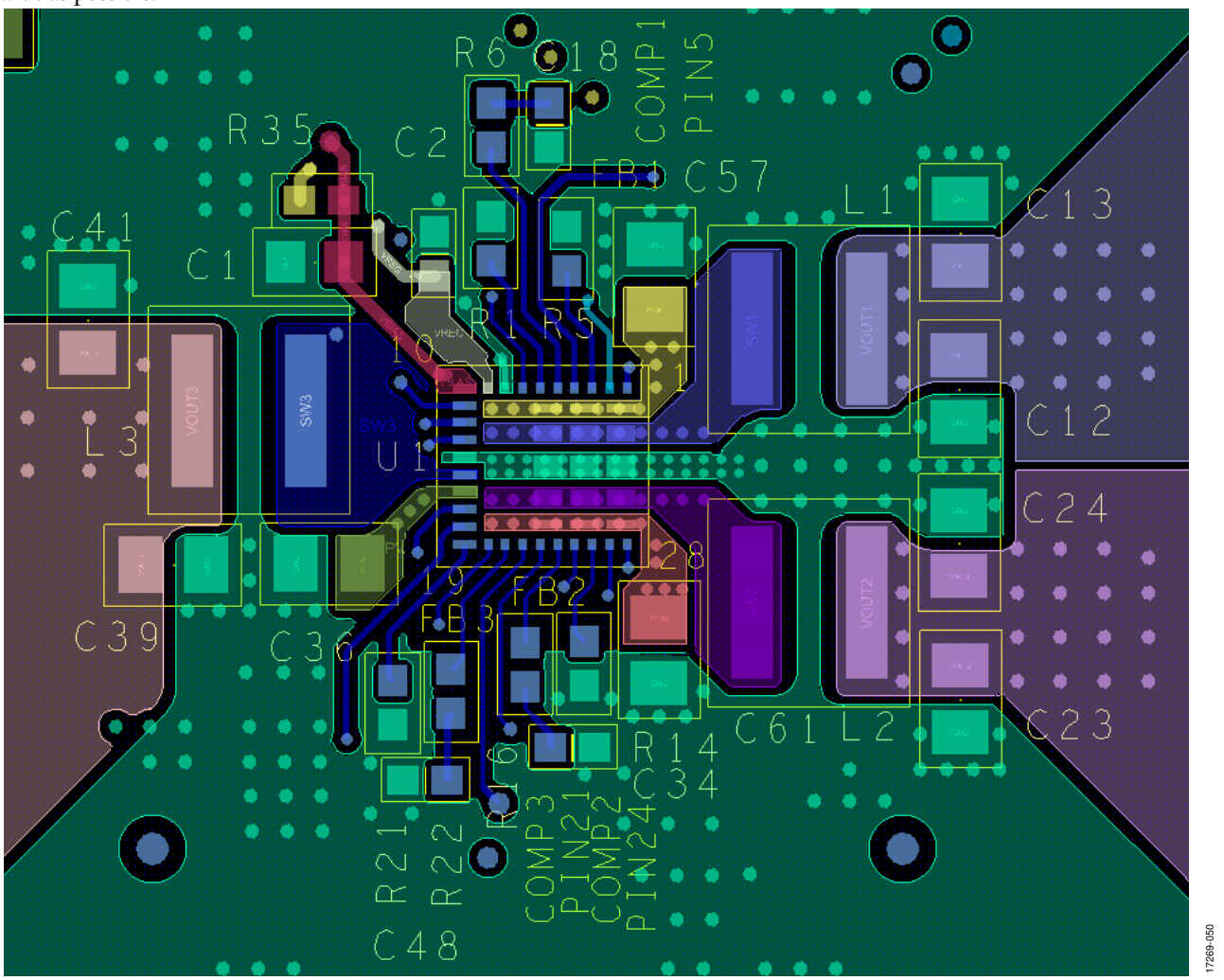


Figure 57. Typical PCB Layout for the ADP5055

REGISTER MAP

Table 14. Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x19	CAPABILITY	[7:0]	PEC	MAX_BUS_SPEED		SMBALRT	RESERVED				0xA0	R
0x7E	STATUS_CML	[7:0]	CMD_ERR	DATA_ERR	PEC_ERR	CRC_ERR	RESERVED		COMM_ERR	RESERVED	0x00	R/W
0xD0	MODEL_ID	[7:0]	MODEL								0x40	R
0xD1	CTRL123	[7:0]	RESERVED					CH3_ON	CH2_ON	CH1_ON	0x00	R/W
0xD2	VID_GO	[7:0]	RESERVED					VID3_GO	VID2_GO	VID1_GO	0x00	W
0xD3	CTRL_MODE1	[7:0]	RESERVED			DVS_AUTO	RESERVED		EN_MODE		0x00	R/W
0xD4	CTRL_MODE2	[7:0]	OCP_BLANKING	PSM3_ON	PSM2_ON	PSM1_ON	RESERVED	DSCG3_ON	DSCG2_ON	DSCG1_ON	0x07	R/W
0xD5	DLY1	[7:0]	RESERVED	DIS_DLY1			RESERVED	EN_DLY1			0x00	R/W
0xD6	DLY2	[7:0]	RESERVED	DIS_DLY2			RESERVED	EN_DLY2			0x00	R/W
0xD7	DLY3	[7:0]	RESERVED	DIS_DLY3			RESERVED	EN_DLY3			0x00	R/W
0xD8	VID1	[7:0]	VID1								0x80	R/W
0xD9	VID2	[7:0]	VID2								0x80	R/W
0xDA	VID3	[7:0]	VID3								0x80	R/W
0xDB	DVS_CFG	[7:0]	RESERVED		DVS_INTVAL3		DVS_INTVAL2		DVS_INTVAL1		0x00	R/W
0xDC	DVS_LIM1	[7:0]	VID1_HIGH				VID1_LOW				0x00	R/W
0xDD	DVS_LIM2	[7:0]	VID2_HIGH				VID2_LOW				0x00	R/W
0xDE	DVS_LIM3	[7:0]	VID3_HIGH				VID3_LOW				0x00	R/W
0xDF	FT_CFG	[7:0]	RESERVED		FT3_TH		FT2_TH		FT1_TH		0x3F	R/W
0xE0	PG_CFG	[7:0]	RESERVED			PWRGD_DLY	RESERVED	PG3_MASK	PG2_MASK	PG1_MASK	0x10	R/W
0xE1	PG_READ	[7:0]	RESERVED					PWRGD3	PWRGD2	PWRGD1	0x00	R
0xE2	STATUS_LCH	[7:0]	INT_LCH	OCP3_LCH	OCP2_LCH	OCP1_LCH	TSD_LCH	PG3_LCH	PG2_LCH	PG1_LCH	0x00	R/W

REGISTER DETAILS

Address: 0x19, Reset: 0xA0, Name: CAPABILITY

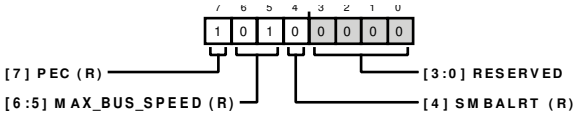


Table 15. Bit Descriptions for CAPABILITY

Bits	Bit Name	Settings	Description	Reset	Access
7	PEC		Checks the packet error capability of device.	0x1	R
		1	Supported.		
[6:5]	MAX_BUS_SPEED		Checks the PMBus speed capability of the device.	0x1	R
		0	400 kHz.		
		1	400 kHz.		
4	SMBALRT		Checks support for the SMBALRT and the SMBus Alert Response Address Protocol.	0x0	R
		0	Not supported.		
[3:0]	RESERVED		Reserved.	0x0	R

Address: 0x7E, Reset: 0x00, Name: STATUS_CML

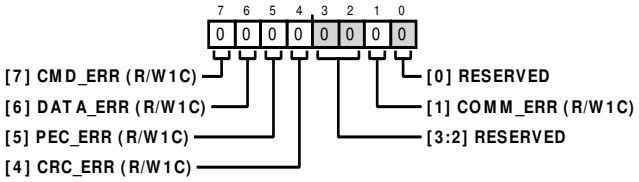


Table 16. Bit Descriptions for STATUS_CML

Bits	Bit Name	Settings	Description	Reset	Access[1]
7	CMD_ERR		Invalid or unsupported command received.	0x0	R/W1C
6	DATA_ERR		Invalid or unsupported data received.	0x0	R/W1C
5	PEC_ERR		Packet error check failed.	0x0	R/W1C
4	CRC_ERR		Memory fault detected, for example, CRC error.	0x0	R/W1C
[3:2]	RESERVED		Reserved.	0x0	R
1	COMM_ERR		Other communication fault not listed in this table.	0x0	R/W1C
0	RESERVED		Reserved.	0x0	R

[1] R/W1C means read or write 1 to clear.

Address: 0xD0, Reset: 0x40, Name: MODEL_ID

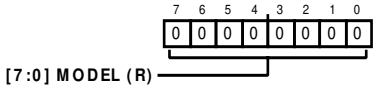


Table 17. Bit Descriptions for MODEL_ID

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	MODEL		Returns specific product models.	0x40	R

Address: 0xD1, Reset: 0x00, Name: CTRL123

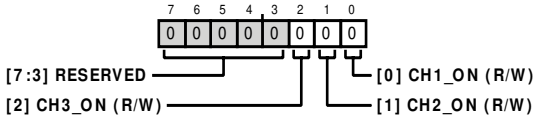


Table 18. Bit Descriptions for CTRL123

Bits	Bit Name	Settings	Description	Reset	Access
[7:3]	RESERVED		Reserved.	0x0	R
2	CH3_ON		Enables or Disables for Channel 3.	0x0	R/W
		0	Disables the channel.		
		1	Enables the channel.		
1	CH2_ON		Enables or Disables for Channel 2.	0x0	R/W
		0	Disables the channel.		
		1	Enables the channel.		
0	CH1_ON		Enables or Disables for Channel 1.	0x0	R/W
		0	Disables the channel.		
		1	Enables the channel.		

Address: 0xD2, Reset: 0x00, Name: VID_GO

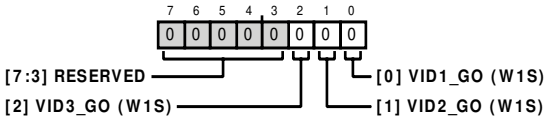


Table 19. Bit Descriptions for VID_GO

Bits	Bit Name	Settings	Description	Reset	Access[1]
[7:3]	RESERVED		Reserved.	0x0	R
2	VID3_GO		If DVS_AUTO = 1, writing to this bit initiates the Channel 3 output voltage transition to the respective VID3 code. This bit self clears. If DVS_AUTO = 0, this bit has no effect, and a write to the VID3 register initiates the Channel 3 output voltage transition. DVS_AUTO can be set through Register 0xD3, Bit 4.	0x0	W1S
1	VID2_GO		If DVS_AUTO = 1, writing to this bit initiates the Channel 2 output voltage transition to the respective VID2 code. This bit self clears. If DVS_AUTO = 0, this bit has no effect, and a write to the VID2 register initiates the Channel 2 output voltage transition. DVS_AUTO can be set through Register 0xD3, Bit 4.	0x0	W1S
0	VID1_GO		If DVS_AUTO = 1, writing to this bit initiates the Channel 1 output voltage transition to the respective VID1 code. This bit self clears. If DVS_AUTO = 0, this bit has no effect, and a write to the VID1 register initiates the Channel 1 output voltage transition. DVS_AUTO can be set through Register 0xD3, Bit 4.	0x0	W1S

[1] W1S means write 1 to set.

Address: 0xD3, Reset: 0x00, Name: CTRL_MODE1

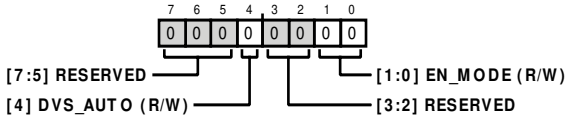


Table 20. Bit Descriptions for CTRL_MODE1

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved.	0x0	R
4	DVS_AUTO		Configures the VIDx execution mode.	0x0	R/W
		0	The output voltage transitions immediately following a write to the VIDx register. The VIDx_GO bit is ignored.		
		1	The output voltage transitions to the VIDx register only with a write of 1 to the VIDx_GO bit.		
[3:2]	RESERVED		Reserved.	0x0	R
[1:0]	EN_MODE		Configures the enabling of the individual channels by the ENx hardware pin and/or the CHx_ON software bit.	0x0	R/W
		00	The ENx pin is used to enable or disable the corresponding channel. The CHx_ON bit is ignored.		
		01	The CHx_ON bit is used to enable or disable the corresponding channel. The ENx pin is ignored.		
		10	Both the ENx pin and the CHx_ON bit are needed to enable the corresponding channel. Logical AND'ed of both signals.		
		11	Either the ENx pin or the CHx_ON bit is needed to enable the corresponding channel. Logic OR connected for both signals.		

Address: 0xD4, Reset: 0x07, Name: CTRL_MODE2

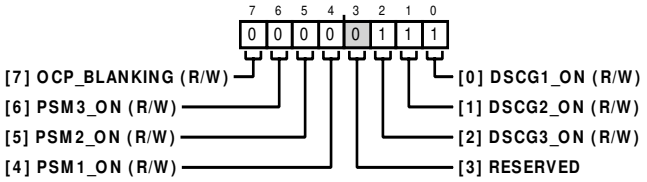


Table 21. Bit Descriptions for CTRL_MODE2

Bits	Bit Name	Settings	Description	Reset	Access
7	OCP_BLANKING		Enables or disables the overcurrent protection (OCP) blanking for all channels.	0x0	R/W
		0	Disables OCP blanking.		
		1	Enables OCP blanking.		
6	PSM3_ON		Configures the operational mode for Channel 3. This bit is ignored when the SYNC/MODE pin is low.	0x0	R/W
		0	Enables FPWM mode.		
		1	Enables automatic PWM/PSM.		
5	PSM2_ON		Configures the operational mode for Channel 2. This bit is ignored when the SYNC/MODE pin is low.	0x0	R/W
		0	Enables FPWM mode.		
		1	Enables automatic PWM/PSM.		
4	PSM1_ON		Configures the operational mode for Channel 1. This bit is ignored when the SYNC/MODE pin is low.	0x0	R/W
		0	Enables FPWM mode.		
		1	Enables automatic PWM/PSM.		
3	RESERVED		Reserved.	0x0	R

Bits	Bit Name	Settings	Description	Reset	Access
2	DSCG3_ON		Configures the output discharge functionality for Channel 3.	0x1	R/W
		0	Disables output discharge function.		
		1	Enables output discharge function.		
1	DSCG2_ON		Configures the output discharge functionality for Channel 2.	0x1	R/W
		0	Disables output discharge function.		
		1	Enables output discharge function.		
0	DSCG1_ON		Configures the output discharge functionality for Channel 1.	0x1	R/W
		0	Disables output discharge function.		
		1	Enables output discharge function.		

Address: 0xD5, Reset: 0x00, Name: DLY1

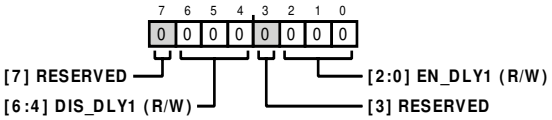


Table 22. Bit Descriptions for DLY1

Bits	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Reserved.	0x0	R
[6:4]	DIS_DLY1		Configures the disable delay of Channel 1 by the EN1 hardware pin and/or the CH1_ON software register (t_{SET} = 2.6 ms at ×1 or 20.8 ms at ×8 timer setting, which can be configured using the CFG2 pin).	0x0	R/W
		000	No delay.		
		001	2 × t_{SET}.		
		010	4 × t_{SET}.		
		011	6 × t_{SET}.		
		100	8 × t_{SET}.		
		101	10 × t_{SET}.		
		110	12 × t_{SET}.		
		111	14 × t_{SET}.		
3	RESERVED		Reserved.	0x0	R
[2:0]	EN_DLY1		Configures the enable delay of Channel 1 by the EN1 hardware pin and/or the CH1_ON software register (t_{SET} = 2.6 ms at ×1 or 20.8 ms at ×8 timer setting, which can be configured using the CFG2 pin).	0x0	R/W
		000	No delay.		
		001	1 × t_{SET}.		
		010	2 × t_{SET}.		
		011	3 × t_{SET}.		
		100	4 × t_{SET}.		
		101	5 × t_{SET}.		
		110	6 × t_{SET}.		
		111	7 × t_{SET}.		

Address: 0xD6, Reset: 0x00, Name: DLY2

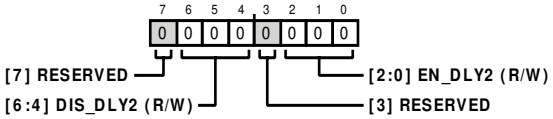


Table 23. Bit Descriptions for DLY2

Bits	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Reserved.	0x0	R
[6:4]	DIS_DLY2		Configures the disable delay of Channel 2 by the EN2 hardware pin and/or the CH2_ON software register (t_{SET} = 2.6 ms at ×1 or 20.8 ms at ×8 timer setting, which can be configured using the CFG2 pin).	0x0	R/W
		000	No delay.		
		001	2 × t_{SET}.		
		010	4 × t_{SET}.		
		011	6 × t_{SET}.		
		100	8 × t_{SET}.		
		101	10 × t_{SET}.		
		110	12 × t_{SET}.		
		111	14 × t_{SET}.		
3	RESERVED		Reserved.	0x0	R
[2:0]	EN_DLY2		Configures the enable delay of Channel 2 by the EN2 hardware pin and/or the CH2_ON software register (t_{SET} = 2.6 ms at ×1 or 20.8 ms at ×8 timer setting, which can be configured using the CFG2 pin).	0x0	R/W
		000	No delay.		
		001	1 × t_{SET}.		
		010	2 × t_{SET}.		
		011	3 × t_{SET}.		
		100	4 × t_{SET}.		
		101	5 × t_{SET}.		
		110	6 × t_{SET}.		
		111	7 × t_{SET}.		

Address: 0xD7, Reset: 0x00, Name: DLY3

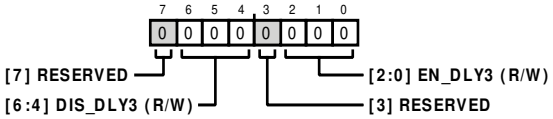


Table 24. Bit Descriptions for DLY3

Bits	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Reserved.	0x0	R
[6:4]	DIS_DLY3		Configures the disable delay of Channel 3 by the EN3 hardware pin and/or the CH3_ON software register (t_{SET} = 2.6 ms at ×1 or 20.8 ms at ×8 timer setting, which can be configured using the CFG2 pin).	0x0	R/W
		000	No delay.		
		001	2 × t_{SET}.		
		010	4 × t_{SET}.		
		011	6 × t_{SET}.		
		100	8 × t_{SET}.		
		101	10 × t_{SET}.		
		110	12 × t_{SET}.		
		111	14 × t_{SET}.		

Bits	Bit Name	Settings	Description	Reset	Access
3	RESERVED		Reserved.	0x0	R
[2:0]	EN_DLY3		Configures the enable delay of Channel 3 by the EN3 hardware pin and/or the CH3_ON software register (t_{SET} = 2.6 ms at ×1 or 20.8 ms at ×8 timer setting, which can be configured using the CFG2 pin).	0x0	R/W
		000	No delay.		
		001	1 × t_{SET}.		
		010	2 × t_{SET}.		
		011	3 × t_{SET}.		
		100	4 × t_{SET}.		
		101	5 × t_{SET}.		
		110	6 × t_{SET}.		
		111	7 × t_{SET}.		

Address: 0xD8, Reset: 0x80, Name: VID1

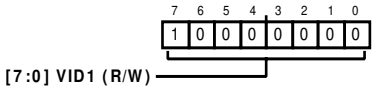


Table 25. Bit Descriptions for VID1

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	VID1		Sets V_{OUT} of Channel 1. This register is ignored and disallowed if it falls outside of the VID1_LOW to VID1_HIGH range. VOUT1 = 408 mV + (1.5 mV × code)	0x80	R/W

Address: 0xD9, Reset: 0x80, Name: VID2

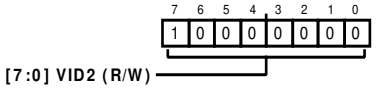


Table 26. Bit Descriptions for VID2

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	VID2		Sets V_{OUT} of Channel 2. This register is ignored and disallowed if it falls outside of the VID2_LOW to VID2_HIGH range. VOUT2 = 408 mV + (1.5 mV × code)	0x80	R/W

Address: 0xDA, Reset: 0x80, Name: VID3

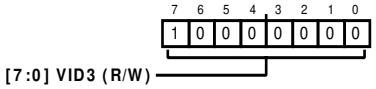


Table 27. Bit Descriptions for VID3

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	VID3		Sets V_{OUT} of Channel 3. This register is ignored and disallowed if it falls outside of the VID3_LOW to VID3_HIGH range. VOUT3 = 408 mV + (1.5 mV × code)	0x80	R/W

Address: 0xDB, Reset: 0x00, Name: DVS_CFG

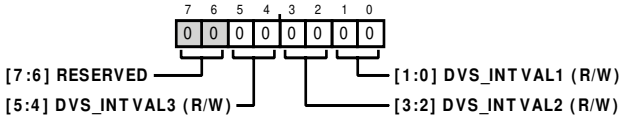


Table 28. Bit Descriptions for DVS_CFG

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	RESERVED		Reserved.	0x0	R
[5:4]	DVS_INTVAL3		Configures the DVS interval for Channel 3.	0x0	R/W
		00	125 µs, at 12 mV/ms slew rate.		
		01	62.5 µs, at 24 mV/ms slew rate.		
		10	31.2 µs, at 48 mV/ms slew rate.		
		11	15.6 µs, at 96 mV/ms slew rate.		
[3:2]	DVS_INTVAL2		Configures the DVS interval for Channel 2.	0x0	R/W
		00	125 µs, at 12 mV/ms slew rate.		
		01	62.5 µs, at 24 mV/ms slew rate.		
		10	31.2 µs, at 48 mV/ms slew rate.		
		11	15.6 µs, at 96 mV/ms slew rate.		
[1:0]	DVS_INTVAL1		Configures the DVS interval for Channel 1.	0x0	R/W
		00	125 µs, at 12 mV/ms slew rate.		
		01	62.5 µs, at 24 mV/ms slew rate.		
		10	31.2 µs, at 48 mV/ms slew rate.		
		11	15.6 µs, at 96 mV/ms slew rate.		

Address: 0xDC, Reset: 0x00, Name: DVS_LIM1

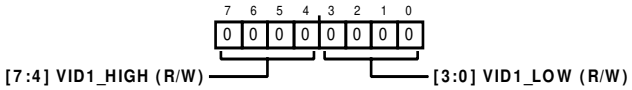


Table 29. Bit Descriptions for DVS_LIM1

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	VID1_HIGH		Configures the allowable upper side limit of VID1 range, which is relative to the default V_{REF} trimming value (V_{REF_TRIM}). If the VID1_HIGH setting is written with a value that is lower than the existing VID1 code, it is ignored. VID1_HIGH = V_{REF_TRIM} + 192 mV − (12 mV × code).	0x0	R/W
[3:0]	VID1_LOW		Configures the allowable lower side limit of VID1 range, which is relative to the default V_{REF} trimming value. If the VID1_LOW setting is written with a value that is higher than the existing VID1 code, it is ignored. VID1_LOW = V_{REF_TRIM} − 190.5 mV + (12 mV × code).	0x0	R/W

Address: 0xDD, Reset: 0x00, Name: DVS_LIM2

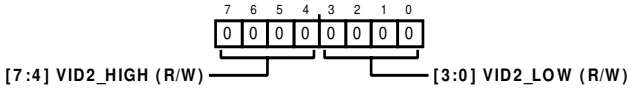


Table 30. Bit Descriptions for DVS_LIM2

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	VID2_HIGH		Configures the allowable upper side limit of VID2 range, which is relative to the default V_{REF} trimming value. If the VID2_HIGH setting is written with a value that is lower than the existing VID2 code, it is ignored. VID2_HIGH = V_{REF_TRIM} + 192 mV − (12 mV × code).	0x0	R/W
[3:0]	VID2_LOW		Configures the allowable lower side limit of VID2 range, which is relative to the default V_{REF} trimming value. If the VID2_LOW setting is written with a value that is higher than the existing VID2 code, it is ignored. VID2_LOW = V_{REF_TRIM} − 190.5 mV + (12 mV × code).	0x0	R/W

Address: 0xDE, Reset: 0x00, Name: DVS_LIM3

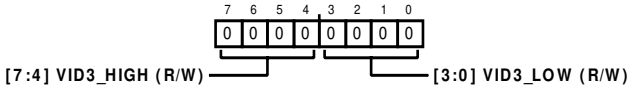


Table 31. Bit Descriptions for DVS_LIM3

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	VID3_HIGH		Configures the allowable upper side limit of VID3 range, which is relative to the default V_{REF} trimming value. If the VID3_HIGH setting is written with a value that is lower than the existing VID3 code, it is ignored. VID3_HIGH = V_{REF_TRIM} + 192 mV − (12 mV × code).	0x0	R/W
[3:0]	VID3_LOW		Configures the allowable lower side limit of VID3 range, which is relative to the default V_{REF} trimming value. If the VID3_LOW setting is written with a value that is higher than the existing VID3 code, it is ignored. VID3_LOW = V_{REF_TRIM} − 190.5 mV + (12 mV × code).	0x0	R/W

Address: 0xDF, Reset: 0x3F, Name: FT_CFG

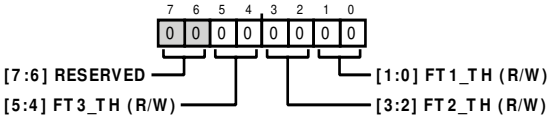


Table 32. Bit Descriptions for FT_CFG

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	RESERVED		Reserved.	0x0	R
[5:4]	FT3_TH		Configures the fast transient sensitivity for Channel 3. These settings are ignored if the fast transient functionality is disabled through the CFG2 pin.	0x3	R/W
		00	No fast transient.		
		01	1.5% window with 3× g_m, where g_m = 350 µA/V.		
		10	1.5% window with 5× g_m, where g_m = 350 µA/V.		
		11	2.5% window with 5× g_m, where g_m = 350 µA/V.		
[3:2]	FT2_TH		Configures the fast transient sensitivity for Channel 2. These settings are ignored if the fast transient functionality is disabled through the CFG2 pin.	0x3	R/W
		00	No fast transient.		
		01	1.5% window with 3× g_m, where g_m = 350 µA/V.		
		10	1.5% window with 5× g_m, where g_m = 350 µA/V.		
		11	2.5% window with 5× g_m, where g_m = 350 µA/V.		

Bits	Bit Name	Settings	Description	Reset	Access
[1:0]	FT1_TH		Configures the fast transient sensitivity for Channel 1. These settings are ignored if the fast transient functionality is disabled through the CFG2 pin.	0x3	R/W
		00	No fast transient.		
		01	1.5% window with 3× g_m, where g_m = 350 µA/V.		
		10	1.5% window with 5× g_m, where g_m = 350 µA/V.		
		11	2.5% window with 5× g_m, where g_m = 350 µA/V.		

Address: 0xE0, Reset: 0x10, Name: PG_CFG

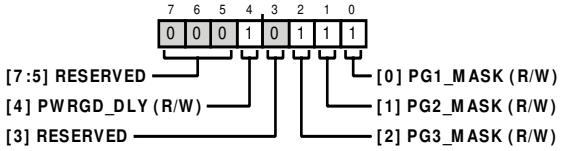


Table 33. Bit Descriptions for PG_CFG

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved.	0x0	R
4	PWRGD_DLY		Configures the delay timer of the PWRGD hardware pin (AND'ed of all internal PWRGD signals).	0x1	R/W
		0	No delay. PWRGD pin goes high immediately.		
		1	PWRGD delay timer = t_{SET} (2.6 ms at ×1 timer and 20.8 ms at ×8 timer).		
3	RESERVED		Reserved.	0x0	R
2	PG3_MASK		Masks or unmasks the Channel 3 PWRGD signal to the external PWRGD hardware pin.	0x0	R/W
		0	Outputs the PWRGD3 signal to the external PWRGD pin.		
		1	Masks the PWRGD3 signal to the external PWRGD pin.		
1	PG2_MASK		Masks or unmasks the Channel 2 PWRGD signal to the external PWRGD hardware pin.	0x0	R/W
		0	Outputs the PWRGD2 signal to the external PWRGD pin.		
		1	Masks the PWRGD2 signal to the external PWRGD pin.		
0	PG1_MASK		Masks or unmasks the Channel 1 PWRGD signal to the external PWRGD hardware pin.	0x0	R/W
		0	Outputs the PWRGD1 signal to the external PWRGD pin.		
		1	Masks the PWRGD1 signal to the external PWRGD pin.		

Address: 0xE1, Reset: 0x00, Name: PG_READ

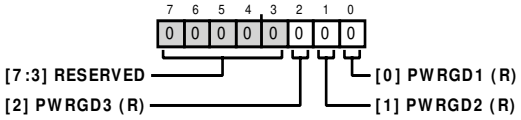


Table 34. Bit Descriptions for PG_READ

Bits	Bit Name	Settings	Description	Reset	Access
[7:3]	RESERVED		Reserved.	0x0	R
2	PWRGD3		Returns the real-time power-good status of Channel 3.	0x0	R
		1	Regulator output within nominal output voltage window.		
1	PWRGD2		Returns the real-time power-good status of Channel 2.	0x0	R
		1	regulator output within nominal output voltage window.		
0	PWRGD1		Returns the real-time power-good status of Channel 1.	0x0	R
		1	Regulator output within nominal output voltage window.		

Address: 0xE2, Reset: 0x00, Name: STATUS_LCH

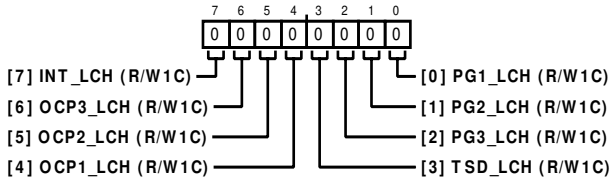


Table 35. Bit Descriptions for STATUS_LCH

Bits	Bit Name	Settings	Description	Reset	Access[1]
7	INT_LCH		Returns the latched status of the initiation procedures of the chip (for example, refuse loading failure).	0x0	R/W1C
		1	Chip initiation failure detected.		
			Latched flags are not reset when the fault disappears but are cleared only when a 1 is written to the appropriate bit, when all ENx pins = 0, or following a power cycle.		
6	OCP3_LCH		Returns the latched status of the Channel 3 overcurrent hiccup failure.	0x0	R/W1C
		1	Overcurrent hiccup failure detected for Channel 3.		
			Latched flags are not reset when the fault disappears but are cleared only when a 1 is written to the appropriate bit, when all ENx pins = 0, or following a power cycle.		
5	OCP2_LCH		Returns the latched status of the Channel 2 overcurrent hiccup failure.	0x0	R/W1C
		1	Overcurrent hiccup failure detected for Channel 2.		
			Latched flags are not reset when the fault disappears but are cleared only when a 1 is written to the appropriate bit, when all ENx pins = 0, or following a power cycle.		
4	OCP1_LCH		Returns the latched status of the Channel 1 overcurrent hiccup failure.	0x0	R/W1C
		1	Overcurrent hiccup failure detected for Channel 1.		
			Latched flags are not reset when the fault disappears but are cleared only when a 1 is written to the appropriate bit, when all ENx pins = 0, or following a power cycle.		
3	TSD_LCH		Returns the latched status of the thermal shutdown failure of the chip.	0x0	R/W1C
		1	Thermal shutdown failure detected.		
			Latched flags are not reset when the fault disappears but are cleared only when a 1 is written to the appropriate bit, when all ENx pins = 0, or following a power cycle.		
2	PG3_LCH		Returns the latched status of the Channel 3 power-good failure.	0x0	R/W1C
		1	Power-good failure detected for Channel 3.		
			Latched flags are not reset when the fault disappears but are cleared only when a 1 is written to the appropriate bit, when all ENx pins = 0, or following a power cycle.		
1	PG2_LCH		Returns the latched status of the Channel 2 power-good failure.	0x0	R/W1C
		1	Power-good failure detected for Channel 2.		
			Latched flags are not reset when the fault disappears but are cleared only when a 1 is written to the appropriate bit, when all ENx pins = 0, or following a power cycle.		
0	PG1_LCH		Returns the latched status of the Channel 1 power-good failure.	0x0	R/W1C
		1	Power-good failure detected for Channel 1.		
			Latched flags are not reset when the fault disappears but are cleared only when a 1 is written to the appropriate bit, when all ENx pins = 0, or following a power cycle.		

[1] R/W1C means read or write 1 to clear.

OUTLINE DIMENSIONS

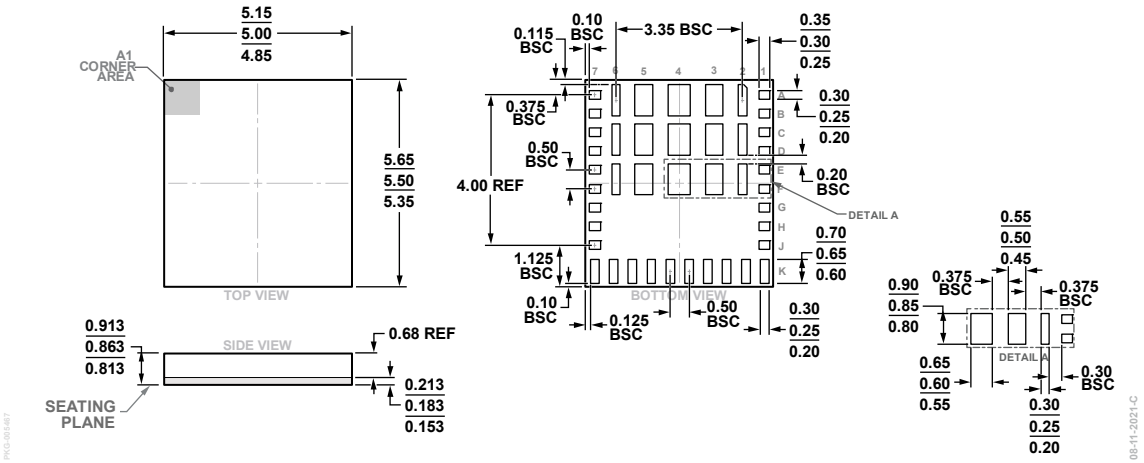


Figure 58. 43-Terminal Land Grid Array [LGA]
(CC-43-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADP5055ACCZ-R7	−40°C to +150°C	43-Terminal Land Grid Array [LGA]	CC-43-1
ADP5055-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.