



A Product Line of  
Diodes Incorporated



## SPECIFICATION FOR APPROVAL

CUSTOMER	_____
NOMINAL FREQUENCY	48.000000 MHz
HOLDER TYPE	TYPE FK 3.2x2.5 SEAM SEALED CRYSTAL CLOCK OSCILLATOR
SPEC. NO. ( P/N )	FK4800024Q
CUSTOMER P/N	_____
ISSUE DATE	May 22, 2018
VERSION	B

APPROVED	PREPARED	QA
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### Diodes Incorporated

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<https://www.diodes.com>

- \*Pb-free
- \*RoHS Compliant
- \*HF-Halogen Free
- \*REACH Compliant
- \*AEC-Q200 Compliant



# TYPE FK 3.2x2.5 SEAM SEALED CRYSTAL CLOCK OSCILLATOR

## FK4800024Q

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### ELECTRICAL SPECIFICATIONS

SRe Part Number : FK4800024Q

Item	Symbol	Specifications	Units	Notes
Nominal Frequency	F <sub>0</sub>	48.000000	MHz	
Frequency Stability	FT	± 50	ppm	**See note
Operating Temperature Range	TR	-40 to +85	°C	
Supply Voltage	V <sub>DD</sub>	+3.3 ± 5.0%	V	
Logic Type	LT	LVC MOS		
Supply Current, Output Enabled	I <sub>DD</sub> /OE	5 / 7	mA	Typ/ Max.
Supply Current, Output Disabled	I <sub>DD</sub> /OD	10	µA	Max.
Duty Cycle (Symmetry)	DC/SY	45 / 55	%	Measured 50% of Waveform
Rise / Fall Time	T <sub>R</sub> /T <sub>F</sub>	5	ns	Max. measured 10/90% of Waveform
Output Voltage "0" Level	V <sub>OL</sub>	10% V <sub>DD</sub>	V	Max at I <sub>OL</sub> = 4.0mA Min.
Output Voltage "1" Level	V <sub>OH</sub>	90% V <sub>DD</sub>	V	Min at I <sub>OH</sub> = -4.0mA Max.
Output Load	CL	15	pF	Max.
Jitter, Phase	RMS	1	ps	Max. 12KHz ~ 20MHz Frequency Band
Jitter, Accumulated	RMS(1-σ)	5	ps	Typ. 20,000 Consecutive Periods
Jitter, Peak to Peak	Pk-Pk	30	ps	Max. 100,000 Random Periods
Start Up Time		10	ms	Max.
Storage Temperature Range		-55 to +125	°C	

※ This product doesn't include harmful substance that stipulated by SONY SS-00259 Level 1 and S-AT2-001 Level 1 standard. RoHS Compliant (Pb - Free).

\*\*Stability includes all combinations of Operating Temperature, Load changes, rated Input (Supply) Voltage changes, Initial Calibration Tolerance (25°C), Aging (1 year at 25°C Average Effective Ambient Temperature), Shock and Vibration.

#### Output Enable / Disable Function

Parameter	Min.	Typ.	Max.	Units	Notes
Input Voltage (Pin1), Output Enable	0.7V <sub>DD</sub>			V	Or Open
Input Voltage (Pin1), Output Disable (low power standby)			0.3V <sub>DD</sub>	V	Output is Hi-Z
Internal Pullup Resistance	30			KΩ	
Output Disable Delay			50	ns	

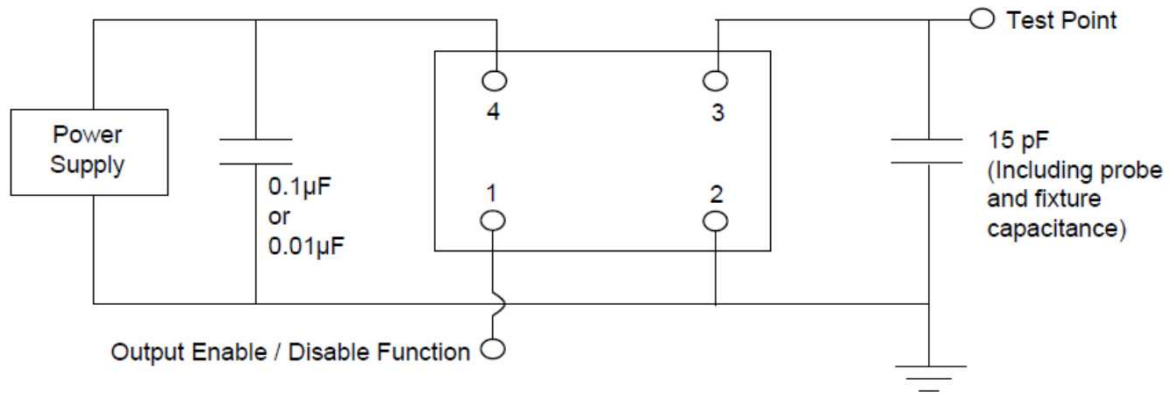


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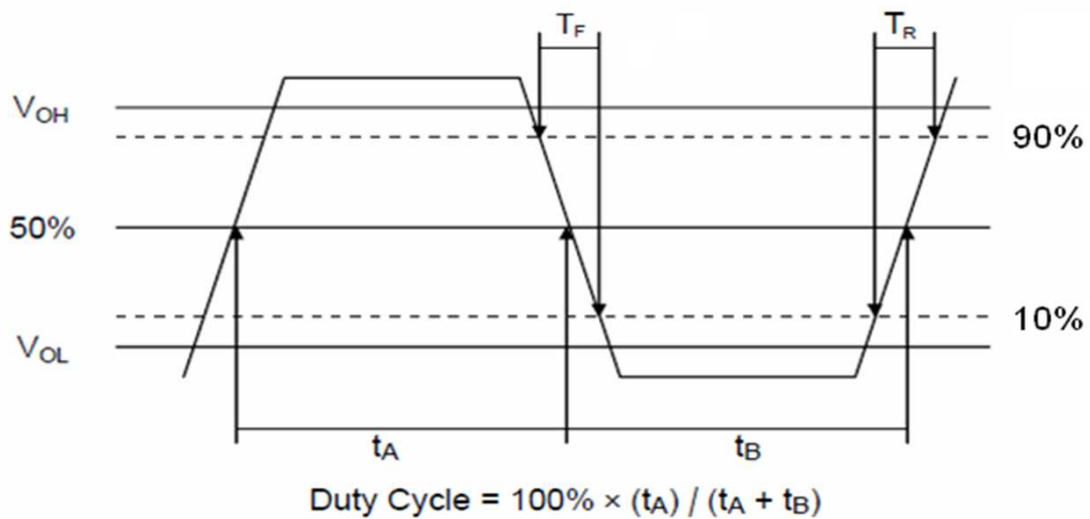
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### TEST CIRCUIT



### OUTPUT WAVEFORM



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## AEC-Q200 RELIABILITY TEST SPECIFICATIONS:

### 1. Initial

- 1.1 Physical Dimensions: JESD22, Method JB1-100
- 1.2 External Visual: MIL-STD-883, Method 2009
- 1.3 Freq. Vs. Temperature: Per Specification/Datasheet

### 2. Mechanical

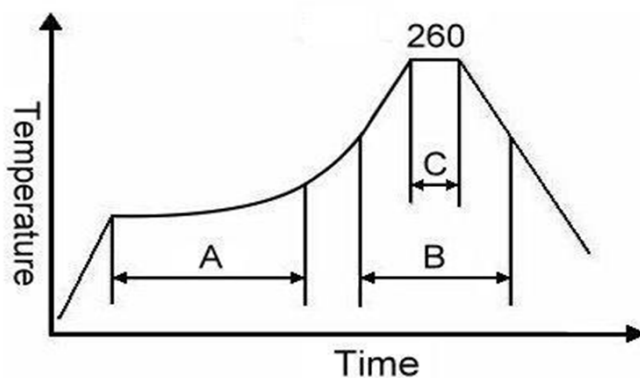
- 2.1 Mechanical Shock: MIL-STD-202 Method 213
- 2.2 Vibration: MIL-STD-202 Method 204
- 2.3 Solderability: J-STD-002
- 2.4 Board Flex: AEC Q200-005
- 2.5 Terminal Strength (SMD): AEC Q200-006

### 3.Environmental

- 3.1 Temp Cycle: JESD22, Method JA-104
- 3.2 Resistance to Solder Heat: MIL-STD-202 Method 210
- 3.3 High Temperature Operating Life: MIL-STD-202, Method 108
- 3.4 High Temp Exposure: MIL-STD-202, Method 108
- 3.5 High Temp & High Humidity: MIL-STD-202, Method 103
- 3.6 Thermal Shock: MIL-STD-202, Method 107

## SUGGESTED IR REFLOW PROFILE

\*As per IPC-JEDEC J-STD-020D



Note:

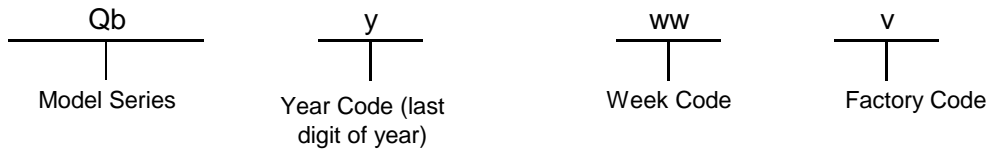
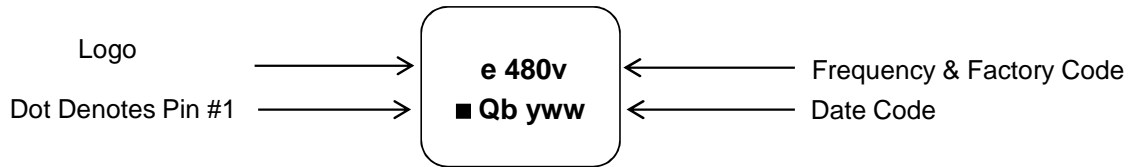
	Stage	Temperature	Time
A	Preheat	150~200°C	60~120 Sec
B	Primary Heat	217°C	60~150 Sec
C	Peak	260°C	10 Sec

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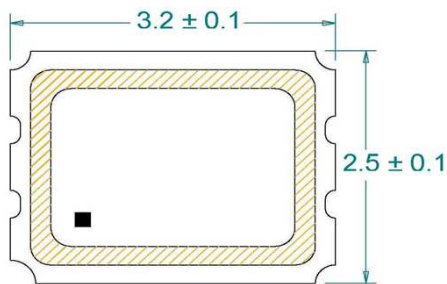
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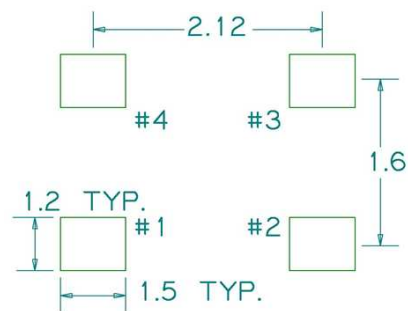
## MARKING



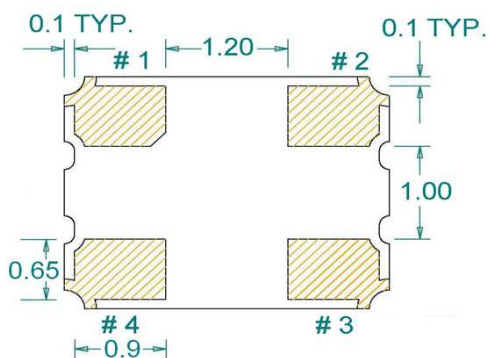
## MECHANICAL DRAWINGS ( Scale: None. Dimensions are in mm.)



### Recommended Land Pattern\*



\*External high-frequency power decoupling is recommended.(see test circuit for minimum recommendation). To ensure optimal performance, do not route traces beneath the package.



(Bottom View)

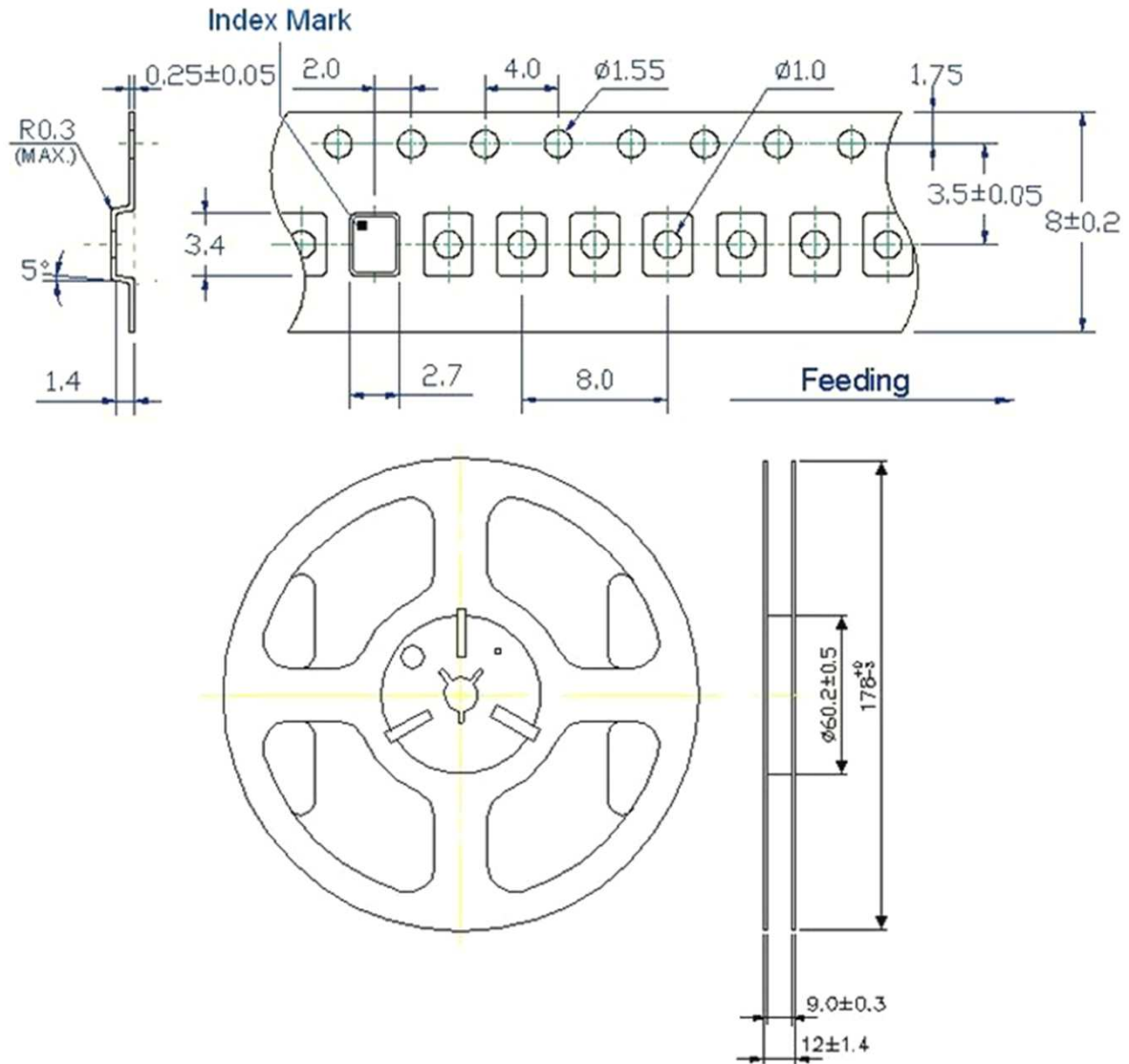
Pin	Function
1	OE
2	Ground
3	Clock Output
4	V <sub>DD</sub>

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## TAPE&REEL



1. 230mm minimum leader which consist of carrier and/or tape followed by a minimum of 160mm of empty carrier tape sealed with cover tape.
2. 160mm minimum trailer of empty carrier tape sealed with cover tape.

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### PACKING

