



BT150S-600R

SCR

17 March 2014

Product data sheet

1. General description

Planar passivated SCR with sensitive gate in a SOT428 (DPAK) surface mountable plastic package. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

2. Features and benefits

- Sensitive gate
- Planar passivated for voltage ruggedness and reliability
- Direct triggering from low power drivers and logic ICs
- Surface mountable package

3. Applications

- General purpose switching
- Protection Circuits

4. Quick reference data

Table 1. Quick reference data

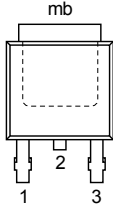

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage	[1]	-	-	600	V
V_{RRM}	repetitive peak reverse voltage		-	-	600	V
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(init)} = 25\text{ }^{\circ}\text{C}$; $t_p = 10\text{ ms}$; Fig. 4; Fig. 5	-	-	35	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{mb} \leq 111\text{ }^{\circ}\text{C}$; Fig. 2; Fig. 3	-	-	4	A
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 25\text{ }^{\circ}\text{C}$; Fig. 7	-	15	200	μA

[1] Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/ μs .



5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K	cathode	 <p style="text-align: center;">DPAK (SOT428)</p>	
2	A	anode ^[1]		
3	G	gate		
mb	A	mounting base; connected to anode		

[1] It is not possible to connect to pin 2 of the SOT428 package.

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BT150S-600R	DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	SOT428

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		[1]	-	600	V
V_{RRM}	repetitive peak reverse voltage			-	600	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{mb} \leq 111\text{ °C}$; Fig. 1		-	2.5	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{mb} \leq 111\text{ °C}$; Fig. 2 ; Fig. 3		-	4	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(\text{init})} = 25\text{ °C}$; $t_p = 10\text{ ms}$; Fig. 4 ; Fig. 5		-	35	A
		half sine wave; $T_{j(\text{init})} = 25\text{ °C}$; $t_p = 8.3\text{ ms}$		-	38	A
I^2t	I^2t for fusing	$t_p = 10\text{ ms}$; SIN		-	6.1	A^2s
di_T/dt	rate of rise of on-state current	$I_T = 10\text{ A}$; $I_G = 50\text{ mA}$; $di_G/dt = 50\text{ mA}/\mu s$		-	50	$A/\mu s$
I_{GM}	peak gate current			-	2	A
V_{RGM}	peak reverse gate voltage			-	5	V
P_{GM}	peak gate power			-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period		-	0.5	W
T_{stg}	storage temperature			-40	150	$^{\circ}C$
T_j	junction temperature		[2]	-	125	$^{\circ}C$

[1] Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/ μs .

[2] Operation above 110 $^{\circ}C$ may require the use of a gate to cathode resistor of 1k Ω or less.

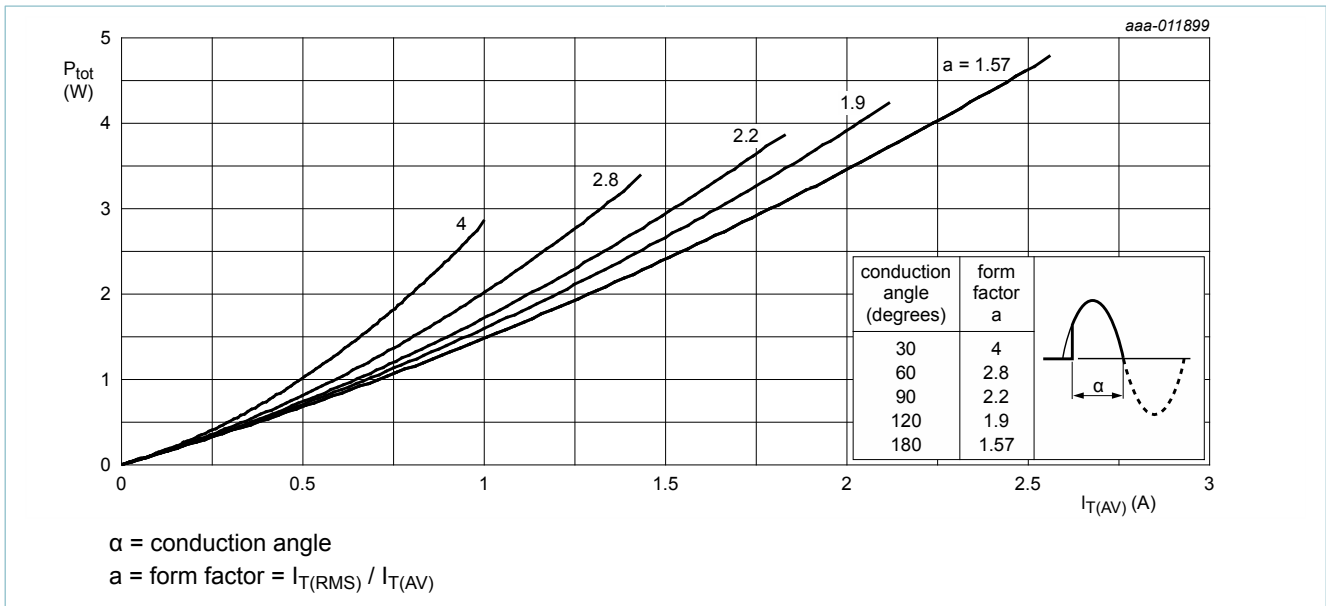


Fig. 1. Total power dissipation as a function of average on-state current; maximum values

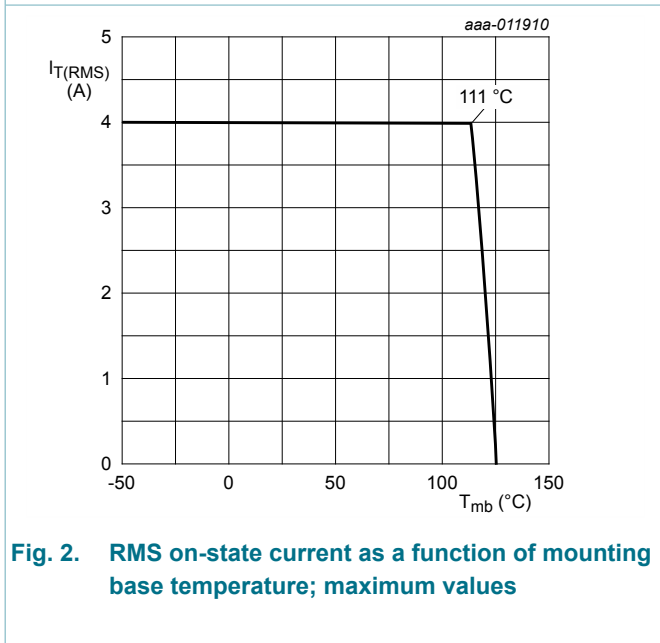


Fig. 2. RMS on-state current as a function of mounting base temperature; maximum values

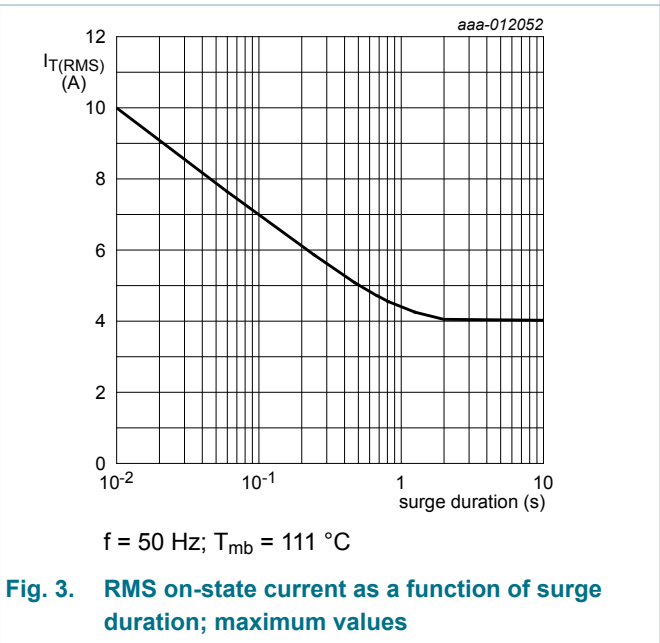


Fig. 3. RMS on-state current as a function of surge duration; maximum values

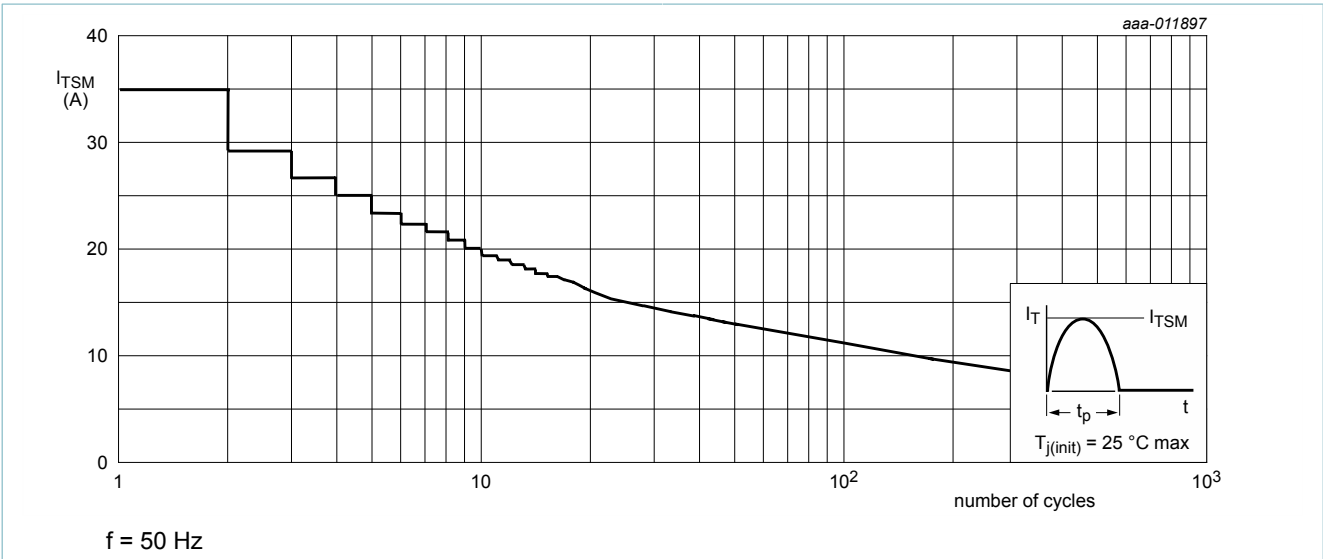


Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

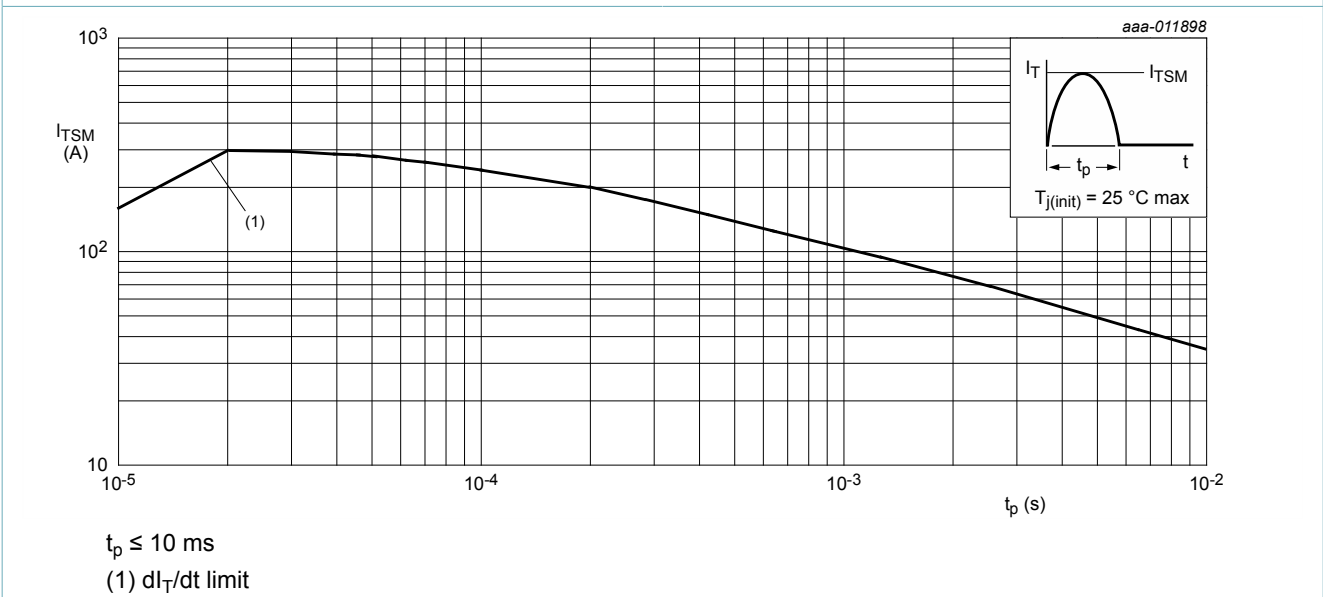
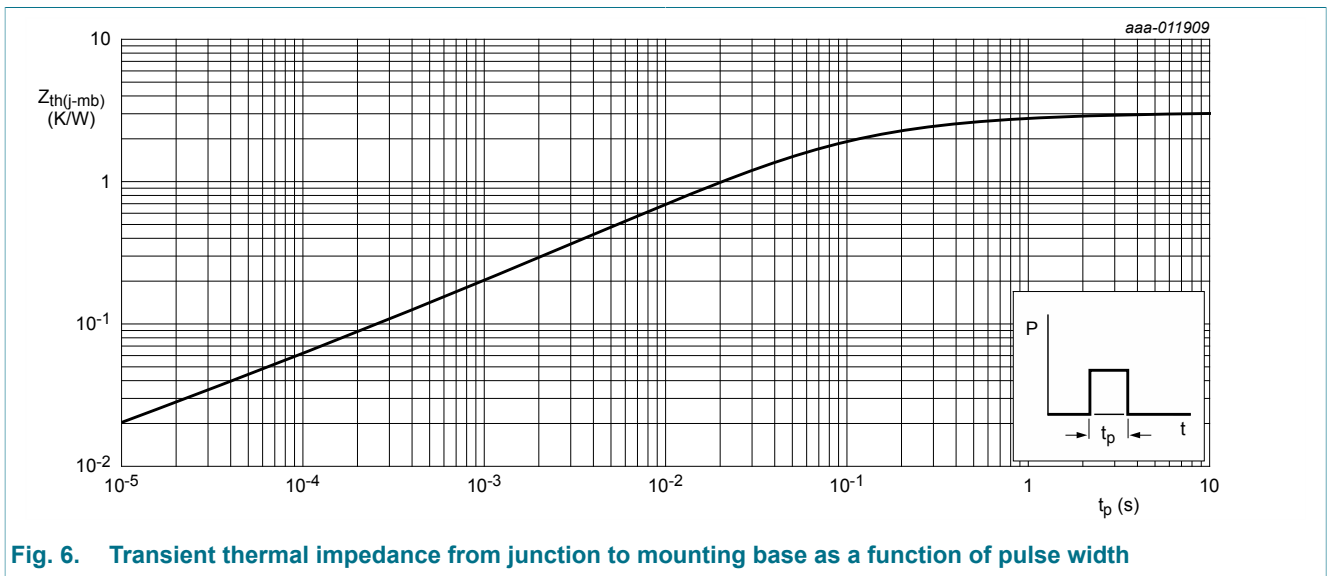


Fig. 5. Non-repetitive peak on-state current as a function of pulse width for sinusoidal currents; maximum values

8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 6	-	-	3	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint	-	75	-	K/W



9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 25\text{ °C}$; Fig. 7	-	15	200	μA
I_L	latching current	$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; $T_j = 25\text{ °C}$; Fig. 8	-	0.17	10	mA
I_H	holding current	$V_D = 12\text{ V}$; $T_j = 25\text{ °C}$; Fig. 9	-	0.1	6	mA
V_T	on-state voltage	$I_T = 5\text{ A}$; $T_j = 25\text{ °C}$; Fig. 10	-	1.23	1.8	V
V_{GT}	gate trigger voltage	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 25\text{ °C}$; Fig. 11	-	0.4	1	V
		$V_D = 600\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 110\text{ °C}$; Fig. 11	0.1	0.2	-	V
I_D	off-state current	$V_D = 600\text{ V}$; $T_j = 125\text{ °C}$	-	0.1	0.5	mA
I_R	reverse current	$V_R = 600\text{ V}$; $T_j = 125\text{ °C}$	-	0.1	0.5	mA
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 402\text{ V}$; $T_j = 125\text{ °C}$; $R_{GK} = 100\ \Omega$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; Fig. 12	-	50	-	$\text{V}/\mu\text{s}$
t_{gt}	gate-controlled turn-on time	$I_{TM} = 10\text{ A}$; $V_D = 600\text{ V}$; $I_G = 5\text{ mA}$; $dI_G/dt = 0.2\text{ A}/\mu\text{s}$; $T_j = 25\text{ °C}$	-	2	-	μs
t_q	commutated turn-off time	$V_{DM} = 402\text{ V}$; $T_j = 125\text{ °C}$; $I_{TM} = 8\text{ A}$; $V_R = 10\text{ V}$; $(dI_T/dt)_M = 10\text{ A}/\mu\text{s}$; $dV_D/dt = 2\text{ V}/\mu\text{s}$; $R_{GK} = 1\text{ k}\Omega$; ($V_{DM} = 67\%$ of V_{DRM})	-	100	-	μs

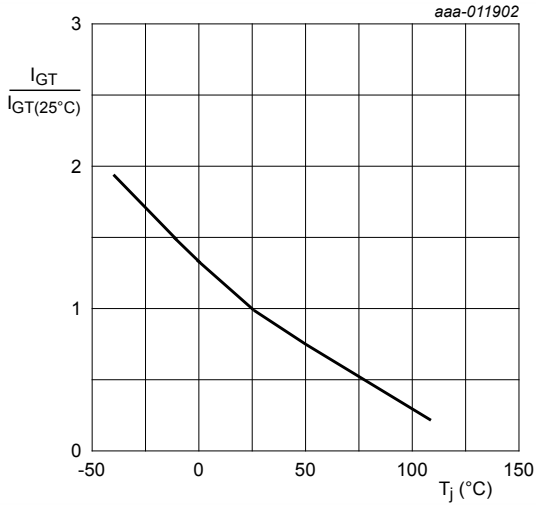
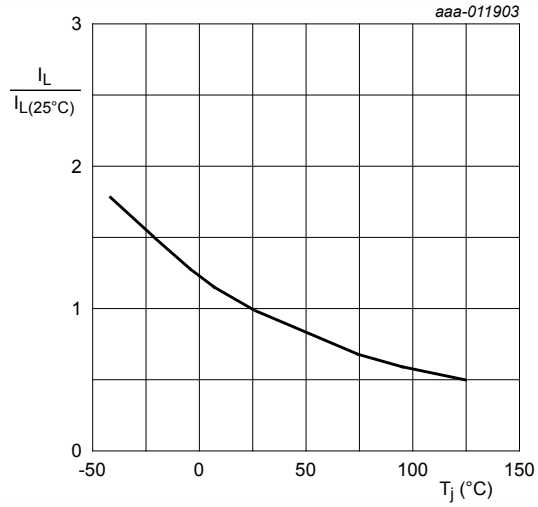
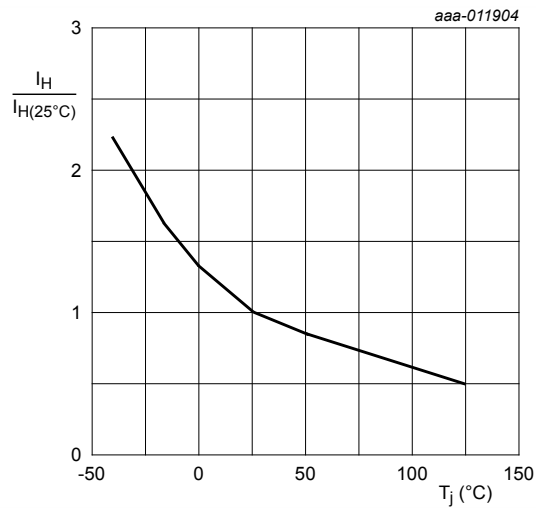


Fig. 7. Normalized gate trigger current as a function of junction temperature



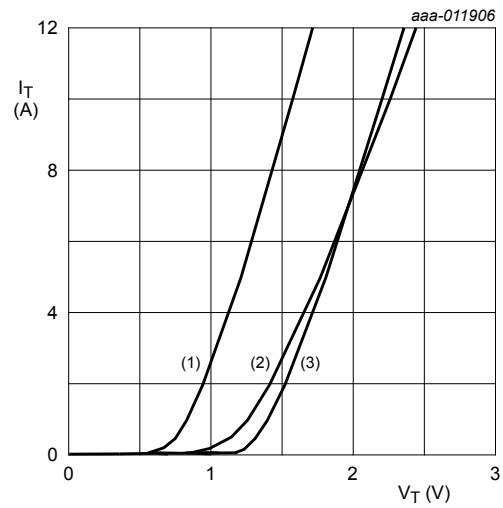
$R_{GK} = 1 \text{ k}\Omega$

Fig. 8. Normalized latching current as a function of junction temperature



$R_{GK} = 1 \text{ k}\Omega$

Fig. 9. Normalized holding current as a function of junction temperature



$V_o = 1.26 \text{ V}; R_s = 0.099 \Omega$

- (1) $T_j = 125^\circ\text{C}$; typical values
- (2) $T_j = 125^\circ\text{C}$; maximum values
- (3) $T_j = 25^\circ\text{C}$; maximum values

Fig. 10. On-state current as a function of on-state voltage

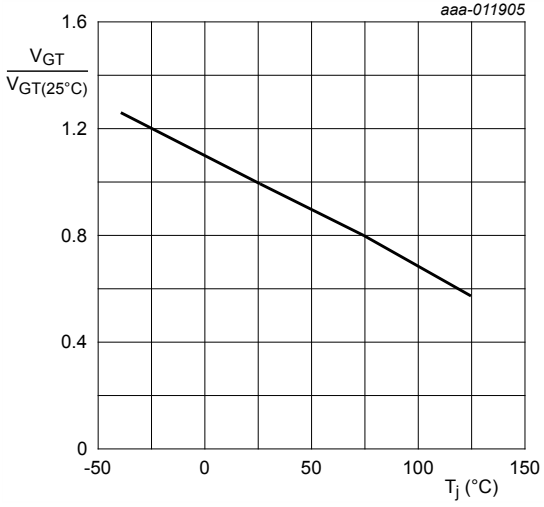
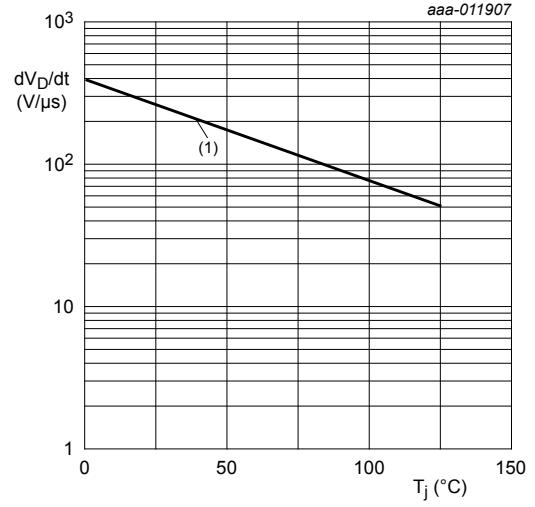


Fig. 11. Normalized gate trigger voltage as a function of junction temperature



(1) $R_{GK} = 100 \Omega$

Fig. 12. Critical rate of rise of off-state voltage as a function of junction temperature; typical values

10. Package outline

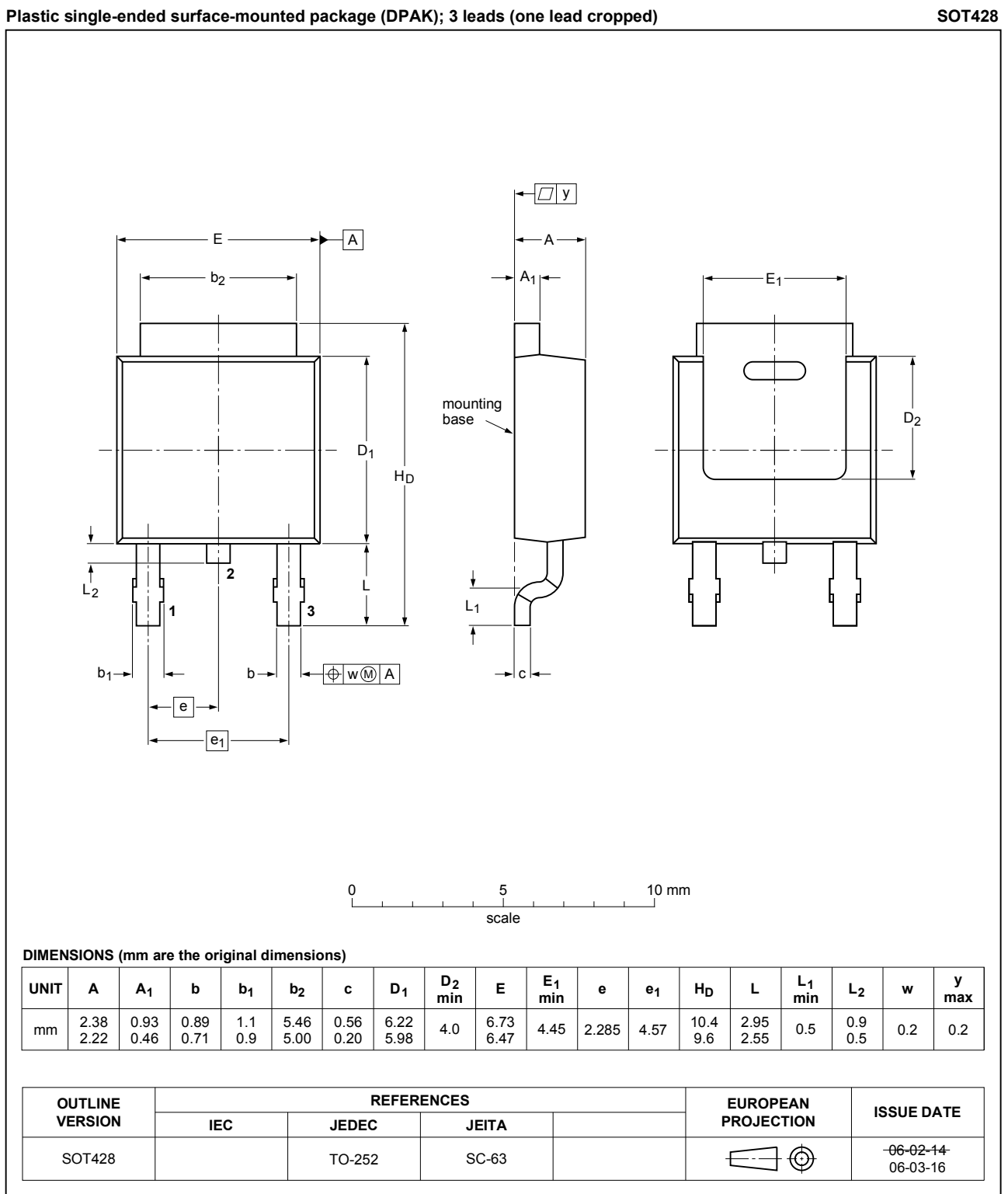


Fig. 13. Package outline DPAK (SOT428)

11. Soldering

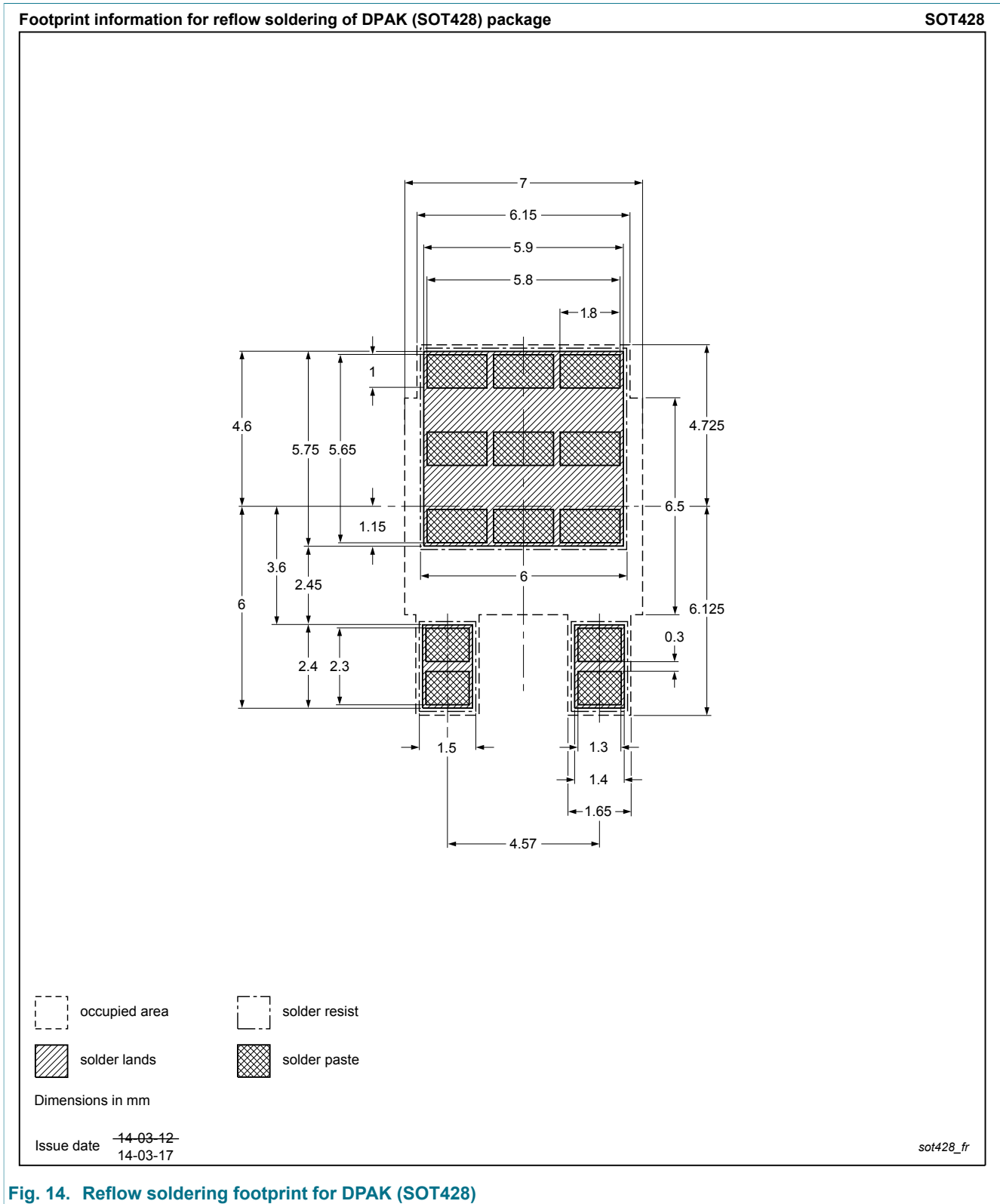


Fig. 14. Reflow soldering footprint for DPAK (SOT428)

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