Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010 Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

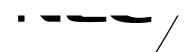
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MOS FIELD EFFECT TRANSISTOR NP82N04MUG, NP82N04NUG

SWITCHING N-CHANNEL POWER MOS FET

DESCRIPTION

The NP82N04MUG and NP82N04NUG are N-channel MOS Field Effect Transistors designed for high current switching applications.

ORDERING INFORMATION

PART NUMBER	LEAD PLATING	PACKING	PACKAGE
NP82N04MUG-S18-AY Note	D 0 (T')	Tube	TO-220 (MP-25K) typ. 1.9 g
NP82N04NUG-S18-AY Note	Pure Sn (Tin)	50 p/tube	TO-262 (MP-25SK) typ. 1.8 g

Note Pb-free (This product does not contain Pb in the external electrode.)

FEATURES

• Non logic level

Super low on-state resistance

 $R_{DS(on)}$ = 4.2 m Ω MAX. (Vgs = 10 V, ID = 41 A)

• High current rating

 $I_{D(DC)} = \pm 82 \text{ A}$

• Low input capacitance

Ciss = 6500 pF TYP.

• Designed for automotive application and AEC-Q101 qualified

ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

	,		
Drain to Source Voltage (V _{GS} = 0 V)	VDSS	40	V
Gate to Source Voltage (VDS = 0 V)	Vgss	±20	V
Drain Current (DC) (Tc = 25°C)	I _{D(DC)}	±82	Α
Drain Current (pulse) Note1	ID(pulse)	±328	Α
Total Power Dissipation (Tc = 25°C)	P _{T1}	143	W
Total Power Dissipation (T _A = 25°C)	P _{T2}	1.8	W
Channel Temperature	Tch	175	°C
Storage Temperature	Tstg	-55 to +175	°C
Repetitive Avalanche Current Note2	lar	43	Α
Repetitive Avalanche Energy Note2	Ear	185	mJ

Notes 1. PW \leq 10 μ s, Duty Cycle \leq 1%

2. Tch $\leq 150^{\circ}$ C, Rg = 25 Ω

THERMAL RESISTANCE

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(TO-220)



(TO-262)

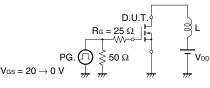


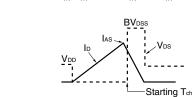
ELECTRICAL CHARACTERISTICS (TA = 25°C)

	•	•				
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	V _{DS} = 40 V, V _{GS} = 0 V			1	μΑ
Gate Leakage Current	Igss	V _{GS} = ±20 V, V _{DS} = 0 V			±100	nA
Gate to Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	2.0		4.0	٧
Forward Transfer Admittance Note	y fs	V _{DS} = 5 V, I _D = 41 A	20	47		S
Drain to Source On-state Resistance Note	RDS(on)	V _{GS} = 10 V, I _D = 41 A		3.4	4.2	mΩ
Input Capacitance	Ciss	V _{DS} = 25 V,		6500	9750	pF
Output Capacitance	Coss	V _{GS} = 0 V,		580	870	pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		370	670	pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 20 V, I _D = 41 A,		39	90	ns
Rise Time	tr	V _{GS} = 10 V,		102	260	ns
Turn-off Delay Time	td(off)	$R_G = 0 \Omega$		67	140	ns
Fall Time	tr			13	40	ns
Total Gate Charge	Q _G	V _{DD} = 32 V,		106	160	nC
Gate to Source Charge	QGS	V _{GS} = 10 V,		29		nC
Gate to Drain Charge	Q _{GD}	I _D = 82 A		35		nC
Body Diode Forward Voltage Note	V _{F(S-D)}	IF = 82 A, VGS = 0 V		0.9	1.5	٧
Reverse Recovery Time	trr	IF = 82 A, VGS = 0 V,		43		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/μs		51		nC

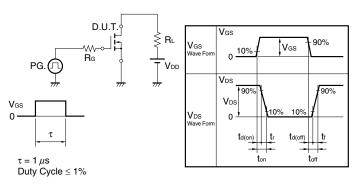
Note Pulsed test

TEST CIRCUIT 1 AVALANCHE CAPABILITY





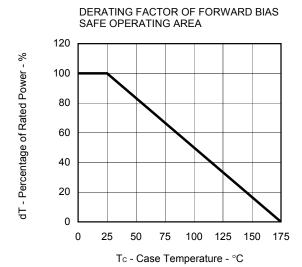
TEST CIRCUIT 2 SWITCHING TIME

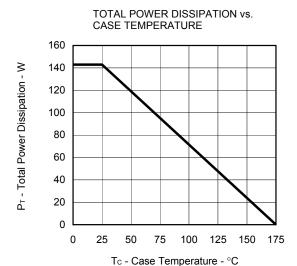


TEST CIRCUIT 3 GATE CHARGE

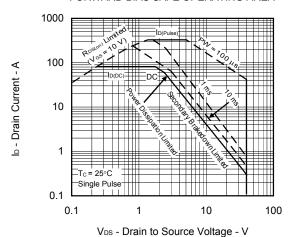
$$\begin{array}{c|c} D.U.T. \\ IG = 2 \text{ mA} \\ \hline \\ PG. \\ \hline \\ \end{array} \begin{array}{c} S \text{ 50 } \Omega \\ \hline \\ \end{array} \begin{array}{c} PG. \\ \hline \\ \end{array} \begin{array}{c} S \text{ 70 } \\ \hline \\ \end{array} \begin{array}{c} PG. \\ \hline \\ \end{array} \begin{array}{c} S \text{ 10 } \\ \hline \end{array} \begin{array}{c} S \text{ 10 } \\ \end{array} \begin{array}{c} S$$

TYPICAL CHARACTERISTICS (TA = 25°C)

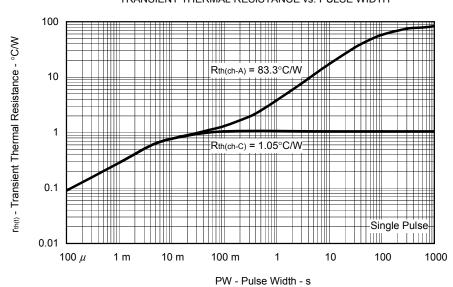


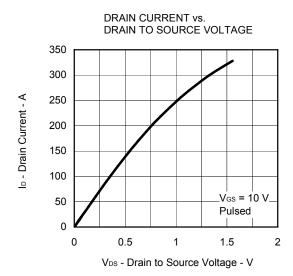


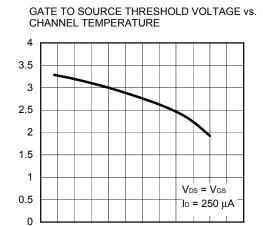
FORWARD BIAS SAFE OPERATING AREA

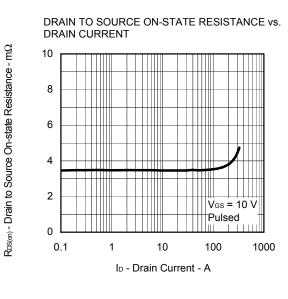


TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

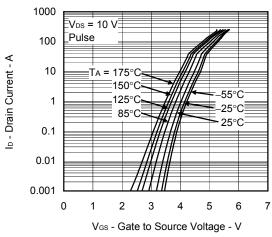




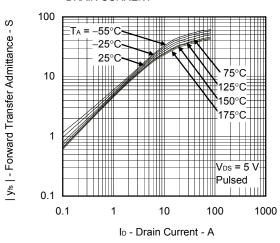




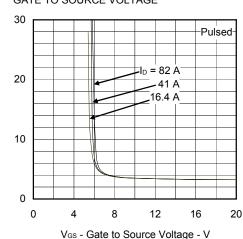




FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



Vos(th) - Gate to Source Threshold Voltage - V

-75

-25

25

75

Tch - Channel Temperature - °C

125

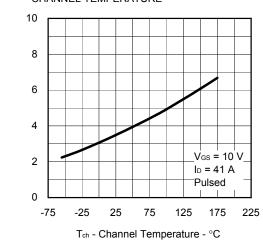
175

225

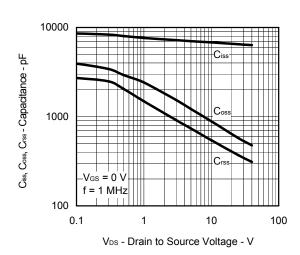
R_{DS(m)} - Drain to Source On-state Resistance - mΩ

R_{DS(ση)} - Drain to Source On-state Resistance - mΩ

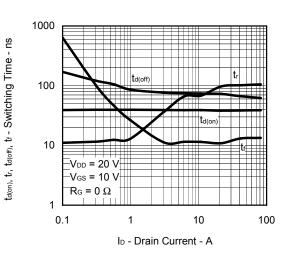
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



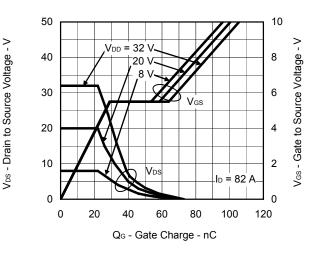
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



SWITCHING CHARACTERISTICS

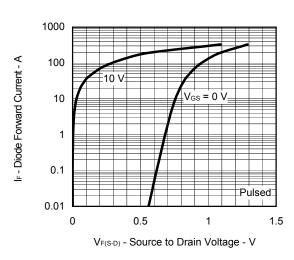


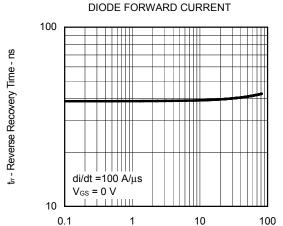
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



REVERSE RECOVERY TIME vs.

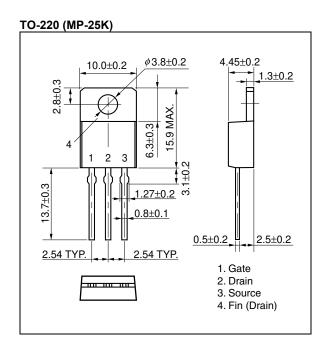
SOURCE TO DRAIN DIODE FORWARD VOLTAGE

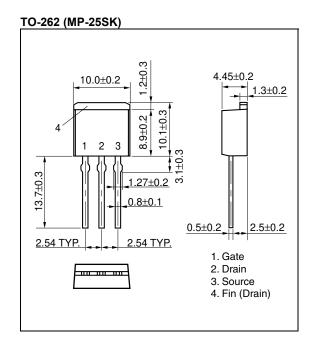




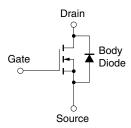
IF - Diode Forward Current - A

PACKAGE DRAWINGS (Unit: mm)





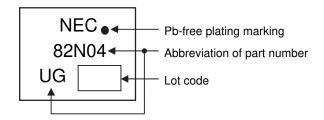
EQUIVALENT CIRCUIT



Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.



MARKING INFORMATION



RECOMMENDED SOLDERING CONDITIONS

These products should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, please contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Wave soldering NP82N04MUG, NP82N04NUG	Maximum temperature (Solder temperature): 260°C or below Time: 10 seconds or less Maximum chlorine content of rosin flux: 0.2% (wt.) or less	THDWS
Partial heating NP82N04MUG, NP82N04NUG	Maximum temperature (Pin temperature): 350°C or below Time (per side of the device): 3 seconds or less Maximum chlorine content of rosin flux: 0.2% (wt.) or less	P350

Caution Do not use different soldering methods together (except for partial heating).

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