

DESCRIPTION

The EV6619L-Q-00A evaluation board is designed to demonstrate the capabilities of the MP6619L, an H-Bridge motor driver. It operates from a supply input voltage (V_{IN}) up to 28V, and can deliver a motor current up to 5A. The MP6619L is typically used to drive a brushed DC motor.

The MP6619L has a configurable current limit (I_{LIMIT}). For simplicity, the output polarity can be controlled by pulling the IN1 and IN2 pins high or low.

Full protection features include over-current protection (OCP), input over-voltage protection (OVP), under-voltage lockout (UVLO), and thermal shutdown. The input control signals for the MP6619L are applied via the connector or generated on the board.

The MP6619L is available in a QFN-19 (3mmx3mm) package. It is recommended to read the MP6619L datasheet prior to making any changes to the EV6619L-Q-00A.

PERFORMANCE SUMMARY

Parameters	Conditions	Value
Input voltage (V _{IN}) range		2.5V to 28V
Maximum output current (IouT_MAX)		5A
VCC voltage (V _{CC})		2.8V to 5.5V
VDD voltage (V _{DD})		3.3V or 5V

EV6619L-Q-00A EVALUATION BOARD



LxW (7.5cmx7.5cm)

Board Number	MPS IC Number	
EV6619L-Q-00A	MP6619LGQ	



QUICK START GUIDE

- 1. Connect the input voltage (2.5V \leq V_{IN} \leq 28V) and input ground to the VIN and GND connectors, respectively.
- 2. Connect the VCC voltage (2.8V \leq V_{CC} \leq 5.5V) and ground to the VCC and GND connectors, respectively.
- 3. Connect the VDD voltage (3.3V or 5V) and ground to the VDD and GND connectors, respectively.
- 4. Set the input control and logic signal through the CN1 connector via the external MCU, or manually through SW1. Manual action requires an external 3.3V or 5V V_{DD} as a pull-up power supply.

Table 1 shows the logic truth table.

Table 1. Logic Truth Table				
EN	INx	OUTx		
0	X ⁽¹⁾	Hi-Z		
1	0	Low		
1	1	High		

Table 1. Logic Truth Table

Note:

1) X denotes N/A.

5. The current control trip value is set by the adjustable resistor (R4). When the ISET pin is floating, the current trip voltage (V_{ITRIP}) is set to the default (200mV). If a resistor is connected between ISET and GND, then VITRIP can be reduced below 200mV to reduce power loss on the sense resistor. The relationship between V_{ITRIP} and the ISET resistor (R_{ISET}) can be calculated with Equation (1):

$$V_{\text{ITRIP}}(V) = 0.2 \times \frac{40}{R_{\text{ISET}}(k\Omega)}$$
(1)

6. The output current limit (I_{OUT LIM}) is determined by V_{ITRIP} and R_{ISEN}. If R_{ISET} is connected between ISET and ground, then I_{OUT LIM} can be estimated with Equation (2):

$$I_{OUT_LIM}(A) = 0.2 \times \frac{40}{R_{ISET}(k\Omega)} \times \frac{1}{R_{ISEN}(\Omega)}$$
(2)

If ISET remains floating, then $I_{OUT \ LIM}$ can be calculated with Equation (3):

$$I_{OUT_LIM}(A) = \frac{0.2}{R_{ISEN}(\Omega)}$$
(3)









EV6619L-Q-00A BILL OF MATERIALS

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
2	C1, C3	100µF	Electrolytic capacitor, 35V	DIP	Jianghai	CD287-35V100
2	C2, C4	4.7µF	Ceramic capacitor, 50V, X7R	1210	Murata	GRM32ER71H475KA88L
2	C5, C7	100nF	Ceramic capacitor, 50V, X7R	0603	Murata	GRM188R71H104KA93D
1	C6	1µF	Ceramic capacitor, 25V, X7R	0805	Murata	GRM21BR71E105KA99L
2	C8, C9	100nF	Ceramic capacitor, 50V, X7R	0805	Murata	GRM21BR71H104KA01L
1	R1	1kΩ	Film resistor, 1%	0805	Yageo	RC0805FR-071KL
2	R2, R5	10Ω	Film resistor, 1%	0603	Yageo	RC0603FR-0710RL
1	R3	40.2kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0740K2L
1	R4	100kΩ	Square trimming potentiometer	DIP	Bourns	3266W-1-104LF
3	R7, R8, R9	4.7kΩ	Film resistor, 5%	0805	Yageo	RC0805JR-074K7L
1	R10	50mΩ	Film resistor, 1%	3720	Cyntec	RL3720WT-R050-FN
1	LED1	50mW	Red LED	0805	Baihong	BL-HUE35A-AV-TRB
1	SW1	25mA	Dial switch, 4-bit	SMD	Wurth	418121270804
4	VDD, VCC, GND1, GND2	1mm	Connector	DIP	Any	
4	VIN1, OUT1, OUT2, GND	2mm	Connector	DIP	Any	
1	CN1	2.54mm	Connector, 4-bit	DIP	Any	
2	J1, J2	2.54mm	Jumper	DIP	Any	
6	nFAULT, GND, ISET, EN, IN2, IN1	1mm	Yellow test point	DIP	Any	
1	U1	MP6619L	2.5V to 28V, 5A, H-bridge motor driver	QFN-19 (3mmx 3mm)	MPS	MP6619LGQ



PCB LAYOUT



Figure 4: Mid-Layer 1

Figure 5: Mid-Layer 2



PCB LAYOUT (continued)



Figure 6: Bottom Layer

Figure 7: Bottom Silk



REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	6/29/2022	Initial Release	-

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