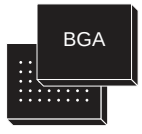
# M59DR032EA
# M59DR032EB

## 32 Mbit (2Mb x 16, Dual Bank, Page )
## 1.8V Supply Flash Memory

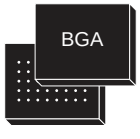
### FEATURES SUMMARY

- SUPPLY VOLTAGE
  - $V_{DD}$ = $V_{DDQ}$ = 1.65V to 2.2V for Program, Erase and Read
  - $V_{PP}$ = 12V for fast Program (optional)
- ASYNCHRONOUS PAGE MODE READ
  - Page Width: 4 Words
  - Page Access: 35ns
  - Random Access: 85ns, 100ns and 120ns
- PROGRAMMING TIME
  - 10µs by Word typical
  - Double Word Program Option
- MEMORY BLOCKS
  - Dual Bank Memory Array: 4 Mbit, 28 Mbit
  - Parameter Blocks (Top or Bottom location)
- DUAL BANK OPERATIONS
  - Read within one Bank while Program or Erase within the other
  - No delay between Read and Write operations
- BLOCK LOCKING
  - All blocks locked at Power up
  - Any combination of blocks can be locked
  - $\overline{WP}$ for Block Lock-Down
- COMMON FLASH INTERFACE (CFI)
  - 64 bit Unique Device Identifier
  - 64 bit User Programmable OTP Cells
- ERASE SUSPEND and RESUME MODES
- 100,000 PROGRAM/ERASE CYCLES per BLOCK
- 20 YEARS DATA RETENTION
  - Defectivity below 1ppm/year
- ELECTRONIC SIGNATURE
  - Manufacturer Code: 0020h
  - Top Device Code, M59DR032EA: 00A0h
  - Bottom Device Code, M59DR032EB: 00A1h

**Figure 1. Packages**




TFBGA48 (ZB)
7 x 12mm




TFBGA48 (ZF)
7 x 7mm

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## SUMMARY DESCRIPTION

The M59DR032E is a 32 Mbit (2Mbit x16) non-volatile Flash memory that may be erased electrically at block level and programmed in-system on a Word-by-Word basis using a 1.65V to 2.2V $V_{DD}$ supply for the circuitry and a 1.65V to 2.2V $V_{DDQ}$ supply for the Input/Output pins. An optional 12V $V_{PP}$ power supply is provided to speed up customer programming.

The device features an asymmetrical block architecture. M59DR032E has an array of 71 blocks and is divided into two banks, Banks A and B, providing Dual Bank operations. While programming or erasing in Bank A, read operations are possible in Bank B or vice versa. Only one bank at a time is allowed to be in program or erase mode. The bank architecture is summarized in Table 2, and the Block Addresses are shown in Appendix A. The Parameter Blocks are located at the top of the memory address space for the M59DR032EA, and at the bottom for the M59DR032EB.

Each block can be erased separately. Erase can be suspended, in order to perform either read or program in any other block, and then resumed. Each block can be programmed and erased over 100,000 cycles.

Program and Erase commands are written to the Command Interface of the memory. An internal Program/Erase Controller takes care of the timings necessary for program and erase operations. The end of a program or erase operation can be detected and any error conditions identified in the Status Register. The command set required to control the memory is consistent with JEDEC standards.

The M59DR032E features an instant, individual block locking scheme that allows any block to be locked or unlocked with no latency, enabling instant code and data protection. All blocks have two levels of protection. They can be individually locked and locked-down preventing any accidental programming or erasure. All blocks are locked at Power Up and Reset.

The device includes a 128 bit Protection Register and a Security Block to increase the protection of a system's design. The Protection Register is divided into two 64 bit segments. The first segment contains a unique device number written by ST, while the second one is one-time-programmable by the user. The user programmable segment can be permanently protected. The Security Block, parameter block 0, can be permanently protected by the user. Figure 4, shows the Security Block and Protection Register Memory Map.

The device is available in TFBGA48 (7 x 12mm and 7 x 7mm, 0.75mm pitch) packages and it is supplied with all the bits erased (set to '1').

**Figure 2. Logic Diagram**

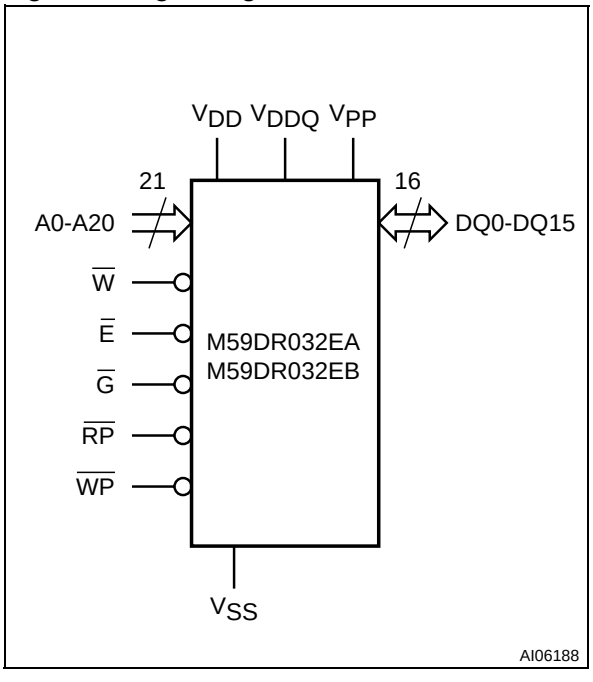



**Table 1. Signal Names**

| | |
|---|---|
| A0-A20 | Address Inputs |
| DQ0-DQ15 | Data Input/Outputs, Command Inputs |
| $\overline{E}$ | Chip Enable |
| $\overline{G}$ | Output Enable |
| $\overline{W}$ | Write Enable |
| $\overline{RP}$ | Reset/Power-Down |
| $\overline{WP}$ | Write Protect |
| $V_{DD}$ | Supply Voltage |
| $V_{DDQ}$ | Supply Voltage for Input/Output Buffers |
| $V_{PP}$ | Optional Supply Voltage for Fast Program & Erase |
| $V_{SS}$ | Ground |
| NC | Not Connected Internally |

**Figure 3. TFBGA Connections (Top view through package)**

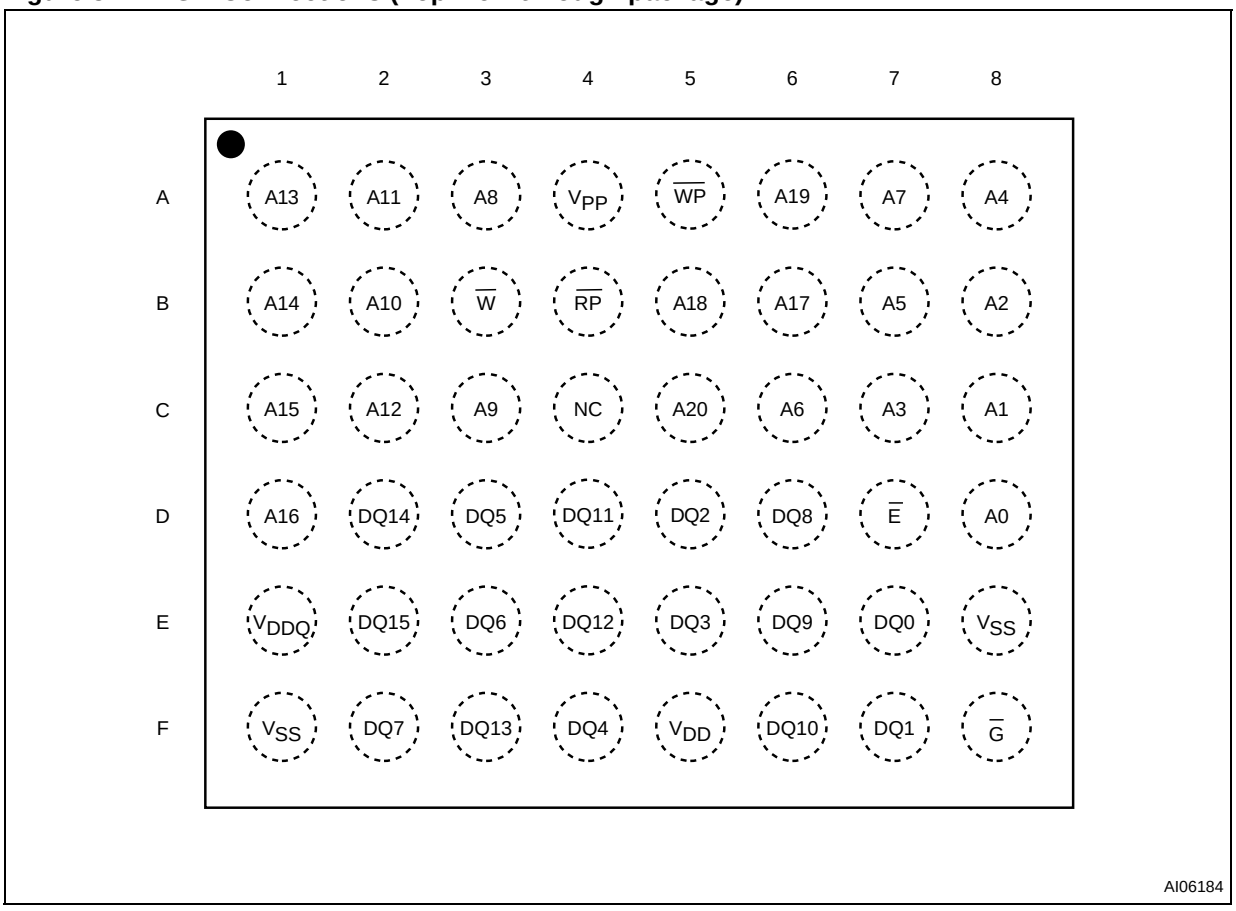
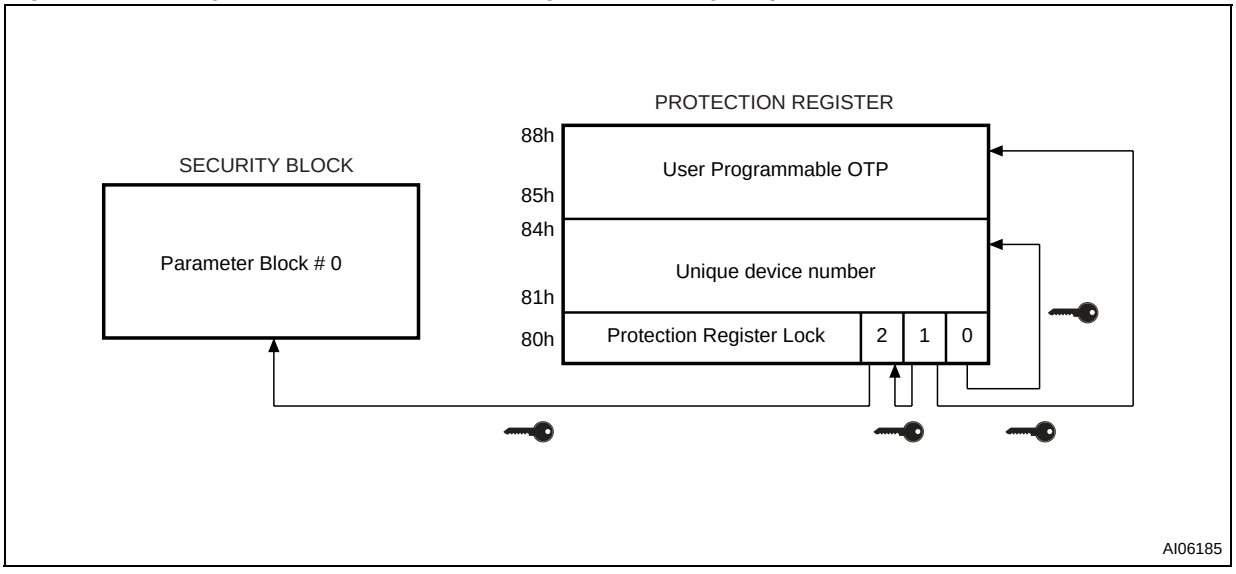



**Table 2. Bank Organization**

| | Bank Size | Parameter Blocks | Main Blocks |
|---|---|---|---|
| Bank A | 4 Mbit | 8 blocks of 4 KWord | 7 blocks of 32 KWord |
| Bank B | 28 Mbit | - | 56 blocks of 32 KWord |

**Figure 4. Security Block and Protection Register Memory Map**



## SIGNAL DESCRIPTIONS

See Figure 2, Logic Diagram, and Table 1, Signal Names, for a brief overview of the signals connected to this device.

**Address Inputs (A0-A20).** The Address Inputs select the cells in the memory array to access during Bus Read operations. During Bus Write operations they control the commands sent to the Command Interface of the internal state machine. During a write operation the address inputs are latched on the falling edge of Chip Enable $\overline{E}$ or Write Enable $\overline{W}$, whichever occurs last.

**Data Input/Output (DQ0-DQ15).** The Data I/O output the data stored at the selected address during a Bus Read operation or input a command or the data to be programmed during a Write Bus operation.

Both input data and commands are latched on the rising edge of Write Enable $\overline{W}$. The data output is the Memory Array, the Common Flash Interface, the Electronic Signature Manufacturer or Device codes, the Block Protection status, the Configuration Register status or the Status Register Data depending on the address.

The data bus is high impedance when the chip is deselected, Output Enable $\overline{G}$ is at $V_{IH}$, or $\overline{RP}$ is at $V_{IL}$.

**Chip Enable ($\overline{E}$).** The Chip Enable input activates the memory control logic, input buffers, decoders and sense amplifiers. When Chip Enable is at $V_{IH}$ the device is deselected and the power consumption is reduced to the standby level.

**Output Enable ($\overline{G}$).** The Output Enable gates the outputs through the data buffers during a read operation. When Output Enable is at $V_{IH}$ the outputs are high impedance.

**Write Enable ($\overline{W}$).** The Write Enable controls the Bus Write operation of the memory's Command Interface.

**Write Protect ($\overline{WP}$).** Write Protect is an input that gives an additional hardware protection for each block. When Write Protect is at $V_{IL}$, the locked-down blocks cannot be locked or unlocked. When Write Protect is at $V_{IH}$, the Lock-Down is disabled and the locked-down blocks can be locked or unlocked. (refer to Table 10, Lock Status).

**Reset/Power-Down Input ($\overline{RP}$).** The Reset/Power-Down input provides hardware reset of the memory, and/or Power-Down functions, depending on the Configuration Register status. A Reset or Power-Down of the memory is achieved by pulling $\overline{RP}$ to $V_{IL}$ for at least $t_{PLPH}$.

The Reset/Power-Down function is set in the Configuration Register (see Set Configuration Register command). If it is set to '0' the Reset function is enabled, if it is set to '1' the Power-Down function is enabled. After a Reset or Power-Up the power save function is disabled and all blocks are locked.

The memory Command Interface is reset on Power Up to Read Array. Either Chip Enable or Write Enable must be tied to $V_{IH}$ during Power Up to allow maximum security and the possibility to write a command on the first rising edge of Write Enable.

After a Reset, when the device is in Read, Erase Suspend Read or Standby, valid data will be output $t_{PHQ7V1}$ after the rising edge of $\overline{RP}$. If the device is in Erase or Program, the operation will be aborted and the reset recovery will take a maximum of $t_{PLQ7V}$. The memory will recover from Power-Down $t_{PHQ7V2}$ after the rising edge of $\overline{RP}$. See Tables 17, 18 and Figure 11.

**$V_{DD}$ and $V_{DDQ}$ Supply Voltage (1.65V to 2.2V).** $V_{DD}$ provides the power supply to the internal core of the memory device. It is the main power supply for all operations (read, program and erase).

$V_{DDQ}$ provides the power supply to the I/O pins. $V_{DD}$ and $V_{DDQ}$ must be at the same voltage.

**$V_{PP}$ Programming Voltage (11.4V to 12.6V).** $V_{PP}$ provides a high voltage power supply for fast factory programming. $V_{PP}$ is required to use the Double Word and Quadruple Word Program commands.

**$V_{SS}$ Ground.** $V_{SS}$ ground is the reference for the core supply. It must be connected to the system ground.

**Note: Each device in a system should have $V_{DD}$, $V_{DDQ}$ and $V_{PP}$ decoupled with a 0.1µF capacitor close to the pin. See Figure 6, AC Measurement Load Circuit. The PCB trace widths should be sufficient to carry the required $V_{PP}$ program and erase currents.**

## BUS OPERATIONS

The following operations can be performed using the appropriate bus cycles: Read Array (Random, and Page Modes), Write, Output Disable, Standby and Reset/Power-Down, see Table 3.

**Read.** Read operations are used to output the contents of the Memory Array, the Electronic Signature, the Status Register, the CFI, the Block Protection Status or the Configuration Register status. Read operation of the memory array is performed in asynchronous page mode, that provides fast access time. Data is internally read and stored in a page buffer. The page has a size of 4 words and is addressed by A0-A1 address inputs. Read operations of the Electronic Signature, the Status Register, the CFI, the Block Protection Status, the Configuration Register status and the Security Code are performed as single asynchronous read cycles (Random Read). Both Chip Enable $\overline{E}$ and Output Enable $\overline{G}$ must be at $V_{IL}$ in order to read the output of the memory.

**Write.** Write operations are used to give commands to the memory or to latch Input Data to be programmed. A write operation is initiated when Chip Enable $\overline{E}$ and Write Enable $\overline{W}$ are at $V_{IL}$ with Output Enable $\overline{G}$ at $V_{IH}$. Addresses are latched on the falling edge of $\overline{W}$ or $\overline{E}$ whichever occurs last. Commands and Input Data are latched on the rising edge of $\overline{W}$ or $\overline{E}$ whichever occurs first. Noise pulses of less than 5ns typical on $\overline{E}$, $\overline{W}$ and $\overline{G}$ signals do not start a write cycle.

**Output Disable.** The data outputs are high impedance when the Output Enable $\overline{G}$ is at $V_{IH}$ with Write Enable $\overline{W}$ at $V_{IH}$.

**Standby.** The memory is in standby when Chip Enable $\overline{E}$ is at $V_{IH}$ and the P/E.C. is idle. The power consumption is reduced to the standby level and the outputs are high impedance, independent of the Output Enable $\overline{G}$ or Write Enable $\overline{W}$ inputs.

**Automatic Standby.** In Read mode, after 150ns of bus inactivity and when CMOS levels are driving the addresses, the chip automatically enters a pseudo-standby mode where consumption is reduced to the CMOS standby value, while outputs still drive the bus.

**Power-Down.** The memory is in Power-Down when the Configuration Register is set for Power-Down and $\overline{RP}$ is at $V_{IL}$. The power consumption is reduced to the Power-Down level, and Outputs are in high impedance, independent of the Chip Enable $\overline{E}$, Output Enable $\overline{G}$ or Write Enable $\overline{W}$ inputs.

**Dual Bank Operations.** The Dual Bank allows data to be read from one bank of memory while a program or erase operation is in progress in the other bank of the memory. Read and Write cycles can be initiated for simultaneous operations in different banks without any delay. Status Register during Program or Erase must be monitored using an address within the bank being modified.

**Table 3. Bus Operations**

| Operation | $\overline{E}$ | $\overline{G}$ | $\overline{W}$ | $\overline{RP}$ | $\overline{WP}$ | DQ15-DQ0 |
|---|---|---|---|---|---|---|
| Read | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | $V_{IH}$ | Data Output |
| Write | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | Data Input |
| Output Disable | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | $V_{IH}$ | $V_{IH}$ | Hi-Z |
| Standby | $V_{IH}$ | X | X | $V_{IH}$ | $V_{IH}$ | Hi-Z |
| Reset / Power-Down | X | X | X | $V_{IL}$ | $V_{IH}$ | Hi-Z |

Note: X = Don't care.

## COMMAND INTERFACE

All Bus Write operations to the memory are interpreted by the Command Interface. Commands consist of one or more sequential Bus Write operations. An internal Program/Erase Controller handles all timings and verifies the correct execution of the Program and Erase commands. Two bus write cycles are required to unlock the Command Interface. They are followed by a setup or confirm cycle. The increased number of write cycles is to ensure maximum data security.

The Program/Erase Controller provides a Status Register whose output may be read at any time to monitor the progress or the result of the operation.

The Command Interface is reset to Read mode when power is first applied or exiting from Reset. Command sequences must be followed exactly. Any invalid combination of commands will reset the device to Read mode

**Read/Reset Command.** The Read/Reset command returns the device to Read mode. One Bus Write cycle is required to issue the Read/Reset command and return the device to Read mode. Subsequent Read operations will read the addressed location and output the data. The write cycle can be preceded by the unlock cycles but it is not mandatory.

**Read CFI Query Command.** The Read CFI Query command is used to read data from the Common Flash Interface (CFI) and the Electronic Signature (Manufacturer or the Device Code, see Table 5). The Read CFI Query Command consists of one Bus Write cycle. Once the command is issued the device enters Read CFI mode. Subsequent Bus Read operations read the Common Flash Interface or Electronic Signature. Once the device has entered Read CFI mode, only the Read/Reset command should be used and no other. Issuing the Read/Reset command returns the device to Read mode.

See Appendix B, Common Flash Interface, Tables 31, 32, and 33 for details on the information contained in the Common Flash Interface memory area.

**Auto Select Command.** The Auto Select command uses the two unlock cycles followed by one write cycle to any bank address to setup the command. Subsequent reads at any address will output the Block Protection status, Protection Register and Protection Register Lock or the Configuration Register status depending on the levels of A0 and A1 (see Tables 6, 7 and 8). Once the Auto Select command has been issued only the Read/Reset command should be used and no other. Issuing the Read/Reset command returns the device to Read mode.

**Set Configuration Register Command.** The M59DR032E contains a Configuration Register, see Table 7, Configuration Register.

It is used to define the status of the Reset/Power-Down functions. The value for the Configuration Register is always presented on A0-A15, the other address bits are ignored. Address input A10 defines the status of the Reset/Power-Down functions. If it is set to '0' the Reset function is enabled, if it is set to '1' the Power-Down function is enabled. At Power Up the Configuration Register bit is set to '0'.

The Set Configuration Register command is used to write a new value to the Configuration Register. The command uses the two unlock cycles followed by one write cycle to setup the command and a further write cycle to write the data and confirm the command.

**Program Command.** The Program command uses the two unlock cycles followed by a write cycle to set up the command and a further write cycle to latch the Address and Data and start the Program Erase Controller. Read operations within the same bank output the Status Register after programming has started.

Note that the Program command cannot change a bit set to '0' back to '1'. One of the Erase Commands must be used to set all the bits in a block or in the whole bank from '0' to '1'. If the Program command is used to try to set a bit from '0' to '1' Status Register Error bit DQ5 will be set to '1', only if $V_{PP}$ is in the range of 11.4V to 12.6V.

**Double Word Program Command.** This feature is offered to improve the programming throughput by writing a page of two adjacent Words in parallel. The $V_{PP}$ supply voltage is required to be from 11.4V to 12.6V for the Double Word Program command.

The command uses the two unlock cycles followed by a write cycle to set up the command. A further two cycles are required to latch the address and data of the two Words and start the Program Erase Controller.

The addresses must be the same except for the A0. The Double Word Program command can be executed in Bypass mode to skip the two unlock cycles.

Note that the Double Word Program command cannot change a bit set to '0' back to '1'. One of the Erase Commands must be used to set all the bits in a block or in the whole bank from '0' to '1'. If the Double Word Program command is used to try to set a bit from '0' to '1' Status Register Error bit DQ5 will be set to '1'.

**Quadruple Word Program Command.** The Quadruple Word Program command improves the

programming throughput by writing a page of four adjacent Words in parallel. The four Words must differ only for the addresses A0 and A1. The $V_{PP}$ supply voltage is required to be from 11.4V to 12.6V for the Quadruple Word Program command.

The command uses the two unlock cycles followed by a write cycle to set up the command. A further four cycles are required to latch the address and data of the four Words and start the Program Erase Controller.

The Quadruple Word Program command can be executed in Bypass mode to skip the two unlock cycles.

Note that the Quadruple Word Program command cannot change a bit set to '0' back to '1'. One of the Erase Commands must be used to set all the bits in a block or in the whole bank from '0' to '1'. If the Quadruple Word Program command is used to try to set a bit from '0' to '1' Status Register Error bit DQ5 will be set to '1'.

**Enter Bypass Mode Command.** The Bypass mode is used to reduce the overall programming time when large memory arrays need to be programmed.

The Enter Bypass Mode command uses the two unlock cycles followed by one write cycle to set up the command. Once in Bypass mode, it is imperative that only the following commands be issued: Exit Bypass, Program, Double Word Program or Quadruple Word Program.

**Exit Bypass Mode Command.** The Exit Bypass Mode command uses two write cycles to be set up and confirmed. The unlock cycles are not required. After the Exit Bypass Mode command, the device resets to Read mode.

**Program in Bypass Mode Command.** The Program in Bypass Mode command can be issued when the device is in Bypass mode (issue an Enter Bypass Mode command). It uses the same sequence of cycles as the Program command with the exception of the unlock cycles.

**Double Word Program in Bypass Mode Command.** The Double Word Program in Bypass Mode command can be issued when the device is in Bypass mode (issue an Enter Bypass Mode command). It uses the same sequence of cycles as the Double Word Program command with the exception of the unlock cycles.

**Quadruple Word Program in Bypass Mode Command.** The Quadruple Word Program in Bypass Mode command can be issued when the device is in Bypass mode (issue an Enter Bypass Mode command). It uses the same sequence of cycles as the Quadruple Word Program command with the exception of the unlock cycles.

**Block Lock Command.** The Block Lock command is used to lock a block and prevent Program or Erase operations from changing the data in it. All blocks are locked at Power-Up or Reset.

Three Bus Write cycles are required to issue the Block Lock command.

- The first two bus cycles unlock the Command Interface.
- The third bus cycle sets up the Block Lock command and latches the block address.

The lock status can be monitored for each block using the Auto Select command. Table 10 shows the Lock Status after issuing a Block Lock command.

The Block Lock bits are volatile, once set they remain set until a hardware Reset or Power-Down/ Power-Up. They are cleared by a Block Unlock command. Refer to the section, Block Locking, for a detailed explanation.

**Block Unlock Command.** The Block Unlock command is used to unlock a block, allowing the block to be programmed or erased.

Three Bus Write cycles are required to issue the Block Unlock command.

- The first two bus cycles unlock the Command Interface.
- The third bus cycle sets up the Block UnLock command and latches the block address.

The lock status can be monitored for each block using the Auto Select command. Table 10 shows the lock status after issuing a Block Unlock command. Refer to the section, Block Locking, for a detailed explanation.

**Block Lock-Down Command.** A locked or unlocked block can be locked-down by issuing the Block Lock-Down command. A locked-down block cannot be programmed or erased, or have its protection status changed when $\overline{WP}$ is low, $V_{IL}$. When $\overline{WP}$ is high, $V_{IH}$, the Lock-Down function is disabled and the locked blocks can be individually unlocked by the Block Unlock command.

Three Bus Write cycles are required to issue the Block Lock-Down command.

- The first two bus cycles unlock the Command Interface.
- The third bus cycle sets up the Block Lock-Down command and latches the block address.

The lock status can be monitored for each block using the Auto Select command. Locked-Down blocks revert to the locked (and not locked-down) state when the device is reset on power-down. Table 10 shows the Lock Status after issuing a Block Lock-Down command. Refer to the section, Block Locking, for a detailed explanation.

**Block Erase Command.** The Block Erase command can be used to erase a block. It sets all the bits within the selected block to '1'. All previous data in the block is lost. If the block is protected then the Erase operation will abort, the data in the block will not be changed and the device will return to Read Array mode. It is not necessary to pre-program the block as the Program/Erase Controller does it automatically before erasing.

Six Bus Write cycles are required to issue the command.

- The first two write cycles unlock the Command Interface.
- The third write cycles sets up the command
- the fourth and fifth write cycles repeat the unlock sequence
- the sixth write cycle latches the block address and confirms the command.

Additional Block Erase confirm cycles can be issued to erase other blocks without further unlock cycles. All blocks must belong to the same bank; if a new block belonging to the other bank is given, the operation is aborted.

The additional Block Erase confirm cycles must be given within the DQ3 erase timeout period. Each time a new confirm cycle is issued the timeout period restarts. The status of the internal timer can be monitored through the level of DQ3, see Status Register section for more details.

Once the command is issued the device outputs the Status Register data when any address within the bank is read.

After the command has been issued the Read/Reset command will be accepted during the DQ3 timeout period, after that only the Erase Suspend command will be accepted.

On successful completion of the Block Erase command, the device returns to Read Array mode.

**Bank Erase Command.** The Bank Erase command can be used to erase a bank. It sets all the bits within the selected bank to '1'. All previous data in the bank is lost. The Bank Erase command will ignore any protected blocks within the bank. If all blocks in the bank are protected then the Bank Erase operation will abort and the data in the bank will not be changed. It is not necessary to pre-program the bank as the Program/Erase Controller does it automatically before erasing.

As for the Block Erase command six Bus Write cycles are required to issue the command.

- The first two write cycles unlock the Command Interface.
- The third write cycles sets up the command
- the fourth and fifth write cycles repeat the unlock sequence
- the sixth write cycle latches the block address and confirms the command.

Once the command is issued the device outputs the Status Register data when any address within the bank is read.

For optimum performance, Bank Erase commands should be limited to a maximum of 100 Program/Erase cycles per Block. After 100 Program/Erase cycles the internal algorithm will still operate properly but some degradation in performance may occur.

Dual operations are not supported during Bank Erase operations and the command cannot be suspended.

On successful completion of the Bank Erase command, the device returns to Read Array mode.

**Erase Suspend Command.** The Erase Suspend command is used to pause a Block Erase operation. In a Dual Bank memory it can be used to read data within the bank where an Erase operation is in progress. It is also possible to program data in blocks not being erased.

One bus write cycle is required to issue the Erase Suspend command. The Program/Erase Controller suspends the Erase operation within 20µs of the Erase Suspend command being issued and bits 7, 6 and/ or 2 of the Status Register are set to '1'. The device is then automatically set to Read mode. The command can be addressed to any bank.

During Erase Suspend the memory will accept the Erase Resume, Program, Read CFI Query, Auto Select, Block Lock, Block Unlock and Block Lock-Down commands.

**Erase Resume Command.** The Erase Resume command can be used to restart the Program/Erase Controller after an Erase Suspend command has paused it. One Bus Write cycle is required to issue the command. The command must be issued to an address within the bank being erased. The unlock cycles are not required.

**Protection Register Program Command.** The Protection Register Program command is used to Program the Protection Register (One-Time-Programmable (OTP) segment and Protection Register Lock). The OTP segment is programmed 16 bits at a time. When shipped all bits in the segment are set to '1'. The user can only program the bits to '0'.

Four write cycles are required to issue the Protection Register Program command.

- The first two bus cycles unlock the Command Interface.
- The third bus cycle sets up the Protection Register Program command.

- The fourth latches the Address and the Data to be written to the Protection Register and starts the Program/Erase Controller.

Read operations output the Status Register content after the programming has started.

The OTP segment can be protected by programming bit 1 of the Protection Register Lock. The segment can be protected by programming bit 1 of the Protection Register Lock. Bit 1 of the Protection Register Lock also protects bit 2 of the Protection Register Lock. Programming bit 2 of the Protection Register Lock will result in a permanent protection of Parameter Block #0 (see Figure 4, Security Block and Protection Register Memory Map). Attempting to program a previously protected Protection Register will result in a Status Register error. The protection of the Protection Register and/or the Security Block is not reversible.

**Table 4. Commands**

| Commands | No of Cycles | Bus Operations | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 1st | | 2nd | | 3rd | | 4th | | 5th | | 6th | | 7th | |
| | | Add | Data | Add | Data | Add | Data | Add | Data | Add | Data | Add | Data | Add | Data |
| Read/Reset | 1+ | X | F0h | Read Memory Array until a new write cycle is initiated. | | | | | | | | | | | |
| | 3+ | 555h | AAh | 2AAh | 55h | 555h | F0h | Read Memory Array until a new write cycle is initiated. | | | | | | | |
| CFI Query | 1+ | 55h | 98h | Read CFI and Electronic Signature until a Read/Reset command is issued. | | | | | | | | | | | |
| Auto Select | 3+ | 555h | AAh | 2AAh | 55h | 555h | 90h | Read Protection Register, Block Protection or Configuration Register Status until a Read/Reset command is issued. | | | | | | | |
| Set Configuration Register | 4 | 555h | AAh | 2AAh | 55h | 555h | 60h | CRD | 03h | | | | | | |
| Program | 4 | 555h | AAh | 2AAh | 55h | 555h | A0h | PA | PD | Read Data Polling or Toggle Bit until Program completes. | | | | | |
| Double Word Program | 5 | 555h | AAh | 2AAh | 55h | 555h | 40h | PA1 | PD1 | PA2 | PD2 | | | | |
| Quadruple Word Program | 5 | 555h | AAh | 2AAh | 55h | 555h | 50h | PA1 | PD1 | PA2 | PD2 | PA3 | PD3 | PA4 | PD4 |
| Enter Bypass Mode | 3 | 555h | AAh | 2AAh | 55h | 555h | 20h | | | | | | | | |
| Exit Bypass Mode | 2 | X | 90h | X | 00h | | | | | | | | | | |
| Program in Bypass Mode | 2 | X | A0h | PA | PD | Read Data Polling or Toggle Bit until Program completes. | | | | | | | | | |
| Double Word Program in Bypass Mode | 3 | X | 40h | PA1 | PD1 | PA2 | PD2 | | | | | | | | |
| Quadruple Word Program in Bypass Mode | 3 | X | 50h | PA1 | PD1 | PA2 | PD2 | PA3 | PD3 | PA4 | PD4 | | | | |
| Block Lock | 4 | 555h | AAh | 2AAh | 55h | 555h | 60h | BA | 01h | | | | | | |
| Block Unlock | 4 | 555h | AAh | 2AAh | 55h | 555h | 60h | BA | D0h | | | | | | |
| Block Lock-Down | 4 | 555h | AAh | 2AAh | 55h | 555h | 60h | BA | 2Fh | | | | | | |
| Block Erase | 6+ | 555h | AAh | 2AAh | 55h | 555h | 80h | 555h | AAh | 2AAh | 55h | BA | 30h | | |
| Bank Erase | 6 | 555h | AAh | 2AAh | 55h | 555h | 80h | 555h | AAh | 2AAh | 55h | BA | 10h | | |
| Erase Suspend | 1 | X | B0h | Read until Toggle stops, then read all the data needed from any Blocks not being erased then Resume Erase. | | | | | | | | | | | |
| Erase Resume | 1 | BA | 30h | Read Data Polling or Toggle Bits until Erase completes or Erase is suspended another time | | | | | | | | | | | |
| Protection Register Program | 4 | 555h | AAh | 2AAh | 55h | PA | C0h | PA | PD | | | | | | |

Note: X = Don't Care, BA = Block Address, PA = Program address, PD = Program Data, CRD = Configuration Register Data. For Coded cycles address inputs A12-A20 are don't care.

**Table 5. Read Electronic Signature**

| Code | Device | $\overline{E}$ | $\overline{G}$ | $\overline{W}$ | A0 | A1 | A7-A2 | A8-A20 | DQ15-DQ0 |
|---|---|---|---|---|---|---|---|---|---|
| Manufacturer Code | | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | $V_{IL}$ | 0 | X | 0020h |
| Device Code | M59DR032EA | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | $V_{IL}$ | 0 | X | 00A0h |
| | M59DR032EB | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | $V_{IL}$ | 0 | X | 00A1h |

Note: X = Don't care.

**Table 6. Read Block Protection**

| Block Status | $\overline{E}$ | $\overline{G}$ | $\overline{W}$ | A0 | A1 | A20-A12 | A7-A2 | Other Addresses | DQ0 | DQ1 | DQ15-DQ2 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Locked Block | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | $V_{IH}$ | Block Address | 0 | X | 1 | 0 | 0000h |
| Unlocked Block | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | $V_{IH}$ | Block Address | 0 | X | 0 | 0 | 0000h |
| Locked-Down Block | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | $V_{IH}$ | Block Address | 0 | X | X | 1 | 0000h |

Note: X = Don't care.

**Table 7. Configuration Register**

| $\overline{RP}$ Function | $\overline{E}$ | $\overline{G}$ | $\overline{W}$ | A0 | A1 | A7-A2 | Other Addresses | DQ10 | DQ9-DQ0 DQ15-DQ11 |
|---|---|---|---|---|---|---|---|---|---|
| Reset | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | $V_{IH}$ | 0 | X | 0 | Don't Care |
| Reset/Power-Down | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | $V_{IH}$ | 0 | X | 1 | Don't Care |

Note: X = Don't care.

**Table 8. Read Protection Register**

| Word | $\overline{E}$ | $\overline{G}$ | $\overline{W}$ | A20-A8 | A7-0 | DQ15-8 | DQ7-3 | DQ2 | DQ1 | DQ0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Lock | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | X | 80h | XXh | 00000b | Security prot.data | OTP prot.data | 0 |
| Unique ID 0 | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | X | 81h | ID data | ID data | ID data | ID data | ID data |
| Unique ID 1 | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | X | 82h | ID data | ID data | ID data | ID data | ID data |
| Unique ID 2 | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | X | 83h | ID data | ID data | ID data | ID data | ID data |
| Unique ID 3 | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | X | 84h | ID data | ID data | ID data | ID data | ID data |
| OTP 0 | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | X | 85h | OTP data | OTP data | OTP data | OTP data | OTP data |
| OTP 1 | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | X | 86h | OTP data | OTP data | OTP data | OTP data | OTP data |
| OTP 2 | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | X | 87h | OTP data | OTP data | OTP data | OTP data | OTP data |
| OTP 3 | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | X | 88h | OTP data | OTP data | OTP data | OTP data | OTP data |

Note: X= Don't care.

**Table 9. Program, Erase Times and Program, Erase Endurance Cycles**

| Parameter | M59DR032E | | | | Unit |
|---|---|---|---|---|---|
| | Min | Max | Typ | Typical after 100k W/E Cycles | |
| Parameter Block (4 KWord) Erase (Preprogrammed) | | 2.5 | 0.3 | 1 | s |
| Main Block (32 KWord) Erase (Preprogrammed) | | 4 | 0.8 | 3 | s |
| Bank Erase (Preprogrammed, Bank A) | | | 3 | 6 | s |
| Bank Erase (Preprogrammed, Bank B) | | | 20 | 30 | s |
| Chip Program (1) | | | 20 | 25 | s |
| Chip Program (Double Word, $V_{PP}$ = 12V) (1) | | | 8 | | s |
| Word Program (2) | | 100 | 10 | | µs |
| Double Word Program ($V_{PP}$ = 12V) | | 100 | 8 | | µs |
| Quadruple Word Program ($V_{PP}$ = 12V) | | 100 | 8 | | µs |
| Program/Erase Cycles (per Block) | 100,000 | | | | cycles |

Note: 1. Excludes the time needed to execute the sequence for program command.
2. Same timing value if $V_{PP}$ = 12V

## BLOCK LOCKING

The M59DR032E features an instant, individual block locking scheme that allows any block to be locked or unlocked with no latency. This locking scheme has two levels of protection.

- Lock/Unlock - this first level allows software-only control of block locking.
- Lock-Down - this second level requires hardware interaction before locking can be changed.

The protection status of each block can be set to Locked, Unlocked, and Lock-Down. Table 10, defines all of the possible protection states ($\overline{WP}$, DQ1, DQ0).

### Reading a Block's Lock Status

The lock status of every block can be read in the Auto Select mode of the device. Subsequent reads at the address specified in Table 6, will output the protection status of that block. The lock status is represented by DQ0 and DQ1. DQ0 indicates the Block Lock/Unlock status and is set by the Lock command and cleared by the Unlock command. It is also automatically set when entering Lock-Down. DQ1 indicates the Lock-Down status and is set by the Lock-Down command. It cannot be cleared by software, only by a hardware reset or power-down.

The following sections explain the operation of the locking system.

### Locked State

The default status of all blocks on power-up or after a hardware reset is Locked (states (0,0,1) or (1,0,1)). Locked blocks are fully protected from any program or erase. Any program or erase operations attempted on a locked block will reset the device to Read Array mode. The Status of a Locked block can be changed to Unlocked or Lock-Down using the appropriate software commands. An Unlocked block can be Locked by issuing the Lock command.

### Unlocked State

Unlocked blocks (states (0,0,0), (1,0,0) (1,1,0)), can be programmed or erased. All unlocked blocks return to the Locked state after a hardware reset or when the device is powered-down. The status of an unlocked block can be changed to Locked or Locked-Down using the appropriate software commands. A locked block can be unlocked by issuing the Unlock command.

### Lock-Down State

Blocks that are Locked-Down (state (0,1,x))are protected from program and erase operations (as for Locked blocks) but their protection status cannot be changed using software commands alone. A Locked or Unlocked block can be Locked-Down by issuing the Lock-Down command. Locked-Down blocks revert to the Locked state when the device is reset or powered-down.

The Lock-Down function is dependent on the $\overline{WP}$ input pin. When $\overline{WP}$=0 ($V_{IL}$), the blocks in the Lock-Down state (0,1,x) are protected from program, erase and protection status changes. When $\overline{WP}$=1 ($V_{IH}$) the Lock-Down function is disabled (1,1,1) and Locked-Down blocks can be individually unlocked to the (1,1,0) state by issuing the software command, where they can be erased and programmed. These blocks can then be re-locked (1,1,1) and unlocked (1,1,0) as desired while $\overline{WP}$ remains High. When $\overline{WP}$ is low, blocks that were previously Locked-Down return to the Lock-Down state (0,1,x) regardless of any changes made while $\overline{WP}$ was High. Device reset or power-down resets all blocks, including those in Lock-Down, to the Locked state.

### Locking Operations During Erase Suspend

Changes to block lock status can be performed during an erase suspend by using the standard locking command sequences to unlock, lock or lock-down a block. This is useful in the case when another block needs to be updated while an erase operation is in progress.

To change block locking during an erase operation, first write the Erase Suspend command, then check the status register until it indicates that the erase operation has been suspended. Next write the desired Lock command sequence to a block and the lock status will be changed. After completing any desired lock, read, or program operations, resume the erase operation with the Erase Resume command.

If a block is locked or locked-down during an erase suspend of the same block, the locking status bits will be changed immediately, but when the erase is resumed, the erase operation will complete.

**Table 10. Lock Status**

| Current Protection Status(1) ($\overline{WP}$, DQ1, DQ0) | | Next Protection Status(1) ($\overline{WP}$, DQ1, DQ0) | | | |
|---|---|---|---|---|---|
| **Current State** | **Program/Erase Allowed** | **After Block Lock Command** | **After Block Unlock Command** | **After Block Lock-Down Command** | **After $\overline{WP}$ transition** |
| 1,0,0 | yes | 1,0,1 | 1,0,0 | 1,1,1 | 0,0,0 |
| 1,0,1(2) | no | 1,0,1 | 1,0,0 | 1,1,1 | 0,0,1 |
| 1,1,0 | yes | 1,1,1 | 1,1,0 | 1,1,1 | 0,1,1 |
| 1,1,1 | no | 1,1,1 | 1,1,0 | 1,1,1 | 0,1,1 |
| 0,0,0 | yes | 0,0,1 | 0,0,0 | 0,1,1 | 1,0,0 |
| 0,0,1(2) | no | 0,0,1 | 0,0,0 | 0,1,1 | 1,0,1 |
| 0,1,1 | no | 0,1,1 | 0,1,1 | 0,1,1 | 1,1,1 or 1,1,0 (3) |

Note: 1. The lock status is defined by the write protect pin and by DQ1 ('1' for a locked-down block) and DQ0 ('1' for a locked block) as read in the Auto Select command with A1 = $V_{IH}$ and A0 = $V_{IL}$.
2. All blocks are locked at power-up, so the default configuration is 001 or 101 according to $\overline{WP}$ status.
3. A $\overline{WP}$ transition to $V_{IH}$ on a locked block will restore the previous DQ0 value, giving a 111 or 110.

## STATUS REGISTER

The Status Register provides information on the current or previous Program or Erase operations. Bus Read operations from any address within the bank, always read the Status Register during Program and Erase operations.

The various bits convey information about the status and any errors of the operation.

The bits in the Status Register are summarized in Table 12, Status Register Bits. Refer to Tables 11 and 12 in conjunction with the following text descriptions.

**Data Polling Bit (DQ7).** When Program operations are in progress, the Data Polling bit outputs the complement of the bit being programmed on DQ7. For a Double Word Program operation, it is the complement of DQ7 for the last Word written to the Command Interface.

During an Erase operation, it outputs a '0'. After completion of the operation, DQ7 will output the bit last programmed or a '1' after erasing.

Data Polling is valid and only effective during P/E.C. operation, that is after the fourth $\overline{W}$ pulse for programming or after the sixth $\overline{W}$ pulse for erase. It must be performed at the address being programmed or at an address within the block being erased. See Figure 21 for the Data Polling flowchart and Figure 12 for the Data Polling waveforms.

DQ7 will also flag an Erase Suspend by switching from '0' to '1' at the start of the Erase Suspend. In order to monitor DQ7 in the Erase Suspend mode an address within a block being erased must be provided. DQ7 will output '1' if the read is attempted on a block being erased and the data value on other blocks. During a program operation in Erase Suspend, DQ7 will have the same behavior as in the normal program.

**Toggle Bit (DQ6).** When Program or Erase operations are in progress, successive attempts to read DQ6 will output complementary data. DQ6 will toggle following the toggling of either $\overline{G}$ or $\overline{E}$. The operation is completed when two successive reads give the same output data. The next read will output the bit last programmed or a '1' after erasing.

The Toggle Bit DQ6 is valid only during P/E.C. operations, that is after the fourth $\overline{W}$ pulse for programming or after the sixth $\overline{W}$ pulse for Erase. DQ6 will be set to '1' if a read operation is attempted on an Erase Suspend block. When erase is suspended DQ6 will toggle during programming operations in a block different from the block in Erase Suspend.

See Figure 15 for Toggle Bit flowchart and Figure 13 for Toggle Bit waveforms.

**Toggle Bit (DQ2).** Toggle Bit DQ2, together with DQ6, can be used to determine the device status during erase operations.

During Erase Suspend a read from a block being erased will cause DQ2 to toggle. A read from a block not being erased will output data. DQ2 will be set to '1' during program operation and to '0' in erase operation. If a read operation is addressed to a block where an erase error has occurred, DQ2 will toggle.

**Error Bit (DQ5).** The Error Bit can be used to identify if an error occurs during a program or erase operation.

The Error Bit is set to '1' when a program or erase operation has failed. When it is set to '0' the program or erase operation was successful.

If any Program command is used to try to set a bit from '0' to '1' Status Register Error bit DQ5 will be set to '1', only if $V_{PP}$ is in the range of 11.4V to 12.6V.

The Error Bit is reset by a Read/Reset command.

**Erase Timer Bit (DQ3).** The Erase Timer bit is used to indicate the timeout period for an erase operation.

When the last block Erase command has been entered to the Command Interface and it is waiting for the erase operation to start, the Erase Timer Bit is set to '0'. When the erase timeout period is finished, DQ3 returns to '1', (80µs to 120µs).

**DQ0, DQ1 and DQ4** are reserved for future use and should be masked.

**Table 11. Polling and Toggle Bits**

| Mode | DQ7 | DQ6 | DQ2 |
|---|---|---|---|
| Program | $\overline{DQ7}$ | Toggle | 1 |
| Erase | 0 | Toggle | N/A |
| Erase Suspend Read (in Erase Suspend block) | 1 | 1 | Toggle |
| Erase Suspend Read (outside Erase Suspend block) | DQ7 | DQ6 | DQ2 |
| Erase Suspend Program | $\overline{DQ7}$ | Toggle | 1 |

**Table 12. Status Register Bits**

| DQ | Name | Logic Level | Definition | Note |
|---|---|---|---|---|
| 7 | Data Polling | '1' | Erase complete or erase block in Erase Suspend. | Indicates the P/E.C. status, check during Program or Erase, and on completion before checking bits DQ5 for Program or Erase success. |
| | | '0' | Erase in progress | |
| | | DQ | Program complete or data of non erase block during Erase Suspend. | |
| | | $\overline{DQ}$ | Program in progress(2) | |
| 6 | Toggle Bit | '-1-0-1-0-1-0-1-' | Erase or Program in progress | Successive reads output complementary data on DQ6 while Programming or Erase operations are in progress. DQ6 remains at constant level when P/E.C. operations are completed or Erase Suspend is acknowledged. |
| | | DQ | Program complete | |
| | | '-1-1-1-1-1-1-1-' | Erase complete or Erase Suspend on currently addressed block | |
| 5 | Error Bit | '1' | Program or Erase Error | This bit is set to '1' in the case of Programming or Erase failure. |
| | | '0' | Program or Erase in progress | |
| 4 | Reserved | | | |
| 3 | Erase Time Bit | '1' | Erase Timeout Period Expired | P/E.C. Erase operation has started. Only possible command entry is Erase Suspend |
| | | '0' | Erase Timeout Period in progress | An additional block to be erased in parallel can be entered to the P/E.C provided that it belongs to the same bank |
| 2 | Toggle Bit | '-1-0-1-0-1-0-1-' | Erase Suspend read in the Erase Suspended Block. Erase Error due to the currently addressed block (when DQ5 = '1'). | Indicates the erase status and allows to identify the erased block. |
| | | 1 | Program in progress or Erase complete. | |
| | | DQ | Erase Suspend read on non Erase Suspend block. | |
| 1 | Reserved | | | |
| 0 | Reserved | | | |

Note: 1. Logic level '1' is High, '0' is Low. -0-1-0-0-0-1-1-1-0- represent bit value in successive read operations.
2. In case of double word program $\overline{DQ7}$ refers to the last word input.

## MAXIMUM RATING

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

**Table 13. Absolute Maximum Ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $T_A$ | Ambient Operating Temperature (1) | –40 to 85 | °C |
| $T_{BIAS}$ | Temperature Under Bias | –40 to 125 | °C |
| $T_{STG}$ | Storage Temperature | –55 to 155 | °C |
| $V_{IO}$ (2) | Input or Output Voltage | –0.5 to $V_{DDQ}$+0.5 | V |
| $V_{DD}$, $V_{DDQ}$ | Supply Voltage | –0.5 to 2.7 | V |
| $V_{PP}$ | Program Voltage | –0.5 to 13 | V |

Note: 1. Depends on range.
2. Minimum Voltage may undershoot to –2V during transition and for less than 20ns.

## DC AND AC PARAMETERS

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement Conditions summarized in Table 14, Operating and AC Measurement Conditions. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

**Table 14. Operating and AC Measurement Conditions**

| Parameter | M59DR032EA, M59DR032EB | | | | | | Units |
|---|---|---|---|---|---|---|---|
| | 85 | | 100 | | 120 | | |
| | Min | Max | Min | Max | Min | Max | |
| $V_{DD}$ Supply Voltage | 1.8 | 2.2 | 1.65 | 2.2 | 1.65 | 2.2 | V |
| $V_{DDQ}$ Supply Voltage | 1.8 | 2.2 | 1.65 | 2.2 | 1.65 | 2.2 | V |
| $V_{PP}$ Supply Voltage | 11.4 | 12.6 | 11.4 | 12.6 | 11.4 | 12.6 | V |
| Ambient Operating Temperature | – 40 | 85 | – 40 | 85 | – 40 | 85 | °C |
| Load Capacitance ($C_L$) | 30 | | 30 | | 30 | | pF |
| Input Rise and Fall Times | | 4 | | 4 | | 4 | ns |
| Input Pulse Voltages | 0 to $V_{DDQ}$ | | 0 to $V_{DDQ}$ | | 0 to $V_{DDQ}$ | | V |
| Input and Output Timing Ref. Voltages | $V_{DDQ}/2$ | | $V_{DDQ}/2$ | | $V_{DDQ}/2$ | | V |

**Figure 5. Testing Input/Output Waveforms**

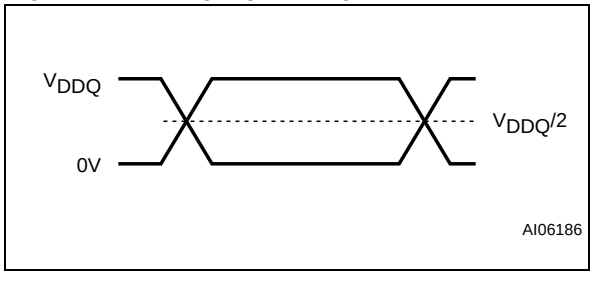



**Figure 6. AC Testing Load Circuit**

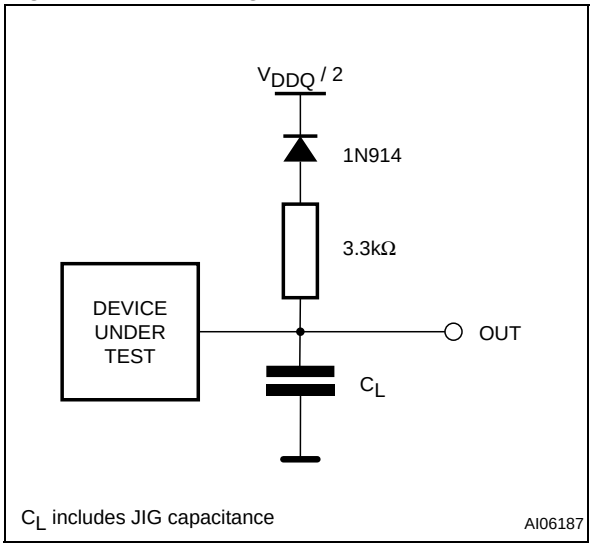



**Table 15. Capacitance**

| Symbol | Parameter | Test Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | | 6 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0V | | 12 | pF |

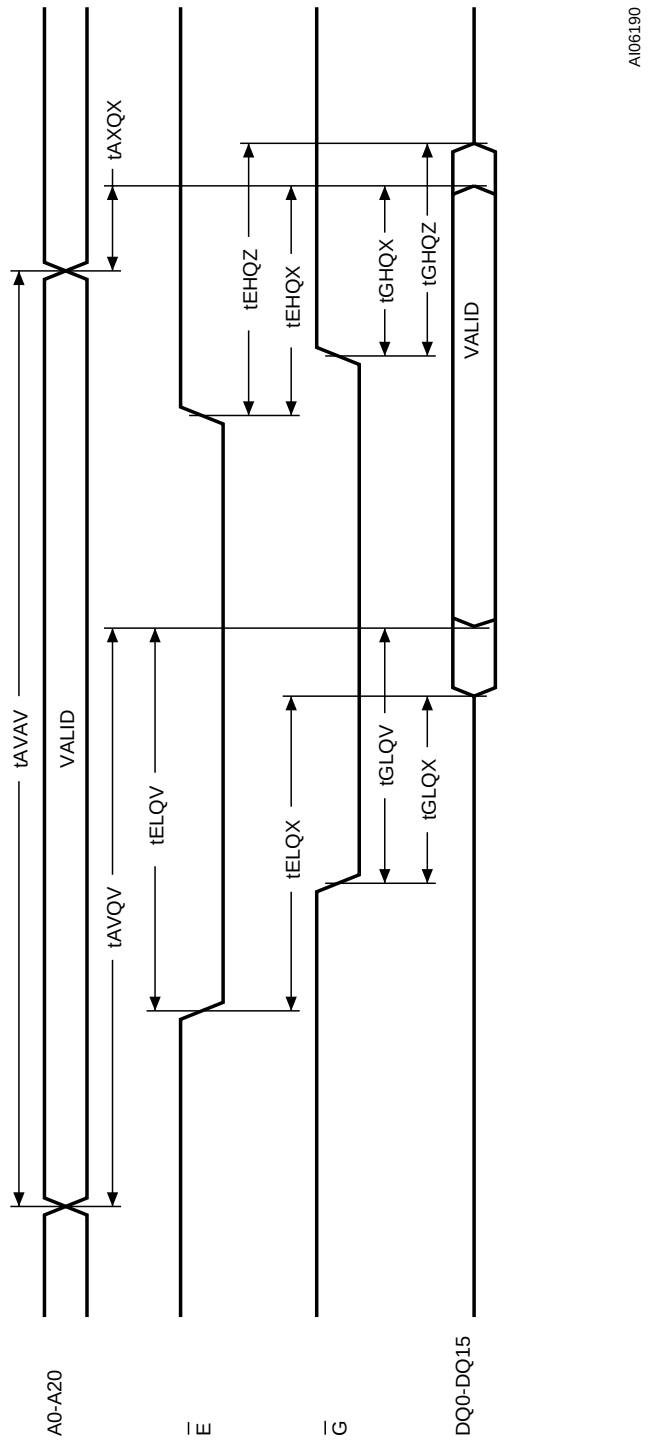
Note: Sampled only, not 100% tested.

**Table 16. DC Characteristics**

| Symbol | Parameter | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Leakage Current | $0V \le V_{IN} \le V_{DD}$ | | | ±1 | µA |
| $I_{LO}$ | Output Leakage Current | $0V \le V_{OUT} \le V_{DD}$ | | | ±5 | µA |
| $I_{CC1}$ | Supply Current (Read Mode) | $\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$, f = 6MHz | | 3 | 6 | mA |
| $I_{CC2}$ | Supply Current (Power-Down) | $\overline{RP} = V_{SS} \pm 0.2V$ | | 2 | 10 | µA |
| $I_{CC3}$ | Supply Current (Standby) | $\overline{E} = V_{DD} \pm 0.2V$ | | 10 | 50 | µA |
| $I_{CC4}$ (1) | Supply Current (Program or Erase) | Word Program, Block Erase in progress | | 10 | 20 | mA |
| $I_{CC5}$ (1) | Supply Current (Dual Bank) | Program/Erase in progress in one Bank, Read in the other Bank | | 13 | 26 | mA |
| $I_{PP1}$ | $V_{PP}$ Supply Current (Program or Erase) | $V_{PP} = 12V \pm 0.6V$ | | 2 | 5 | mA |
| $I_{PP2}$ | $V_{PP}$ Supply Current (Standby or Read) | $V_{PP} \le V_{DD}$ | | 0.2 | 5 | µA |
| | | $V_{PP} = 12V \pm 0.6V$ | | 100 | 400 | µA |
| $V_{IL}$ | Input Low Voltage | | –0.5 | | 0.4 | V |
| $V_{IH}$ | Input High Voltage | | $V_{DDQ}$ –0.4 | | $V_{DDQ}$ + 0.4 | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 100µA | | | 0.1 | V |
| $V_{OH}$ | Output High Voltage CMOS | $I_{OH}$ = –100µA | $V_{DDQ}$ –0.1 | | | V |
| $V_{PP}$ (2,3) | $V_{PP}$ Supply Voltage (Program or Erase) | | –0.4 | | $V_{DD}$ + 0.4 | V |
| | | Double Word Program | 11.4 | | 12.6 | V |

Note: 1. Sampled only, not 100% tested.
2. $V_{PP}$ may be connected to 12V power supply for a total of less than 100 hrs.
3. For standard program/erase operation $V_{PP}$ is don't care.

**Figure 7. Random Read AC Waveforms**




**Note:** Write Enable ($\overline{W}$) = High.

**Figure 8. Page Read AC Waveforms**

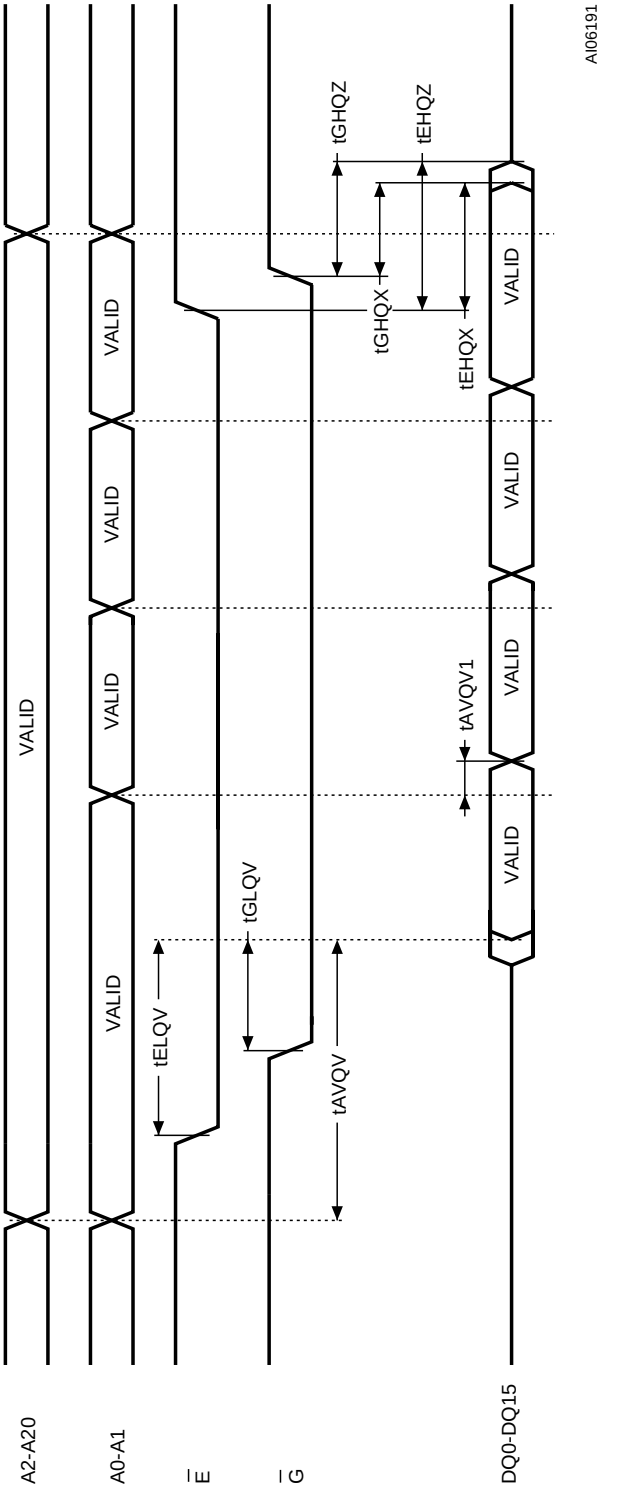
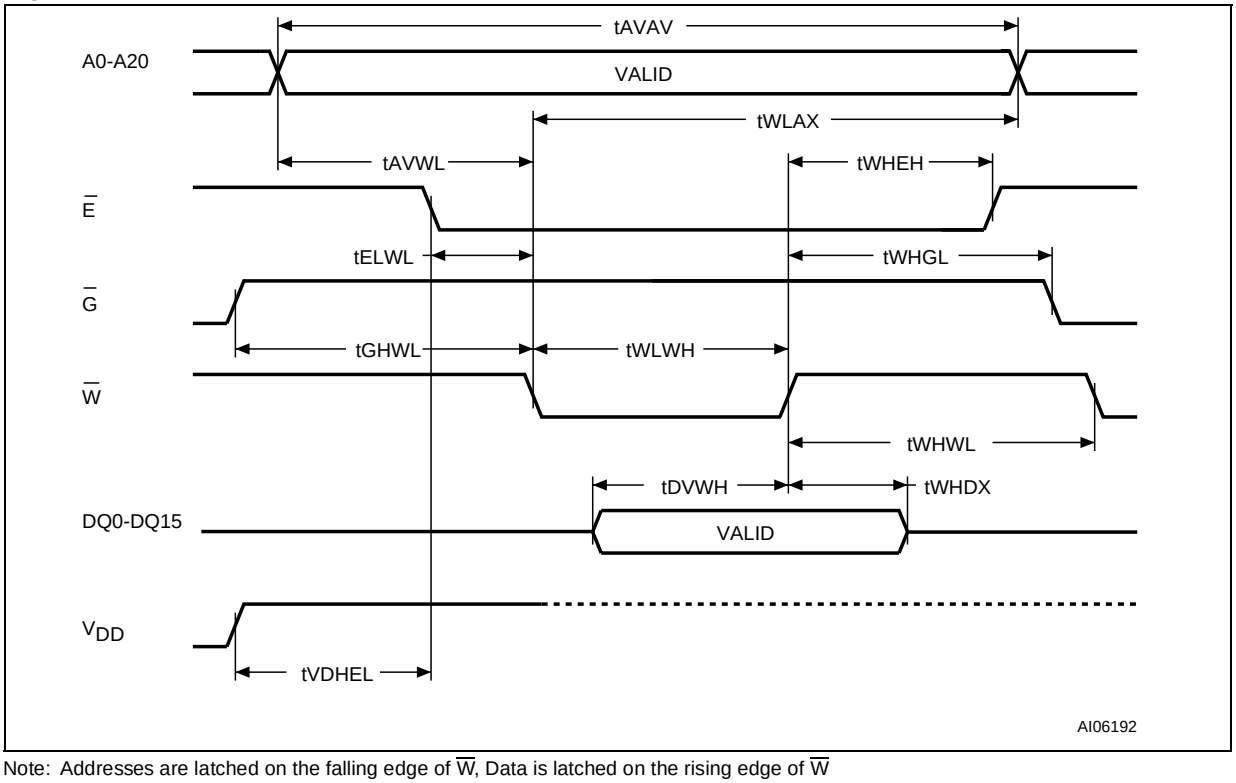


**Table 17. Read AC Characteristics**

| Symbol | Alt | Parameter | Test Condition | M59DR032E | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 85 | | 100 | | 120 | | |
| | | | | Min | Max | Min | Max | Min | Max | |
| $t_{AVAV}$ | $t_{RC}$ | Address Valid to Next Address Valid | $\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$ | 85 | | 100 | | 120 | | ns |
| $t_{AVQV}$ | $t_{ACC}$ | Address Valid to Output Valid (Random) | $\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$ | | 85 | | 100 | | 120 | ns |
| $t_{AVQV1}$ | $t_{PAGE}$ | Address Valid to Output Valid (Page) | $\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$ | | 30 | | 35 | | 45 | ns |
| $t_{ELQX}$ (1) | $t_{LZ}$ | Chip Enable Low to Output Transition | $\overline{G} = V_{IL}$ | 0 | | 0 | | 0 | | ns |
| $t_{ELQV}$ (2) | $t_{CE}$ | Chip Enable Low to Output Valid | $\overline{G} = V_{IL}$ | | 85 | | 100 | | 120 | ns |
| $t_{GLQX}$ (1) | $t_{OLZ}$ | Output Enable Low to Output Transition | $\overline{E} = V_{IL}$ | 0 | | 0 | | 0 | | ns |
| $t_{GLQV}$ (2) | $t_{OE}$ | Output Enable Low to Output Valid | $\overline{E} = V_{IL}$ | | 25 | | 25 | | 35 | ns |
| $t_{EHQX}$ | $t_{OH}$ | Chip Enable High to Output Transition | $\overline{G} = V_{IL}$ | 0 | | 0 | | 0 | | ns |
| $t_{EHQZ}$ (1) | $t_{HZ}$ | Chip Enable High to Output Hi-Z | $\overline{G} = V_{IL}$ | | 20 | | 25 | | 35 | ns |
| $t_{GHQX}$ | $t_{OH}$ | Output Enable High to Output Transition | $\overline{E} = V_{IL}$ | 0 | | 0 | | 0 | | ns |
| $t_{GHQZ}$ (1) | $t_{DF}$ | Output Enable High to Output Hi-Z | $\overline{E} = V_{IL}$ | | 20 | | 25 | | 35 | ns |
| $t_{AXQX}$ | $t_{OH}$ | Address Transition to Output Transition | $\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$ | 0 | | 0 | | 0 | | ns |

Note: 1. Sampled only, not 100% tested.
2. $\overline{G}$ may be delayed by up to $t_{ELQV} - t_{GLQV}$ after the falling edge of $\overline{E}$ without increasing $t_{ELQV}$.

**Figure 9. Write AC Waveforms, Write Enable Controlled**

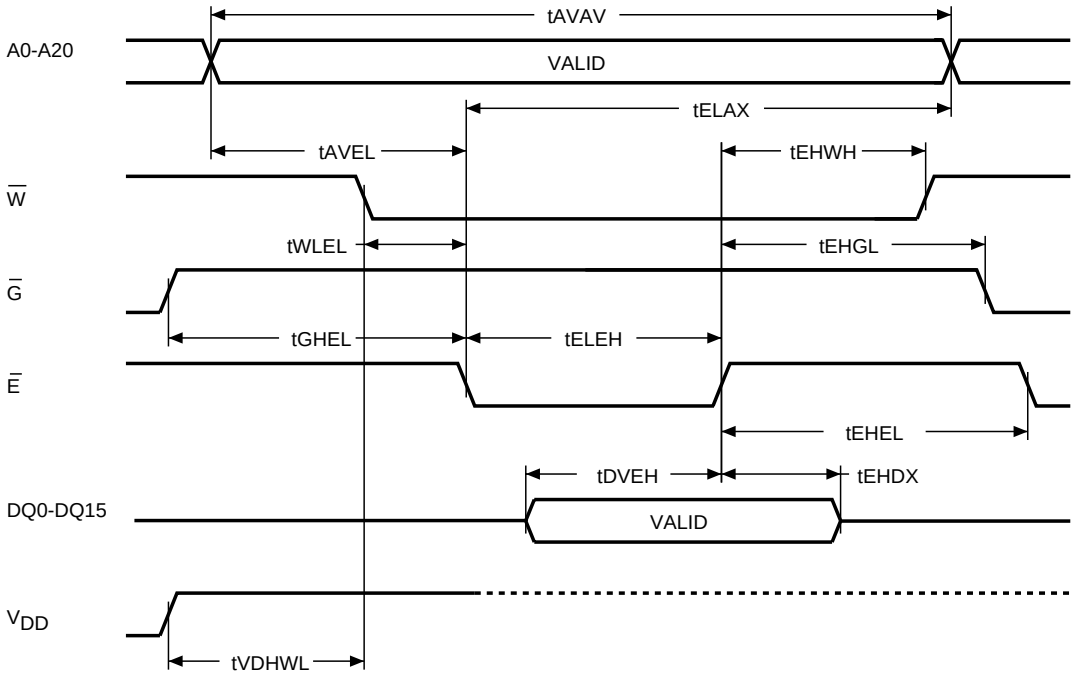



Note: Addresses are latched on the falling edge of $\overline{W}$, Data is latched on the rising edge of $\overline{W}$

**Table 18. Write AC Characteristics, Write Enable Controlled**

| Symbol | Alt | Parameter | M59DR032E | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | 85 | | 100 | | 120 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{AVAV}$ | $t_{WC}$ | Address Valid to Next Address Valid | 85 | | 100 | | 120 | | ns |
| $t_{ELWL}$ | $t_{CS}$ | Chip Enable Low to Write Enable Low | 0 | | 0 | | 0 | | ns |
| $t_{WLWH}$ | $t_{WP}$ | Write Enable Low to Write Enable High | 50 | | 50 | | 50 | | ns |
| $t_{DVWH}$ | $t_{DS}$ | Input Valid to Write Enable High | 40 | | 50 | | 50 | | ns |
| $t_{WHDX}$ | $t_{DH}$ | Write Enable High to Input Transition | 0 | | 0 | | 0 | | ns |
| $t_{WHEH}$ | $t_{CH}$ | Write Enable High to Chip Enable High | 0 | | 0 | | 0 | | ns |
| $t_{WHWL}$ | $t_{WPH}$ | Write Enable High to Write Enable Low | 30 | | 30 | | 30 | | ns |
| $t_{AVWL}$ | $t_{AS}$ | Address Valid to Write Enable Low | 0 | | 0 | | 0 | | ns |
| $t_{WLAX}$ | $t_{AH}$ | Write Enable Low to Address Transition | 50 | | 50 | | 50 | | ns |
| $t_{GHWL}$ | | Output Enable High to Write Enable Low | 0 | | 0 | | 0 | | ns |
| $t_{VDHEL}$ | $t_{VCS}$ | $V_{DD}$ High to Chip Enable Low | 50 | | 50 | | 50 | | µs |
| $t_{WHGL}$ | $t_{OEH}$ | Write Enable High to Output Enable Low | 30 | | 30 | | 30 | | ns |
| $t_{PLQ7V}$ | | $\overline{RP}$ Low to Reset Complete During Program/Erase | | 15 | | 15 | | 15 | µs |

**Figure 10. Write AC Waveforms, Chip Enable Controlled**




Note: Addresses are latched on the falling edge of $\overline{E}$, Data is latched on the rising edge of $\overline{E}$.

**Table 19. Write AC Characteristics, Chip Enable Controlled**

| Symbol | Alt | Parameter | M59DR032E | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | 85 | | 100 | | 120 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{AVAV}$ | $t_{WC}$ | Address Valid to Next Address Valid | 85 | | 100 | | 120 | | ns |
| $t_{WLEL}$ | $t_{WS}$ | Write Enable Low to Chip Enable Low | 0 | | 0 | | 0 | | ns |
| $t_{ELEH}$ | $t_{CP}$ | Chip Enable Low to Chip Enable High | 50 | | 50 | | 50 | | ns |
| $t_{DVEH}$ | $t_{DS}$ | Input Valid to Chip Enable High | 40 | | 50 | | 50 | | ns |
| $t_{EHDX}$ | $t_{DH}$ | Chip Enable High to Input Transition | 0 | | 0 | | 0 | | ns |
| $t_{EHWH}$ | $t_{WH}$ | Chip Enable High to Write Enable High | 0 | | 0 | | 0 | | ns |
| $t_{EHEL}$ | $t_{CPH}$ | Chip Enable High to Chip Enable Low | 30 | | 30 | | 30 | | ns |
| $t_{AVEL}$ | $t_{AS}$ | Address Valid to Chip Enable Low | 0 | | 0 | | 0 | | ns |
| $t_{ELAX}$ | $t_{AH}$ | Chip Enable Low to Address Transition | 50 | | 50 | | 50 | | ns |
| $t_{GHEL}$ | | Output Enable High Chip Enable Low | 0 | | 0 | | 0 | | ns |
| $t_{VDHWL}$ | $t_{VCS}$ | $V_{DD}$ High to Write Enable Low | 50 | | 50 | | 50 | | µs |
| $t_{EHGL}$ | $t_{OEH}$ | Chip Enable High to Output Enable Low | 30 | | 30 | | 30 | | ns |
| $t_{PLQ7V}$ | | $\overline{RP}$ Low to Reset Complete During Program/Erase | | 15 | | 15 | | 15 | µs |

**Figure 11. Reset/Power-Down AC Waveform**

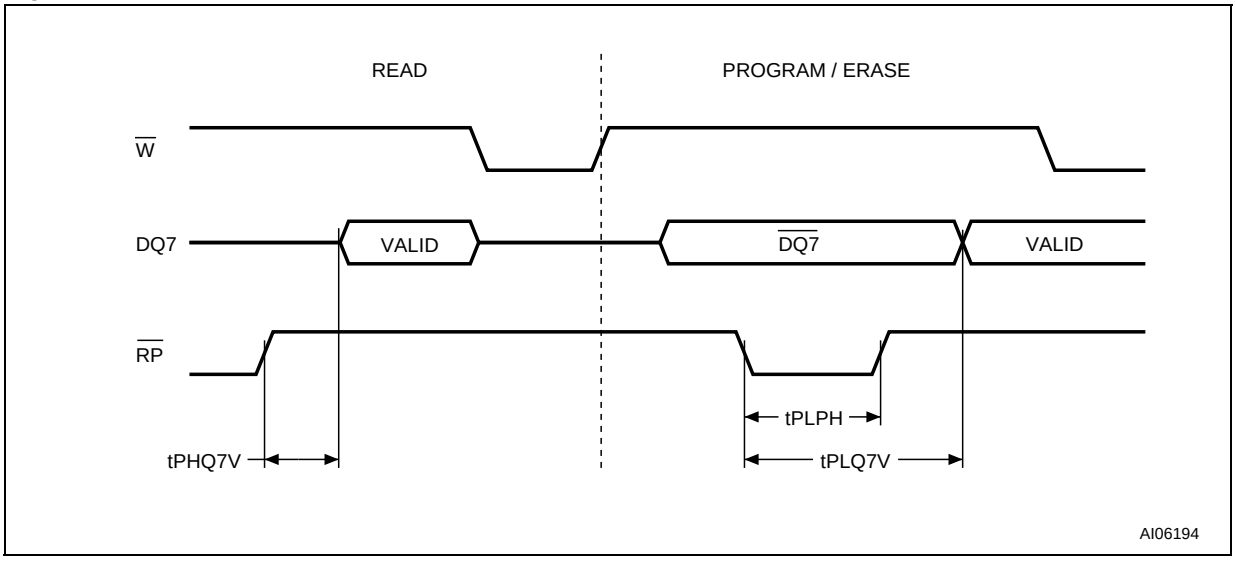



**Table 20. Reset/Power-Down AC Characteristics**

| Symbol | Alt | Parameter | Test Condition | M59DR032E | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 85 | | 100 | | 120 | | |
| | | | | Min | Max | Min | Max | Min | Max | |
| $t_{PHQ7V1}$ | | $\overline{RP}$ High to Data Valid (Read Mode) | | | 150 | | 150 | | 150 | ns |
| $t_{PHQ7V2}$ | | $\overline{RP}$ High to Data Valid (Power-Down enabled) | | | 50 | | 50 | | 50 | µs |
| $t_{PLQ7V}$ | | $\overline{RP}$ Low to Reset Complete | During Program | | 10 | | 10 | | 10 | µs |
| | | | During Erase | | 20 | | 20 | | 20 | µs |
| $t_{PLPH}$ | $t_{RP}$ | $\overline{RP}$ Pulse Width | | 50 | | 50 | | 50 | | ns |

**Figure 12. Data Polling DQ7 AC Waveforms**

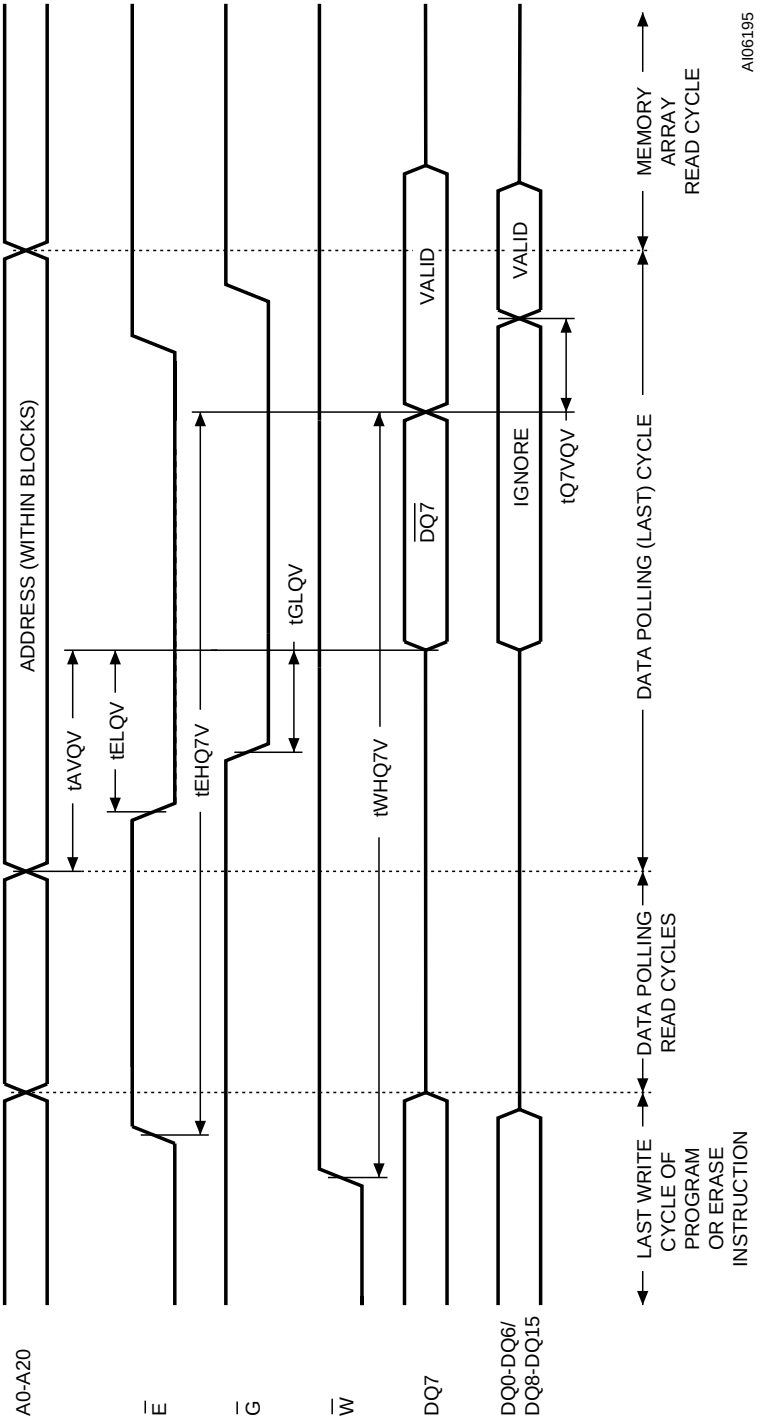
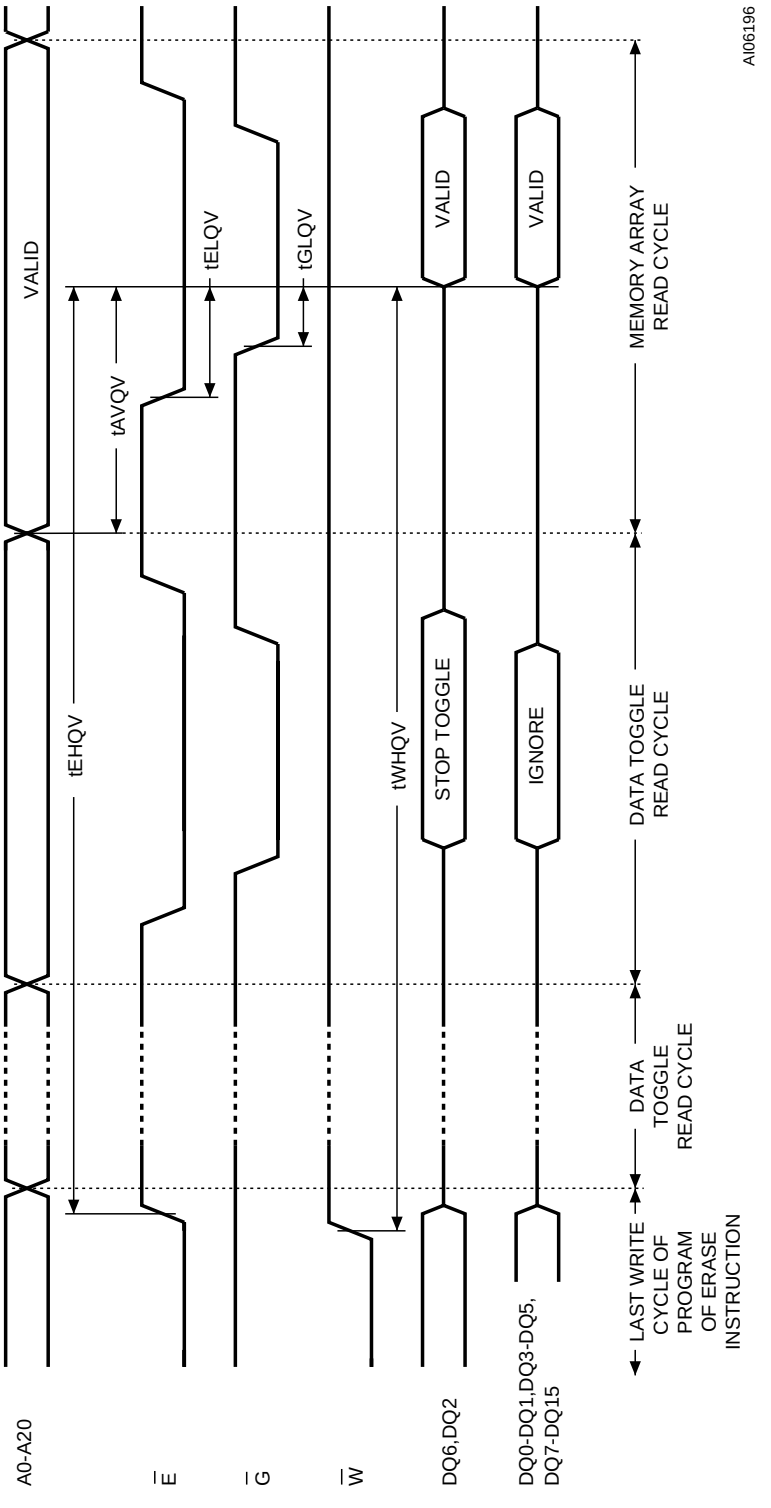


**Figure 13. Data Toggle DQ6, DQ2 AC Waveforms**




Note: All other timings are as a normal Read cycle.

**Table 21. Data Polling and Toggle Bits AC Characteristics**

| Symbol | Parameter | M59DR032E | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| $t_{WHQ7V}$ | Write Enable High to DQ7 Valid (Program, $\overline{W}$ Controlled) | 8 | 100 | µs |
| | Write Enable High to DQ7 Valid (Block Erase, $\overline{W}$ Controlled) | 0.8 | 4 | s |
| $t_{EHQ7V}$ | Chip Enable High to DQ7 Valid (Program, $\overline{E}$ Controlled) | 8 | 100 | µs |
| | Chip Enable High to DQ7 Valid (Block Erase, $\overline{E}$ Controlled) | 0.8 | 4 | s |
| $t_{Q7VQV}$ | Q7 Valid to Output Valid (Data Polling) | | 0 | ns |
| $t_{WHQV}$ | Write Enable High to Output Valid (Program) | 8 | 100 | µs |
| | Write Enable High to Output Valid (Block Erase) | 0.8 | 4 | s |
| $t_{EHQV}$ | Chip Enable High to Output Valid (Program) | 8 | 100 | µs |
| | Chip Enable High to Output Valid (Block Erase) | 0.8 | 4 | s |

Note: All other timings are defined in Read AC Characteristics

**Figure 14. Data Polling Flowchart**

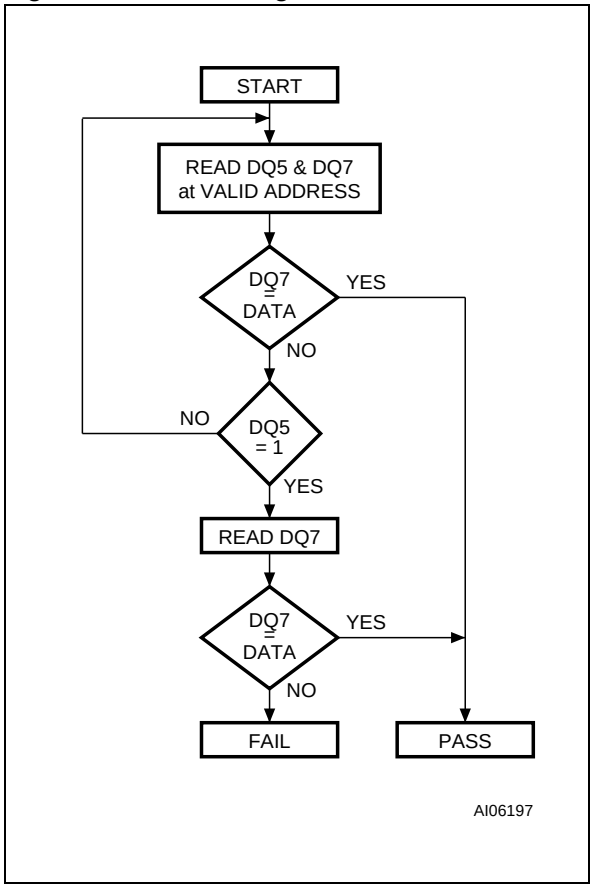
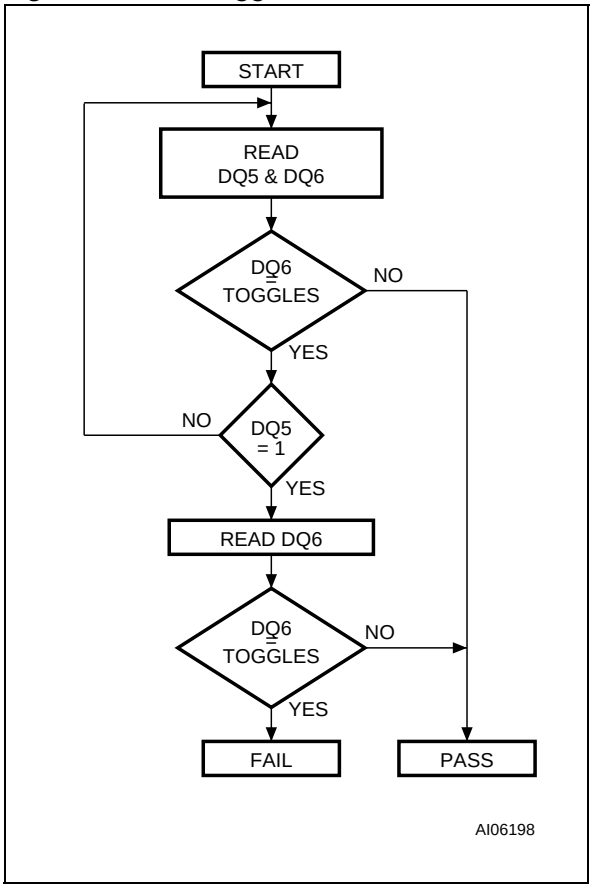
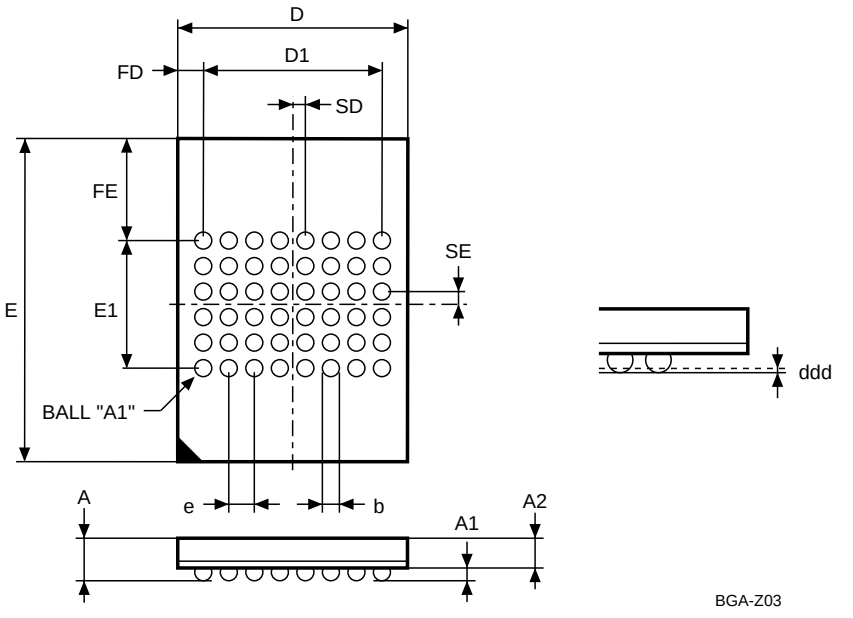



**Figure 15. Data Toggle Flowchart**



## PACKAGE MECHANICAL

**Figure 16. TFBGA48 7x12mm - 8x6 ball array, 0.75 mm pitch, Package Outline**

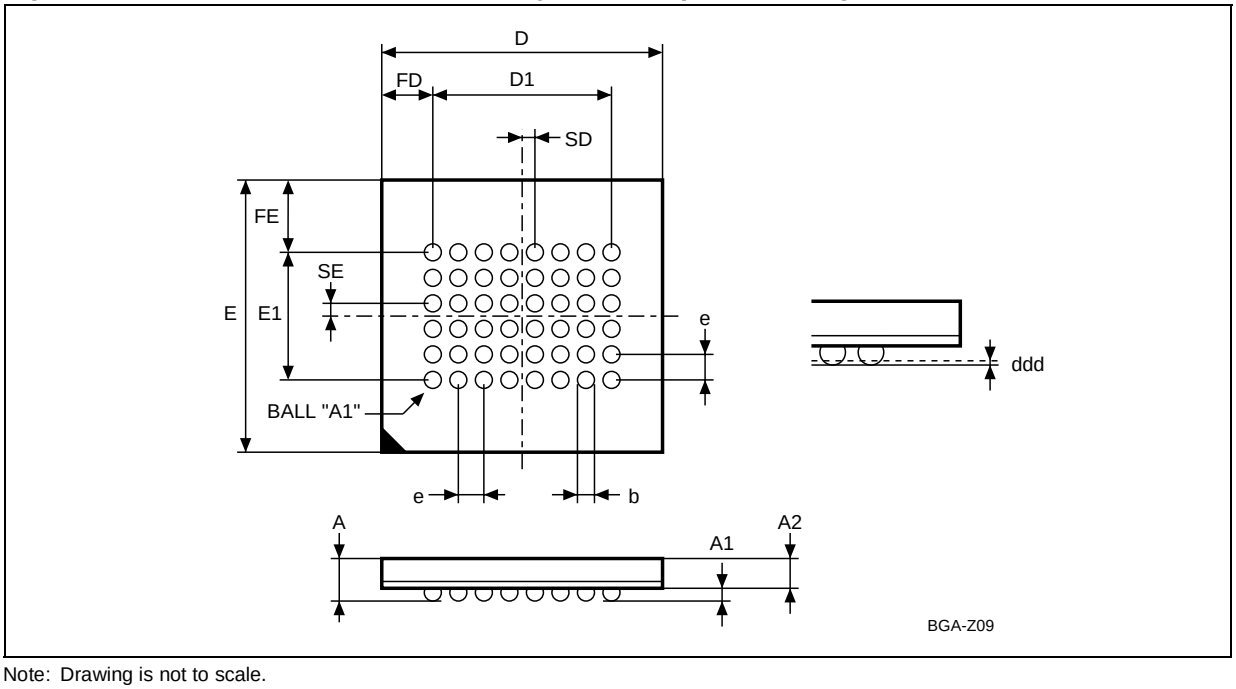



Note: Drawing is not to scale.

**Table 22. TFBGA48 7x12mm - 8x6 ball array, 0.75 mm pitch, Package Mechanical Data**

| Symbol | millimeters | | | inches | | |
|---|---|---|---|---|---|---|
| | Typ | Min | Max | Typ | Min | Max |
| A | | | 1.350 | | | 0.0531 |
| A1 | 0.300 | 0.200 | 0.350 | 0.0118 | 0.0079 | 0.0138 |
| A2 | | | 1.000 | | | 0.0394 |
| b | | 0.300 | 0.550 | | 0.0118 | 0.0217 |
| D | 7.000 | 6.900 | 7.100 | 0.2756 | 0.2717 | 0.2795 |
| D1 | 5.250 | – | – | 0.2067 | – | – |
| ddd | | | 0.100 | | | 0.0039 |
| E | 12.000 | 11.900 | 12.100 | 0.4724 | 0.4685 | 0.4764 |
| E1 | 3.750 | – | – | 0.1476 | – | – |
| e | 0.750 | – | – | 0.0295 | – | – |
| SD | 0.375 | – | – | 0.0148 | – | – |
| SE | 0.375 | – | – | 0.0148 | – | – |
| FE | 4.125 | – | – | 0.1624 | – | – |
| FD | 0.875 | – | – | 0.0344 | – | – |

**Figure 17. TFBGA48 7x7mm - 8x6 ball array, 0.75 mm pitch, Package Outline**




Note: Drawing is not to scale.

**Table 23. TFBGA48 7x7mm - 8x6 ball array, 0.75 mm pitch, Package Mechanical Data**

| Symbol | millimeters | | | inches | | |
|---|---|---|---|---|---|---|
| | Typ | Min | Max | Typ | Min | Max |
| A | | | 1.200 | | | 0.0472 |
| A1 | | 0.200 | | | 0.0079 | |
| A2 | 0.800 | | | 0.0315 | | |
| b | 0.400 | 0.350 | 0.450 | 0.0157 | 0.0138 | 0.0177 |
| D | 7.000 | 6.900 | 7.100 | 0.2756 | 0.2717 | 0.2795 |
| D1 | 5.250 | – | – | 0.2067 | – | – |
| ddd | | | 0.100 | | | 0.0039 |
| E | 7.000 | 6.900 | 7.100 | 0.2756 | 0.2717 | 0.2795 |
| E1 | 3.750 | – | – | 0.1476 | – | – |
| e | 0.750 | – | – | 0.0295 | – | – |
| FD | 0.875 | – | – | 0.0344 | – | – |
| FE | 1.625 | – | – | 0.0640 | – | – |
| SD | 0.375 | – | – | 0.0148 | – | – |
| SE | 0.375 | – | – | 0.0148 | – | – |

**Figure 18. TFBGA48 Daisy Chain - Package Connections (Top view through package)**

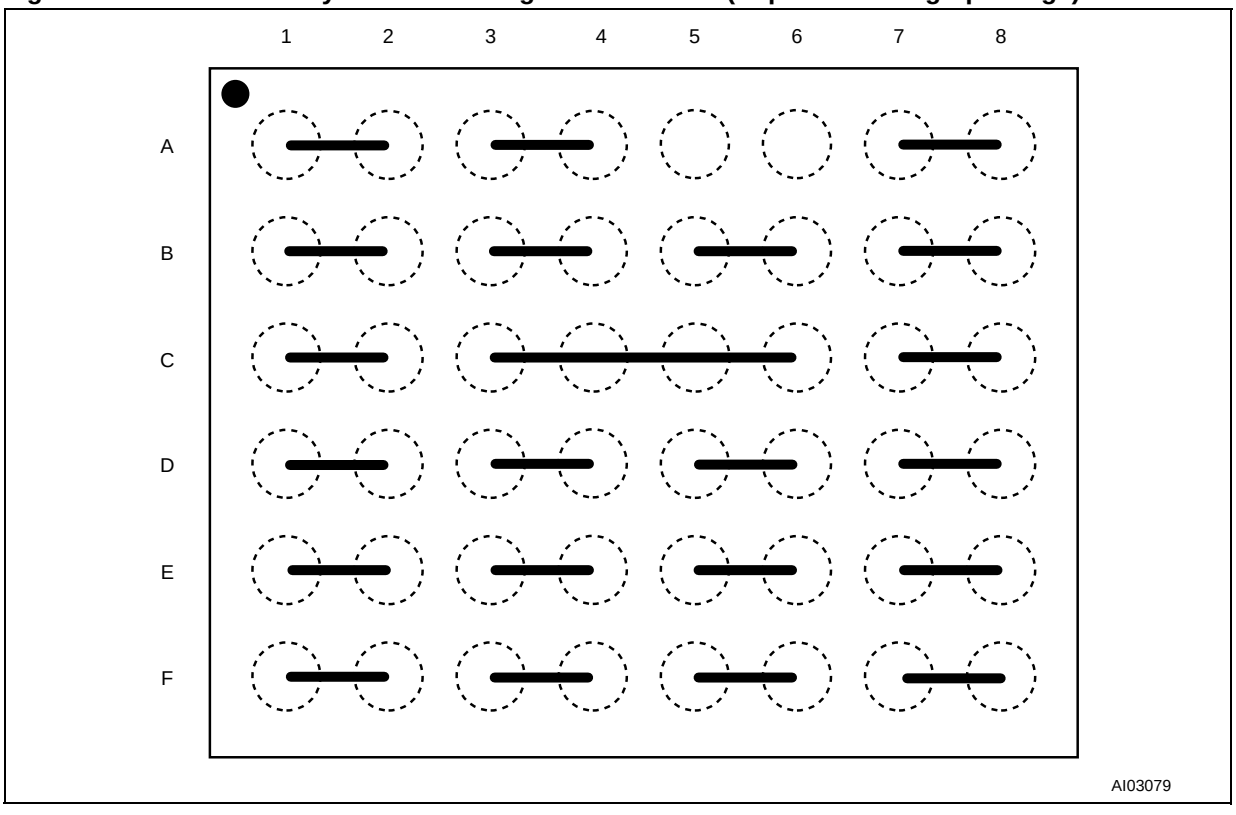
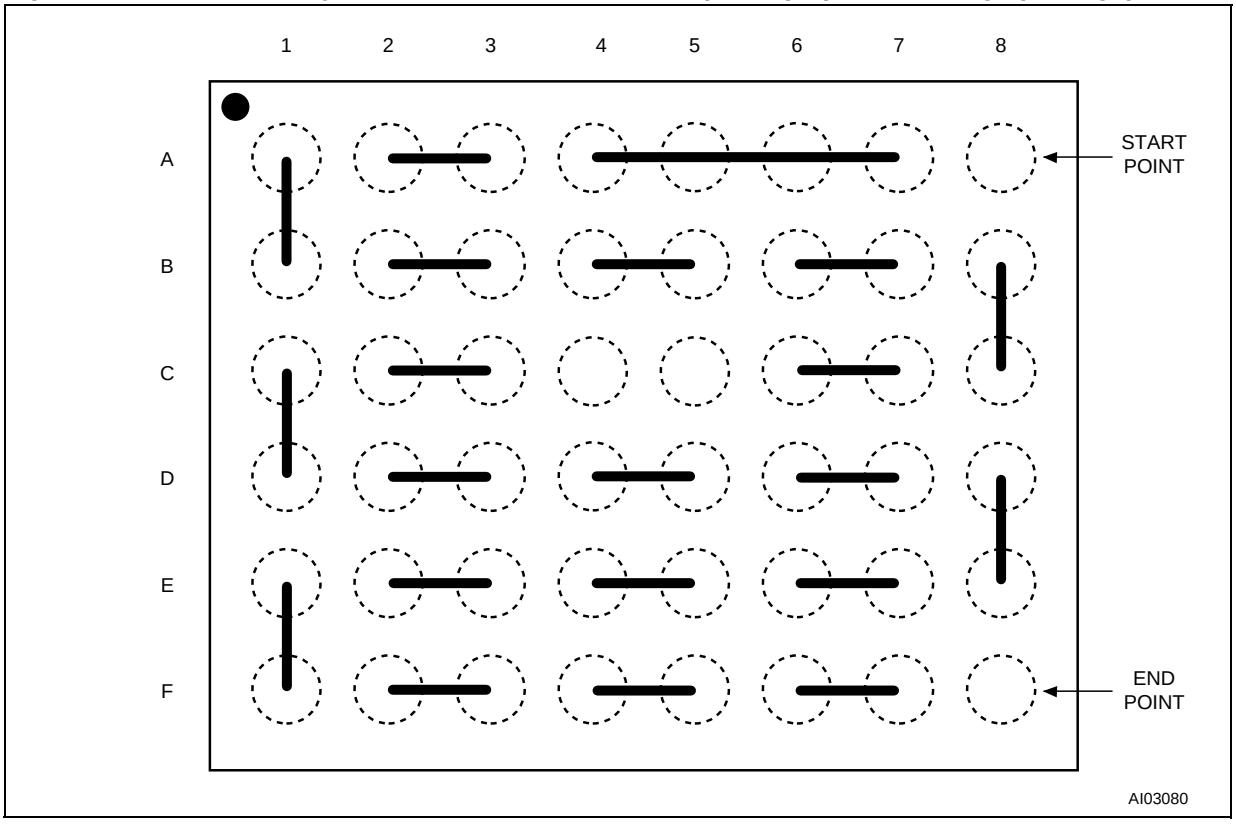



**Figure 19. TFBGA48 Daisy Chain - PCB Connection Proposal (Top view through package)**



## PART NUMBERING

### Table 24. Ordering Information Scheme

Example: M59DR032EA 10 ZB 6 T

**Device Type**
M59

**Architecture**
D = Dual Bank, Page Mode

**Operating Voltage**
R = 1.8V

**Device Function**
032EA = 32 Mbit (x16), Dual Bank: 1/8-7/8 partitioning, Top Boot
032EB = 32 Mbit (x16), Dual Bank: 1/8-7/8 partitioning, Bottom Boot

**Random Speed**
85 = 85ns
10 = 100ns
12 = 120ns

**Package**
ZB = TFBGA48: 7 x 12mm, 0.75mm pitch
ZF = TFBGA48: 7 x 7mm, 0.75mm pitch

**Temperature Range**
1 = 0 to 70°C
6 = –40 to 85°C

**Option**
blank = Standard Packing
T = Tape & Reel packing
E = Lead-Free Package, Standard Packing
F = Lead-Free Package, Tape & Reel Packing

**Table 25. Daisy Chain Ordering Scheme**

Example: M59DR032E -ZB T

**Device Type**

M59DR032E

**Daisy Chain**

ZB = TFBGA48: 7x12mm, 0.75mm pitch

ZF = TFBGA48: 7 x 7mm, 0.75mm pitch

**Option**

blank = Standard Packing

T = Tape & Reel packing

E = Lead-Free Package, Standard Packing

F = Lead-Free Package, Tape & Reel Packing

Devices are shipped from the factory with the memory content bits erased to '1'. For a list of available options (Speed, Package, etc.) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

## APPENDIX A. BLOCK ADDRESSES

**Table 26. Bank A, Top Boot Block Addresses M59DR032EA**

| # | Size (KWord) | Address Range |
|---|---|---|
| 14 | 4 | 1FF000h-1FFFFFh |
| 13 | 4 | 1FE000h-1FEFFFh |
| 12 | 4 | 1FD000h-1FDFFFh |
| 11 | 4 | 1FC000h-1FCFFFh |
| 10 | 4 | 1FB000h-1FBFFFh |
| 9 | 4 | 1FA000h-1FAFFFh |
| 8 | 4 | 1F9000h-1F9FFFh |
| 7 | 4 | 1F8000h-1F8FFFh |
| 6 | 32 | 1F0000h-1F7FFFh |
| 5 | 32 | 1E8000h-1EFFFFh |
| 4 | 32 | 1E0000h-1E7FFFh |
| 3 | 32 | 1D8000h-1DFFFFh |
| 2 | 32 | 1D0000h-1D7FFFh |
| 1 | 32 | 1C8000h-1CFFFFh |
| 0 | 32 | 1C0000h-1C7FFFh |

**Table 27. Bank B, Top Boot Block Addresses M59DR032EA**

| # | Size (KWord) | Address Range |
|---|---|---|
| 55 | 32 | 1B8000h-1BFFFFh |
| 54 | 32 | 1B0000h-1B7FFFh |
| 53 | 32 | 1A8000h-1AFFFFh |
| 52 | 32 | 1A0000h-1A7FFFh |
| 51 | 32 | 198000h-19FFFFh |
| 50 | 32 | 190000h-197FFFh |
| 49 | 32 | 188000h-18FFFFh |
| 48 | 32 | 180000h-187FFFh |
| 47 | 32 | 178000h-17FFFFh |
| 46 | 32 | 170000h-177FFFh |
| 45 | 32 | 168000h-16FFFFh |
| 44 | 32 | 160000h-167FFFh |
| 43 | 32 | 158000h-15FFFFh |
| 42 | 32 | 150000h-157FFFh |
| 41 | 32 | 148000h-14FFFFh |
| 40 | 32 | 140000h-147FFFh |
| 39 | 32 | 138000h-13FFFFh |
| 38 | 32 | 130000h-137FFFh |
| 37 | 32 | 128000h-12FFFFh |
| 36 | 32 | 120000h-127FFFh |
| 35 | 32 | 118000h-11FFFFh |
| 34 | 32 | 110000h-117FFFh |
| 33 | 32 | 108000h-10FFFFh |
| 32 | 32 | 100000h-107FFFh |
| 31 | 32 | 0F8000h-0FFFFFh |
| 30 | 32 | 0F0000h-0F7FFFh |
| 29 | 32 | 0E8000h-0EFFFFh |
| 28 | 32 | 0E0000h-0E7FFFh |
| 27 | 32 | 0D8000h-0DFFFFh |
| 26 | 32 | 0D0000h-0D7FFFh |
| 25 | 32 | 0C8000h-0CFFFFh |
| 24 | 32 | 0C0000h-0C7FFFh |
| 23 | 32 | 0B8000h-0BFFFFh |
| 22 | 32 | 0B0000h-0B7FFFh |
| 21 | 32 | 0A8000h-0AFFFFh |
| 20 | 32 | 0A0000h-0A7FFFh |
| 19 | 32 | 098000h-09FFFFh |
| 18 | 32 | 090000h-097FFFh |
| 17 | 32 | 088000h-08FFFFh |
| 16 | 32 | 080000h-087FFFh |
| 15 | 32 | 078000h-07FFFFh |
| 14 | 32 | 070000h-077FFFh |
| 13 | 32 | 068000h-06FFFFh |
| 12 | 32 | 060000h-067FFFh |
| 11 | 32 | 058000h-05FFFFh |
| 10 | 32 | 050000h-057FFFh |
| 9 | 32 | 048000h-04FFFFh |
| 8 | 32 | 040000h-047FFFh |
| 7 | 32 | 038000h-03FFFFh |
| 6 | 32 | 030000h-037FFFh |
| 5 | 32 | 028000h-02FFFFh |
| 4 | 32 | 020000h-027FFFh |
| 3 | 32 | 018000h-01FFFFh |
| 2 | 32 | 010000h-017FFFh |
| 1 | 32 | 008000h-00FFFFh |
| 0 | 32 | 000000h-007FFFh |

**Table 28. Bank B, Bottom Boot Block Addresses M59DR032EB**

| # | Size (KWord) | Address Range |
|---|---|---|
| 55 | 32 | 1F8000h-1FFFFFh |
| 54 | 32 | 1F0000h-1F7FFFh |
| 53 | 32 | 1E8000h-1EFFFFh |
| 52 | 32 | 1E0000h-1E7FFFh |
| 51 | 32 | 1D8000h-1DFFFFh |
| 50 | 32 | 1D0000h-1D7FFFh |
| 49 | 32 | 1C8000h-1CFFFFh |
| 48 | 32 | 1C0000h-1C7FFFh |
| 47 | 32 | 1B8000h-1BFFFFh |
| 46 | 32 | 1B0000h-1B7FFFh |
| 45 | 32 | 1A8000h-1AFFFFh |
| 44 | 32 | 1A0000h-1A7FFFh |
| 43 | 32 | 198000h-19FFFFh |
| 42 | 32 | 190000h-197FFFh |
| 41 | 32 | 188000h-18FFFFh |
| 40 | 32 | 180000h-187FFFh |
| 39 | 32 | 178000h-17FFFFh |
| 38 | 32 | 170000h-177FFFh |
| 37 | 32 | 168000h-16FFFFh |
| 36 | 32 | 160000h-167FFFh |
| 35 | 32 | 158000h-15FFFFh |
| 34 | 32 | 150000h-157FFFh |
| 33 | 32 | 148000h-14FFFFh |
| 32 | 32 | 140000h-147FFFh |
| 31 | 32 | 138000h-13FFFFh |
| 30 | 32 | 130000h-137FFFh |
| 29 | 32 | 128000h-12FFFFh |
| 28 | 32 | 120000h-127FFFh |
| 27 | 32 | 118000h-11FFFFh |
| 26 | 32 | 110000h-117FFFh |
| 25 | 32 | 108000h-10FFFFh |
| 24 | 32 | 100000h-107FFFh |
| 23 | 32 | 0F8000h-0FFFFFh |
| 22 | 32 | 0F0000h-0F7FFFh |
| 21 | 32 | 0E8000h-0EFFFFh |
| 20 | 32 | 0E0000h-0E7FFFh |
| 19 | 32 | 0D8000h-0DFFFFh |
| 18 | 32 | 0D0000h-0D7FFFh |
| 17 | 32 | 0C8000h-0CFFFFh |
| 16 | 32 | 0C0000h-0C7FFFh |
| 15 | 32 | 0B8000h-0BFFFFh |
| 14 | 32 | 0B0000h-0B7FFFh |
| 13 | 32 | 0A8000h-0AFFFFh |
| 12 | 32 | 0A0000h-0A7FFFh |
| 11 | 32 | 098000h-09FFFFh |
| 10 | 32 | 090000h-097FFFh |
| 9 | 32 | 088000h-08FFFFh |
| 8 | 32 | 080000h-087FFFh |
| 7 | 32 | 078000h-07FFFFh |
| 6 | 32 | 070000h-077FFFh |
| 5 | 32 | 068000h-06FFFFh |
| 4 | 32 | 060000h-067FFFh |
| 3 | 32 | 058000h-05FFFFh |
| 2 | 32 | 050000h-057FFFh |
| 1 | 32 | 048000h-04FFFFh |
| 0 | 32 | 040000h-047FFFh |

**Table 29. Bank A, Bottom Boot Block Addresses M59DR032EB**

| # | Size (KWord) | Address Range |
|---|---|---|
| 14 | 32 | 038000h-03FFFFh |
| 13 | 32 | 030000h-037FFFh |
| 12 | 32 | 028000h-02FFFFh |
| 11 | 32 | 020000h-027FFFh |
| 10 | 32 | 018000h-01FFFFh |
| 9 | 32 | 010000h-017FFFh |
| 8 | 32 | 008000h-00FFFFh |
| 7 | 4 | 007000h-007FFFh |
| 6 | 4 | 006000h-006FFFh |
| 5 | 4 | 005000h-005FFFh |
| 4 | 4 | 004000h-004FFFh |
| 3 | 4 | 003000h-003FFFh |
| 2 | 4 | 002000h-002FFFh |
| 1 | 4 | 001000h-001FFFh |
| 0 | 4 | 000000h-000FFFh |

## APPENDIX B. COMMON FLASH INTERFACE

The Common Flash Interface is a JEDEC approved, standardized data structure that can be read from the Flash memory device. It allows a system software to query the device to determine various electrical and timing parameters, density information and functions supported by the memory. The system can interface easily with the device, enabling the software to upgrade itself when necessary.

When the Read CFI Query Command is issued the device enters CFI Query mode and the data structure is read from the memory. Tables 30, 31, 32 and 33 show the address used to retrieve each data. The Query data is always presented on the lowest order data outputs (DQ0-DQ7), the other outputs (DQ8-DQ15) are set to 0.

The CFI data structure contains also a security area starting at address 81h. This area can be accessed only in read mode and it is impossible to change after it has been written by ST. Issue a Read command to return to Read mode.

**Table 30. Query Structure Overview**

| Offset | Sub-section Name | Description |
|---|---|---|
| 00h | Reserved | Reserved for algorithm-specific information |
| 10h | CFI Query Identification String | Command set ID and algorithm data offset |
| 1Bh | System Interface Information | Device timing & voltage information |
| 27h | Device Geometry Definition | Flash device layout |
| P | Primary Algorithm-specific Extended Query table | Additional information specific to the Primary Algorithm (optional) |
| A | Alternate Algorithm-specific Extended Query table | Additional information specific to the Alternate Algorithm (optional) |

**Table 31. CFI Query Identification String**

| Offset | Data | Description |
|---|---|---|
| 00h | 0020h | Manufacturer Code |
| 01h | 00A1h - bottom<br>00A0h - top | Device Code |
| 02h-0Fh | reserved | Reserved |
| 10h | 0051h | Query Unique ASCII String "QRY" |
| 11h | 0052h | Query Unique ASCII String "QRY" |
| 12h | 0059h | Query Unique ASCII String "QRY" |
| 13h | 0002h | Primary Algorithm Command Set and Control Interface ID code 16 bit ID code defining a specific algorithm |
| 14h | 0000h | |
| 15h | offset = P = 0040h | Address for Primary Algorithm extended Query table |
| 16h | 0000h | |
| 17h | 0000h | Alternate Vendor Command Set and Control Interface ID Code second vendor - specified algorithm supported (note: 0000h means none exists) |
| 18h | 0000h | |
| 19h | value = A = 0000h | Address for Alternate Algorithm extended Query table<br>note: 0000h means none exists |
| 1Ah | 0000h | |

**Table 32. CFI Query System Interface Information**

| Offset | Data | Description |
|---|---|---|
| 1Bh | 0017h | $V_{DD}$ Logic Supply Minimum Program/Erase or Write voltage<br>bit 7 to 4 BCD value in volts<br>bit 3 to 0 BCD value in 100 millivolts |
| 1Ch | 0022h | $V_{DD}$ Logic Supply Maximum Program/Erase or Write voltage<br>bit 7 to 4 BCD value in volts<br>bit 3 to 0 BCD value in 100 millivolts |
| 1Dh | 0000h | $V_{PP}$ [Programming] Supply Minimum Program/Erase voltage<br>bit 7 to 4 HEX value in volts<br>bit 3 to 0 BCD value in 100 millivolts<br>Note: This value must be 0000h if no $V_{PP}$ pin is present |
| 1Eh | 00C0h | $V_{PP}$ [Programming] Supply Maximum Program/Erase voltage<br>bit 7 to 4 HEX value in volts<br>bit 3 to 0 BCD value in 100 millivolts<br>Note: This value must be 0000h if no $V_{PP}$ pin is present |
| 1Fh | 0004h | Typical timeout per single byte/word program (multi-byte program count = 1), $2^n$ µs<br>(if supported; 0000h = not supported) |
| 20h | 0003h | Typical timeout for maximum-size multi-byte program or page write, $2^n$ µs<br>(if supported; 0000h = not supported) |
| 21h | 000Ah | Typical timeout per individual block erase, $2^n$ ms<br>(if supported; 0000h = not supported) |
| 22h | 0000h | Typical timeout for full chip erase, $2^n$ ms<br>(if supported; 0000h = not supported) |
| 23h | 0003h | Maximum timeout for byte/word program, $2^n$ times typical (offset 1Fh)<br>(0000h = not supported) |
| 24h | 0004h | Maximum timeout for multi-byte program or page write, $2^n$ times typical (offset 20h)<br>(0000h = not supported) |
| 25h | 0002h | Maximum timeout per individual block erase, $2^n$ times typical (offset 21h)<br>(0000h = not supported) |
| 26h | 0000h | Maximum timeout for chip erase, $2^n$ times typical (offset 22h)<br>(0000h = not supported) |

**Table 33. Device Geometry Definition**

| Offset Word Mode | Data | Description |
|---|---|---|
| 27h | 0016h | Device Size = $2^n$ in number of bytes |
| 28h | 0001h | Flash Device Interface Code description: Asynchronous x16 |
| 29h | 0000h | |
| 2Ah | 0000h | Maximum number of bytes in multi-byte program or page = $2^n$ |
| 2Bh | 0000h | |
| 2Ch | 0002h | Number of Erase Block Regions within device<br>bit 7 to 0 = x = number of Erase Block Regions<br>Note: 1. x = 0 means no erase blocking, i.e. the device erases at once in "bulk."<br>2. x specifies the number of regions within the device containing one or more contiguous Erase Blocks of the same size. For example, a 128KB device (1Mb) having blocking of 16KB, 8KB, four 2KB, two 16KB, and one 64KB is considered to have 5 Erase Block Regions. Even though two regions both contain 16KB blocks, the fact that they are not contiguous means they are separate Erase Block Regions.<br>3. By definition, symmetrically block devices have only one blocking region. |
| M59DR032EA | M59DR032EA | Erase Block Region Information |
| 2Dh | 003Eh | bit 31 to 16 = z, where the Erase Block(s) within this Region are (z) times 256 bytes in size. The value z = 0 is used for 128 byte block size.<br>e.g. for 64KB block size, z = 0100h = 256 => 256 * 256 = 64K |
| 2Eh | 0000h | |
| 2Fh | 0000h | |
| 30h | 0001h | bit 15 to 0 = y, where y+1 = Number of Erase Blocks of identical size within the Erase Block Region:<br>e.g. y = D15-D0 = FFFFh => y+1 = 64K blocks [maximum number]<br>y = 0 means no blocking (# blocks = y+1 = "1 block")<br>Note: y = 0 value must be used with number of block regions of one as indicated by (x) = 0 |
| 31h | 0007h | |
| 32h | 0000h | |
| 33h | 0020h | |
| 34h | 0000h | |
| M59DR032EB | M59DR032EB | |
| 2Dh | 0007h | |
| 2Eh | 0000h | |
| 2Fh | 0020h | |
| 30h | 0000h | |
| 31h | 003Eh | |
| 32h | 0000h | |
| 33h | 0000h | |
| 34h | 0001h | |

## REVISION HISTORY

**Table 34. Document Revision History**

| Date | Version | Revision Details |
|---|---|---|
| 05-Feb-2002 | -01 | First Issue |
| 04-Apr-2002 | -02 | Document classified as Preliminary Data. Top and Bottom Device Codes modified, Program commands text clarified, Table 4, Commands modified, Table 9, Program and Erase Times modified, Status Register Error bit DQ5 text clarified, Table 21, Data Polling and Toggle Bits AC Characteristics modified. |
| 05-Sep-2002 | 2.1 | Revision numbering modified: a minor revision will be indicated by incrementing the digit after the dot, and a major revision, by incrementing the digit before the dot (revision version 02 equals 2.0).<br>Locked block condition at Reset specified in the Summary Description. Read CFI Query Command, Auto Select Command, Enter Bypass Mode Command, Block Erase Command, Bank Erase Command and Erase Suspend Command specified. Auto Select command modified in Table 4, Commands. States of lines A8-A20 modified in Table 5, Read Electronic Signature. States of lines A8-A20 modified in Table 8, Read Protection Register. Note corresponding to DQ3 at ‘0’ specified in Table 12, Status Register Bits. |
| 04-Dec-2002 | 2.2 | Figures 18 and 19 added (TFBGA48 Daisy Chain - Package Connections (Top view through package) and TFBGA48 Daisy Chain - PCB Connection Proposal (Top view through package), respectively).<br>85ns Speed Class added. |
| 22-Apr-2003 | 3.0 | Document promoted from Preliminary Data to full Datasheet status.<br>TFBGA48, 7 x 7mm, 0.75mm pitch package added. 85ns Speed Class characterized. Performance of Bank Erase Command specified. |