EP610, EP910, EP1810

Classic EPLD Family

The Altera Classic device family offers a solution to high-speed, low-power logic integration. Fabricated on advanced CMOS technology, Classic devices also have a Turbo-only version.

Classic devices support 100% TTL emulation and can easily integrate multiple PAL- and GAL-type devices with densities ranging from 300 to 900 usable gates. The Classic family provides pin-to-pin logic delays as low as 10 ns and counter frequencies as high as 100 MHz. Classic devices are available in a wide range of packages, including ceramic dual in-line package (CerDIP), plastic dual in-line package (PDIP), plastic J-lead chip carrier (PLCC), ceramic J-lead chip carrier (JLCC), pin-grid array (PGA), and small-outline integrated circuit (SOIC) packages.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

Classic
EPLD Family

May 1999, ver. 5 Data Sheet

Features

- Complete device family with logic densities of 300 to 900 usable gates (see Table 1)
- Device erasure and reprogramming with non-volatile EPROM configuration elements
- Fast pin-to-pin logic delays as low as 10 ns and counter frequencies as high as 100 MHz
- 24 to 68 pins available in dual in-line package (DIP), plastic J-lead chip carrier (PLCC), pin-grid array (PGA), and small-outline integrated circuit (SOIC) packages
- Programmable security bit for protection of proprietary designs
- 100% generically tested to provide 100% programming yield
- Programmable registers providing D, T, JK, and SR flipflops with individual clear and clock controls
- Software design support featuring the Altera® MAX+PLUS® II development system on Windows-based PCs, as well as Sun SPARCstation, HP 9000 Series 700/800, IBM RISC System/6000 workstations, and third-party development systems
- Programming support with Altera's Master Programming Unit (MPU); programming hardware from Data I/O, BP Microsystems, and other third-party programming vendors
- Additional design entry and simulation support provided by EDIF, library of parameterized modules (LPM), Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, and VeriBest

Table 1. Classic Device Features

Feature	EP610 EP610I	EP910 EP910I	EP1810
Usable gates	300	450	900
Macrocells	16	24	48
Maximum user I/O pins	22	38	64
t_{PD} (ns)	10	12	20
f_{CNT} (MHz)	100	76.9	50

General Description

The Altera Classic™ device family offers a solution to high-speed, low-power logic integration. Fabricated on advanced CMOS technology, Classic devices also have a Turbo-only version, which is described in this data sheet.

Classic devices support 100% TTL emulation and can easily integrate multiple PAL- and GAL-type devices with densities ranging from 300 to 900 usable gates. The Classic family provides pin-to-pin logic delays as low as 10 ns and counter frequencies as high as 100 MHz. Classic devices are available in a wide range of packages, including ceramic dual in-line package (CerDIP), plastic dual in-line package (PDIP), plastic J-lead chip carrier (PLCC), ceramic J-lead chip carrier (JLCC), pin-grid array (PGA), and small-outline integrated circuit (SOIC) packages.

EPROM-based Classic devices can reduce active power consumption without sacrificing performance. This reduced power consumption makes the Classic family well suited for a wide range of low-power applications.

Classic devices are 100% generically tested devices in windowed packages and can be erased with ultra-violet (UV) light, allowing design changes to be implemented quickly.

Classic devices use sum-of-products logic and a programmable register. The sum-of-products logic provides a programmable-AND/fixed-OR structure that can implement logic with up to eight product terms. The programmable register can be individually programmed for D, T, SR, or JK flipflop operation or can be bypassed for combinatorial operation. In addition, macrocell registers can be individually clocked either by a global clock or by any input or feedback path to the AND array. Altera's proprietary programmable I/O architecture allows the designer to program output and feedback paths for combinatorial or registered operation in both active-high and active-low modes. These features make it possible to implement a variety of logic functions simultaneously.

Classic devices are supported by Altera's MAX+PLUS II development system, a single, integrated package that offers schematic, text—including VHDL, Verilog HDL, and the Altera Hardware Description Language (AHDL)—and waveform design entry, compilation and logic synthesis, simulation and timing analysis, and device programming. The MAX+PLUS II software provides EDIF 2 0 0 and 3 0 0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and workstation-based EDA tools. The MAX+PLUS II software runs on Windows-based PCs, as well as Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 workstations. These devices also contain on-board logic test circuitry to allow verification of function and AC specifications during standard production flow.

For more information, see the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet*.

Functional Description

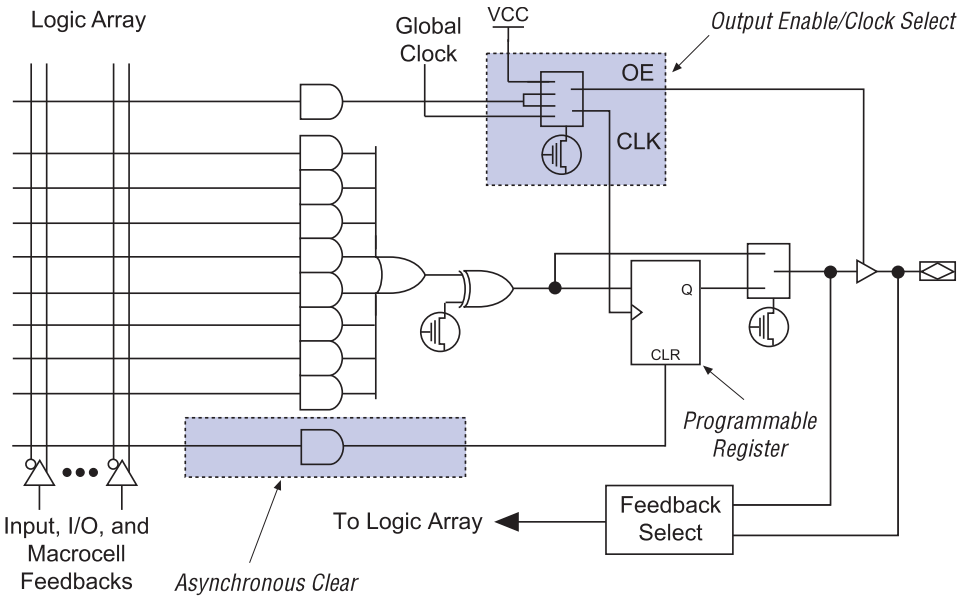
The Classic architecture includes the following elements:

- Macrocells
- Programmable registers
- Output enable/clock select
- Feedback select

Macrocells

Classic macrocells, shown in Figure 1, can be individually configured for both sequential and combinatorial logic operation. Eight product terms form a programmable-AND array that feeds an OR gate for combinatorial logic implementation. An additional product term is used for asynchronous clear control of the internal register; another product term implements either an output enable or a logic-array-generated clock. Inputs to the programmable-AND array come from both the true and complement signals of the dedicated inputs, feedbacks from I/O pins that are configured as inputs, and feedbacks from macrocell outputs. Signals from dedicated inputs are globally routed and can feed the inputs of all device macrocells. The feedback multiplexer controls the routing of feedback signals from macrocells and from I/O pins. For additional information on feedback select configurations, see Figure 3 on page 749.

Figure 1. Classic Device Macrocell



The eight product terms of the programmable-AND array feed the 8-input OR gate, which then feeds one input to an XOR gate. The other input to the XOR gate is connected to a programmable bit that allows the array output to be inverted. Altera's MAX+PLUS II software uses the XOR gate to implement either active-high or active-low logic, or De Morgan's inversion to reduce the number of product terms needed to implement a function.

Programmable Registers

To implement registered functions, each macrocell register can be individually programmed for D, T, JK, or SR operation. If necessary, the register can be bypassed for combinatorial operation. During design compilation, the MAX+PLUS II software selects the most efficient register operation for each registered function to minimize the logic resources needed by the design. Registers have an individual asynchronous clear function that is controlled by a dedicated product term. These registers are cleared automatically during power-up.

In addition, macrocell registers can be individually clocked by either a global clock or any input or feedback path to the AND array. Altera's proprietary programmable I/O architecture allows the designer to program output and feedback paths for combinatorial or registered operation in both active-high and active-low modes. These features make it possible to simultaneously implement a variety of logic functions.

Output Enable/Clock Select

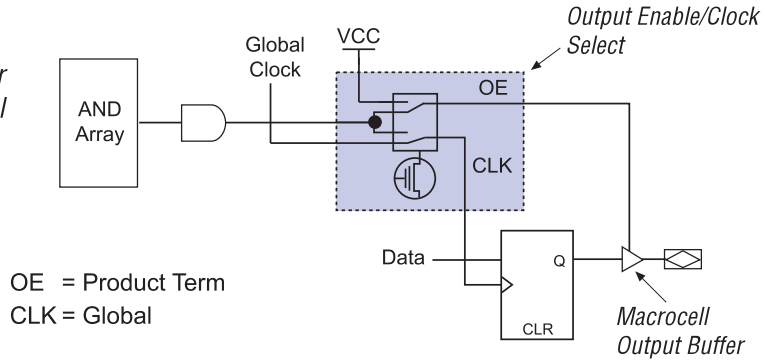
Figure 2 shows the two operating modes (Modes 0 and 1) provided by the output enable/clock (OE/CLK) select. The OE/CLK select, which is controlled by a single programmable bit, can be individually configured for each macrocell. In Mode 0, the tri-state output buffer is controlled by a single product term. If the output enable is high, the output buffer is enabled. If the output enable is low, the output has a high-impedance value. In Mode 0, the macrocell flipflop is clocked by its global clock input signal.

In Mode 1, the output enable buffer is always enabled, and the macrocell register can be triggered by an array clock signal generated by a product term. This mode allows registers to be individually clocked by any signal on the AND array. With both true and complement signals in the AND array, the register can be configured to trigger on a rising or falling edge. This product-term-controlled clock configuration also supports gated clock structures.

Figure 2. Classic Output Enable/Clock Select

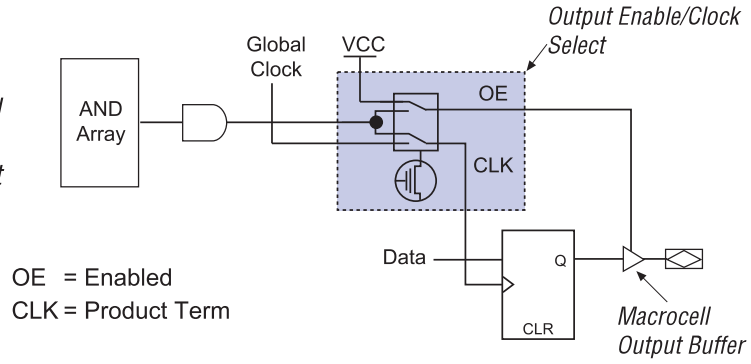
Mode 0

In Mode 0, the register is clocked by the global clock signal. The output is enabled by the logic from the product term.



Mode 1

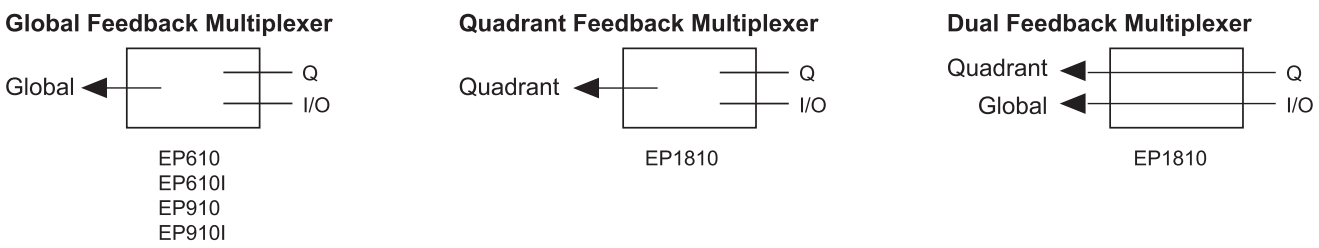
In Mode 1, the output is permanently enabled and the register is clocked by the product term, which allows gated clocks to be generated.



Feedback Select

Each macrocell in a Classic device provides feedback selection that is controlled by the feedback multiplexer. This feedback selection allows the designer to feed either the macrocell output or the I/O pin input associated with the macrocell back into the AND array. The macrocell output can be either the Q output of the programmable register or the combinatorial output of the macrocell. Different devices have different feedback multiplexer configurations. See Figure 3.

Figure 3. Classic Feedback Multiplexer Configurations



EP610, EP610I, EP910, and EP910I devices have a global feedback configuration; either the macrocell output (Q) or the I/O pin input (I/O) can feed back to the AND array so that it is accessible to all other macrocells.

EP1810 macrocells can have either of two feedback configurations: quadrant or dual. Most macrocells in EP1810 devices have a quadrant feedback configuration; either the macrocell output or I/O pin input can feed back to other macrocells in the same quadrant. Selected macrocells in EP1810 devices have a dual feedback configuration: the output of the macrocell feeds back to other macrocells in the same quadrant, and the I/O pin input feeds back to all macrocells in the device. If the associated I/O pin is not used, the macrocell output can optionally feed all macrocells in the device. In this case, the output of the macrocell passes through the tri-state buffer and uses the feedback path between the buffer and the I/O pin.

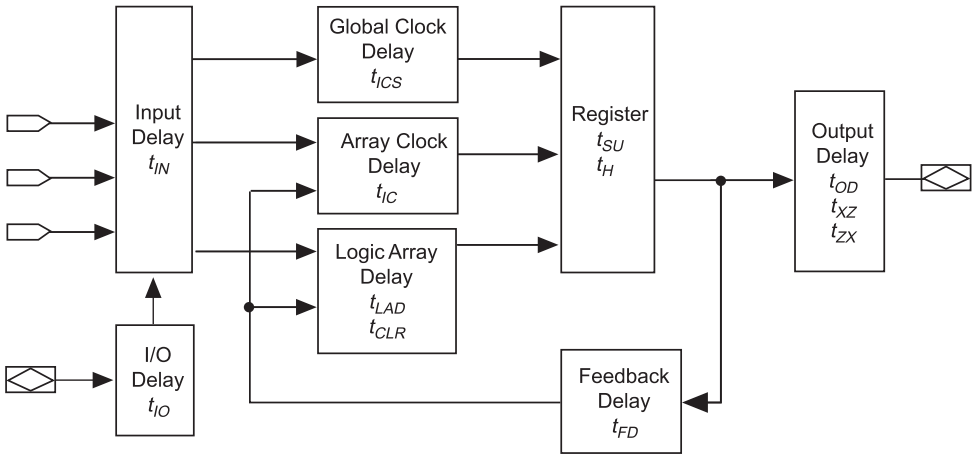
Design Security

Classic devices contain a programmable security bit that controls access to the data programmed into the device. When this bit is programmed, a proprietary design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security because data within configuration elements is invisible. The security bit that controls this function and other program data is reset only when the device is erased.

Timing Model

Device timing can be analyzed with the MAX+PLUS II software, with a variety of popular industry-standard EDA simulators and timing analyzers, or with the timing model shown in Figure 4. Devices have fixed internal delays that allow the user to determine the worst-case timing for any design. The MAX+PLUS II software provides timing simulation, point-to-point delay prediction, and detailed timing analysis for system-level performance evaluation.

Figure 4. Classic Timing Model

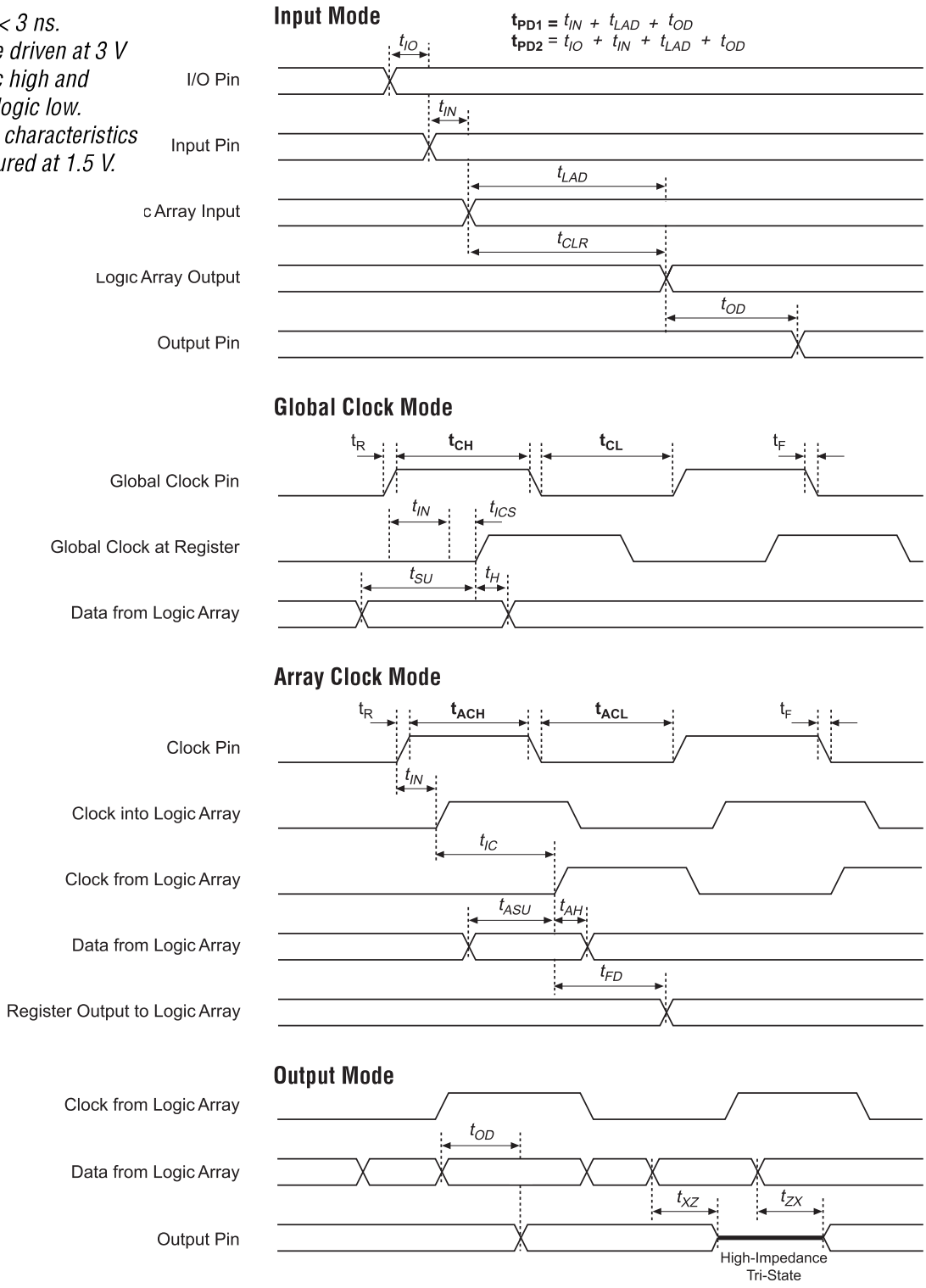


Timing information can be derived from the timing model and parameters for a particular device. External timing parameters represent pin-to-pin timing delays, and can be calculated from the sum of internal parameters. Figure 5 shows the internal timing relationship for internal and external delay parameters.

For more information on device timing, refer to *Application Note 78 (Understanding MAX 5000 & Classic Timing)* in this data book.

Figure 5. Classic Switching Waveforms

t_R and t_F < 3 ns.
Inputs are driven at 3 V for a logic high and 0 V for a logic low.
All timing characteristics are measured at 1.5 V.



Turbo Bit Option

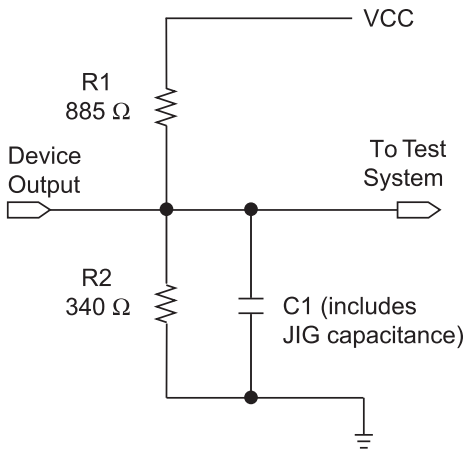
Many Classic devices contain a programmable Turbo Bit™ option to control the automatic power-down feature that enables the low-standby-power mode. When the Turbo Bit option is turned on, the low-standby-power mode is disabled. All AC values are tested with the Turbo Bit option turned on. When the device is operating with the Turbo Bit option turned off (non-Turbo mode), a non-Turbo adder must be added to the appropriate AC parameter to determine worst-case timing. The non-Turbo adder is specified in the "AC Operating Conditions" tables for each Classic device that supports the Turbo mode.

Generic Testing

Classic devices are fully functionally tested. Complete testing of each programmable EPROM configuration element and all internal logic elements before and after packaging ensures 100% programming yield. See Figure 6 for AC test measurement conditions. These devices also contain on-board logic test circuitry to allow verification of function and AC specifications during standard production flow.

Figure 6. AC Test Conditions

Power-supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, signi cant reductions in observable noise immunity can result.



Device Programming

Classic devices can be programmed on 486- and Pentium-based PCs with the MAX+PLUS II Programmer, an Altera Logic Programmer card, the MPU, and the appropriate device adapter. The MPU performs continuity checking to ensure adequate electrical contact between the adapter and the device.

Data I/O, BP Microsystems, and other programming hardware manufacturers also offer programming support for Altera devices. See *Programming Hardware Manufacturers* for more information.

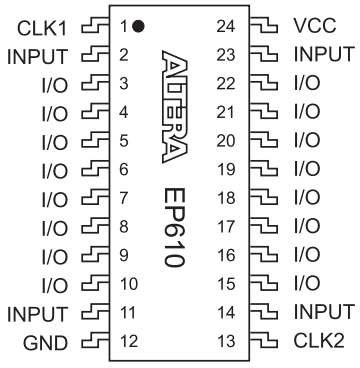
Notes:

Features

- High-performance, 16-macrocell Classic EPLD
  - Combinatorial speeds with t_{PD} as fast as 10 ns
  - Counter frequencies of up to 100 MHz
  - Pipelined data rates of up to 125 MHz
- Programmable I/O architecture with up to 20 inputs or 16 outputs and 2 clock pins
- EP610 and EP610I devices are pin-, function-, and programming file-compatible
- Programmable clock option for independent clocking of all registers
- Macrocells individually programmable as D, T, JK, or SR flipflops, or for combinatorial operation
- Available in the following packages (see Figure 7):
  - 24-pin small-outline integrated circuit (plastic SOIC only)
  - 24-pin ceramic and plastic dual in-line package (CerDIP and PDIP)
  - 28-pin plastic J-lead chip carrier (PLCC)

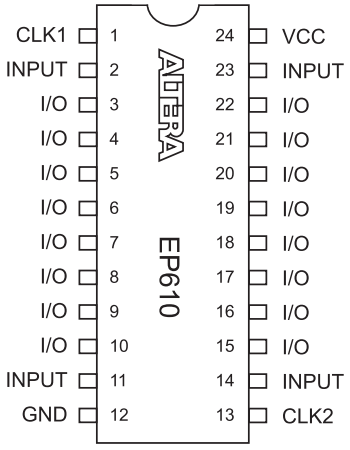
Figure 7. EP610 Package Pin-Out Diagrams

Package outlines not drawn to scale. Windows in ceramic packages only.



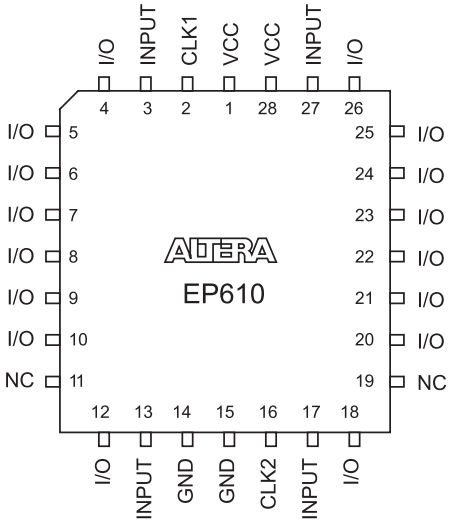
24-Pin SOIC

EP610



24-Pin DIP

EP610
EP610I



28-Pin PLCC

EP610
EP610I

General Description

EP610 devices have 16 macrocells, 4 dedicated input pins, 16 I/O pins, and 2 global clock pins (see Figure 8). Each macrocell can access signals from the global bus, which consists of the true and complement forms of the dedicated inputs and the true and complement forms of either the output of the macrocell or the I/O input. The CLK1 signal is a dedicated global clock input for the registers in macrocells 9 through 16. The CLK2 signal is a dedicated global clock input for registers in macrocells 1 through 8.

Figure 8. EP610 Block Diagram

Numbers without parentheses are for DIP and SOIC packages. Numbers in parentheses are for J-lead packages.

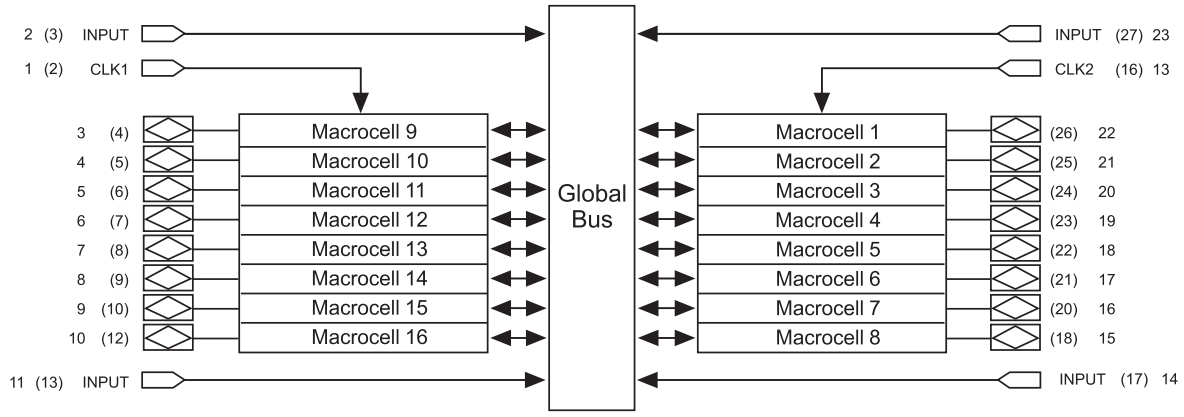


Figure 9 shows the typical supply current (I_{CC}) versus frequency of EP610 devices.

Figure 9. I_{CC} vs. Frequency of EP610 Devices

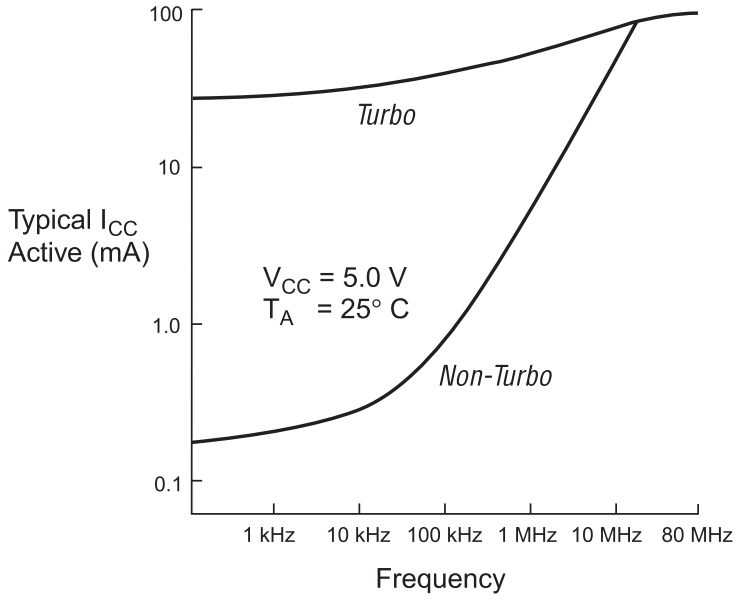
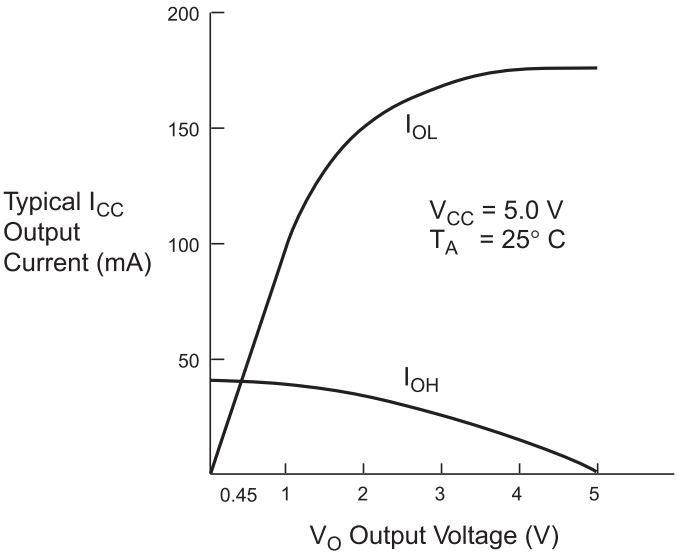


Figure 10 shows the typical output drive characteristics of EP610 devices.

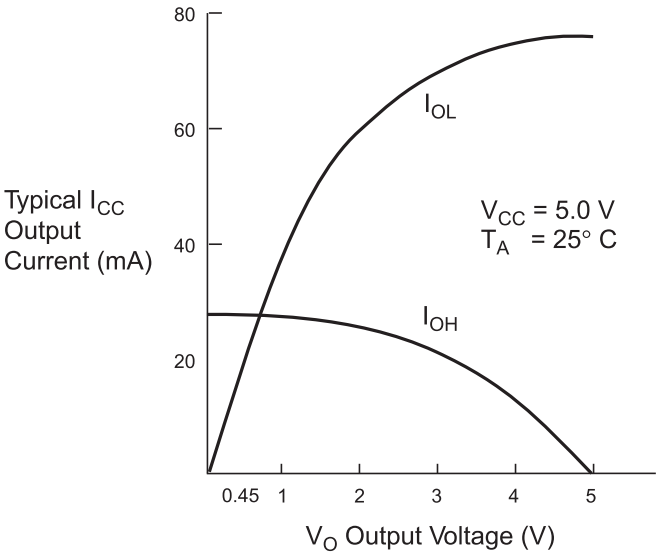
Figure 10. Output Drive Characteristics of EP610 Devices

Drive characteristics may exceed shown curves.

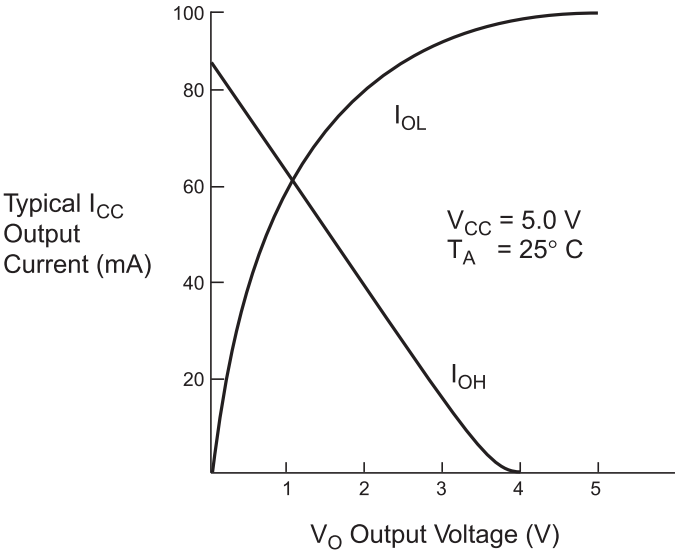
EP610-15 & EP610-20 EPLDs



EP610-25, EP610-30 & EP610-35 EPLDs



EP610I EPLDs



Operating Conditions

Tables 2 through 7 provide information on absolute maximum ratings, recommended operating conditions, operating conditions, and capacitance for EP610 and EP610I devices.

Table 2. EP610 & EP610I Device Absolute Maximum Ratings *Notes (1), (2)*

Symbol	Parameter	Conditions	EP610		EP610I		Unit
			Min	Max	Min	Max	
V_{CC}	Supply voltage	With respect to ground *(3)*	–2.0	7.0	–2.0	7.0	V
V_I	DC input voltage		–2.0	7.0	–0.5	V_{CC} + 0.5	V
I_{MAX}	DC V_{CC} or ground current		–175	175			mA
I_{OUT}	DC output current, per pin		–25	25			mA
T_{STG}	Storage temperature	No bias	–65	150	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	–65	135	° C
T_J	Junction temperature	Ceramic packages, under bias		150		150	° C
		Plastic packages, under bias		135		135	° C

Table 3. EP610 & EP610I Device Recommended Operating Conditions *Note (2)*

Symbol	Parameter	Conditions	EP610		EP610I		Unit
			Min	Max	Min	Max	
V_{CC}	Supply voltage	*(4)*	4.75 (4.5)	5.25 (5.5)	4.75	5.25	V
V_I	Input voltage		–0.3	V_{CC} + 0.3	–0.3	V_{CC} + 0.3	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	0	70	° C
		For industrial use	–40	85	–40	85	° C
t_R	Input rise time	*(5)*		100 (50)		500	ns
t_F	Input fall time	*(5)*		100 (50)		500	ns

Table 4. EP610 & EP610I Device DC Operating Conditions *Note (6)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	High-level input voltage		2.0	V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC *(7)*	2.4		V
	High-level CMOS output voltage	I_{OH} = –0.6 mA DC *(7)*, *(8)*	3.84		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC *(7)*		0.45	V
I_I	I/O pin leakage current of dedicated input pins	V_I = V_{CC} or ground	–10	10	µA
I_{OZ}	Tri-state output leakage current	V_O = V_{CC} or ground	–10	10	µA

Table 5. EP610 & EP610I Device Capacitance *Note (9)*

Symbol	Parameter	Conditions	EP610-15 EP610-20		EP610-25 EP610-30 EP610-35		EP610I		Unit
			Min	Max	Min	Max	Min	Max	
C_{IN}	Input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		10		20		8	pF
$C_{I/O}$	I/O pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		12		20		8	pF
C_{CLK1}	CLK1 pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		20		20		10	pF
C_{CLK2}	CLK2 pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		20		50		12	pF

Table 6. EP610 Device I_{CC} Supply Current *Notes (2), (10)*

Symbol	Parameter	Conditions	Speed Grade	EP610			Unit
				Min	Typ	Max	
I_{CC1}	V_{CC} supply current (non-Turbo, standby)	V_I = V_{CC} or ground, no load *(11), (12)*			20	150	µA
I_{CC2}	V_{CC} supply current (non-Turbo, active)	V_I = V_{CC} or ground, no load, f = 1.0 MHz *(11), (12)*			5	10 (15)	mA
I_{CC3}	V_{CC} supply current (Turbo, active)	V_I = V_{CC} or ground, no load, f = 1.0 MHz *(12)*	-15, -20		60	90 (115)	mA
			-25, -30, -35		45	60 (75)	mA

Table 7. EP610I Device I_{CC} Supply Current *Note (10)*

Symbol	Parameter	Conditions	EP610I			Unit
			Min	Typ	Max	
I_{CC1}	V_{CC} supply current (non-Turbo, standby)	V_I = V_{CC} or ground, no load, *(11), (12)*		20	150	µA
I_{CC2}	V_{CC} supply current (non-Turbo, active)	V_I = V_{CC} or ground, no load, f = 1.0 MHz *(11), (12)*		3	8	mA
I_{CC3}	V_{CC} supply current (Turbo, active)	V_I = V_{CC} or ground, no load, f = 1.0 MHz *(12)*		65	105	mA

Notes to tables:

(1) See the *Operating Requirements for Altera Devices Data Sheet* in this data book.
(2) Numbers in parentheses are for industrial-temperature-range devices.
(3) The minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V (EP610) or –0.5 V (EP610I) or overshoot to 7.0 V (EP610) or V_{CC} + 0.5 V (EP610I) for input currents less than 100 mA and periods less than 20 ns.
(4) For EP610 devices, maximum V_{CC} rise time is 50 ms. For EP610I devices, maximum V_{CC} rise time is unlimited with monotonic rise.
(5) For EP610-15 and EP610-20 devices: t_R and t_F = 40 ns.
For EP610-15 and EP610-20 clocks: t_R and t_F = 20 ns.
(6) These values are specified in Table 3 on page 758.
(7) The I_{OH} parameter refers to high-level TTL or CMOS output current; the I_{OL} parameter refers to low-level TTL output current.
(8) This parameter does not apply to EP610I devices.
(9) The device capacitance is measured at 25° C and is sample-tested only.
(10) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(11) When the Turbo Bit option is not set (non-Turbo mode), EP610 devices enter standby mode if no logic transitions occur for 100 ns after the last transition. When the Turbo Bit option is not set, EP610I devices enter standby mode if no logic transitions occur for 75 ns after the last transition.
(12) Measured with a device programmed as a 16-bit counter.

Tables 8 and 9 show the timing parameters for EP610-15 and EP610-20 devices.

Table 8. EP610-15 & EP610-20 External Timing Parameters *Notes (1), (2)*

Symbol	Parameter	Conditions	EP610-15		EP610-20		Non-Turbo Adder	Unit
			Min	Max	Min	Max	*(3)*	
t_{PD1}	Input to non-registered output	C1 = 35 pF		15.0		20.0	20.0	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		17.0		22.0	20.0	ns
t_{PZX}	Input to output enable	C1 = 35 pF		15.0		20.0	20.0	ns
t_{PXZ}	Input to output disable	C1 = 5 pF *(4)*		15.0		20.0	20.0	ns
t_{CLR}	Asynchronous output clear time	C1 = 35 pF		15.0		20.0	20.0	ns
f_{MAX}	Maximum clock frequency	*(5)*	83.3		62.5		0.0	MHz
t_{SU}	Global clock input setup time		9.0		11.0		20.0	ns
t_{H}	Global clock input hold time		0.0		0.0		0.0	ns
t_{CH}	Global clock high time		6.0		8.0		0.0	ns
t_{CL}	Global clock low time		6.0		8.0		0.0	ns
t_{CO1}	Global clock to output delay			11.0		13.0	0.0	ns
t_{CNT}	Global clock minimum period			12.0		16.0	0.0	ns
f_{CNT}	Maximum internal global clock frequency	*(6)*	83.3		62.5		0.0	MHz
t_{ASU}	Array clock input setup time		6.0		8.0		20.0	ns
t_{AH}	Array clock input hold time		6.0		8.0		0.0	ns
t_{ACH}	Array clock high time		7.0		9.0		0.0	ns
t_{ACL}	Array clock low time		7.0		9.0		0.0	ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF *(7)*	1.0		1.0		1.0	ns
t_{ACO1}	Array clock to output delay			15.0		20.0	20.0	ns
t_{ACNT}	Array clock minimum period			14.0		18.0	0.0	ns
f_{ACNT}	Array clock internal maximum frequency	*(6)*	71.4		55.6		0.0	MHz

Table 9. EP610-15 & EP610-20 Internal Timing Parameters (Part 1 of 2)

Symbol	Parameter	Conditions	EP610-15		EP610-20		Unit
			Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			4.0		4.0	ns
t_{IO}	I/O input pad and buffer delay			2.0		2.0	ns
t_{LAD}	Logic array delay			6.0		11.0	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		5.0		5.0	ns
t_{ZX}	Output buffer enable delay	C1 = 35 pF		5.0		5.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		5.0		5.0	ns

Table 9. EP610-15 & EP610-20 Internal Timing Parameters (Part 2 of 2)

Symbol	Parameter	Conditions	EP610-15		EP610-20		Unit
			Min	Max	Min	Max	
t_{SU}	Register setup time		5.0		4.0		ns
t_{H}	Register hold time		4.0		7.0		ns
t_{IC}	Array clock delay			6.0		11.0	ns
t_{ICS}	Global clock delay			2.0		4.0	ns
t_{FD}	Feedback delay			1.0		1.0	ns
t_{CLR}	Register clear time			6.0		11.0	ns

Tables 10 and 11 show the timing parameters for EP610-25, EP610-30 and EP610-35 devices.

Table 10. EP610-25, EP610-30 & EP610-35 External Timing Parameters *Notes (1), (2)*

Symbol	Parameter	Conditions	EP610-25		EP610-30		EP610-35		Non-Turbo Adder	Unit
			Min	Max	Min	Max	Min	Max	*(3)*	
t_{PD1}	Input to non-registered output	C1 = 35 pF		25.0		30.0		35.0	30.0	ns
t_{PD2}	I/O input to non-registered output			27.0		32.0		37.0	30.0	ns
t_{PZX}	Input to output enable			25.0		30.0		35.0	30.0	ns
t_{PXZ}	Input to output disable	C1 = 5 pF *(4)*		25.0		30.0		35.0	30.0	ns
t_{CLR}	Asynchronous output clear time	C1 = 35 pF		27.0		32.0		37.0	30.0	ns
f_{MAX}	Maximum frequency	*(5)*	47.6		41.7		37.0		0.0	MHz
t_{SU}	Global clock input setup time		21.0		24.0		27.0		30.0	ns
t_{H}	Global clock input hold time		0.0		0.0		0.0		0.0	ns
t_{CH}	Global clock high time		10.0		11.0		12.0		0.0	ns
t_{CL}	Global clock low time		10.0		11.0		12.0		0.0	ns
t_{CO1}	Global clock to output delay			15.0		17.0		20.0	0.0	ns
t_{CNT}	Global clock minimum period			25.0		30.0		35.0	0.0	ns
f_{CNT}	Maximum internal global clock frequency	*(6)*	40.0		33.3		28.6		0.0	MHz
t_{ASU}	Array clock input setup time		8.0		8.0		8.0		30.0	ns
t_{AH}	Array clock input hold time		12.0		12.0		12.0		0.0	ns
t_{ACH}	Array clock high time		10.0		11.0		12.0		0.0	ns
t_{ACL}	Array clock low time		10.0		11.0		12.0		0.0	ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF *(7)*	1.0		1.0		1.0			ns
t_{ACO1}	Array clock to output delay			27.0		32.0		37.0	30.0	ns
t_{ACNT}	Array clock minimum period			25.0		30.0		35.0	0.0	ns
f_{ACNT}	Maximum internal global clock frequency	*(6)*	40.0		33.3		28.6		0.0	MHz

Table 11. EP610-25, EP610-30 & EP610-35 Internal Timing Parameters

Symbol	Parameter	Condition	EP610-25		EP610-30		EP610-35		Unit
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			8.0		9.0		11.0	ns
t_{IO}	I/O input pad and buffer delay			2.0		2.0		2.0	ns
t_{LAD}	Logic array delay			11.0		14.0		15.0	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		6.0		7.0		9.0	ns
t_{ZX}	Output buffer enable delay	C1 = 35 pF		6.0		7.0		9.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		6.0		7.0		9.0	ns
t_{SU}	Register setup time		11.0		11.0		12.0		ns
t_{H}	Register hold time		10.0		10.0		10.0		ns
t_{IC}	Array clock delay			13.0		16.0		17.0	ns
t_{ICS}	Global clock delay			1.0		1.0		0.0	ns
t_{FD}	Feedback delay			3.0		5.0		8.0	ns
t_{CLR}	Register clear time			13.0		16.0		17.0	ns

Notes to tables:

(1) These values are specified in Table 3 on page 758.
(2) See *Application Note 78 (Understanding MAX 5000 & Classic Timing)* in this data book for information on internal timing parameters.
(3) The non-Turbo adder must be added to this parameter when the Turbo Bit option is off.
(4) Sample-tested only for an output change of 500 mV.
(5) The $\mathbf{f_{MAX}}$ values represent the highest frequency for pipelined data.
(6) Measured with a device programmed as a 16-bit counter.
(7) Sample-tested only. This parameter is a guideline based on extensive device characterization. This parameter applies for both global and array clocking.

Tables 12 and 13 show the timing parameters for EP610I devices.

Table 12. EP610I External Timing Parameters *Notes (1), (2)*

Symbol	Parameter	Conditions	EP610I-10		EP610I-12		EP610I-15		Non-Turbo Adder	Unit
			Min	Max	Min	Max	Min	Max	*(3)*	
t_{PD1}	Input to non-registered output	C1 = 35 pF		10.0		12.0		15.0	25.0	ns
t_{PD2}	I/O input to non-registered output			10.0		12.0		15.0	25.0	ns
t_{PZX}	Input to output enable			15.0		15.0		18.0	25.0	ns
t_{PXZ}	Input to output disable	C1 = 5 pF *(4)*		13.0		15.0		18.0	25.0	ns
t_{CLR}	Asynchronous output clear time	C1 = 35 pF		13.0		15.0		18.0	25.0	ns
f_{MAX}	Maximum frequency	*(5)*	125.0		100.0		83.3		0.0	MHz
t_{SU}	Global clock input setup time		7.0		9.0		12.0		25	ns
t_{H}	Global clock input hold time		0.0		0.0		0.0		0.0	ns
t_{CH}	Global clock high time		5.0		5.0		5.0		0.0	ns
t_{CL}	Global clock low time		5.0		5.0		5.0		0.0	ns
t_{CO1}	Global clock to output delay			6.5		8.0		8.0	0.0	ns
t_{CNT}	Global clock minimum period			10.0		12.0		15.0	25.0	ns
f_{CNT}	Maximum internal global clock frequency	*(6)*	100.0		83.3		66.0		0.0	MHz
t_{ASU}	Array clock input setup time		1.5		3.0		4.0		25.0	ns
t_{AH}	Array clock input hold time		5.5		6.0		6.0		0.0	ns
t_{ACH}	Array clock high time		5.0		5.0		6.0		0.0	ns
t_{ACL}	Array clock low time		5.0		5.0		6.0		0.0	ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF *(7)*	1.0		1.0		1.0			ns
t_{ACO1}	Array clock to output delay			12.0		14.0		16.0	25.0	ns
t_{ACNT}	Array clock minimum period			10.0		12.0		15.0	25.0	ns
f_{ACNT}	Maximum internal array clock frequency	*(6)*	100.0		83.3		66.0		0.0	MHz

Table 13. EP610 Internal Timing Parameters

Symbol	Parameter	Conditions	EP610I-10		EP610I-12		EP610I-15		Unit
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			1.5		4.0		4.0	ns
t_{IO}	I/O input pad and buffer delay			0.0		0.0		0.0	ns
t_{LAD}	Logic array delay			5.5		6.0		9.0	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		3.0		2.0		2.0	ns
t_{ZX}	Output buffer enable delay	C1 = 35 pF		8.0		5.0		6.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		6.0		5.0		6.0	ns
t_{SU}	Register setup time		3.5		5.0		5.0		ns
t_{H}	Register hold time		3.5		4.0		7.0		ns
t_{IC}	Array clock delay			7.5		8.0		10.0	ns
t_{ICS}	Global clock delay			2.0		2.0		2.0	ns
t_{FD}	Feedback delay			1.0		1.0		1.0	ns
t_{CLR}	Register clear time			8.5		9.0		12.0	ns

Notes to tables:

(1) These values are specified in Table 3 on page 758.
(2) See *Application Note 78 (Understanding MAX 5000 & Classic Timing)* in this data book for more information on Classic timing parameters.
(3) The non-Turbo adder must be added to this parameter when the Turbo Bit option is off.
(4) Sample-tested only for an output change of 500 mV.
(5) The $\mathbf{f_{MAX}}$ values represent the highest frequency for pipelined data.
(6) Measured with a device programmed as a 16-bit counter.
(7) Sample-tested only. This parameter is a guideline based on extensive device characterization. This parameter applies for both global and array clocking.

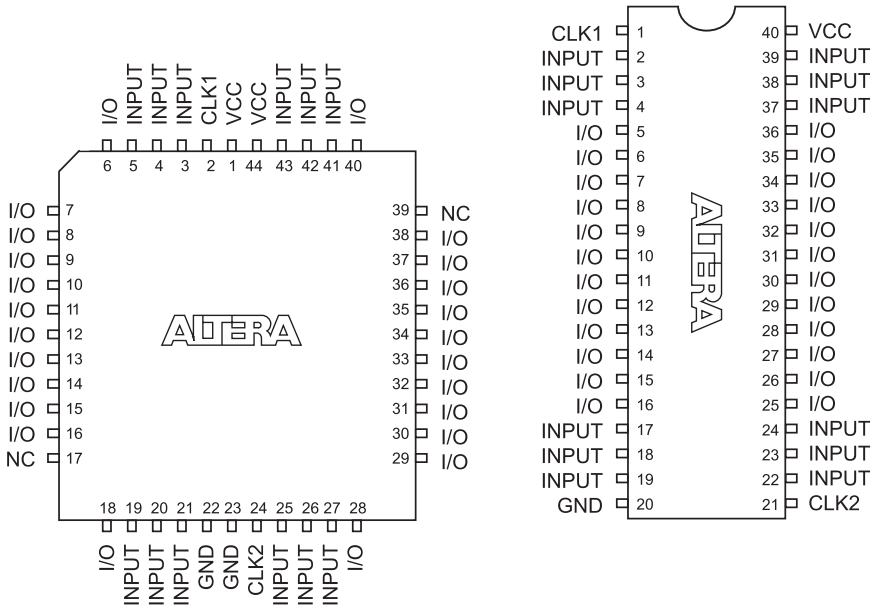
Notes:

Features

- High-performance, 24-macrocell Classic EPLD
  - Combinatorial speeds with t_{PD} as fast as 12 ns
  - Counter frequencies of up to 76.9 MHz
  - Pipelined data rates of up to 125 MHz
- Programmable I/O architecture with up to 36 inputs or 24 outputs
- EP910 and EP910I devices are pin-, function-, and programming file-compatible
- Programmable clock option for independent clocking of all registers
- Macrocells individually programmable as D, T, JK, or SR flipflops, or for combinatorial operation
- Available in the following packages (see Figure 11)
  - 44-pin plastic J-lead chip carrier (PLCC)
  - 40-pin ceramic and plastic dual in-line packages (CerDIP and PDIP)

Figure 11. EP910 Package Pin-Out Diagrams

Package outlines are not drawn to scale. Windows in ceramic packages only.



General Description

Altera EP910 devices can implement up to 450 usable gates of SSI and MSI logic functions. EP910 devices have 24 macrocells, 12 dedicated input pins, 24 I/O pins, and 2 global clock pins (see Figure 12). Each macrocell can access signals from the global bus, which consists of the true and complement forms of the dedicated inputs and the true and complement forms of either the output of the macrocell or the I/O input. The `CLK1` and `CLK2` signals are the dedicated clock inputs for the registers in macrocells 13 through 24 and 1 through 12, respectively.

Figure 12. EP910 Block Diagram

Numbers without parentheses are for DIP packages. Numbers in parentheses are for J-lead packages.

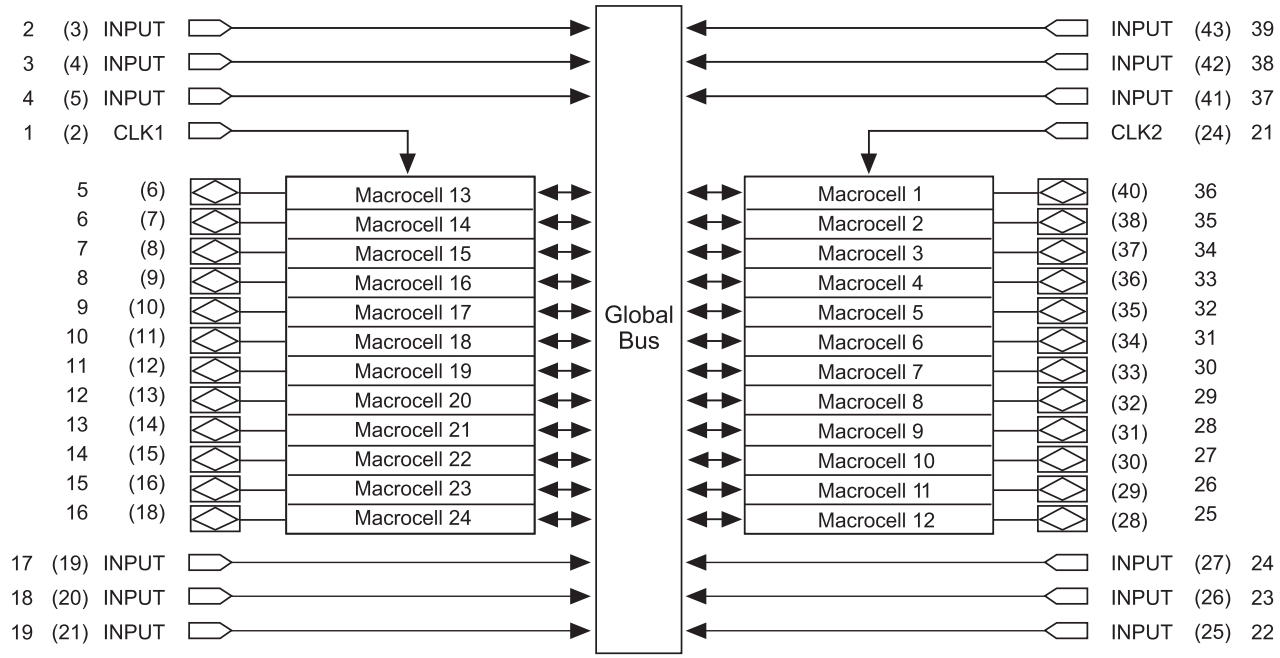


Figure 13 shows the typical supply current (I_{CC}) versus frequency of EP910 devices.

Figure 13. I_{CC} vs. Frequency of EP910 Devices

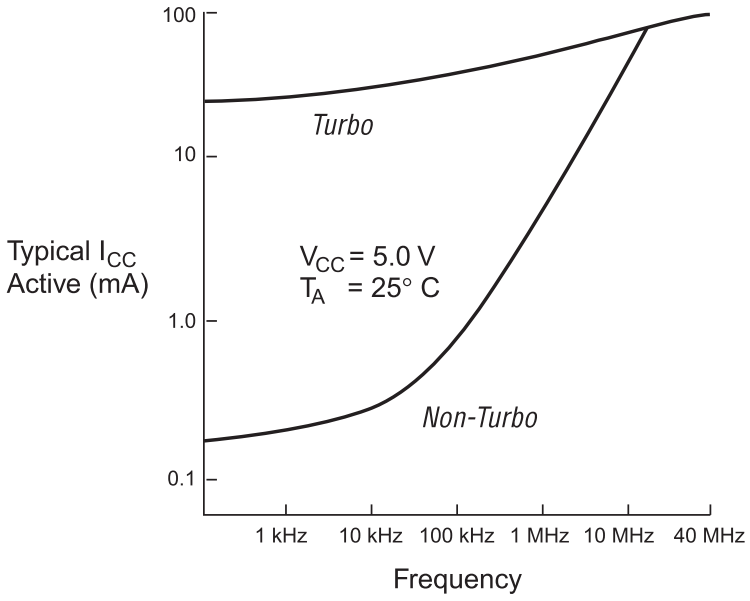
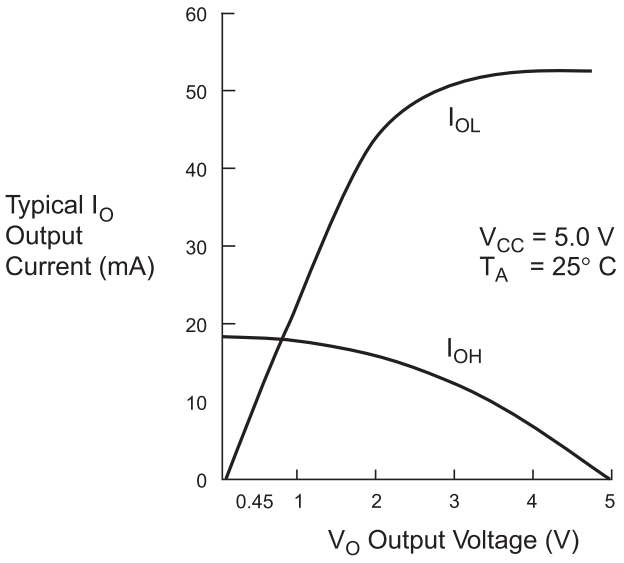


Figure 14 shows the typical output drive characteristics of EP910 devices.

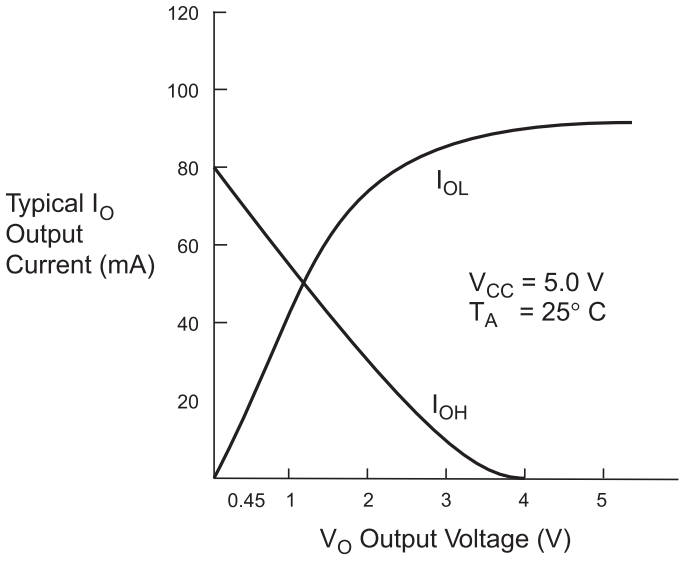
Figure 14. Output Drive Characteristics of EP910 Devices

Drive characteristics may exceed shown curves.

EP910 EPLDs



EP910I EPLDs



Operating Conditions

Tables 14 through 18 provide information on absolute maximum ratings, recommended operating conditions, operating conditions, and capacitance for EP910 and EP910I devices.

Table 14. EP910 & EP910I Device Absolute Maximum Ratings *Notes (1), (2)*

Symbol	Parameter	Conditions	EP910		EP910I		Unit
			Min	Max	Min	Max	
V_{CC}	Supply voltage	With respect to ground *(3)*	–2.0	7.0	–2.0	7.0	V
V_I	DC input voltage		–2.0	7.0	–0.5	V_{CC} + 0.5	V
I_{MAX}	DC V_{CC} or ground current		–250	250			mA
I_{OUT}	DC output current, per pin		–25	25			mA
T_{STG}	Storage temperature	No bias	–65	150	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	–65	135	° C
T_J	Junction temperature	Ceramic packages, under bias		150		150	° C
		Plastic packages, under bias		135		135	° C

Table 15. EP910 & EP910I Device Recommended Operating Conditions *Note (2)*

Symbol	Parameter	Conditions	EP910		EP910I		Unit
			Min	Max	Min	Max	
V_{CC}	Supply voltage	*(4)*	4.75 (4.5)	5.25 (5.5)	4.75	5.25	V
V_I	Input voltage		–0.3	V_{CC} + 0.3	–0.3	V_{CC} + 0.3	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	0	70	° C
		For industrial use	–40	85			° C
t_R	Input rise time	*(5)*		100 (50)		500	ns
t_F	Input fall time	*(5)*		100 (50)		500	ns

Table 16. EP910 & EP910I Device DC Operating Conditions *Notes (6), (7)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	High-level input voltage		2.0	V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC *(8)*	2.4		V
	High-level CMOS output voltage	I_{OH} = –0.6 mA DC *(8)*, *(9)*	3.84		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC *(8)*		0.45	V
I_I	I/O leakage current of dedicated input pins	V_I = V_{CC} or ground	–10	10	µA
I_{OZ}	Tri-state output leakage current	V_O = V_{CC} or ground	–10	10	µA

Table 17. EP910 & EP910I Device Capacitance *Note (6)*

Symbol	Parameter	Conditions	EP910		EP910I		Unit
			Min	Max	Min	Max	
C_{IN}	Input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		20		8	pF
$C_{I/O}$	I/O pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		20		8	pF
C_{CLK1}	CLK1 pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		20		10	pF
C_{CLK2}	CLK2 pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		60		12	pF

Table 18. EP910 & EP910I Device I_{CC} Supply Current *Notes (2), (6), (7)*

Symbol	Parameter	Conditions	EP910			EP910I			Unit
			Min	Typ	Max	Min	Typ	Max	
I_{CC1}	V_{CC} supply current (non-Turbo, standby)	V_I = V_{CC} or ground, no load *(10), (11)*		20	150		60	150	µA
I_{CC2}	V_{CC} supply current (non-Turbo, active)	V_I = V_{CC} or ground, no load, f = 1.0 MHz *(10), (11)*		6	20		4	12	mA
I_{CC3}	V_{CC} supply current (Turbo, active)	V_I = V_{CC} or ground, no load, f = 1.0 MHz *(11)*		45	80 (100)		120	150	mA

Notes to tables:

(1) See the *Operating Requirements for Altera Devices Data Sheet* in this data book.
(2) Numbers in parentheses are for industrial-temperature-range devices.
(3) The minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V (EP910) or –0.5 V (EP910I) or overshoot to 7.0 V (EP910) or V_{CC} + 0.5 V (EP910I) for input currents less than 100 mA and periods less than 20 ns.
(4) Maximum V_{CC} rise time for EP910 devices = 50 ms; for EP910I devices, maximum V_{CC} rise time is unlimited with monotonic rise.
(5) For all clocks: t_R and t_F = 100 ns (50 ns for the industrial-temperature-range version).
(6) These values are specified in Table 15 on page 770.
(7) The device capacitance is measured at 25° C and is sample-tested only.
(8) The I_{OH} parameter refers to high-level TTL or CMOS output current; the I_{OL} parameter refers to low-level TTL output current.
(9) This parameter does not apply to EP910I devices.
(10) When the Turbo Bit option is not set (non-Turbo mode), an EP910 device will enter standby mode if no logic transitions occur for 100 ns after the last transition, and an EP910I device will enter standby mode if no logic transitions occur for 75 ns after the last transition.
(11) Measured with a device programmed as a 24-bit counter.

Tables 19 and 20 show the timing parameters for EP910 devices.

Table 19. EP910 External Timing Parameters *Notes (1), (2)*

Symbol	Parameter	Conditions	EP910-30		EP910-35		EP910-40		Non-Turbo Adder *(3)*	Unit
			Min	Max	Min	Max	Min	Max		
t_{PD1}	Input to non-registered output	C1 = 35 pF		30.0		35.0		40.0	30.0	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		33.0		38.0		43.0	30.0	ns
t_{PZX}	Input to output enable	C1 = 35 pF		30.0		35.0		40.0	30.0	ns
t_{PXZ}	Input to output disable	C1 = 5 pF *(4)*		30.0		35.0		40.0	30.0	ns
t_{CLR}	Asynchronous output clear time	C1 = 35 pF		33.0		38.0		43.0	30.0	ns
f_{MAX}	Maximum frequency	*(5)*	41.7		37.0		32.3		0.0	MHz
t_{SU}	Global clock input setup time		24.0		27.0		31.0		30.0	ns
t_{H}	Global clock input hold time		0.0		0.0		0.0		0.0	ns
t_{CH}	Global clock high time		12.0		13.0		15.0		0.0	ns
t_{CL}	Global clock low time		12.0		13.0		15.0		0.0	ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		18		21.0		24.0	0.0	ns
t_{CNT}	Global clock minimum clock period	*(6)*		30.0		35.0		40.0	0.0	ns
f_{CNT}	Maximum internal global clock frequency	*(6)*	33.3		28.6		25.0		0.0	MHz
t_{ASU}	Array clock input setup time		10.0		10.0		10.0		30.0	ns
t_{AH}	Array clock input hold time		15.0		15.0		15.0		0.0	ns
t_{ACH}	Array clock high time		15.0		16.0		17.0		0.0	ns
t_{ACL}	Array clock low time		15.0		16.0		17.0		0.0	ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF *(7)*	1.0		1.0		1.0			ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		33.0		38.0		43.0	30.0	ns
t_{ACNT}	Array clock minimum clock period			30.0		35.0		40.0	0.0	ns
f_{ACNT}	Maximum internal array clock frequency	*(6)*	33.3		28.6		25.0		0.0	MHz

Table 20. EP910 Internal Timing Parameters

Symbol	Parameter	Condition	EP910-30		EP910-35		EP910-40		Unit
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			9.0		10.0		13.0	ns
t_{IO}	I/O input pad and buffer delay			3.0		3.0		3.0	ns
t_{LAD}	Logic array delay			14.0		16.0		17.0	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		7.0		9.0		10.0	ns
t_{ZX}	Output buffer enable delay	C1 = 35 pF		7.0		9.0		10.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		7.0		9.0		10.0	ns
t_{SU}	Register setup time		12.0		13.0		15.0		ns
t_{H}	Register hold time		12.0		12.0		12.0		ns
t_{IC}	Array clock delay			17.0		19.0		20.0	ns
t_{ICS}	Global clock delay			2.0		2.0		1.0	ns
t_{FD}	Feedback delay			4.0		6.0		8.0	ns
t_{CLR}	Register clear time			17.0		19.0		20.0	ns

Notes to tables:

(1) These values are specified in Table 15 on page 770.
(2) See *Application Note 78 (Understanding MAX 5000 & Classic Timing)* in this data book for more information on Classic timing parameters.
(3) The non-Turbo adder must be added to this parameter when the Turbo Bit option is off.
(4) Sample-tested only for an output change of 500 mV.
(5) The $\mathbf{f_{MAX}}$ values represent the highest frequency for pipelined data.
(6) Measured with a device programmed as a 24-bit counter.
(7) Sample-tested only. This parameter is a guideline based on extensive device characterization and applies for both global and array clocking.

Tables 21 and 22 show the timing parameters for EP910I devices.

Table 21. EP910I External Timing Parameters *Notes (1), (2)*

Symbol	Parameter	Conditions	EP910I-12		EP910I-15		EP910I-25		Non-Turbo Adder	Unit
			Min	Max	Min	Max	Min	Max	*(3)*	
t_{PD1}	Input to non-registered output	C1 = 35 pF		12.0		15.0		25.0	40.0	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		12.0		15.0		25.0	40.0	ns
t_{PZX}	Input to output enable	C1 = 35 pF		15.0		18.0		28.0	40.0	ns
t_{PXZ}	Input to output disable	C1 = 35 pF *(4)*		15.0		18.0		28.0	40.0	ns
t_{CLR}	Asynchronous output clear time	C1 = 35 pF		15.0		18.0		28.0	40.0	ns
f_{MAX}	Global clock maximum frequency	*(5)*	125.0		100.0		62.5		0.0	MHz
t_{SU}	Global clock input setup time		8.0		11.0		16.0		40.0	ns
t_{H}	Global clock input hold time		0.0		0.0		0.0		0.0	ns
t_{CH}	Global clock high time		5.0		6.0		10.0		0.0	ns
t_{CL}	Global clock low time		5.0		6.0		10.0		0.0	ns
t_{CO1}	Global clock to output delay			8.0		9.0		14.0	0.0	ns
t_{CNT}	Global clock minimum clock period	C1 = 35 pF		13.0		15.0		25.0	40.0	ns
f_{CNT}	Maximum internal global clock frequency	*(6)*	76.9		66.6		40.0		0.0	MHz
t_{ASU}	Array clock input setup time		3.0		4.0		8.0		40.0	ns
t_{AH}	Array clock input hold time		6.0		7.0		8.0			ns
t_{ACH}	Array clock high time		6.0		7.5		12.5			ns
t_{ACL}	Array clock low time		6.0		7.5		12.5			ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF *(7)*	1.0		1.0		1.0			ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		16.0		18.0		22.0	40.0	ns
t_{ACNT}	Array clock minimum clock period			13.0		15.0		25.0	40.0	ns
f_{ACNT}	Maximum internal array clock frequency	*(6)*	76.9		66.6		40.0			MHz

Table 22. EP910I Internal Timing Parameters

Symbol	Parameter	Condition	EP910I-12		EP910I-15		EP910I-25		Unit
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			2.0		3.0		2.0	ns
t_{IO}	I/O input pad and buffer delay			0.0		0.0		0.0	ns
t_{LAD}	Logic array delay			8.0		9.0		17.0	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		2.0		3.0		6.0	ns
t_{ZX}	Output buffer enable delay	C1 = 35 pF		5.0		6.0		9.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		5.0		6.0		9.0	ns
t_{SU}	Register setup time		4.0		5.0		5.0		ns
t_{H}	Register hold time		4.0		6.0		11.0		ns
t_{IC}	Array clock delay			12.0		12.0		14.0	ns
t_{ICS}	Global clock delay			4.0		3.0		6.0	ns
t_{FD}	Feedback delay			1.0		1.0		3.0	ns
t_{CLR}	Register clear time			11.0		12.0		20.0	ns

Notes to tables:

(1) These values are specified in Table 15 on page 770.
(2) See *Application Note 78 (Understanding MAX 5000 & Classic Timing)* in this data book for information on internal timing parameters.
(3) The non-Turbo adder must be added to this parameter when the Turbo Bit option is off.
(4) Sample-tested only for an output change of 500 mV.
(5) The $\mathbf{f_{MAX}}$ values represent the highest frequency for pipelined data.
(6) Measured with the device programmed as a 24-bit counter.
(7) Sample-tested only. This parameter is a guideline based on extensive device characterization and applies for both global and array clocking.

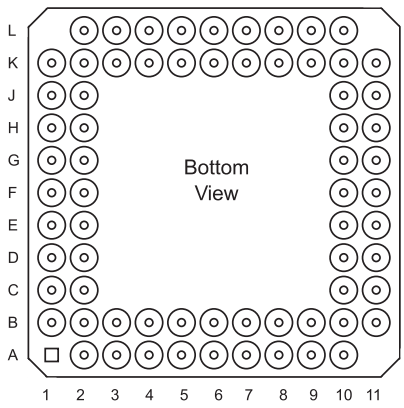
Notes:

Features

- High-performance, 48-macrocell Classic EPLD
  - Combinatorial speeds with t_{PD} as fast as 20 ns
  - Counter frequencies of up to 50 MHz
  - Pipelined data rates of up to 62.5 MHz
- Programmable I/O architecture with up to 64 inputs or 48 outputs
- Programmable clock option for independent clocking of all registers
- Macrocells individually programmable as D, T, JK, or SR flipflops, or for combinatorial operation
- Available in the following packages (see Figure 15)
  - 68-pin ceramic pin-grid array (PGA)
  - 68-pin plastic J-lead chip carrier (PLCC)

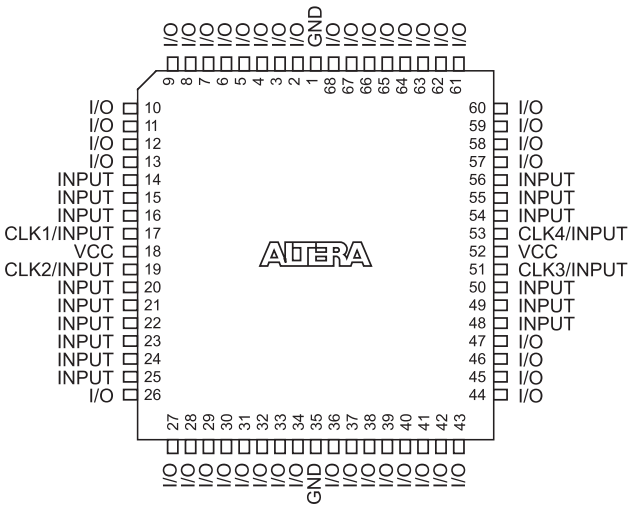
Figure 15. EP1810 Package Pin-Out Diagrams

Package outlines not drawn to scale. See Table 32 on page 785 of this data sheet for PGA package pin-out information. Windows in ceramic packages only.



68-Pin PGA

EP1810



68-Pin PLCC

EP1810

General Description

Altera EP1810 devices offer LSI density, TTL-equivalent speed, and low-power consumption. EP1810 devices have 48 macrocells, 16 dedicated input pins, and 48 I/O pins (see Figure 16). EP1810 devices are divided into four quadrants, each containing 12 macrocells. Of the 12 macrocells in each quadrant, 8 have quadrant feedback and are "local" macrocells (see "Feedback Select" on page 749 of this data sheet for more information). The remaining 4 macrocells in the quadrant are "global" macrocells. Both local and global macrocells can access signals from the global bus, which consists of the true and complement forms of the dedicated inputs and the true and complement forms of the feedbacks from the global macrocells.

EP1810 devices also have four dedicated inputs (one in each quadrant) that can be used as quadrant clock inputs. If the dedicated input is used as a clock pin, the input feeds the clock input of all registers in that particular quadrant.

Figure 16. EP1810 Block Diagram

Pin numbers are for J-lead packages. Pin numbers in parentheses are for PGA packages.

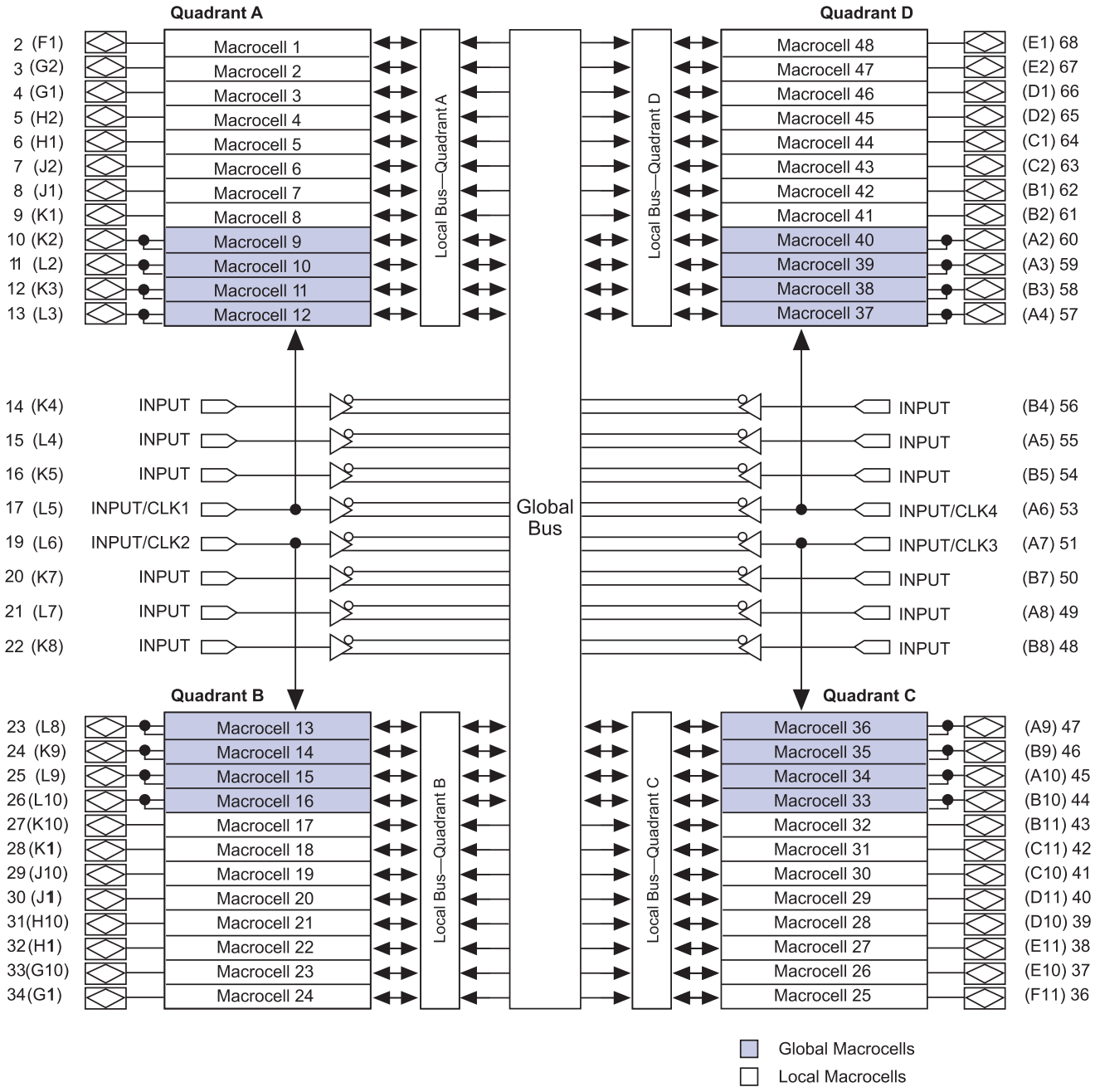


Figure 17 shows the typical supply current (I_{CC}) versus frequency for EP1810 EPLDs.

Figure 17. I_{CC} vs. Frequency of EP1810 Devices

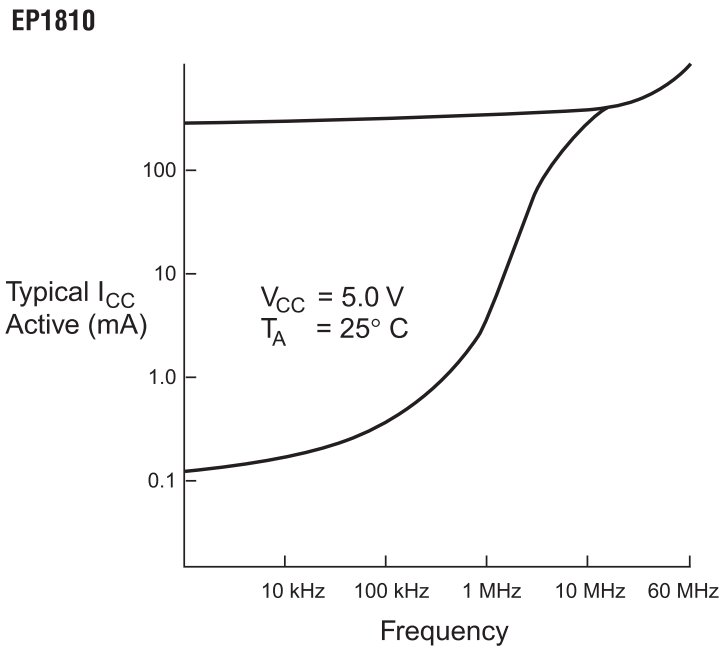
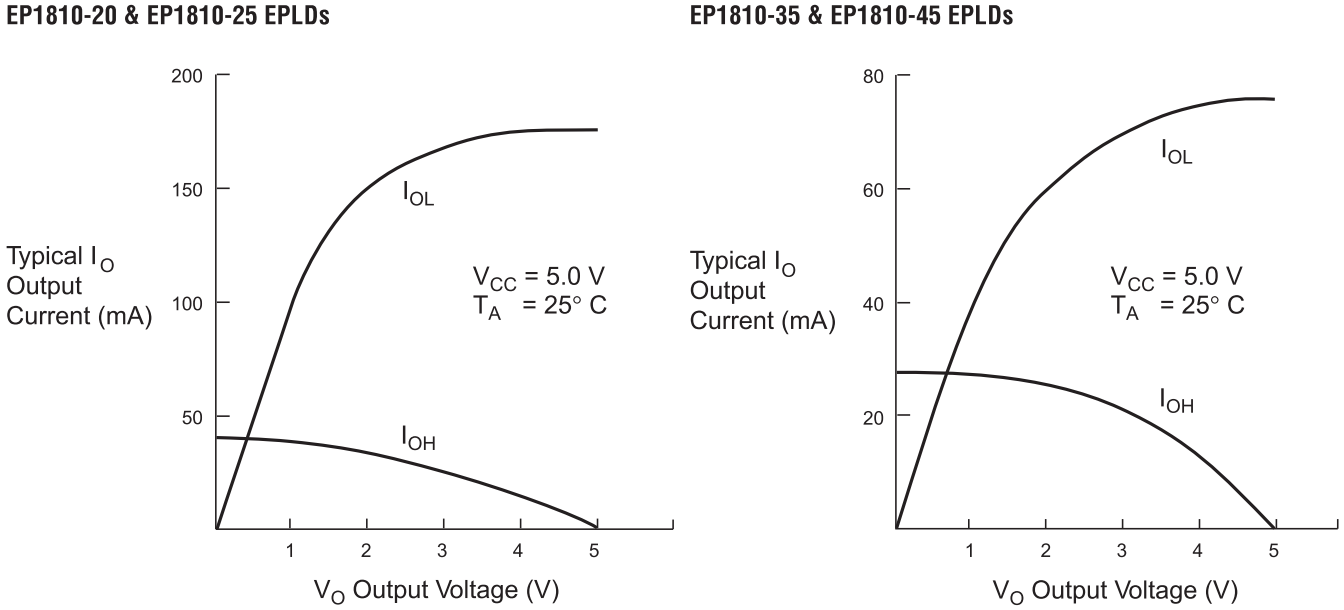


Figure 18 shows the output drive characteristics of EP1810 devices.

Figure 18. Output Drive Characteristics of EP1810 Devices

Drive characteristics may exceed shown curves.



Operating Conditions

Tables 23 through 27 provide information on absolute maximum ratings, recommended operating conditions, operating conditions, and capacitance for EP1810 devices.

Table 23. EP1810 Device Absolute Maximum Ratings *Notes (1), (2)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to ground *(3)*	–2.0 (–0.5)	7.0	V
V_I	DC input voltage	With respect to ground *(3)*	–2.0 (–0.5)	7.0	V
I_{MAX}	DC V_{CC} or ground current		–300 (–400)	300 (400)	mA
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Ceramic packages, under bias		150	° C
		Plastic packages, under bias		135	° C

Table 24. EP1810 Device Recommended Operating Conditions *Note (2)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	*(4)*	4.75 (4.5)	5.25 (5.5)	V
V_I	Input voltage		–0.3	V_{CC} + 0.3	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
		For industrial use	–40	85	° C
t_R	Input rise time	*(5)*		50	ns
t_F	Input fall time	*(5)*		50	ns

Table 25. EP1810 Device DC Operating Conditions *Notes (6), (7)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	High-level input voltage		2.0	V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC *(8)*	2.4		V
	High-level CMOS output voltage	I_{OH} = –0.6 mA DC *(8)*	3.84		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC *(8)*		0.45	V
I_I	I/O pin leakage current of dedicated input pins	V_I = V_{CC} or ground	–10	10	µA
I_{OZ}	Tri-state output leakage current	V_O = V_{CC} or ground	–10	10	µA

Table 26. EP1810 Device Capacitance *Note (9)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		20	pF
C_{IO}	I/O pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		20	pF
C_{CLK1}	C_{CLK1} pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		25	pF
C_{CLK2}	C_{CLK2} pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		160	pF

Table 27. EP1810 Device I_{CC} Supply Current *Notes (2), (6), (7)*

Symbol	Parameter	Conditions	Speed Grade	Min	Typ	Max	Unit
I_{CC1}	V_{CC} supply current (non-Turbo, standby)	V_I = V_{CC} or ground, no load, *(10)*	-20, -25		50	150	µA
			-35, -45		35	150	µA
I_{CC2}	V_{CC} supply current (non-Turbo, active)	V_I = V_{CC} or ground, no load, f = 1.0 MHz *(10)*	-20, -25		20	40	mA
			-35, -45		10	30 (40)	mA
I_{CC3}	V_{CC} supply current (Turbo, active)	V_I = V_{CC} or ground, no load f = 1.0 MHz *(10)*	-20, -25		180	225 (250)	mA
			-35, -45		100	180 (240)	mA

Notes to tables:

(1) See the *Operating Requirements for Altera Devices Data Sheet* in this data book.
(2) Numbers in parentheses are for industrial-temperature-range devices.
(3) The minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for input currents less than 100 mA and periods less than 20 ns.
(4) Maximum V_{CC} rise time is 50 ms.
(5) For EP1810 clocks: t_R and t_F = 100 ns (50 ns for industrial-temperature-range versions).
(6) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(7) These values are specified in Table 24 on page 781.
(8) The I_{OH} parameter refers to high-level TTL or CMOS output current; the I_{OL} parameter refers to low-level TTL output current.
(9) The device capacitance is measured at 25° C and is sample-tested only.
(10) Measured with a device programmed as four 12-bit counters.

Tables 28 through 31 show the timing parameters for EP1810-20, EP1810-25, EP1810-35, and EP1810-45 devices.

Table 28. EP1810-20 & EP1810-25 External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	EP1810-20		EP1810-25		Non-Turbo Adder	Unit
			Min	Max	Min	Max	*(2)*	
t_{PD1}	Input to non-registered output	C1 = 35 pF		20.0		25.0	25.0	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		22.0		28.0	25.0	ns
t_{SU}	Global clock setup time		13.0		17.0		25.0	ns
t_{H}	Global clock hold time		0.0		0.0		0.0	ns
t_{CH}	Global clock high time		8.0		10.0		0.0	ns
t_{CL}	Global clock low time		8.0		10.0		0.0	ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		15.0		18.0	0.0	ns
t_{CNT}	Minimum global clock period	*(3)*		20.0		25.0	0.0	ns
f_{CNT}	Maximum internal frequency	*(3)*	50.0		40.0		0.0	MHz
t_{ASU}	Array clock setup time		8.0		10.0		25.0	ns
t_{AH}	Array clock hold time		8.0		10.0		0.0	ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		20.0		25.0	25.0	ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF *(4)*	1.0		1.0		0.0	ns
t_{ACNT}	Array clock maximum clock period	*(3)*		20.0		25.0	0.0	ns
f_{ACNT}	Maximum internal array clock frequency	*(3)*	50.0		40.0		0.0	ns
f_{MAX}	Maximum clock frequency	*(5)*	62.5		50.0		0.0	MHz

Table 29. EP1810-20 and EP1810-25 Internal Timing Parameters

Symbol	Parameter	Conditions	EP1810-20		EP1810-25		Non-Turbo Adder	Unit
			Min	Max	Min	Max	*(2)*	
t_{IN}	Input pad and buffer delay			5.0		7.0	0.0	ns
t_{IO}	I/O input pad and buffer delay			2.0		3.0	0.0	ns
t_{LAD}	Logic array delay			9.0		12.0	25.0	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		6.0		6.0	0.0	ns
t_{ZX}	Output buffer enable delay	C1 = 35 pF		6.0		6.0	0.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF *(6)*		6.0		6.0	0.0	ns
t_{SU}	Register setup time		8.0		10.0		0.0	ns
t_{H}	Register hold time		5.0		10.0		0.0	ns
t_{IC}	Array clock delay			9.0		12.0	25.0	ns
t_{ICS}	Global clock delay			4.0		5.0	0.0	ns
t_{FD}	Feedback delay			3.0		3.0	–25.0	ns
t_{CLR}	Register clear time			9.0		12.0	25.0	ns

Table 30. EP1810-35 & EP1810-45 External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	EP1810-35		EP1810-45		Non-Turbo Adder	Unit
			Min	Max	Min	Max	*(2)*	
t_{PD1}	Input to non-registered output	C1 = 35 pF		35.0		45.0	30.0	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		40.0		50.0	30.0	ns
t_{SU}	Global clock setup time		25.0		30.0		30.0	ns
t_{H}	Global clock hold time		0.0		0.0		0.0	ns
t_{CH}	Global clock high time		12.0		15.0		0.0	ns
t_{CL}	Global clock low time		12.0		15.0		0.0	ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		20.0		25.0	0.0	ns
t_{CNT}	Minimum global clock period	*(3)*		35.0		45.0	0.0	ns
f_{CNT}	Maximum internal frequency	*(3)*	28.6		22.2		0.0	MHz
t_{ASU}	Array clock setup time		10.0		11.0		30.0	ns
t_{AH}	Array clock hold time		15.0		18.0		0.0	ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		35.0		45.0	30.0	ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF *(4)*	1.0		1.0			ns
t_{ACNT}	Array clock maximum clock period	*(3)*		35.0		45.0	0.0	ns
f_{ACNT}	Maximum internal array clock frequency	*(3)*	28.6		22.2		0.0	ns
f_{MAX}	Maximum clock frequency	*(5)*	40		33.3		0.0	MHz

Table 31. EP1810-35 & EP1810-45 Internal Timing Parameters

Symbol	Parameter	Conditions	EP1810-35		EP1810-45		Non-Turbo Adder	Unit
			Min	Max	Min	Max	*(2)*	
t_{IN}	Input pad and buffer delay			7.0		6.0	0.0	ns
t_{IO}	I/O input pad and buffer delay			5.0		5.0	0.0	ns
t_{LAD}	Logic array delay			19.0		28.0	30.0	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		9.0		11.0	0.0	ns
t_{ZX}	Output buffer enable delay	C1 = 35 pF		9.0		11.0	0.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF *(6)*		9.0		11.0	0.0	ns
t_{SU}	Register setup time		10.0		10.0		0.0	ns
t_{H}	Register hold time		15.0		18.0		0.0	ns
t_{IC}	Array clock delay			19.0		28.0	30.0	ns
t_{ICS}	Global clock delay			4.0		8.0	0.0	ns
t_{FD}	Feedback delay			6.0		7.0	–30.0	ns
t_{CLR}	Register clear time			24.0		32.0	30.0	ns

Notes to tables:
(1) These values are specified in Table 24 on page 781.
(2) The non-Turbo adder must be added to this parameter when the Turbo Bit option is off.
(3) Measured with a device programmed as four 12-bit counters.
(4) Sample-tested only. This parameter is a guideline based on extensive device characterization. This parameter applies for both global and array clocking.
(5) The f_{MAX} values represent the highest frequency for pipelined data.
(6) Sample-tested only for an output change of 500 mV.

Pin-Out Information

Table 32 provides pin-out information for EP1810 devices in 68-pin PGA packages.

Table 32. EP1810 PGA Pin-Outs

Pin	Function	Pin	Function	Pin	Function	Pin	Function
A2	I/O	B9	I/O	F10	GND	K4	INPUT
A3	I/O	B10	I/O	F11	I/O	K5	INPUT
A4	I/O	B11	I/O	G1	I/O	K6	VCC
A5	INPUT	C1	I/O	G2	I/O	K7	INPUT
A6	CLK4/INPUT	C2	I/O	G10	I/O	K8	INPUT
A7	CLK3/INPUT	C10	I/O	G11	I/O	K9	I/O
A8	INPUT	C11	I/O	H1	I/O	K10	I/O
A9	I/O	D1	I/O	H2	I/O	K11	I/O
A10	I/O	D2	I/O	H10	I/O	L2	I/O
B1	I/O	D10	I/O	H11	I/O	L3	I/O
B2	I/O	D11	I/O	J1	I/O	L4	INPUT
B3	I/O	E1	I/O	J2	I/O	L5	CLK1/INPUT
B4	INPUT	E2	I/O	J10	I/O	L6	CLK2/INPUT
B5	INPUT	E10	I/O	J11	I/O	L7	INPUT
B6	VCC	E11	I/O	K1	I/O	L8	I/O
B7	INPUT	F1	I/O	K2	I/O	L9	I/O
B8	INPUT	F2	GND	K3	I/O	L10	I/O