

TLE9852QX

Arm® Cortex®-M0 Microcontroller with LIN and H-Bridge NFET Driver for Automotive Applications AD_Step



1 Overview

Features

- 32-bit Arm® Cortex®-M0 Core
 - up to 40 MHz clock frequency
 - one clock per machine cycle architecture
 - single cycle multiplier
- On-chip memory
 - 48 KB Flash (including EEPROM)
 - 4 KB EEPROM (emulated in Flash)
 - 512 bytes 100 Time Programmable Memory (100TP)
 - 4 KB RAM
 - Boot ROM for startup firmware and Flash routines
- Math Co-Processor Unit with Divider Unit for signed and unsigned 32-bit division operations
- On-chip OSC and PLL for clock generation
 - PLL loss-of-lock detection
- MOSFET Driver including charge pump for H-Bridge motor applications
- High-Side Switch with cyclic sense option and PWM functionality, e.g. for supplying LEDs or switch panels (min. 150 mA)
- 4 High Voltage Monitor Input pins for wake-up and with cyclic sense with analog measurement option
- 10 General-purpose I/O Ports (GPIO)
- 5 Analog input Ports
- 10-Bit A/D Converter with 5 analog inputs + VBAT_SENSE + VS + 4 high voltage monitoring inputs
- 8-Bit A/D Converter with 9 inputs for voltage and temperature supervision
- Measurement unit with 11 channels together with the onboard 10-Bit A/D converter and data post processing
- 16-Bit timers - GPT12, Timer 2 and Timer 21
- Capture/compare unit for PWM signal generation (CCU6)



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Overview

- 2 full duplex serial interfaces (UART1, UART2), UART1 with LIN support
- 2 synchronous serial channels (SSC1, SSC2)
- On-chip debug support via 2-wire SWD
- 1 LIN 2.2 transceiver
- Single power supply $V_S = 5.5\text{ V to }28\text{ V}$
- Extended supply voltage range $V_S = 3\text{ V to }28\text{ V}$
- Low-dropout voltage regulators (LDO)
- 5 V voltage supply VDDEXT for external loads (e.g. Hall-sensor)
- Core logic supply at 1.5 V
- Programmable window watchdog (WDT1) with independent on-chip clock source
- Power saving modes:
 - Micro Controller Unit slow-down mode
 - Sleep Mode with cyclic sense option
 - Cyclic wake-up during Sleep Mode
 - Stop Mode with cyclic sense option
- Power-on and undervoltage/brownout reset generator
- Overtemperature protection incl. shutdown
- Short circuit protection for all voltage regulators and actuators (High Side Switch)
- Loss of clock detection with fail safe mode for power switches
- Temperature Range $T_j = -40^\circ\text{C to }+150^\circ\text{C}$
- Package VQFN-48-31 with LTI feature
- Green package (RoHS compliant)
- AEC Qualified

Potential applications

- Window lift
- ... and other LIN addressed motor control applications

Product validation

Qualified for Automotive Applications. Product Validation according to AEC-Q100/101

Description

TLE985x devices integrate an Arm® Cortex®-M0 processor and peripherals for motor control, power supply and communication. Two integrated measurement units (analog-to-digital converters) for monitoring temperature, battery voltage and four monitoring inputs help to save pins. These inputs can be operated directly with battery voltage, which saves costs on additional components such as external voltage dividers or shutdown transistors. Furthermore, the chips are equipped with two full duplex serial interfaces (UART) with LIN support.

A new feature in the TLE985x family is its adaptive MOSFET driver. The control algorithm is able to compensate MOSFET parameter spread in the system by automatically adjusting the gate current according to required switching times. This allows an optimization of the system concerning EME (electro-magnetic emissions, slow slew rates) as well as power dissipation (short dead times) simultaneously.

Overview

The product family includes several devices with different flash sizes (48 - 96KB) and temperature ranges (T_j up to 175°C). In addition, different numbers of half-bridge drivers for uni- or bidirectional DC motor applications are offered.

All TLE985x products are based on the same hardware and software platform as Infineon's other Embedded Power products (TLE984x, TLE986x and TLE987x), thus enabling design synergies and allowing customers to reuse parts of the software. The devices come in a leadless VQFN package with a footprint of 7x7 mm.

| Type | Package | Marking |
|-----------|------------|-----------|
| TLE9852QX | VQFN-48-31 | TLE9852QX |

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Block Diagram

2 Block Diagram

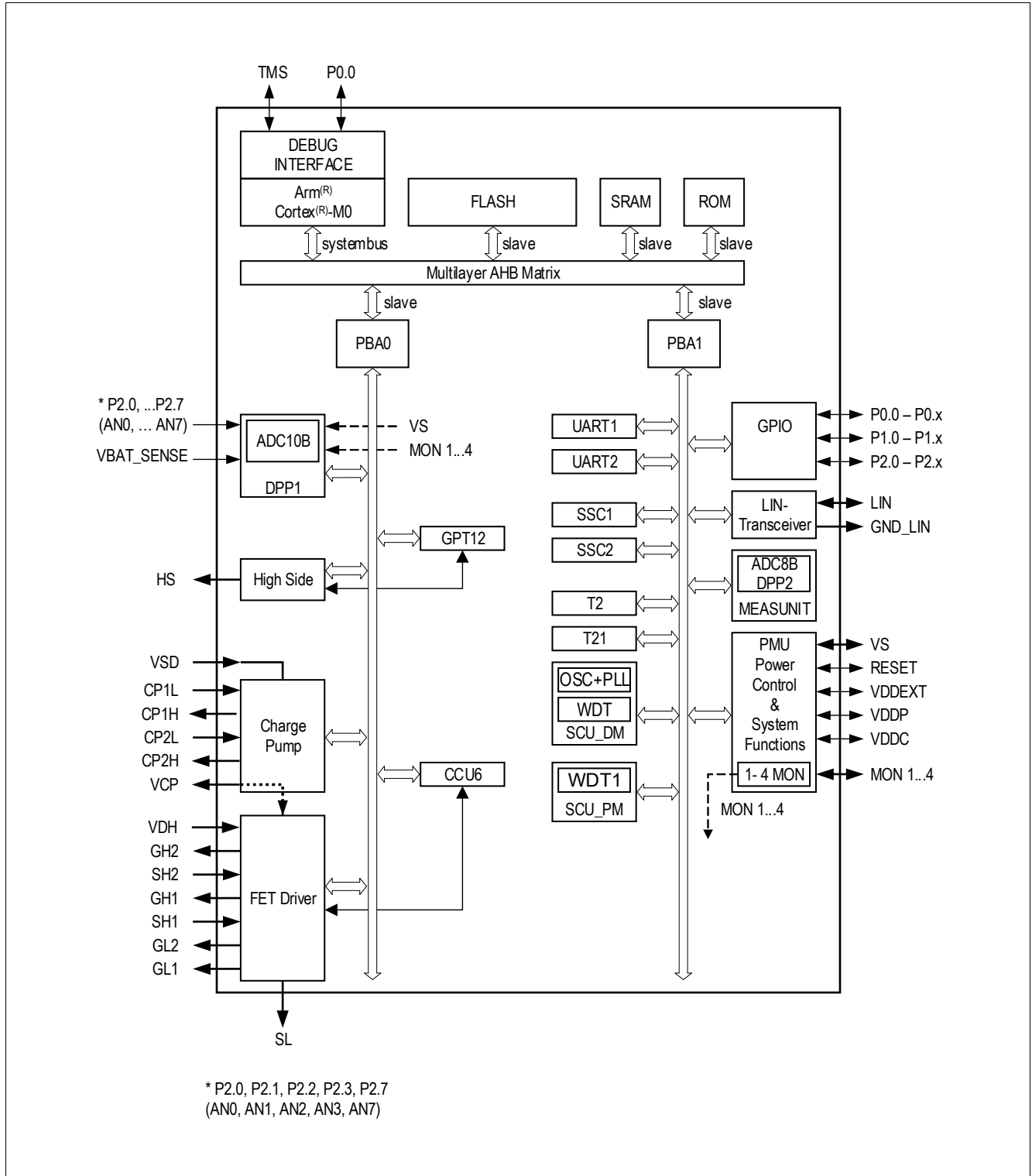


Figure 1 Block Diagram TLE9852QX

General Device Information

3 General Device Information

3.1 Pin Configurations

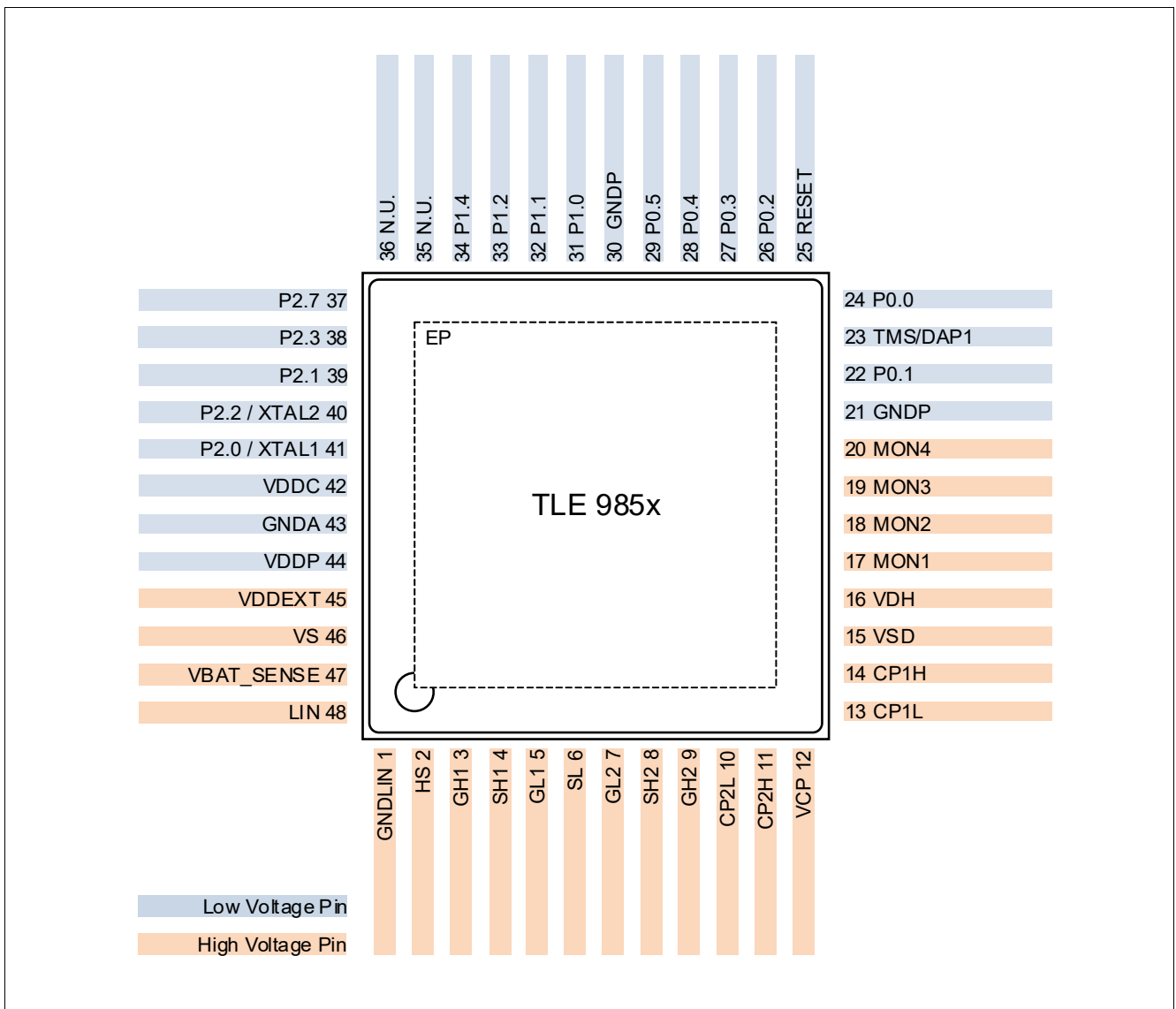


Figure 2 Pin Configuration VQFN-48, TLE9852QX

General Device Information

3.2 Pin Definitions and Functions

After reset, all pins are configured as input (except supply and LIN pins) with one of the following settings:

- Pull-up enabled only (PU)
- Pull-down enabled only (PD)
- Input with both pull-up and pull-down disabled (I)
- Output with output stage deactivated = high impedance state (Hi-Z)

The functions and default states of the TLE9852QX external pins are provided in the following table.

Type: indicates the pin type.

- I/O: Input or output
- I: Input only
- O: Output only
- P: Power supply

Not all alternate functions listed, see [Chapter 14](#).

Table 1 Pin Definitions and Functions

| Symbol | Pin Number | Type | Reset State | Function |
|-----------|------------|------|-------------|---|
| P0 | | | | Port 0 Port 0 is a 6-Bit bidirectional general purpose I/O port. Alternate functions can be assigned and are listed in the Port description. Main function is listed below. |
| P0.0 | 24 | I/O | I/PU | SWD_CLK Serial Wire Debug Clock GPIO General Purpose IO Alternate function mapping see Table 7 |
| P0.1 | 22 | I/O | I/PU | GPIO General Purpose IO Alternate function mapping see Table 7 |
| P0.2 | 26 | I/O | I/PD | GPIO General Purpose IO Alternate function mapping see Table 7 |
| P0.3 | 27 | I/O | I/PU | GPIO General Purpose IO Alternate function mapping see Table 7 |
| P0.4 | 28 | I/O | I/PU | GPIO General Purpose IO Alternate function mapping see Table 7 |
| P0.5 | 29 | I/O | I/PU | GPIO General Purpose IO Alternate function mapping see Table 7 |
| P1 | | | | Port 1 Port 1 is a 4-Bit bidirectional general purpose I/O port. Alternate functions can be assigned and are listed in the Port description. Main function is listed below. |
| P1.0 | 31 | I/O | I | GPIO General Purpose IO Alternate function mapping see Table 8 |
| P1.1 | 32 | I/O | I | GPIO General Purpose IO Alternate function mapping see Table 8 |
| P1.2 | 33 | I/O | I | GPIO General Purpose IO Alternate function mapping see Table 8 |

General Device Information

Table 1 Pin Definitions and Functions (cont'd)

| Symbol | Pin Number | Type | Reset State | Function |
|-----------|------------|--------|-------------|---|
| P1.4 | 34 | I/O | I | GPIO General Purpose IO Alternate function mapping see Table 8 |
| P2 | | | | Port 2 Port 2 is a 5-Bit general purpose input-only port. Alternate functions can be assigned and are listed in the Port description. Main function is listed below. |
| P2.0 | 41 | I | I | AN0 XTAL1 ¹⁾ ADC1 analog input channel 6 External oscillator input Alternate function mapping see Table 9 |
| P2.1 | 39 | I | I | AN1 ADC1 analog input channel 7 Alternate function mapping see Table 9 |
| P2.2 | 40 | I O | I Hi-Z | AN2 XTAL2 ¹⁾ ADC1 analog input channel 8 External oscillator output Alternate function mapping see Table 9 |
| P2.3 | 38 | I | I | AN3 ADC1 analog input channel 9 Alternate function mapping see Table 9 |
| P2.7 | 37 | I | I | AN7 ADC1 analog input channel 12 Alternate function mapping see Table 9 |

Power Supply

| | | | | |
|--------|--------|---|---|---|
| VS | 46 | P | – | Battery supply input |
| VDDP | 44 | P | – | I/O port supply (5.0 V). Do not connect external loads. For buffer and bypass capacitors. |
| VDDC | 42 | P | – | Core supply (1.5 V during Active Mode, 0.9 V during Stop Mode). Do not connect external loads. For buffer/bypass capacitor. |
| VDDEXT | 45 | P | – | External voltage supply output (5.0 V, 40 mA) |
| GNDP | 21, 30 | P | – | Core supply ground |
| GND A | 43 | P | – | Analog supply ground |
| GNDLIN | 1 | P | – | LIN ground |

Monitor Inputs

| | | | | |
|------|----|---|---|------------------------------|
| MON1 | 17 | I | I | High Voltage Monitor Input 1 |
| MON2 | 18 | I | I | High Voltage Monitor Input 2 |
| MON3 | 19 | I | I | High Voltage Monitor Input 3 |
| MON4 | 20 | I | I | High Voltage Monitor Input 4 |

High Side Switch Outputs

| | | | | |
|----|---|---|------|-------------------------|
| HS | 2 | O | Hi-Z | High Side Switch output |
|----|---|---|------|-------------------------|

LIN Interface

| | | | | |
|-----|----|-----|----|--------------------------------|
| LIN | 48 | I/O | PU | LIN bus interface input/output |
|-----|----|-----|----|--------------------------------|

Charge Pump

| | | | | |
|------|----|---|---|---|
| CP1H | 14 | P | – | Charge Pump Capacity 1 High, connect external C |
|------|----|---|---|---|

General Device Information

Table 1 Pin Definitions and Functions (cont'd)

| Symbol | Pin Number | Type | Reset State | Function |
|--------|------------|------|-------------|---|
| CP1L | 13 | P | – | Charge Pump Capacity 1 Low, connect external C |
| CP2H | 11 | P | – | Charge Pump Capacity 2 High, connect external C |
| CP2L | 10 | P | – | Charge Pump Capacity 2 Low, connect external C |
| VCP | 12 | P | – | Charge Pump Capacity |
| VSD | 15 | P | – | Battery supply input for Charge Pump |

MOSFET Driver

| | | | | |
|-----|----|---|---|---------------------------------------|
| VDH | 16 | P | – | Voltage Drain High Side MOSFET Driver |
| GH1 | 3 | P | – | Gate High Side FET 1 |
| GH2 | 9 | P | – | Gate High Side FET 2 |
| SH1 | 4 | P | – | Source High Side FET 1 |
| SH2 | 8 | P | – | Source High Side FET 2 |
| GL1 | 5 | P | – | Gate Low Side FET 1 |
| GL2 | 7 | P | – | Gate Low Side FET 2 |
| SL | 6 | P | – | Source Low Side FETs |

Others

| | | | | |
|------------|--------|-----|--------|---|
| TMS | 23 | I | I/PD | TMS test mode select input DAP1 |
| RESET | 25 | I/O | I/O/PU | Bidirectional reset input/output, not available during Sleep Mode |
| VBAT_SENSE | 47 | I | I | Battery supply voltage sense input |
| EP | – | – | – | Exposed Pad, connect to GND |
| N.U. | 35, 36 | I | – | Not used, shall be connected to GND |

1) configurable by user

Modes of Operations

4 Modes of Operations

This highly integrated circuit contains analog and digital functional blocks. For system and interface control an embedded 32-Bit Arm® Cortex®-M0 microcontroller is included. For internal and external power supply purposes, on-chip low drop-out regulators are existent. An internal oscillator (no external components necessary) provides a cost effective and suitable clock in particular for LIN slave nodes. As communication interface, a LIN transceiver and several High Voltage Monitor Inputs with adjustable threshold and filters are available. Furthermore one High-Side Switch (e.g. for driving LEDs or powering of switches), a driver for 4 n-channel MOSFETs including a two-stage charge pump and several general purpose input/outputs (GPIO) with pulse-width modulation (PWM) capabilities are available.

The Micro Controller Unit supervision and system protection including reset feature is controlled by a programmable window watchdog. A cyclic wake-up circuit, supply voltage supervision and integrated temperature sensors are available on-chip.

All relevant modules offer power saving modes in order to support terminal 30 connected automotive applications. A wake-up from the power saving mode is possible via a LIN bus message, via the monitoring inputs or repetitive with a programmable time period (cyclic wake-up).

The integrated circuit is available in a VQFN-48-31 package with 0.5 mm pitch and is designed to withstand the challenging conditions of automotive applications.

The TLE9852QX has several operational modes mainly to support low power consumption requirements. The low power modes and state transitions are depicted in **Figure 3** below.

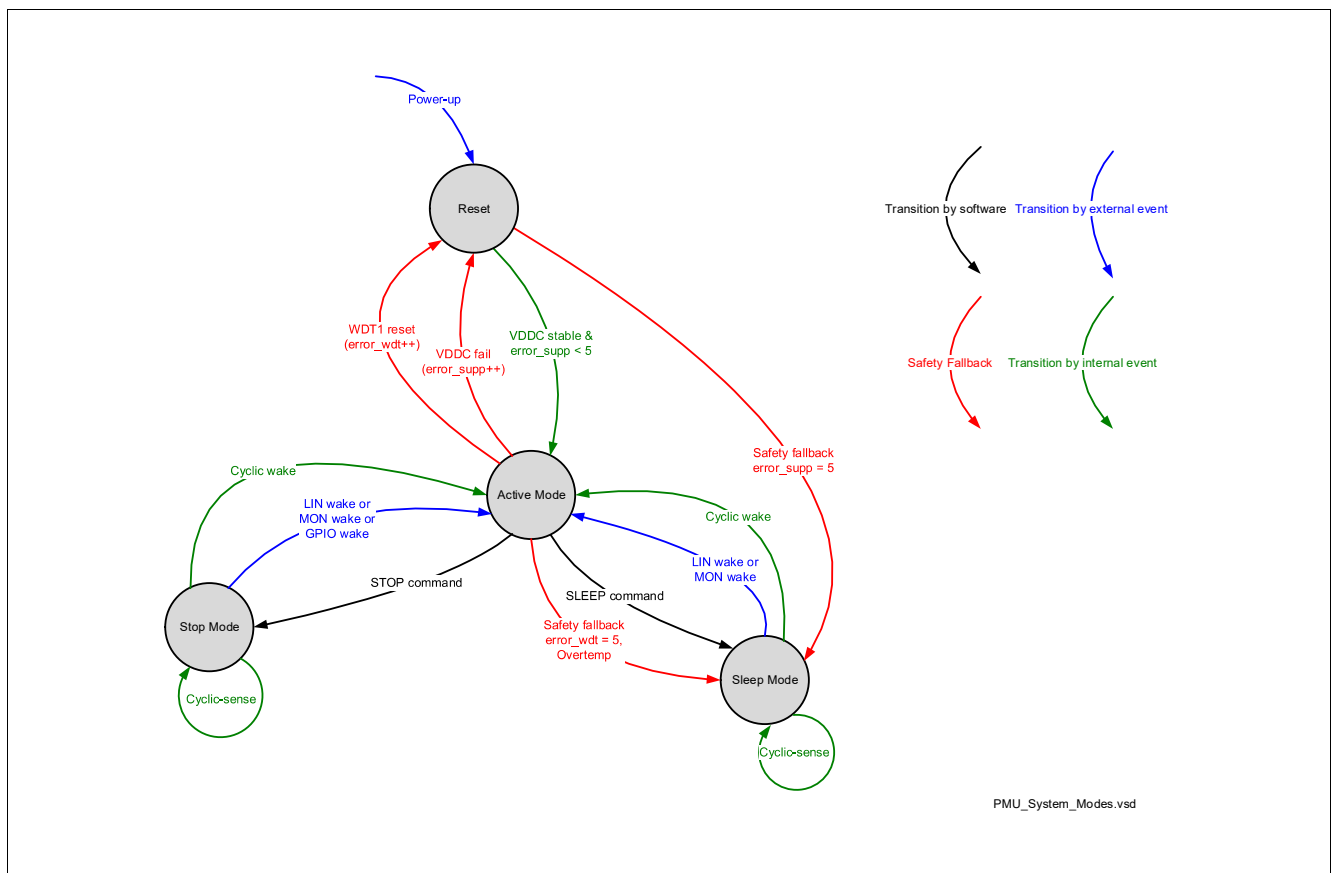


Figure 3 Power Control State Diagram

Modes of Operations

Reset Mode

The Reset Mode is a transition mode e.g. during power-up of the device after a power-on reset. In this mode the on-chip power supplies are enabled and all other modules are initialized. Once the core supply VDDC is stable, the Active Mode is entered. In case the watchdog timer WDT1 fails for more than four times, a fail-safe transition to the Sleep Mode is done.

Active Mode

In Active Mode all modules are activated and the TLE9852QX is fully operational.

Stop Mode

The Stop Mode is one out of two major low power modes. The transition to the low power modes is done by setting the respective Bits in the mode control register. In Stop Mode the embedded microcontroller is still powered allowing faster wake-up reaction times, but not clocked. A wake-up from this mode is possible by LIN bus activity, the High Voltage Monitor Input pins or the respective 5V GPIOs.

Sleep Mode

The Sleep Mode is a major low-power mode. The transition to the low-power modes is done by setting the respective Bits in the Micro Controller Unit mode control register. The sleep time is configurable. In Sleep Mode the embedded microcontroller power supply is deactivated, allowing the lowest system power consumption, but the wake-up time is longer compared to the Stop Mode. In this mode a 64 bit wide buffer for data storage is available. A wake-up from this mode is possible by LIN bus activity or the High Voltage Monitor Input pins and cyclic wake. A wake-up from Sleep Mode behaves similar to a power-on reset. While changing into Sleep Mode, no incoming wake-requests are lost (i.e. no dead-time). It is possible to enter sleep-mode even with LIN dominant.

Cyclic Wake-up Mode

The cyclic wake-up mode is a special operating mode of the Sleep Mode and the Stop Mode. The transition to the cyclic wake-up mode is done by first setting the respective Bits in the mode control register followed by the SLEEP or STOP command. Additional to the cyclic wake-up behavior (wake-up after a programmable time period), the wake-up sources of the normal Stop Mode and Sleep Mode are available.

Cyclic Sense Mode

The cyclic sense mode is a special operating mode of the Sleep Mode and the Stop Mode. The transition to the cyclic sense mode is done by first setting the respective Bits in the mode control register followed by the STOP or SLEEP command. In cyclic sense mode the High Side Switch can be switched on periodically for biasing some switches for example. The wake-up condition is configurable, when the sense result of defined monitor inputs at a window of interest changed compared to the previous wake-up period or reached a defined state respectively. In this case the Active Mode is entered immediately.

The following table shows the possible power mode configurations of each major module or function respectively.

Table 2 Power Mode Configurations

| Module/function | Active Mode | Sleep Mode | Stop Mode | Comment |
|------------------|-------------|---------------|---------------|--------------|
| VPRE, VDDP, VDDC | ON | OFF | ON | – |
| VDDEXT | ON/OFF | OFF | cyclic ON/OFF | – |
| HS | ON/OFF | cyclic ON/OFF | cyclic ON/OFF | cyclic sense |

Modes of Operations

Table 2 Power Mode Configurations (cont'd)

| Module/function | Active Mode | Sleep Mode | Stop Mode | Comment |
|----------------------------|---------------------------------|-------------------------------------|-------------------------------------|--|
| Bridge Driver | ON/OFF | OFF ¹⁾ | OFF ¹⁾ | – |
| LIN TRx | ON/OFF | wake-up only / OFF | wake-up only/ OFF | – |
| MONx (wake-up) | n.a. | disabled/static/ cyclic | disabled/static/ cyclic | cyclic: combined with HS=on |
| MONx (measurement) | ON/OFF | OFF | OFF | available on all channels |
| VS sense | ON/OFF brownout detection | brownout detection | brownout detection | brownout det. done in PCU |
| VBAT_SENSE | ON/OFF | OFF | OFF | – |
| GPIO 5V | ON | OFF | ON | – |
| WDT1 | ON | OFF | OFF | – |
| CYCLIC WAKE | n.a. | cyclic wake-up/ cyclic sense/OFF | cyclic wake-up/ cyclic sense/OFF | cyclic sense with HS; wake-up needs MC for enter Sleep Mode again |
| Measurement | ON ²⁾ | OFF | OFF | – |
| Micro Controller Unit | ON/slow- down/STOP | OFF | OFF | – |
| CLOCK GEN (MC) | ON | OFF | OFF | – |
| LP_CLK (f_{LP_CLK}) | ON | OFF | OFF | WDT1 |
| LP_CLK2 (f_{LP_CLK2}) | ON | ON | ON | for cyclic wake-up |

1) Bridge Driver “Hold Mode” is available in sleep mode and stop mode.

2) May not be switched off due to safety reasons

Wake-up Source Prioritization

All wake-up sources have the same priority. In order to handle the asynchronous nature of the wake-up sources, the first wake-up signal will initiate the wake-up sequence. Nevertheless all wake-up sources are latched in order to provide all wake-up events to the application software. The software can clear the wake-up source flags. It is ensured, that no wake-up event is lost.

As default wake-up sources, MON inputs and cyclic wake are activated after power-on reset, LIN is disabled as wake-up source by default.

Wake-up Levels and Transitions

The wake-up can be triggered by rising, falling or both signal edges for each monitor input individually.

5 Power Management Unit (PMU)

5.1 Features

- System modes control (startup, sleep, stop and active)
- Power management (cyclic wake, cyclic sense)
- Control of system voltage regulators with diagnosis (overload, short, overvoltage)
- Fail safe mode detection and operation in case of system errors
- Wake-up sources configuration and management (LIN, MON, GPIOs)
- System error logging

5.2 Introduction

The purpose of the power management unit is to ensure the fail safe behavior of the system IC. Therefore the power management unit controls all system modes including the corresponding transitions. The power management unit is responsible for generating all needed voltage supplies for the embedded MCU (VDDC, VDDP) and the external supply (VDDEXT). Additionally, the PMU provides well defined sequences for the system mode transitions and generates hierarchical reset priorities. The reset priorities control the reset behavior of all system functionalities especially the reset behavior of the embedded MCU. All these functions are controlled by finite state machines. The system master functionality of the PMU requires the generation of an independent logic supply and system clock. Therefore the PMU has a module internal logic supply and system clock which works independently of the MCU clock.

Power Management Unit (PMU)

5.2.1 Block Diagram

The following figure shows the structure of the Power Management Unit. **Table 3** describes the submodules more detailed.

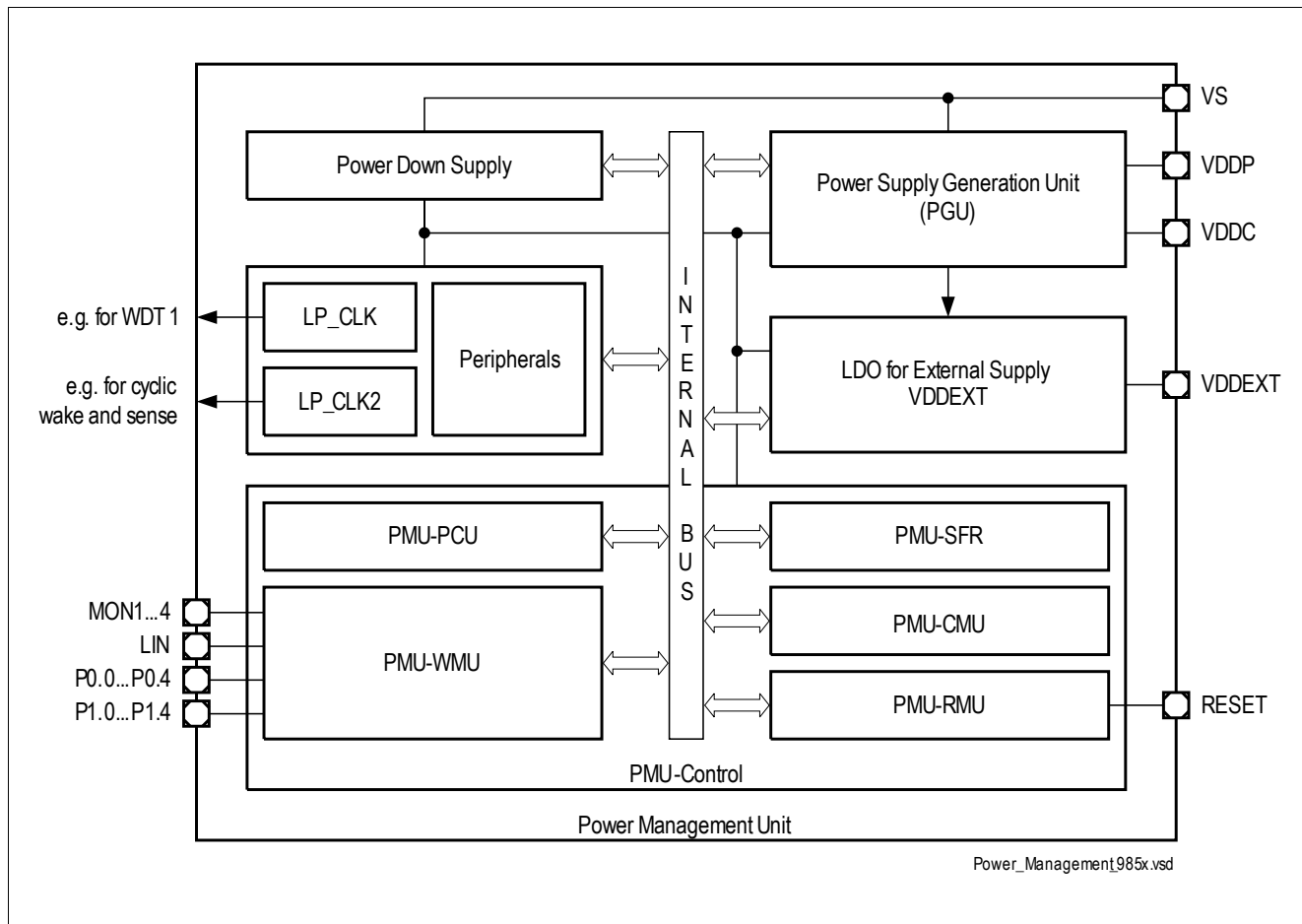


Figure 4 Power Management Unit Block Diagram

Table 3 Description of PMU Submodules

| Mod. Name | Modules | Functions |
|-----------------------------|---|--|
| Power Down Supply | Independent Supply Voltage Generation for PMU | This supply is dedicated to the PMU to ensure an independent operation from generated power supplies (VDDP, VDDC). |
| LP_CLK (= f_{LP_CLK}) | <ul style="list-style-type: none"> - Clock Source for all PMU submodules - Backup Clock Source for System (can be selected as fsys clock source through SCU_APCLK.SYSCLKSEL) - Clock Source for WDT1 | <p>This ultra low power oscillator generates the clock for the PMU.</p> <p>This clock is also used as backup clock for the system in case of PLL Clock failure and as independent clock source for WDT1.</p> |
| LP_CLK2 (= f_{LP_CLK2}) | Clock Source for PMU | This ultra low power oscillator generates the clock for the PMU in Stop Mode and in the cyclic modes. |

Power Management Unit (PMU)
Table 3 Description of PMU Submodules (cont'd)

| Mod. Name | Modules | Functions |
|------------------------------------|--|---|
| Peripherals | Peripheral Blocks of PMU | These blocks include the analog peripherals to ensure a stable and fail safe PMU startup and operation (bandgap, bias). |
| Power Supply Generation Unit (PGU) | Voltage regulators for VDDP and VDDC | This block includes the voltage regulators for the pad supply (VDDP) and the core supply (VDDC). |
| VDDEXT | Voltage regulator for VDDEXT to supply external modules (e.g. Sensors) | This voltage regulator is a dedicated supply for external modules. |
| PMU-SFR | All PMU relevant Extended Special Function Registers | This module contains all PMU relevant registers, which are needed to control and monitor the PMU. |
| PMU-PCU | Power Control Unit of the PMU | This block is responsible for controlling all power related actions within the PGU Module. It also contains all regulator related diagnosis like under- and overvoltage detection, overcurrent and short circuit diagnoses. |
| PMU-WMU | Wake-up Management Unit of the PMU | This block is responsible for controlling all Wake-up related actions within the PMU Module. |
| PMU-CMU | Cyclic Management Unit of the PMU | This block is responsible for controlling all actions within cyclic mode. |
| PMU-RMU | Reset Management Unit of the PMU | This block generates resets triggered by the PMU like undervoltage or short circuit reset, and passes all resets to the relevant modules and their register. A reset status register with every reset source is available. |

Power Management Unit (PMU)

5.2.2 PMU Modes Overview

The following state diagram shows the available modes of the device.

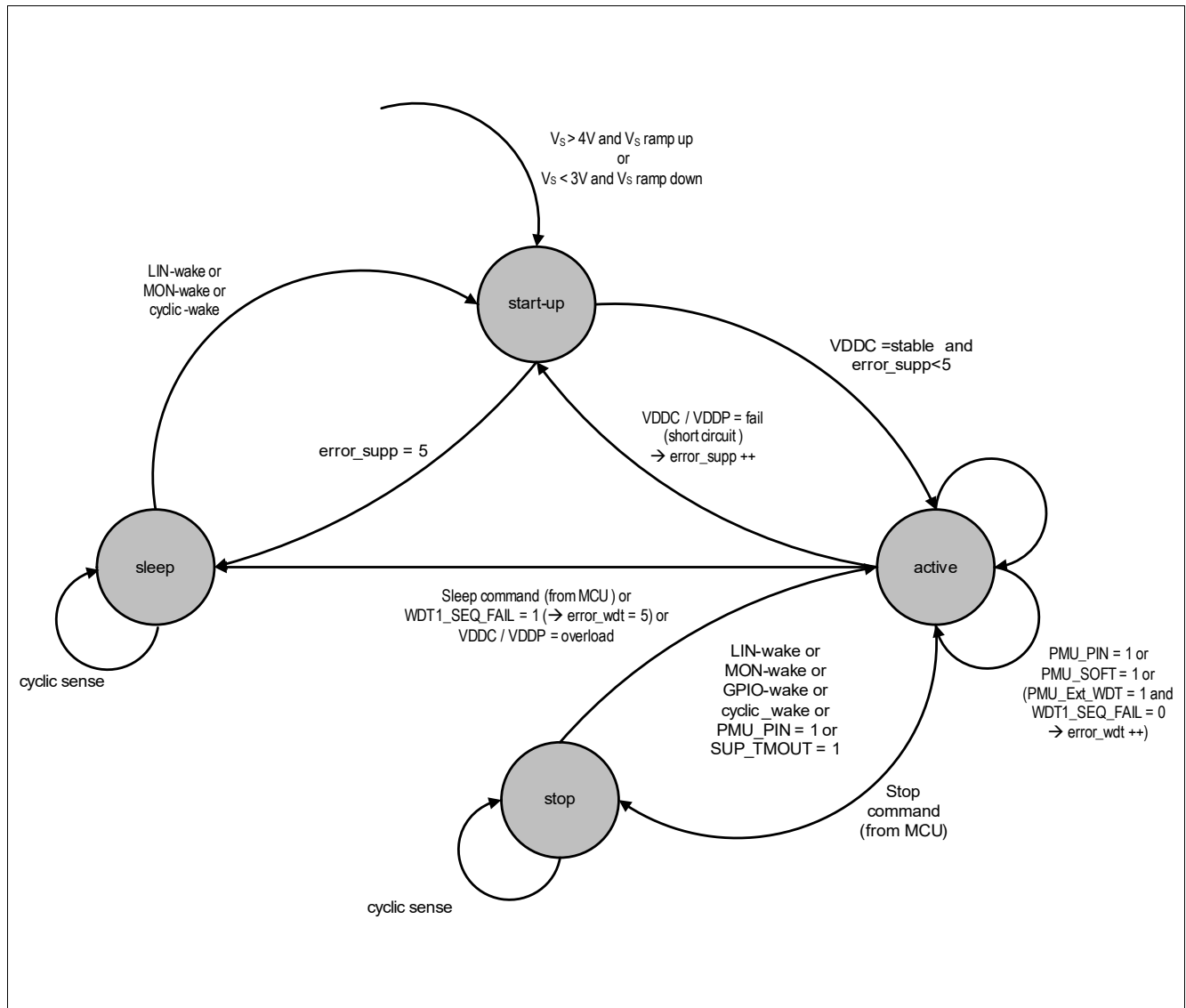


Figure 5 Power Management Unit System Modes

Power Management Unit (PMU)

5.3 Power Supply Generation (PGU)

5.3.1 Voltage Regulator 5.0V (VDDP)

This module represents the 5 V voltage regulator, which provides the pad supply for the parallel port pins and other 5 V analog functions (e.g. LIN Transceiver).

Features

- 5 V low-drop voltage regulator
- Overcurrent Monitoring and Shutdown with MCU signalling (Interrupt)
- Overvoltage monitoring with MCU signalling (Interrupt)
- Undervoltage monitoring with MCU signalling (Interrupt)
- Undervoltage monitoring with Reset (UnderVoltage Reset, V_{DDPUV})
- Overtemperature Shutdown with MCU signalling (Interrupt)
- Pre-Regulator for VDDC Regulator
- GPIO Supply
- Pull Down Current Source at the output for Sleep Mode only

The output capacitor C_{VDDP} is mandatory to ensure a proper regulator functionality.

Power Management Unit (PMU)

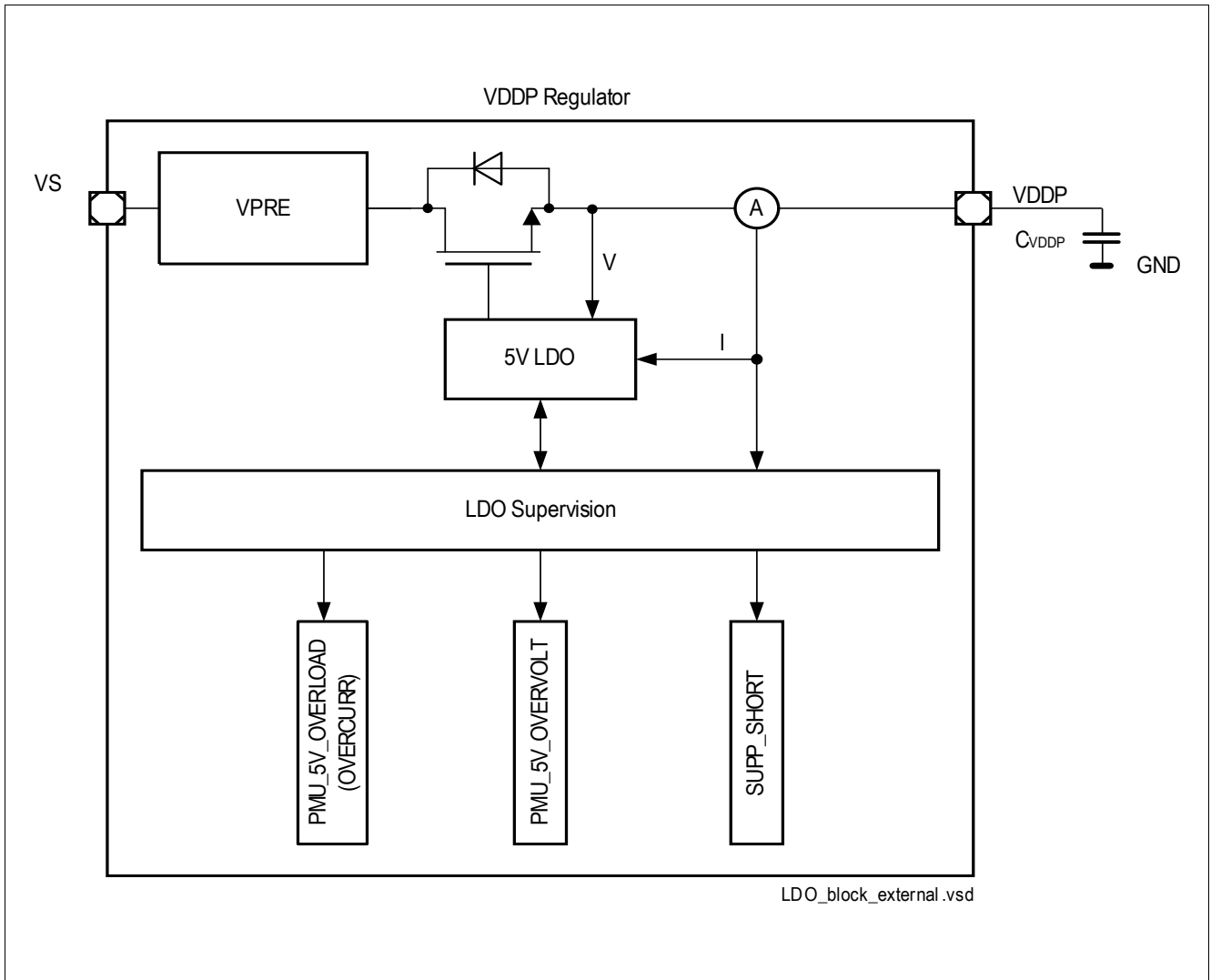


Figure 6 Module Block Diagram of VDDP Voltage Regulator

Power Management Unit (PMU)

5.3.2 Voltage Regulator 1.5V (VDDC)

This module represents the 1.5 V voltage regulator, which provides the supply for the microcontroller core, digital peripherals and other chip internal analog 1.5 V functions (e.g. ADC).

Features

- 1.5 V low-drop voltage regulator
- Overcurrent monitoring and Shutdown with MCU signalling (Interrupt)
- Overvoltage monitoring with MCU signalling (Interrupt)
- Undervoltage monitoring with MCU signalling (interrupt)
- Undervoltage monitoring with reset
- Overtemperature Shutdown with MCU signalling (Interrupt)
- Pull Down Current Source at the output for Sleep Mode only

The output capacitor C_{VDDC} is mandatory to ensure a proper regulator functionality.

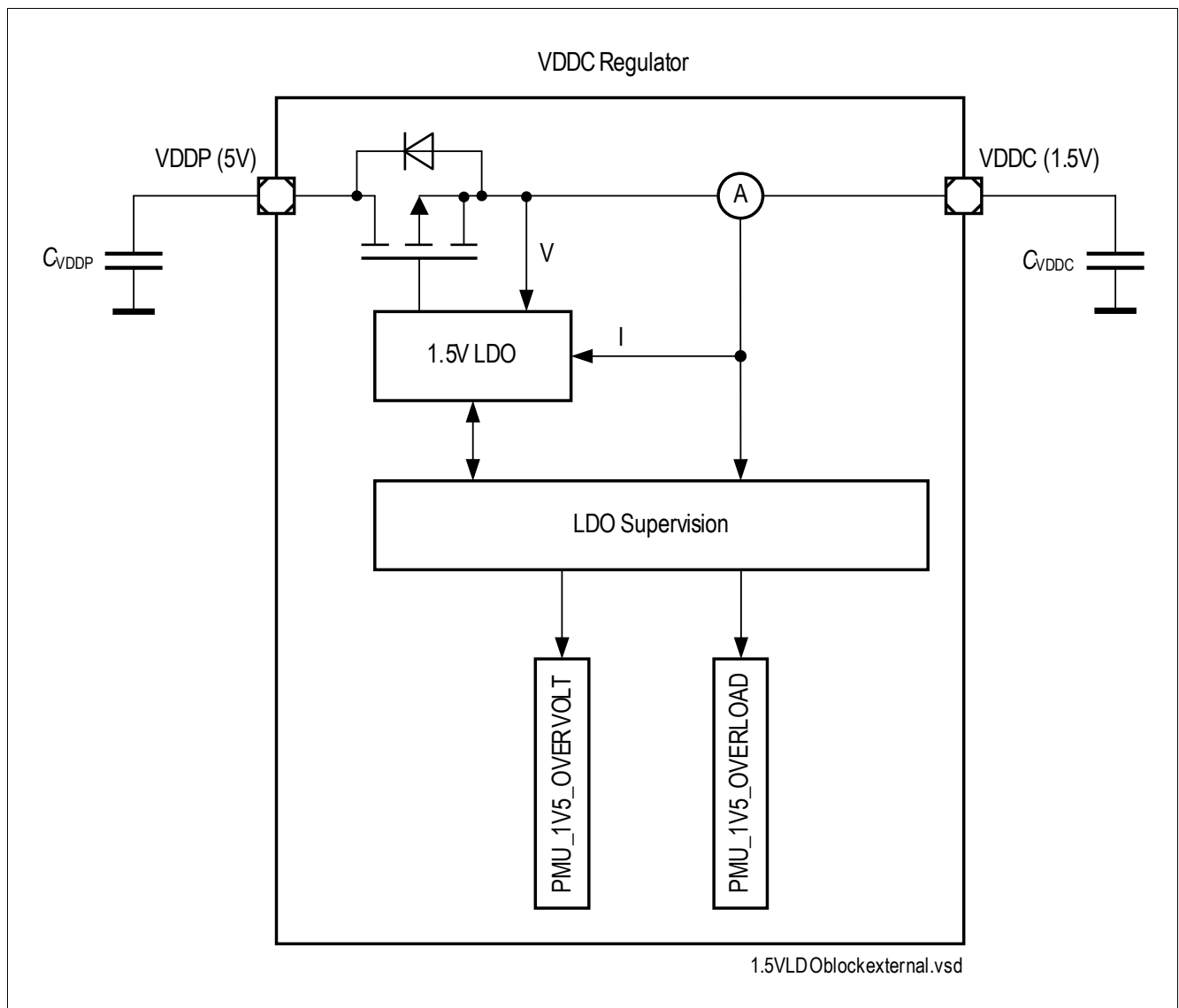


Figure 7 Module Block Diagram of VDDC Voltage Regulator

Power Management Unit (PMU)

5.3.3 External Voltage Regulator 5.0V (VDDEXT)

This module represents the 5 V voltage regulator, which serves as a supply for external circuits. It can be used e.g. to supply an external sensor, LEDs or potentiometers.

Features

- Switchable (by software) 5 V low-drop voltage regulator
- Switch-on undervoltage blanking time in order to drive small capacitive loads
- Intrinsic current limitation
- Undervoltage monitoring and shutdown with MCU signalling (Interrupt)
- Overtemperature Shutdown with MCU signalling (Interrupt)
- Resistive discharge path at the output if the regulator is off
- Cyclic sense option together with GPIOs
- Low current mode available to ensure reduced stop mode current consumption. In this mode current capability is reduced to I_{VDDEXT_LCM}

The output capacitor C_{VDDEXT} is mandatory to ensure a proper regulator functionality.

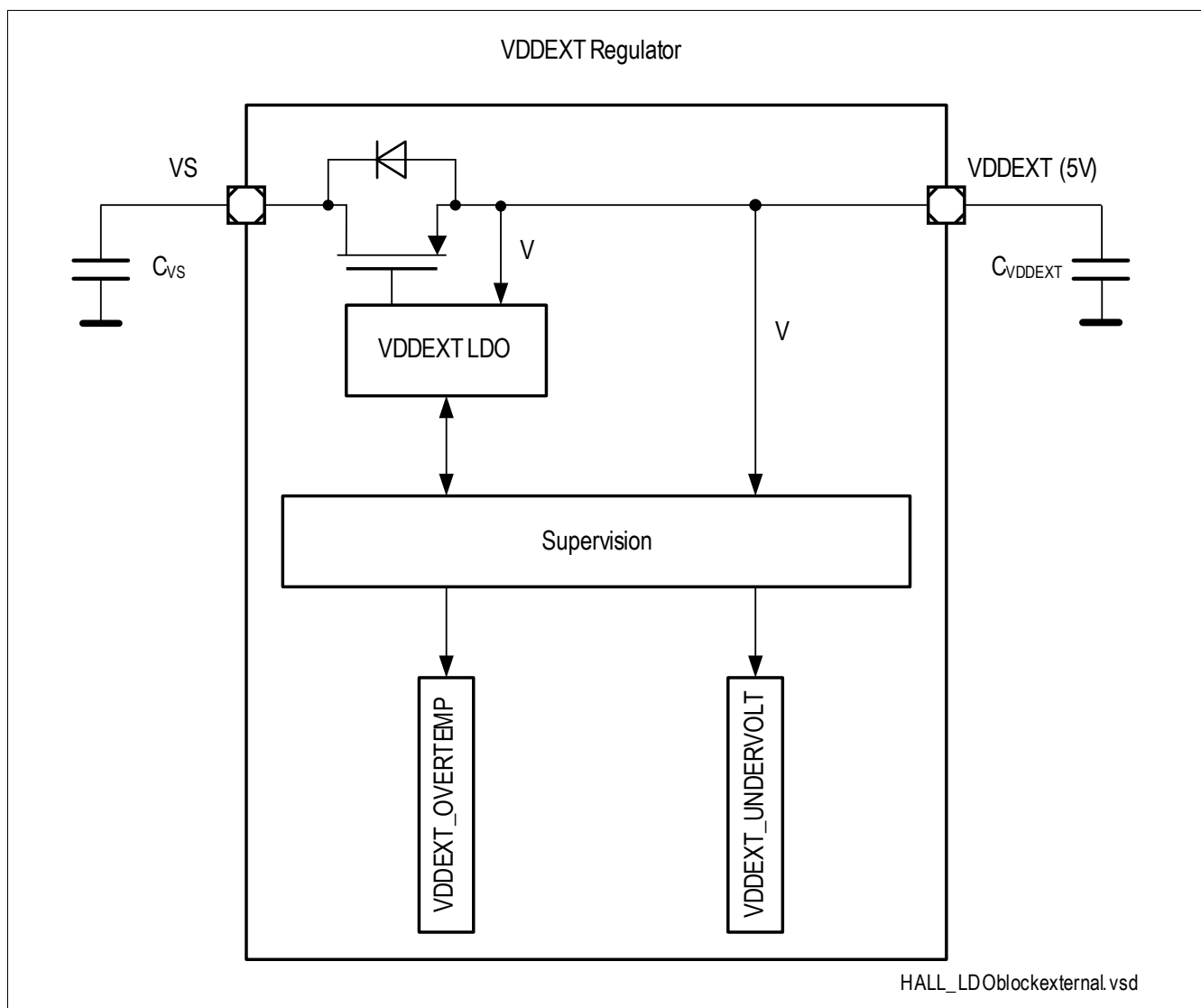


Figure 8 Module Block Diagram

Power Management Unit (PMU)

5.3.4 Power-on Reset Concept

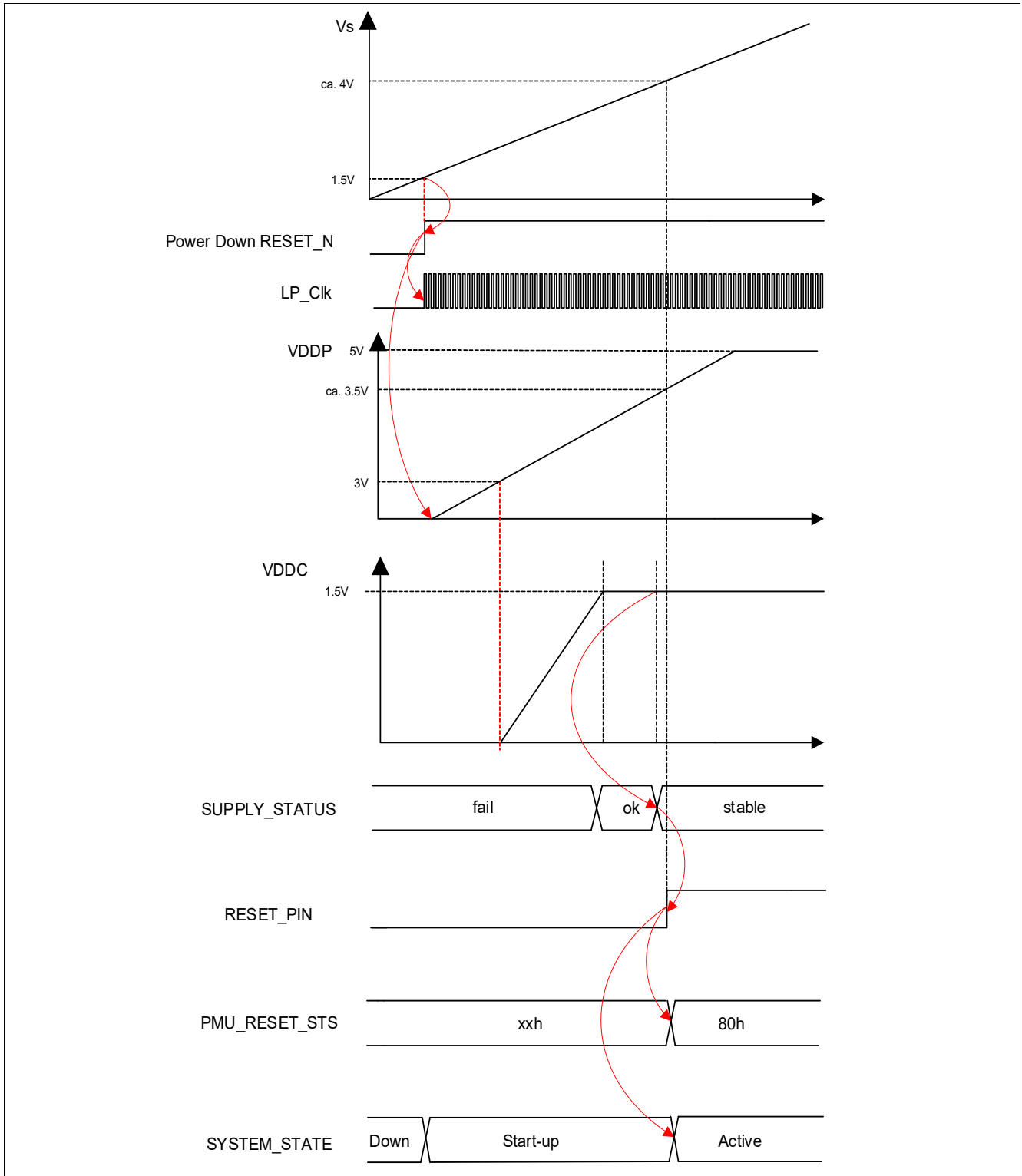


Figure 9 Power-on Reset Concept

6 System Control Unit - Digital Modules (SCU-DM)

6.1 Features

- Flexible clock configuration features
- Reset management of all system resets
- System modes control for all power modes (active, power down, sleep)
- Interrupt enabling for many system peripherals
- General purpose input output control
- Debug mode control of system peripherals

6.2 Introduction

The System Control Unit (SCU) supports all central control tasks in the TLE9852QX. The SCU is made up of the following sub-modules:

- Clock System and Control (CGU)
- Reset Control (RCU)
- Power Management (PCU)
- Interrupt Management (ICU)
- General Port Control
- Flexible Peripheral Management
- Module Suspend Control
- Watchdog Timer (WDT)
- Error Detection and Correction in Data Memory
- Miscellaneous Control
- Register Mapping

System Control Unit - Digital Modules (SCU-DM)

6.2.1 Block Diagram

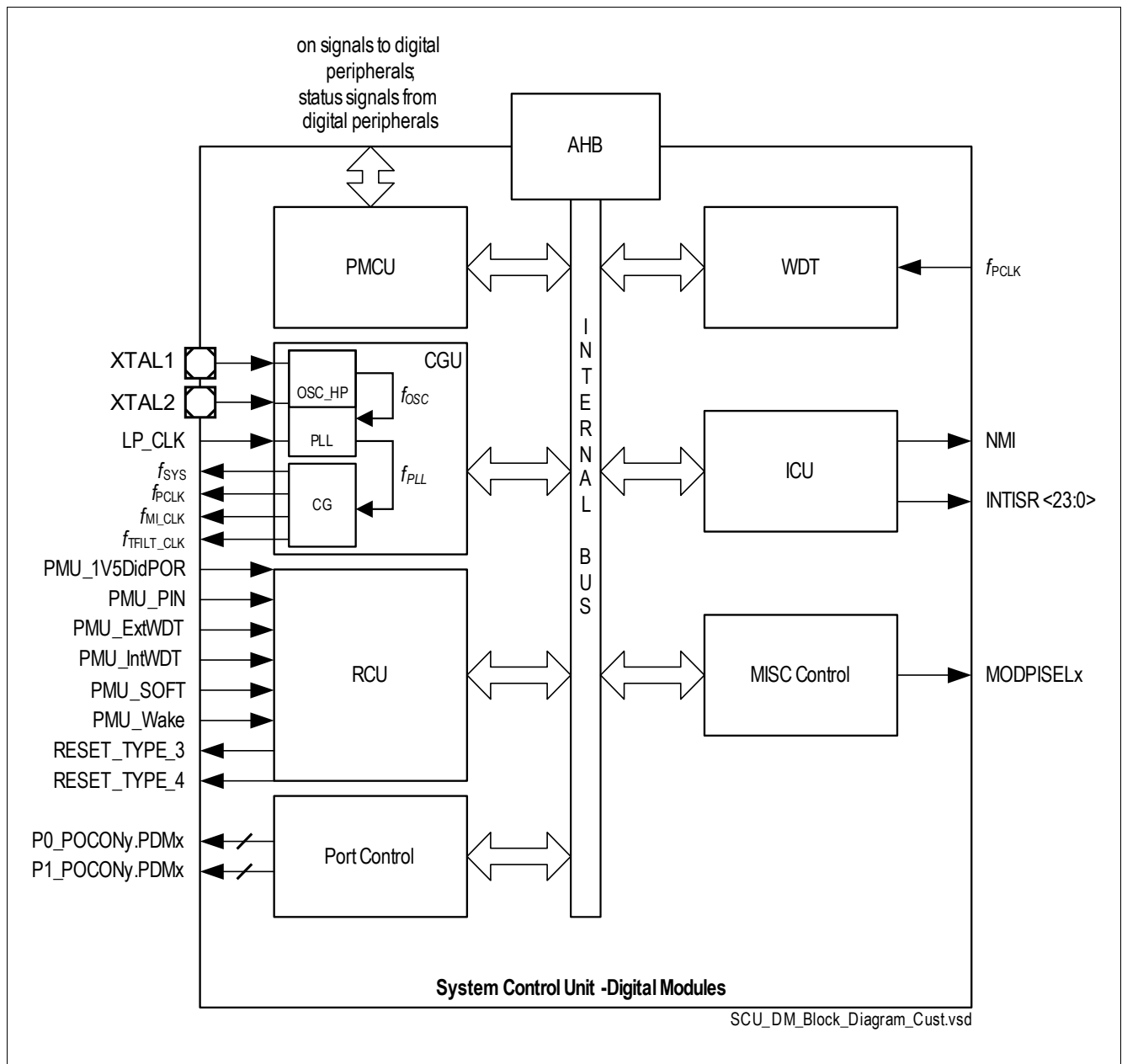


Figure 10 System Control Unit - Digital Modules Block Diagram

IO description of SCU_DM:

- CGU:
 - f_{sys} ; system clock
 - LP_CLK; low-power backup clock
- RCU:
 - 1V5DidPOR; Undervoltage reset of power down supply
 - PMU_PIN; Reset generated by reset pin
 - PMU_ExtWDT; WDT1 reset
 - PMU_IntWDT; WDT (SCU) reset

System Control Unit - Digital Modules (SCU-DM)

- PMU_SOFT; Software reset
- PMU_Wake; Stop Mode exit with reset
- Reset_Type_3; Peripheral reset (contains all resets)
- Reset_Type_4; Peripheral reset (without SOFT and WDT reset)
- Port Control:
 - P0_POCONy.PDMx; driver strength control
 - P1_POCONy.PDMx; driver strength control
- MISC:
 - MODPISELx; Mode selection registers for UART (source selection) and Timer (trigger or count selection)
- WDT (Watchdog Timer in SCU-DM): f_{SYS} ; System clock

System Control Unit - Digital Modules (SCU-DM)

6.3 Clock Generation Unit

The Clock Generation Unit (CGU) provides a flexible clock generation for TLE9852QX. During user program execution the frequency can be programmed for an optimal ratio between performance and power consumption. Therefore the power consumption can be adapted to the actual application state.

The CGU in the TLE9852QX consists of one oscillator circuit (OSC_HP), a Phase-Locked Loop (PLL) module including an internal oscillator (OSC_PLL) and a Clock Control Unit (CCU). The CGU can convert a low-frequency input/external clock signal to a high-frequency internal clock.

The system clock f_{SYS} is generated out of the following selectable clocks:

- PLL clock output f_{PLL}
- Direct clock from oscillator OSC_HP f_{OSC}
- Direct output of internal Oscillator f_{INTOSC}
- Low precision clock f_{LP_CLK} (HW-enabled for startup after reset and during power-down wake-up sequence)

The following sections describe the different parts of the CGU.

6.3.1 Low Precision Clock

The clock source LP_CLK is a low-precision RC oscillator (LP-OSC, see f_{LP_CLK}) that is enabled by hardware as an independent clock source for the TLE9852QX startup after reset and during the power-down wake-up sequence. There is no user configuration possible on f_{LP_CLK} .

6.3.2 High Precision Oscillator Circuit (OSC_HP)

The high precision oscillator circuit, designed to work with both an external crystal oscillator or an external stable clock source, consists of an inverting amplifier with XTAL1 as input, and XTAL2 as output.

Figure 11 shows the recommended external circuitries for both operating modes, External Crystal Mode and External Input Clock Mode.

6.3.2.1 External Input Clock Mode

When supplying the clock signal directly, not using an external crystal and bypassing the oscillator, the input frequency needs to be equal to or greater than 4 MHz if the PLL VCO part is used.

When using an external clock signal it must be connected to XTAL1. XTAL2 is left open (unconnected).

6.3.2.2 External Crystal Mode

When using an external crystal, its frequency can be within the range of 4 MHz to 16 MHz. An external oscillator load circuitry must be used, connected to both pins, XTAL1 and XTAL2. It consists normally of the two load capacitances C1 and C2, for some crystals a series damping resistor might be necessary. The exact values and related operating range are dependent on the crystal and have to be determined and optimized together with the crystal vendor using the negative resistance method. As starting point for the evaluation, the following load cap values may be used:

Table 4 External CAP Capacitors

| Fundamental Mode Crystal Frequency (approx., MHz) | Load Caps C_1, C_2 (pF) |
|---|---------------------------|
| 4 | 33 |
| 8 | 18 |
| 12 | 12 |
| 16 | 10 |

System Control Unit - Digital Modules (SCU-DM)

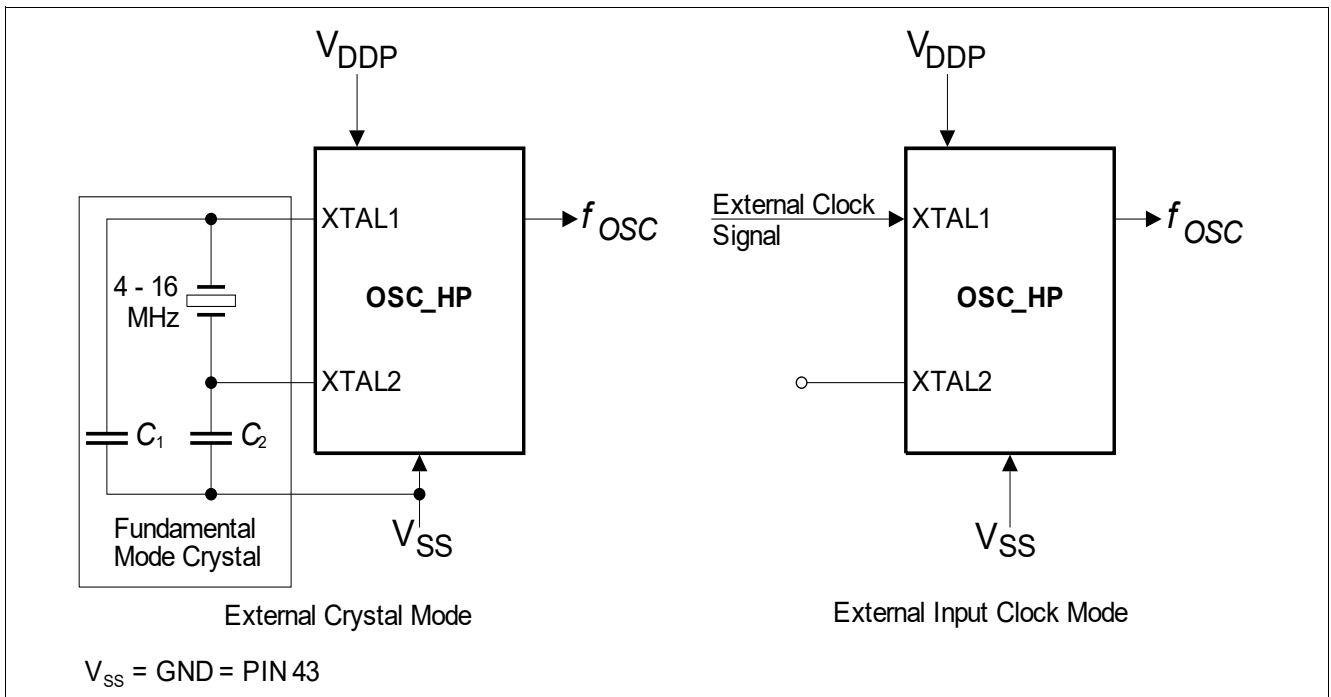


Figure 11 TLE9852QX External Circuitry for the OSC_HP

System Control Unit - Digital Modules (SCU-DM)

6.3.3 Clock Control Unit

The Clock Control Unit (CCU) receives the clock from the PLL f_{PLL} , the external input clock f_{OSC} , the internal input clock f_{INTOSC} , or the low-precision input clock f_{LP_CLK} . The system frequency is derived from one of these clock sources.

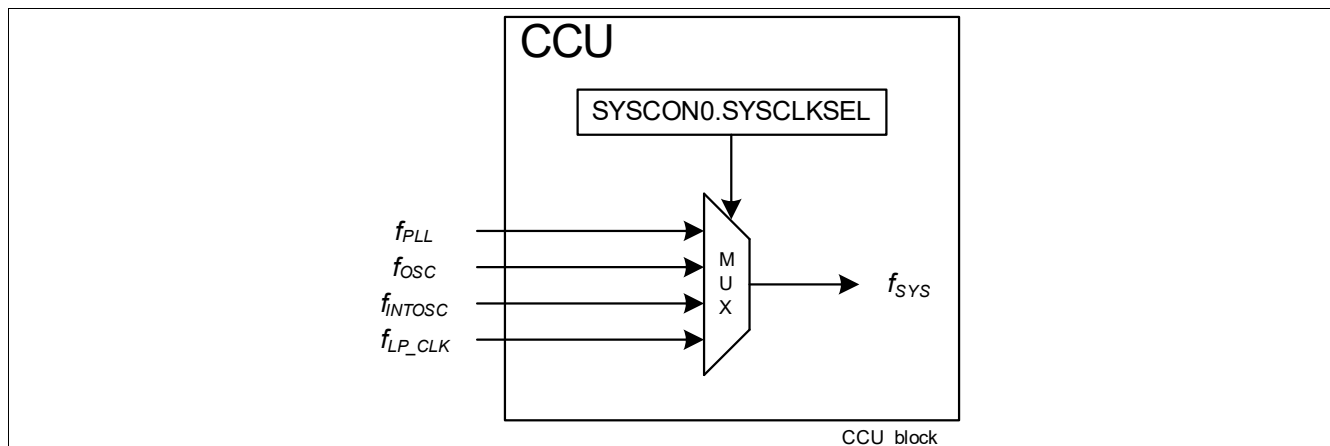


Figure 12 Clock Inputs to Clock Control Unit

The CCU generates all necessary clock signals within the microcontroller from the system clock. It consists of:

- Clock slow down circuitry
- Centralized enable/disable circuit for clock control

In normal running mode, the main module frequencies (synchronous unless otherwise stated) are as follows:

- System frequency, f_{SYS} = up to 40 MHz (measurement interface clock MI_CLK is derived from this clock)
- CPU clock (CCLK, SCLK) = up to 40 MHz (divide-down of NVM access clock)
- NVM access clock (NVMACCCLK) = up to 40 MHz
- Peripheral clock (PCLK, PCLK2, NVMCLK) = up to 40 MHz (equals CPU clock; must be same or higher)

Some peripherals are clocked by PCLK, others clocked by PCLK2 and the NVM is clocked by both NVMCLK and NVMACCCLK. During normal running mode, PCLK = PCLK2 = NVMCLK = CCLK. On wake-up from power-down mode, PCLK2 is restored similarly like NVMCLK, whereas PCLK is restored only after PLL is locked.

For optimized NVM access (read/write) with reduced wait state(s) and with respect to system requirements on CPU operational frequency, bit field NVMCLKFAC is provided for setting the frequency factor between the NVM access clock NVMACCCLK and the CPU clock CCLK.

For the slow down mode, the operating frequency is reduced using the slow down circuitry with clock divider setting at the bit field CLKREL. Bit field CLKREL is only effective when slow down mode is enabled via SFR bit PMCON0.SD bit. Note that the slow down setting of bit field CLKREL correspondingly reduces the NVMACCCLK clock. Slow down setting does not influence the erase and write cycles for the NVM.

Peripherals UART1, UART2, T2 and T21 are not influenced by CLKREL and either not by NVMCLKFAC, to allow functional LIN communication in slow down mode.

System Control Unit - Digital Modules (SCU-DM)

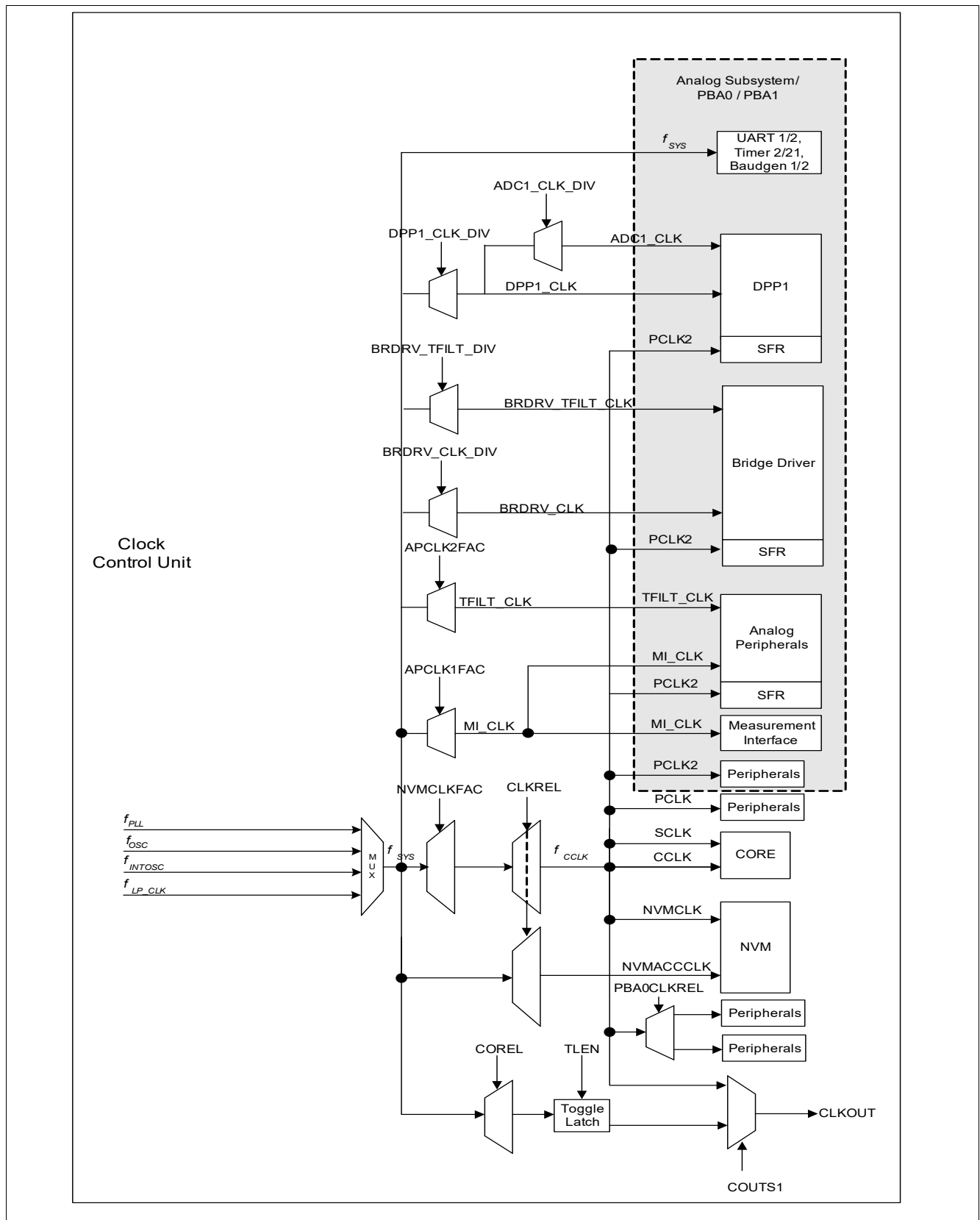


Figure 13 Clock Generation from f_{sys} ; CLKOUT Generation

System Control Unit - Power Modules (SCU-PM)

7 System Control Unit - Power Modules (SCU-PM)

7.1 Features

- Clock Watchdog Unit (CWU): supervision of all power modules relevant clocks with NMI signalling.
- Interrupt Control Unit (ICU): all system relevant interrupt flags and status flags.
- Power Control Unit (PCU): takes over control when device enters and exits Sleep and Stop Mode.
- External Watchdog (WDT1): independent system watchdog to monitor system activity

7.2 Introduction

7.2.1 Block Diagram

The System Control Unit of the power modules consists of the sub-modules in the figure shown below:

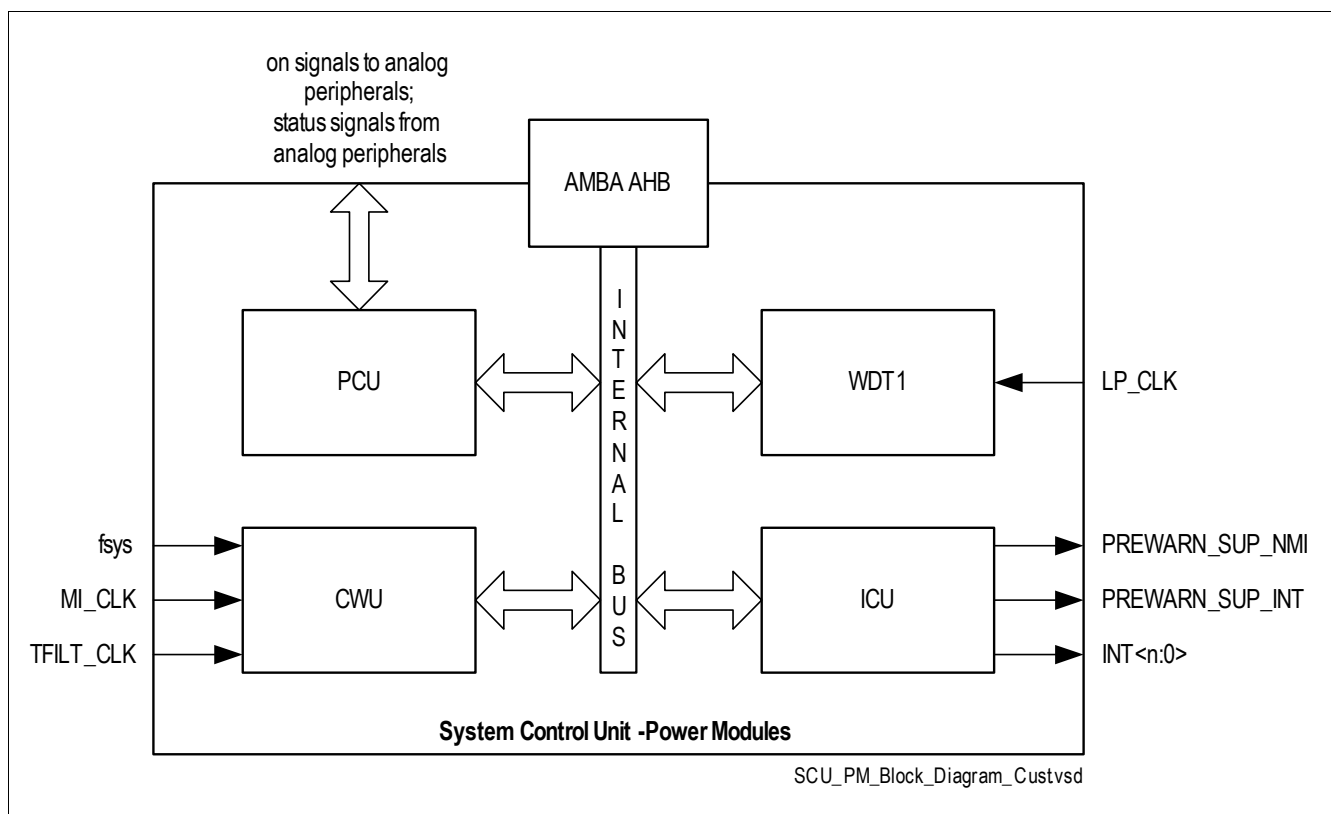


Figure 14 Block diagram of System Control Unit - Power Modules

IO description of SCU_PM:

- CWU:
 - check of f_{sys} = system frequency: output of PLL
 - check of MI_CLK = measurement interface clock (analog clock): derived out of f_{sys} by division factors 1/2/3/4
 - check of TFILT_CLK = clock used for digital filters: derived out of f_{sys} by configurable division factors

System Control Unit - Power Modules (SCU-PM)

- ICU:
 - PREWARN_SUP_NMI = generation of Prewarn-Supply NMI
 - PREWARN_CLK_INT = generation of Prewarn-Clock Watchdog NMI
 - INT = generation of MISC interrupts

8 Arm® Cortex®-M0 Core

8.1 Features

The key features of the Arm® Cortex®-M0 implemented are listed below.

Processor Core. A low gate count core, with low latency interrupt processing:

- Thumb® + Thumb-2® Instruction Set
- Banked stack pointer (SP) only
- Handler and thread modes
- Thumb and debug states
- Interruptible-continued instructions LDM/STM, Push/Pop for low interrupt latency
- Automatic processor state saving and restoration for low latency Interrupt Service Routine (ISR) entry and exit
- Arm® architecture v6-M Style
- Arm®v6 unaligned accesses
- SysTick (typ. 1ms)

Nested Vectored Interrupt Controller (NVIC) closely integrated with the processor core to achieve low latency interrupt processing:

- External interrupts, configurable from 1 to 24
- 7 interrupt priority registers for levels from 0 up to 192 in steps of 64
- Dynamic repriorization of interrupts
- Priority grouping. This enables selection of pre-empting interrupt levels and non pre-empting interrupt levels
- Support for tail-chaining and late arrival of interrupts. This enables back-to-back interrupt processing without the overhead of state saving and restoration between interrupts.
- Processor state automatically saved on interrupt entry, and restored on interrupt exit, with no instruction overhead

Bus interfaces

- Advanced High-performance Bus-Lite (AHB-Lite) interfaces

8.2 Introduction

The Arm® Cortex®-M0 processor is a leading 32-bit processor and provides a high-performance and cost-optimized platform for a broad range of applications including microcontrollers, automotive body systems and industrial control systems. Like the other Arm® Cortex® family processors, the Arm® Cortex®-M0 processor implements the Thumb®-2 instruction set architecture. With the optimized feature set the Arm® Cortex®-M0 delivers 32-bit performance in an application space that is usually associated with 8- and 16-bit microcontrollers.

8.2.1 Block Diagram

Figure 15 shows the functional blocks of the Arm® Cortex®-M0.

Arm® Cortex®-M0 Core

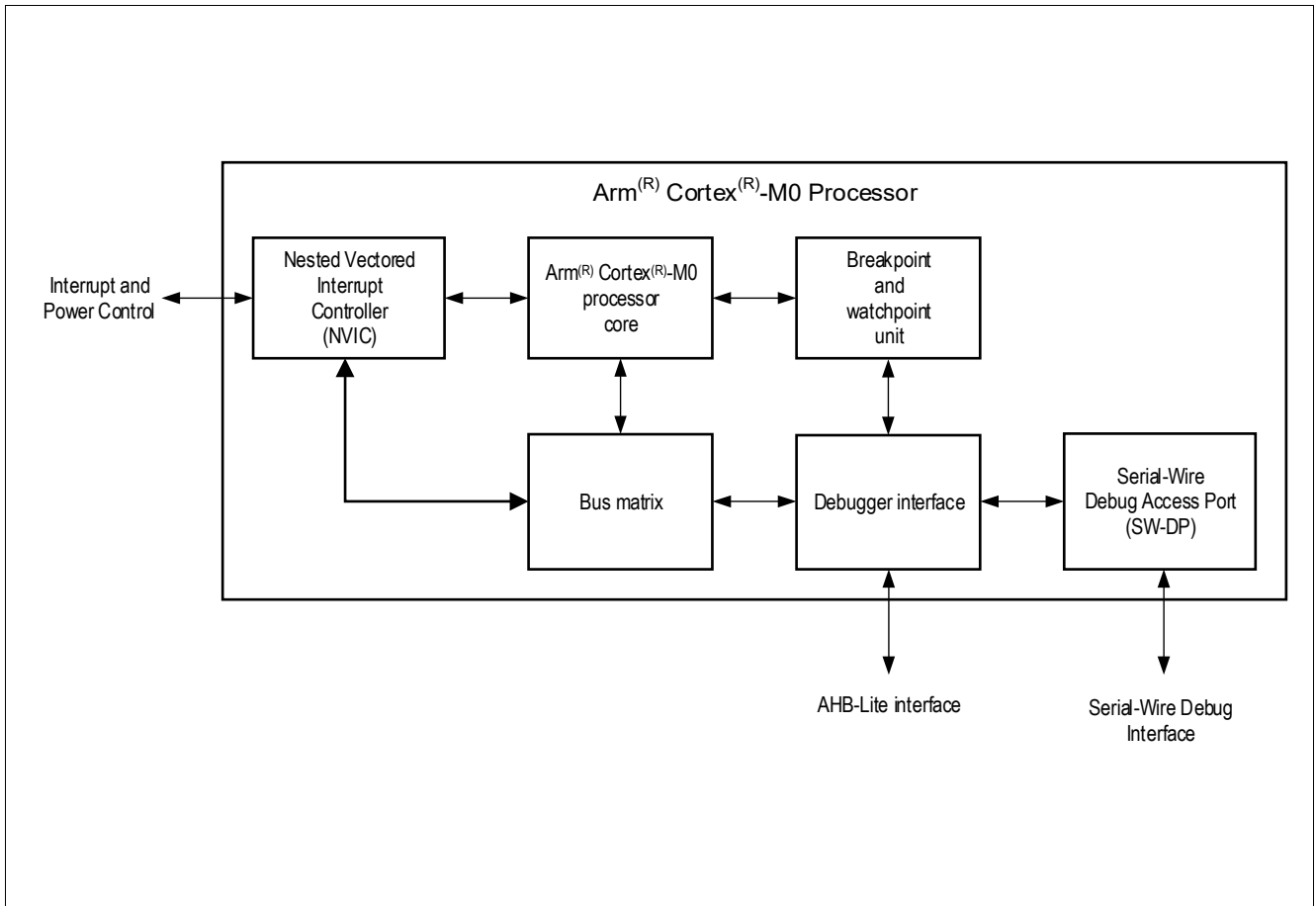


Figure 15 Arm® Cortex®-M0 Block Diagram

Address Space Organization

9 Address Space Organization

The TLE9852QX manipulates operands in the following memory spaces:

- 48 KB of Flash memory in code space
- 24 KB Boot ROM memory in code space (used for boot code and IP storage)
- 4 KB RAM memory in Arm® Cortex®-M0 code region (RAM can be fetched, read/written as program memory)
- Special function registers (SFRs) in peripheral linear address space

The on-chip memory modules available in the TLE9852QX are:

| | |
|------------------------|--|
| BROM, 24K | 00000000 _H / 00005FFF _H |
| reserved | |
| Flash, 48K | 11000000 _H / 1100BFFF _H |
| reserved | 1100C000 _H / 17FFFFFF _H |
| SRAM, 4K | 18000000 _H / 18000FFF _H |
| reserved | 18001000 _H / 3FFFFFFF _H |
| PBA0 | 40000000 _H / 47FFFFFF _H |
| PBA1 | 48000000 _H / 5FFFFFFF _H |
| reserved | 60000000 _H / DFFFFFFF _H |
| Private Peripheral Bus | E0000000 _H / E0FFFFFF _H |
| reserved | E01FFFFFF _H / FFFFFFFF _H |

Figure 16 TLE9852QX Memory Map

Memory Control Unit

10 Memory Control Unit

10.1 Features

- Provides Memory access to ROM, RAM, NVM, Config Sector through AHB-Lite Interface
- MBIST for RAM
- MBIST for ROM
- NVM Configuration with Special Function Registers through AHB-Lite Interface
- Hardware Memory Protection Logic
- Stack overflow detection

10.2 Introduction

10.2.1 Block Diagram

The Memory Control Unit (MCU) is divided in the following sub-modules:

- NVM Memory module (embedded Flash Memory)
- RAM memory module
- BootROM memory module
- Memory protection Unit (MPU) module

Memory Control Unit

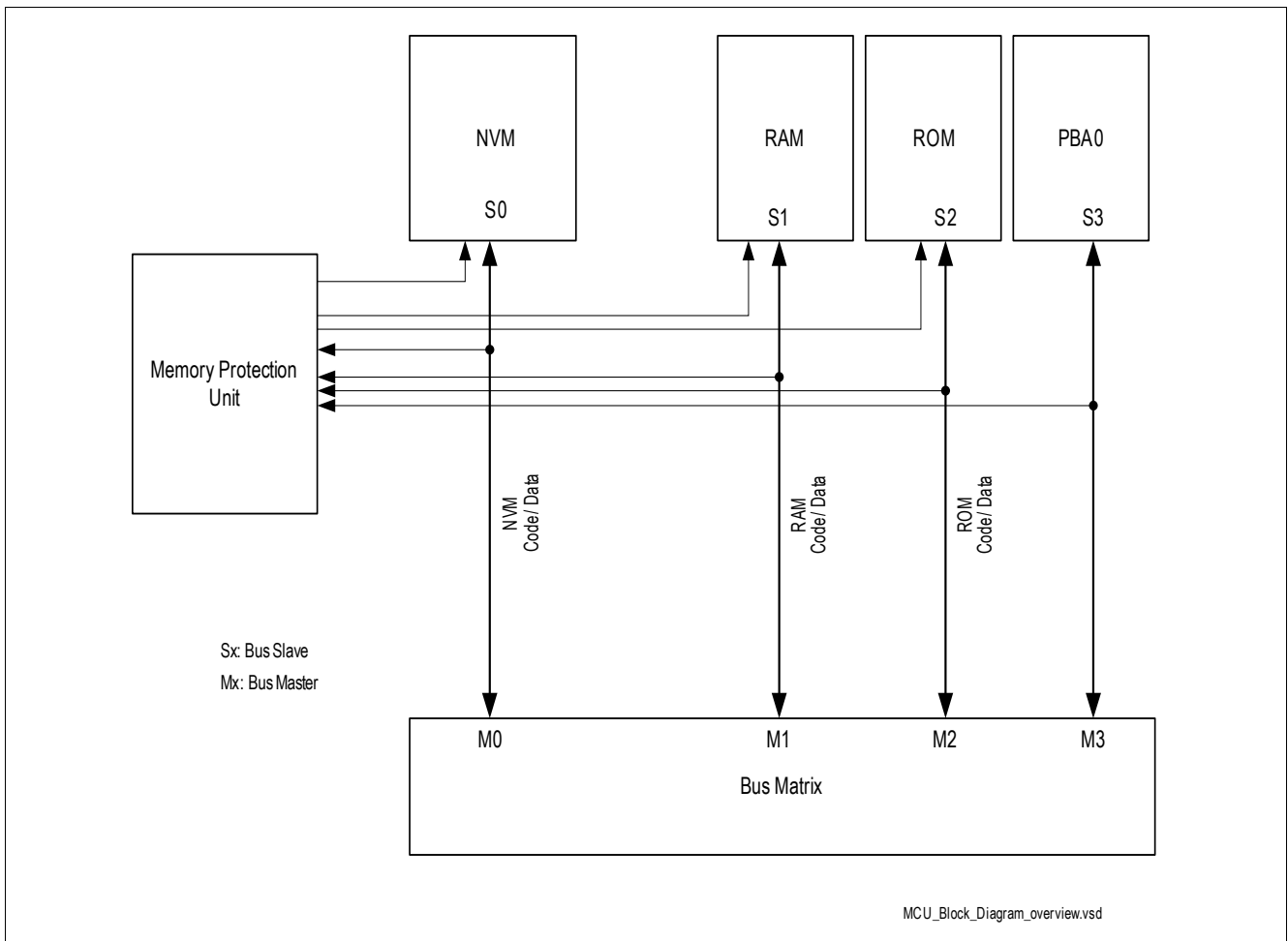


Figure 17 Memory Control Unit Block View

Functional Features for RAM

- 4 KB RAM
- Error correction code (ECC) for detection of single bit and double bit errors and dynamic correction of single bit errors
- Single byte access

Memory Control Unit

10.3 NVM Module (Flash Memory)

The Flash memory provides an embedded user-programmable non-volatile memory, allowing fast and reliable storage of user code and data.

Features

- In-System Programming via LIN (Flash mode) and SWD
- Error Correction Code (ECC) for detection of single Bit and double Bit errors and dynamic correction of single Bit errors on Data Block (Double words, 64 bits).
- Interrupt and signaling of double bit error by NMI, address of double bit error readable by FW API user routine
- Possibility of checking single bit error occurrence by ROM routines
- Program width of 128 Byte (page)
- Minimum erase width of 128 Byte (page)
- Integrated hardware support for EEPROM emulation
- 8 Byte read access
- Physical read access time: max. 75 ns
- Code read access acceleration integrated (read buffer)
- Page program time: typ. 3 ms
- Page erase (128 bytes) and sector erase (4K bytes) time: typ. 4 ms
- 4 individual protection passwords for NVM customer BSL region, code region, data linear region, and data mapped region
- Security option to protect read out via debug interface in application run mode
- Write/erase access to 100TP (e.g. option bytes) is possible via the debug interface

Note: The user has to ensure that no flash operations which change the content of the flash get interrupted at any time.

The clock for the NVM is supplied with the system frequency f_{sys} . Integrated firmware routines are provided to ease NVM, and other operations including EEPROM emulation.

Interrupt System

11 Interrupt System

11.1 Features

- 22 interrupt nodes for on-chip peripherals
- 8 NMI nodes for critical system events
- Maximum flexibility (resp. priority and node grouping) for all interrupt nodes

11.2 Introduction

11.2.1 Overview

The TLE9852QX supports 24 interrupt vectors with 4 priority levels. 20 of these interrupt vectors are assigned to the on-chip peripherals: GPT12, SSC1, SSC2, CCU6, High-Side Switch, WAKEUP, Bridge Driver, Charge Pump, Differential Unit, Math Divider, GPIOs, MONs and A/D Converter are each assigned to one dedicated interrupt vector; while UART1 and Timer2 or UART2, External Interrupt 2 and Timer21 share interrupt vectors. Two vectors are dedicated for External Interrupt 0 and 1.

Table 5 Interrupt Vector Table

| Service Request | Node ID | Description |
|-----------------|---------|--|
| GPT1 | 0 | GPTimer 1 Interrupt |
| GPT2 | 1 | GPTimer 2 Interrupt |
| MU | 2 | MU interrupt / ADC2, VBG interrupt |
| ADC1 | 3 | ADC10 Bit interrupt |
| CCU0 | 4 | CCU6 node 0 interrupt |
| CCU1 | 5 | CCU6 node 1 interrupt |
| CCU2 | 6 | CCU6 node 2 interrupt |
| CCU3 | 7 | CCU6 node 3 interrupt |
| SSC1 | 8 | SSC1 interrupt (receive, transmit, error) |
| SSC2 | 9 | SSC2 interrupt (receive, transmit, error) |
| UART1 | 10 | UART1 interrupt (receive, transmit), Timer2, LIN sync, LIN |
| UART2 | 11 | UART2 interrupt (receive, transmit), Timer21, External Interrupt (EINT2) |
| EXINT0 | 12 | External interrupt (EINT0), wake-up |
| EXINT1 | 13 | External interrupt (EINT1) |
| WAKEUP | 14 | Wake-up interrupt (generated by a wake-up event) |
| Math Div | 15 | Hardware Divider Unit Interrupt |
| rfu | 16 | Reserved for future use |
| CP | 17 | Charge Pump |
| BDRV | 18 | Bridge Driver |

Interrupt System
Table 5 Interrupt Vector Table (cont'd)

| Service Request | Node ID | Description |
|-----------------|---------|--------------------------|
| HS | 19 | High Side Interrupt |
| rfu | 20 | reserved for future use |
| DU | 21 | Differential Unit - DPP1 |
| MONx | 22 | MONx Interrupt |
| Port 2.x | 23 | Port 2.x - DPP1 |

Table 6 NMI Interrupt Table

| Service Request | Node | Description |
|------------------------------|------|-----------------------------------|
| Watchdog Timer NMI | NMI | Watchdog Timer overflow |
| MI_CLK Watchdog Timer NMI | NMI | MI_CLK Watchdog Timer Overflow |
| PLL NMI | NMI | PLL Loss-of-Lock |
| Overtemperature NMI | NMI | System Overtemperature |
| Oscillator Watchdog NMI | NMI | Oscillator Watchdog |
| NVM Map Error NMI | NMI | NVM Map Error |
| ECC Error NMI | NMI | RAM / NVM Uncorrectable ECC Error |
| Supply Prewarning NMI | NMI | Supply Prewarning |
| Stack overflow | NMI | Stack Overflow |

12 Math Divider Module

12.1 Features

The MATH Coprocessor includes the following features:

- Divide function with operand pre-processing and result post-processing
- AHB-Interface supports Byte/half word/ word Register access
- Supports fast execution kernel clock faster than interface clock

12.2 Introduction

The MATH Coprocessor (MATH) module supports the CPU in math-intensive computations with a Divider Unit (DIV) for signed and unsigned 32-bit division operations.

12.3 Block Diagram

Figure 18 shows a block diagram of the MATH Coprocessor.

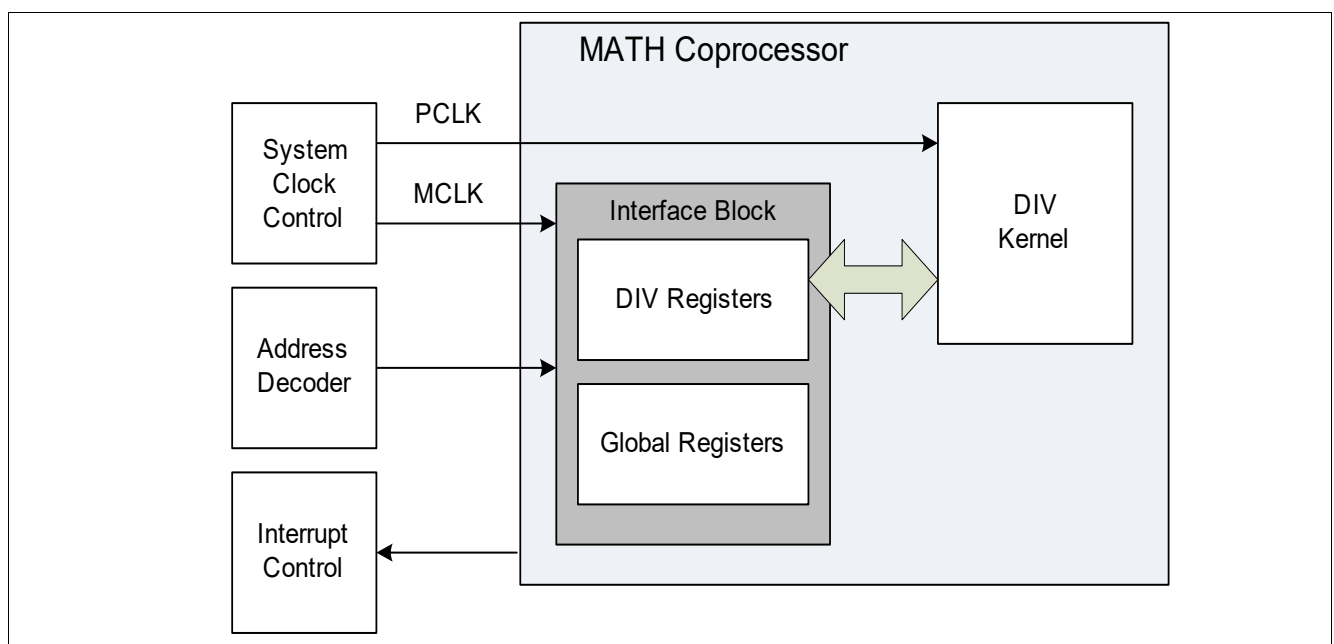


Figure 18 MATH Coprocessor Block Diagram

Watchdog Timer (WDT1)**13 Watchdog Timer (WDT1)****13.1 Features**

In Active Mode, the WDT1 acts as a windowed watchdog timer, which provides a highly reliable and safe way to recover from software or hardware failures.

The WDT1 is always enabled in Active Mode. In Sleep Mode, Stop Mode and Debug Mode the WDT1 is disabled.

Functional Features

- Watchdog Timer is operating with a from the system clock (f_{SYS}) independent clock source (f_{LP_CLK})
- Windowed Watchdog Timer with programmable timing (16, 32, 48, ..., 1008ms period) in Active Mode
- Long open window (200 ms) after power-up, reset, wake-up
- Short open window (30 ms) to facilitate Flash programming
- System safety shutdown to Sleep Mode after 5 missed WDT1 services
- Watchdog is disabled in Debug Mode
- Watchdog cannot be deactivated in Normal Mode
- Watchdog reset is stored in reset status register

Watchdog Timer (WDT1)

13.2 Introduction

The behavior of the Watchdog Timer in Active Mode is depicted in **Figure 19**.

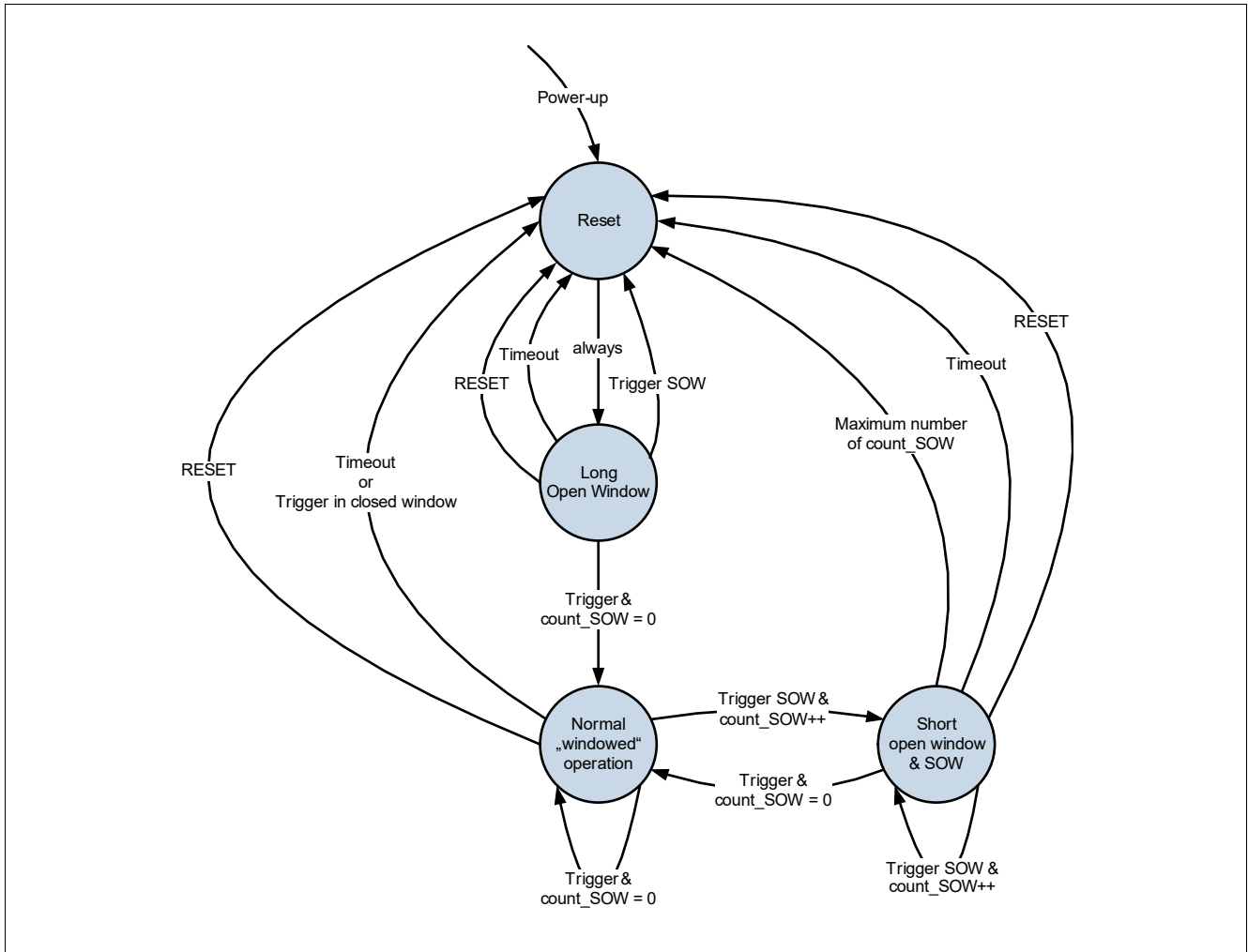


Figure 19 Watchdog Timer Behavior

14 GPIO Ports and Peripheral I/O

The TLE9852QX has 15 port pins organized into three parallel ports: Port 0 (P0), Port 1 (P1) and Port 2 (P2). Each port pin has a pair of internal pull-up and pull-down devices that can be individually enabled or disabled. P0 and P1 are bidirectional and can be used as general purpose input/output (GPIO) or to perform alternate input/output functions for the on-chip peripherals. When configured as an output, the open drain mode can be selected. On Port 2 (P2) analog inputs are shared with general purpose input.

14.1 Features

- 10 GPIOs and 5 analog inputs.
- Strong pull-up at Reset-pin and Hall-inputs (except P2.x)

Bidirectional Port Features (P0, P1)

- Configurable pin direction
- Configurable pull-up/pull-down devices
- Configurable open drain mode
- Configurable drive strength
- Transfer of data through digital inputs and outputs (general purpose I/O)
- Possible readback of pin status when GPIO is configured as output (short detection)
- Alternate input/output for on-chip peripherals

Analog Port Features (P2)

- Configurable pull-up/pull-down devices
- Transfer of data through digital inputs
- Alternate inputs for on-chip peripherals

GPIO Ports and Peripheral I/O

14.2 Introduction

14.2.1 Port 0 and Port 1

Figure 20 shows the block diagram of an TLE9852QX bidirectional port pin. Each port pin is equipped with a number of control and data bits, thus enabling very flexible usage of the pin.

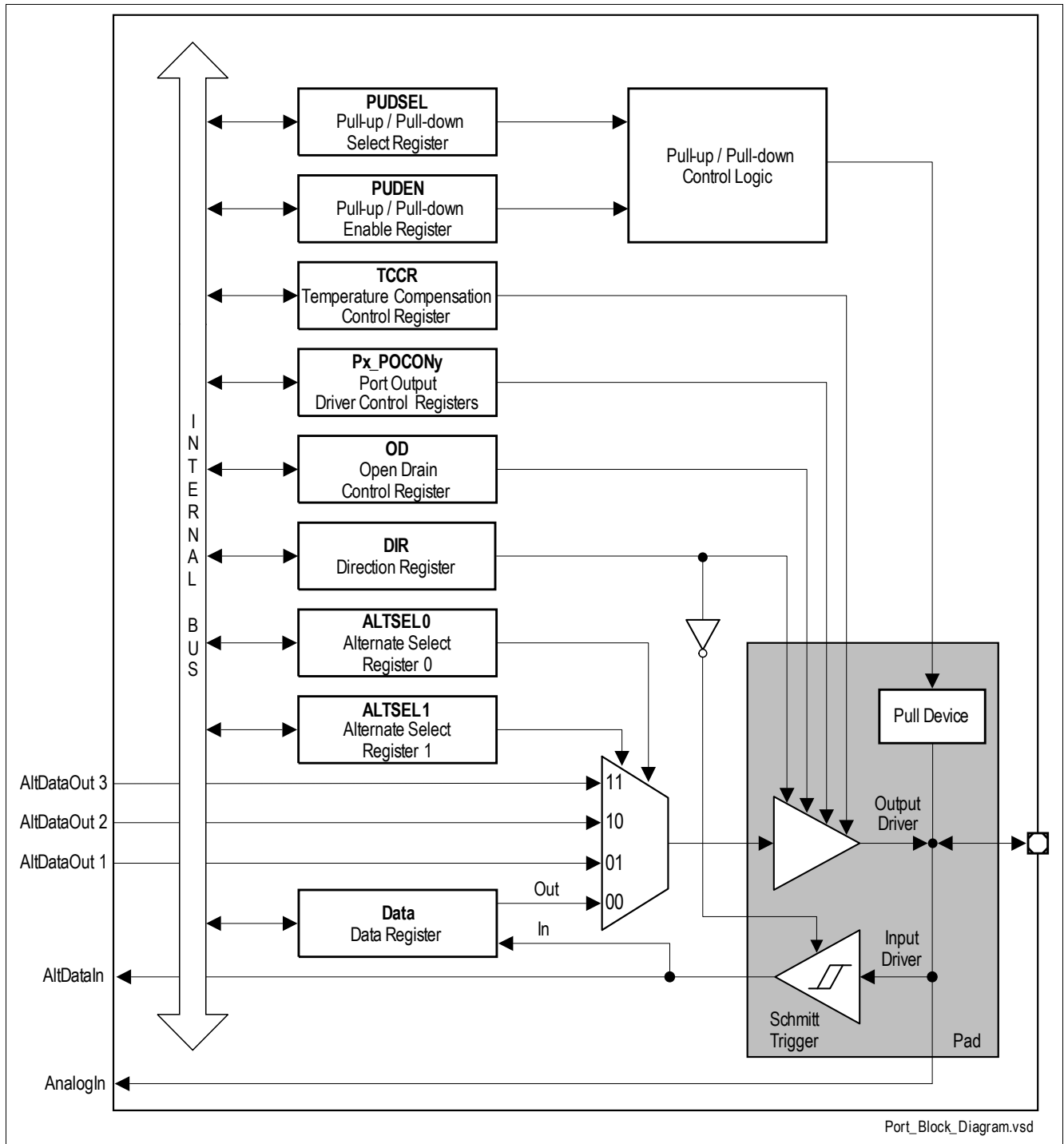


Figure 20 General Structure of Bidirectional Port

GPIO Ports and Peripheral I/O

14.2.2 Port 2

Figure 21 shows the structure of an input-only port pin. Each P2 pin can only function in input mode. Register P2_DIR is provided to enable or disable the input driver. When the input driver is enabled, the actual voltage level present at the port pin is translated into a logic 0 or 1 via a Schmitt-Trigger device and can be read via the register P2_DATA. Each pin can also be programmed to activate an internal weak pull-up or pull-down device. Register P2_PUDSEL selects whether a pull-up or the pull-down device is activated while register P2_PUDEN enables or disables the pull device. The analog input (AnalogIn) bypasses the digital circuitry and Schmitt-Trigger device for direct feed-through to the ADC input channel.

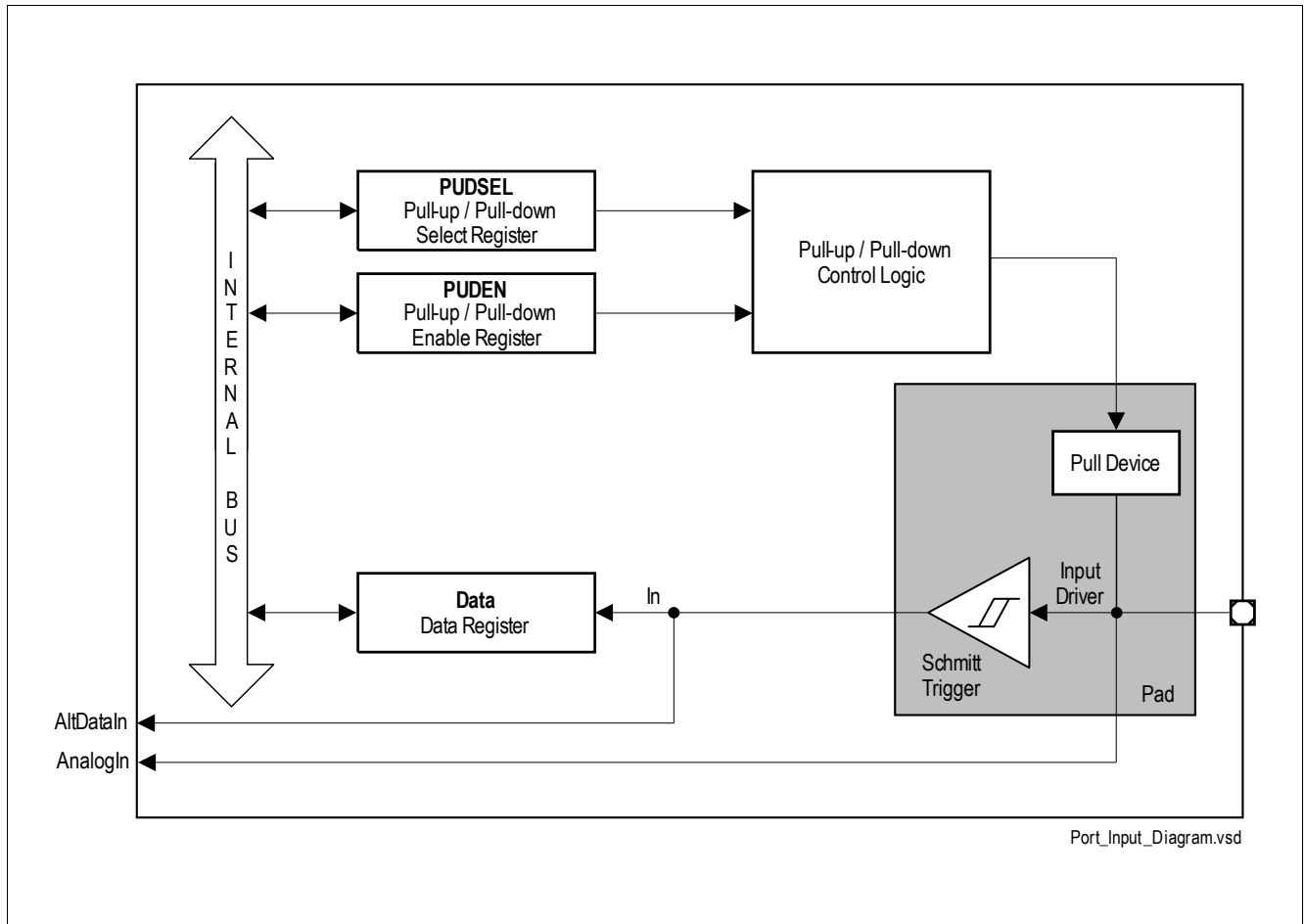


Figure 21 General Structure of Input Port

14.3 Functional Description

An overview of the available alternate functions of the GPIOs is provided in [Chapter 14.3.1](#).

GPIO Ports and Peripheral I/O

14.3.1 Alternate Functions

The following chapters describe the Portx.y mapping to their alternate functions.

14.3.1.1 Port 0 Functions

Port 0 alternate function mapping according [Table 7](#)

Table 7 Port 0 Input/Output Functions

| Port Pin | Input/Output | Select | Connected Signal(s) | From/to Module |
|----------|--------------|--------|---------------------|----------------|
| P0.0 | Input | GPI | P0_DATA.P0 | |
| | | INP1 | T12HR_0 | CCU6 |
| | | INP2 | T4INA | GPT12 |
| | | INP3 | T2_0 | Timer 2 |
| | | INP4 | SWD_CLK | SWD |
| | | INP5 | EXINT2_3 | SCU |
| | Output | GPO | P0_DATA.P0 | |
| | | ALT1 | T3OUT_0 | GPT12 |
| | | ALT2 | EXF21_0 | Timer 21 |
| | | ALT3 | UART2_RXDO | UART2 |
| P0.1 | Input | GPI | P0_DATA.P1 | |
| | | INP1 | T13HR_0 | CCU6 |
| | | INP2 | UART1_RXD | UART1 |
| | | INP3 | T2EX_1 | Timer 2 |
| | | INP4 | T21_0 | Timer 21 |
| | | INP5 | EXINT0_3 | SCU |
| | | INP6 | T4INC | GPT12 |
| | | INP7 | CAPINA | GPT12 |
| | | INP8 | SSC12_S_SCK_0 | SSC1/2 |
| | | INP9 | CC62_0 | CCU6 |
| | Output | GPO | P0_DATA.P1 | |
| | | ALT1 | T6OUT_0 | GPT12 |
| | | ALT2 | CC62_0 | CCU6 |
| | | ALT3 | SSC12_M_SCK | SSC1/2 |

GPIO Ports and Peripheral I/O

Table 7 Port 0 Input/Output Functions (cont'd)

| Port Pin | Input/Output | Select | Connected Signal(s) | From/to Module |
|----------|--------------|--------|---------------------|----------------|
| P0.2 | Input | GPI | P0_DATA.P2 | |
| | | INP1 | T2EUDA | GPT12 |
| | | INP2 | CTRAP_0 | CCU6 |
| | | INP3 | SSC12_M_MRST_0 | SSC1/2 |
| | | INP4 | T21EX_0 | Timer 21 |
| | | INP5 | EXINT1_3 | SCU |
| | Output | GPO | P0_DATA.P2 | |
| | | ALT1 | SSC12_S_MRST | SSC1/2 |
| | | ALT2 | UART1_TXD | UART1 |
| | | ALT3 | EXF2_0 | Timer 2 |
| P0.3 | Input | GPI | P0_DATA.P3 | |
| | | INP1 | SSC1_S_SCK | SSC1 |
| | | INP2 | T4EUDA | GPT12 |
| | | INP3 | CAPINB | GPT12 |
| | | INP4 | EXINT1_2 | SCU |
| | | INP5 | T3EUDD | GPT12 |
| | | INP6 | CCPOS0_1 | CCU6 |
| | Output | GPO | P0_DATA.P3 | |
| | | ALT1 | SSC1_M_SCK | SSC1 |
| | | ALT3 | T6OUT_1 | GPT12 |
| P0.4 | Input | GPI | P0_DATA.P4 | |
| | | INP1 | SSC1_S_MTSR | SSC1 |
| | | INP2 | CC60_0 | CCU6 |
| | | INP3 | T21_2 | Timer 21 |
| | | INP4 | EXINT2_2 | SCU |
| | | INP5 | T3EUDA | GPT12 |
| | | INP6 | CCPOS1_1 | CCU6 |
| | Output | GPO | P0_DATA.P4 | |
| | | ALT1 | SSC1_M_MTSR | SSC1 |
| | | ALT3 | CLKOUT_0 | SCU |

GPIO Ports and Peripheral I/O
Table 7 Port 0 Input/Output Functions (cont'd)

| Port Pin | Input/Output | Select | Connected Signal(s) | From/to Module |
|----------|--------------|--------|---------------------|----------------|
| P0.5 | Input | GPI | P0_DATA.P5 | |
| | | INP1 | SSC1_M_MRST | SSC1 |
| | | INP2 | EXINT0_0 | SCU |
| | | INP3 | T21EX_2 | Timer 21 |
| | | INP4 | T5INA | GPT12 |
| | | INP5 | CCPOS2_1 | CCU6 |
| | Output | GPO | P0_DATA.P5 | |
| | | ALT1 | SSC1_S_MRST | SSC1 |
| | | ALT2 | COOUT60_0 | CCU6 |
| | | ALT3 | LIN_RXD | LIN |
| | | | | |

GPIO Ports and Peripheral I/O

14.3.1.2 Port 1 Functions

Port 1 alternate function mapping according [Table 8](#)

Table 8 Port 1 Input / Output Functions

| Port Pin | Input/Output | Select | Connected Signal(s) | From/to Module |
|----------|--------------|-------------|---------------------|----------------|
| P1.0 | Input | GPI | P1_DATA.P0 | |
| | | INP1 | T3INC | GPT12 |
| | | INP2 | CC61_0 | CCU6 |
| | | INP3 | SSC2_S_SCK | SSC2 |
| | Output | INP4 | T4EUIDB | GPT12 |
| | | GPO | P1_DATA.P0 | |
| | | ALT1 | SSC2_M_SCK | SSC2 |
| | | ALT2 | CC61_0 | CCU6 |
| P1.1 | Input | ALT3 | UART2_TXD | UART2 |
| | | GPI | P1_DATA.P1 | |
| | | INP1 | T6EUDA | GPT12 |
| | | INP2 | T5INB | GPT12 |
| | | INP3 | T3EUDC | GPT12 |
| | | INP4 | SSC2_S_MTSR | SSC2 |
| | Output | INP5 | T21EX_3 | Timer 21 |
| | | INP6 | UART2_RXD | UART2 |
| P1.2 | Input | GPO | P1_DATA.P1 | |
| | | ALT1 | SSC2_M_MTSR | SSC2 |
| | | ALT2 | COOUT61_0 | CCU6 |
| | | ALT3 | EXF21_1 | Timer 21 |
| | | GPI | P1_DATA.P2 | |
| | | INP1 | EXINT0_1 | SCU |
| | Output | INP2 | T21_1 | Timer 21 |
| | | INP3 | T2INA | GPT12 |
| INP4 | | SSC2_M_MRST | SSC2 | |
| INP5 | | CCPOS2_2 | CCU6 | |
| Output | GPO | P1_DATA.P2 | | |
| | ALT1 | SSC2_S_MRST | SSC2 | |
| | ALT2 | COOUT63_0 | CCU6 | |
| | ALT3 | T3OUT_1 | GPT12 | |

GPIO Ports and Peripheral I/O
Table 8 Port 1 Input / Output Functions (cont'd)

| Port Pin | Input/Output | Select | Connected Signal(s) | From/to Module |
|----------|--------------|--------|---------------------|----------------|
| P1.4 | Input | GPI | P1_DATA.P4 | |
| | | INP1 | EXINT2_1 | SCU |
| | | INP2 | T21EX_1 | Timer 21 |
| | | INP3 | T2INB | GPT12 |
| | | INP4 | T5EUDA | GPT12 |
| | | INP5 | SSC12_S_MTSR_0 | SSC1/2 |
| | | INP6 | CCPOS1_2 | CCU6 |
| | Output | GPO | P1_DATA.P4 | |
| | | ALT1 | CLKOUT_1 | SCU |
| | | ALT2 | COU62_0 | CCU6 |
| | | ALT3 | SSC12_M_MTSR | SSC1/2 |

GPIO Ports and Peripheral I/O

14.3.1.3 Port 2 Functions

Port 2 alternate function mapping according [Table 9](#)

Table 9 Port 2 Input Functions

| Port Pin | Input/Output | Select | Connected Signal(s) | From/to Module |
|----------|----------------|--------|--------------------------|----------------|
| P2.0 | Input | GPI | P2_DATA.P0 | |
| | | INP1 | EXINT1_1 | SCU |
| | | INP2 | CCPOS0_2 | CCU6 |
| | | INP3 | T5EUDB | GPT12 |
| | | INP4 | T13HR_2 | CCU6 |
| | | ANALOG | AN0 | ADC |
| | | IN | XTAL (in) ¹⁾ | XTAL |
| P2.1 | Input | GPI | P2_DATA.P1 | |
| | | INP1 | CCPOS0_0 | CCU6 |
| | | INP2 | EXINT1_0 | SCU |
| | | INP3 | T12HR_1 | CCU6 |
| | | INP4 | CC61_1 | CCU6 |
| | | INP5 | T4EUDD | GPT12 |
| | | INP6 | T2EX_3 | Timer2 |
| | | INP7 | LIN_TXD | LIN |
| | | INP8 | SSC12_S_SCK_1 | SSC1/2 |
| | | ANALOG | AN1 | ADC |
| P2.2 | Input / Output | GPI | P2_DATA.P2 | |
| | | INP1 | T6EUDB | GPT12 |
| | | INP2 | T2EX_0 | Timer 2 |
| | | INP3 | T12HR_2 | CCU6 |
| | | INP4 | CTRAP_2 | CCU6 |
| | | ANALOG | AN2 | ADC |
| | | OUT | XTAL (out) ¹⁾ | XTAL |

GPIO Ports and Peripheral I/O
Table 9 Port 2 Input Functions (cont'd)

| Port Pin | Input/Output | Select | Connected Signal(s) | From/to Module |
|----------|--------------|--------|---------------------|----------------|
| P2.3 | Input | GPI | P2_DATA.P3 | |
| | | INP1 | CCPOS1_0 | CCU6 |
| | | INP2 | EXINT0_2 | SCU |
| | | INP3 | CTRAP_1 | CCU6 |
| | | INP4 | T3IND | GPT12 |
| | | INP5 | CC60_1 | CCU6 |
| | | INP6 | T2EUDB | GPT12 |
| | | INP7 | T2_2 | Timer2 |
| | | INP8 | T2EX_2 | Timer2 |
| | | INP9 | SSC12_S_MTSR_1 | SSC1/2 |
| | | ANALOG | AN3 | ADC |
| P2.7 | Input | GPI | P2_DATA.P7 | |
| | | INP1 | CCPOS2_0 | CCU6 |
| | | INP2 | EXINT2_0 | SCU |
| | | INP3 | T13HR_1 | CCU6 |
| | | INP4 | CC62_1 | CCU6 |
| | | INP5 | T3EUDB | GPT12 |
| | | INP6 | T4EUDC | GPT12 |
| | | INP7 | T2_1 | Timer2 |
| | | INP8 | SSC12_M_MRST_1 | SSC1/2 |
| | | ANALOG | AN7 | ADC |

1) configurable by user

General Purpose Timer Units (GPT12)

15 General Purpose Timer Units (GPT12)

15.1 Features

15.1.1 Features Block GPT1

The following list summarizes the supported features:

- $f_{\text{GPT}}/4$ maximum resolution
- 3 independent timers/counters
- Timers/counters can be concatenated
- 4 operating modes:
 - Timer Mode
 - Gated Timer Mode
 - Counter Mode
 - Incremental Interface Mode
- Reload and Capture functionality
- Shared interrupt: Node 0

15.1.2 Features Block GPT2

The following list summarizes the supported features:

- $f_{\text{GPT}}/2$ maximum resolution
- 2 independent timers/counters
- Timers/counters can be concatenated
- 3 operating modes:
 - Timer Mode
 - Gated Timer Mode
 - Counter Mode
- Extended capture/reload functions via 16-bit capture/reload register CAPREL
- Shared interrupt: Node 1

15.2 Introduction

The General Purpose Timer Unit blocks GPT1 and GPT2 have very flexible multifunctional timer structures which may be used for timing, event counting, pulse width measurement, pulse generation, frequency multiplication, and other purposes.

They incorporate five 16-bit timers that are grouped into the two timer blocks GPT1 and GPT2. Each timer in each block may operate independently in a number of different modes such as Gated timer or Counter Mode, or may be concatenated with another timer of the same block.

Each block has alternate input/output functions and specific interrupts associated with it. Input signals can be selected from several sources by register PISEL.

The GPT module is clocked with clock f_{GPT} . f_{GPT} is a clock derived from f_{SYS} .

General Purpose Timer Units (GPT12)

15.2.1 Block Diagram GPT1

Block GPT1 contains three timers/counters: The core timer T3 and the two auxiliary timers T2 and T4. The maximum resolution is $f_{GPT}/4$. The auxiliary timers of GPT1 may optionally be configured as reload or capture registers for the core timer.

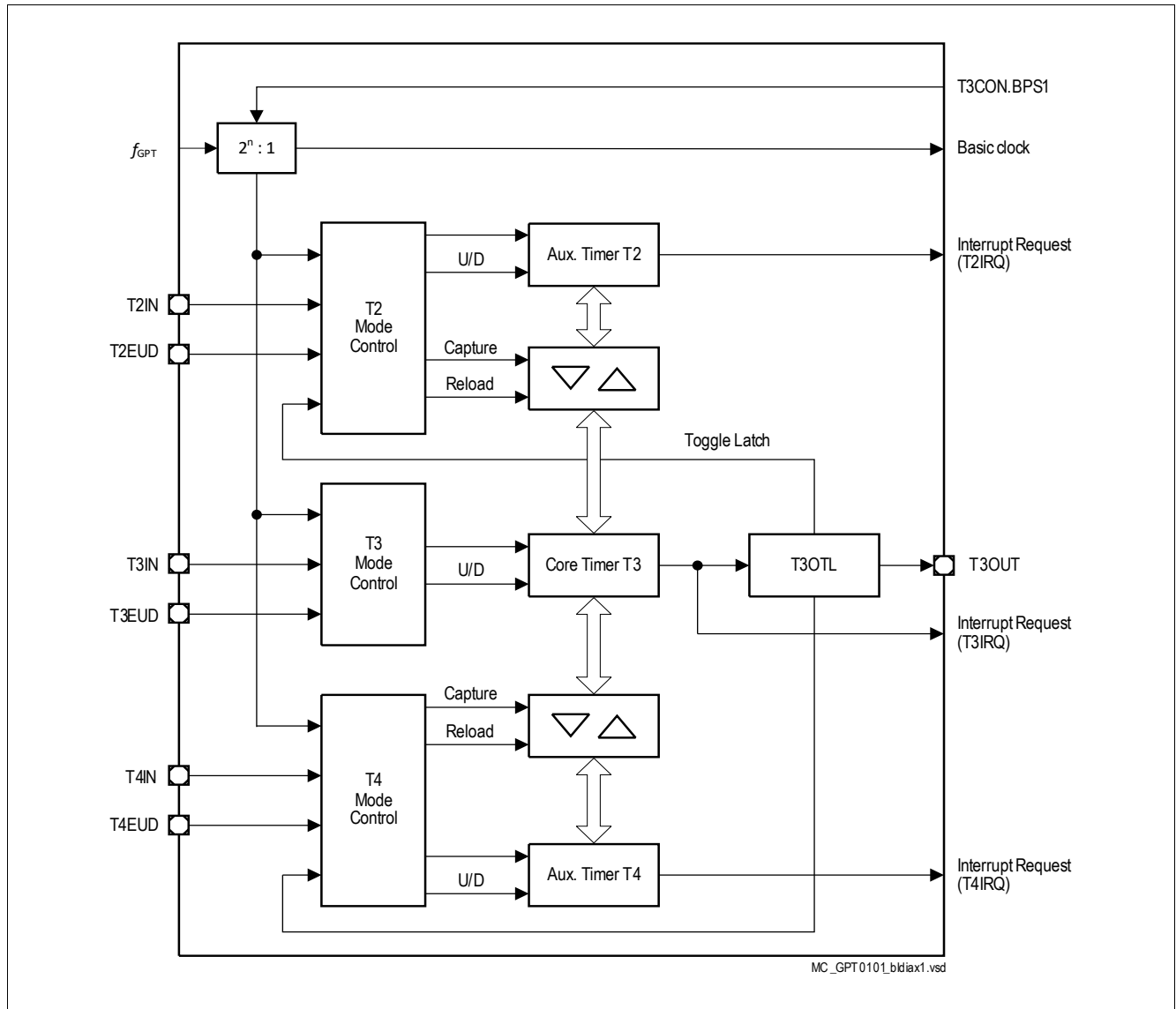


Figure 22 GPT1 Block Diagram (n = 2 ... 5)

General Purpose Timer Units (GPT12)

15.2.2 Block Diagram GPT2

Block GPT2 contains two timers/counters: The core timer T6 and the auxiliary timer T5. The maximum resolution is $f_{GPT}/2$. An additional Capture/Reload register (CAPREL) supports capture and reload operation with extended functionality.

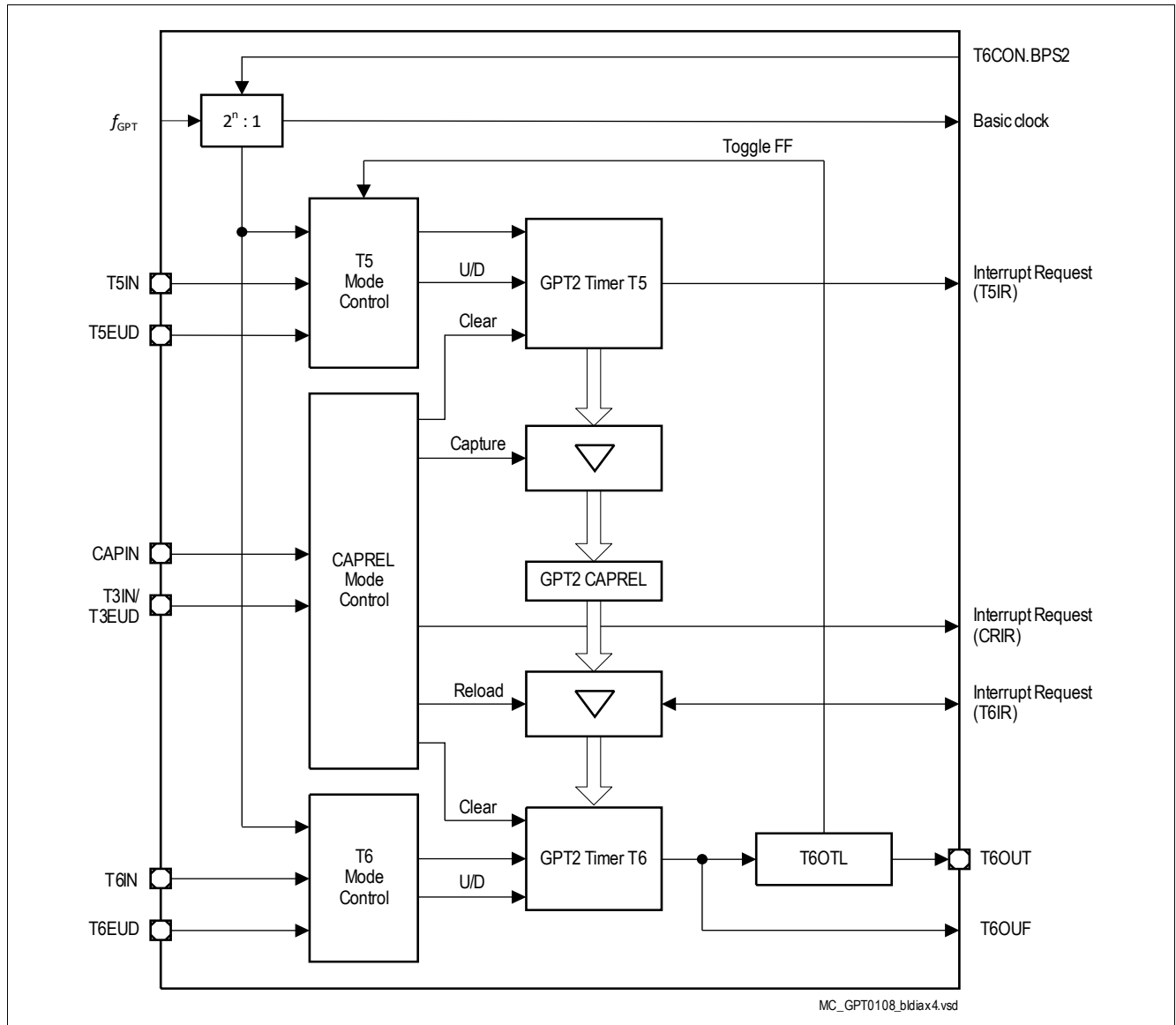


Figure 23 GPT2 Block Diagram

16 Timer2 and Timer21

16.1 Features

- 16-bit auto-reload mode
 - selectable up or down counting
- One channel 16-bit capture mode
- Baud-rate generator for U(S)ART

16.2 Introduction

Two functionally identical timers are implemented: Timer 2 and 21. The description refers to Timer 2 only, but applies to Timer 21 as well.

The timer modules are general purpose 16-bit timer. Timer 2 can function as a timer or counter in each of its modes. As a timer, it counts with an input clock of $f_{sys}/12$ (if prescaler is disabled). As a counter, Timer 2 counts 1-to-0 transitions on pin T2. In the counter mode, the maximum resolution for the count is $f_{sys}/24$ (if prescaler is disabled).

Timer2 and Timer21
16.2.1 Timer2 and Timer21 Modes Overview
Table 10 Port Registers

| Mode | Description |
|------------------------|--|
| Auto-reload | Up/Down Count Disabled <ul style="list-style-type: none"> • Count up only • Start counting from 16-Bit reload value, overflow at FFFF_H • Reload event configurable for trigger by overflow condition only, or by negative/positive edge at input pin T2EX as well • Programmable reload value in register RC2 • Interrupt is generated with reload events. |
| Auto-reload | Up/Down Count Enabled <ul style="list-style-type: none"> • Count up or down, direction determined by level at input pin T2EX • No interrupt is generated • Count up <ul style="list-style-type: none"> – Start counting from 16-Bit reload value, overflow at FFFF_H – Reload event triggered by overflow condition – Programmable reload value in register RC2 • Count down <ul style="list-style-type: none"> – Start counting from FFFF_H, underflow at value defined in register RC2 – Reload event triggered by underflow condition – Reload value fixed at FFFF_H |
| Channel capture | <ul style="list-style-type: none"> • Count up only • Start counting from 0000_H, overflow at FFFF_H • Reload event triggered by overflow condition • Reload value fixed at 0000_H • Capture event triggered by falling/rising edge at pin T2EX • Captured timer value stored in register RC2 • Interrupt is generated with reload or capture event |

17 Capture/Compare Unit 6 (CCU6)

17.1 Feature Set Overview

This section gives an overview over the different building blocks and their main features.

Timer 12 Block Features

- Three capture/compare channels, each channel can be used either as capture or as compare channel
- Generation of a three-phase PWM supported (six outputs, individual signals for High Side and low-side switches)
- 16-bit resolution, maximum count frequency = peripheral clock
- Dead-time control for each channel to avoid short-circuits in the power stage
- Concurrent update of T12 registers
- Center-aligned and edge-aligned PWM can be generated
- Single-shot mode supported
- Start can be controlled by external events
- Capability of counting external events
- Multiple interrupt request sources
- Hysteresis-like control mode

Timer 13 Block Features

- One independent compare channel with one output
- 16-bit resolution, maximum count frequency = peripheral clock
- Concurrent update of T13 registers
- Can be synchronized to T12
- Interrupt generation at period-match and compare-match
- Single-shot mode supported
- Start can be controlled by external events
- Capability of counting external events

Additional Specific Functions

- Block commutation for Brushless DC-drives implemented
- Position detection via Hall-sensor pattern
- Noise filter supported for position input signals
- Automatic rotational speed measurement and commutation control for block commutation
- Integrated error handling
- Fast emergency stop without CPU load via external signal ($\overline{\text{CTRAP}}$)
- Control modes for multi-channel AC-drives
- Output levels can be selected and adapted to the power stage

Capture/Compare Unit 6 (CCU6)**17.2 Introduction**

The CCU6 unit is made up of a Timer T12 Block with three capture/compare channels and a Timer T13 Block with one compare channel. The T12 channels can independently generate PWM signals or accept capture triggers, or they can jointly generate control signal patterns to drive AC-motors or inverters.

A rich set of status bits, synchronized updating of parameter values via shadow registers, and flexible generation of interrupt request signals provide means for efficient software-control.

Note: The capture/compare module itself is named CCU6 (capture/compare unit 6). A capture/compare channel inside this module is named CC6x.

Capture/Compare Unit 6 (CCU6)

17.2.1 Block Diagram

The Timer T12 can work in capture and/or compare mode for its three channels. The modes can also be combined (e.g. a channel works in compare mode, whereas another channel works in capture mode). The Timer T13 can work in compare mode only. The multi-channel control unit generates output patterns which can be modulated by T12 and/or T13. The modulation sources can be selected and combined for the signal modulation.

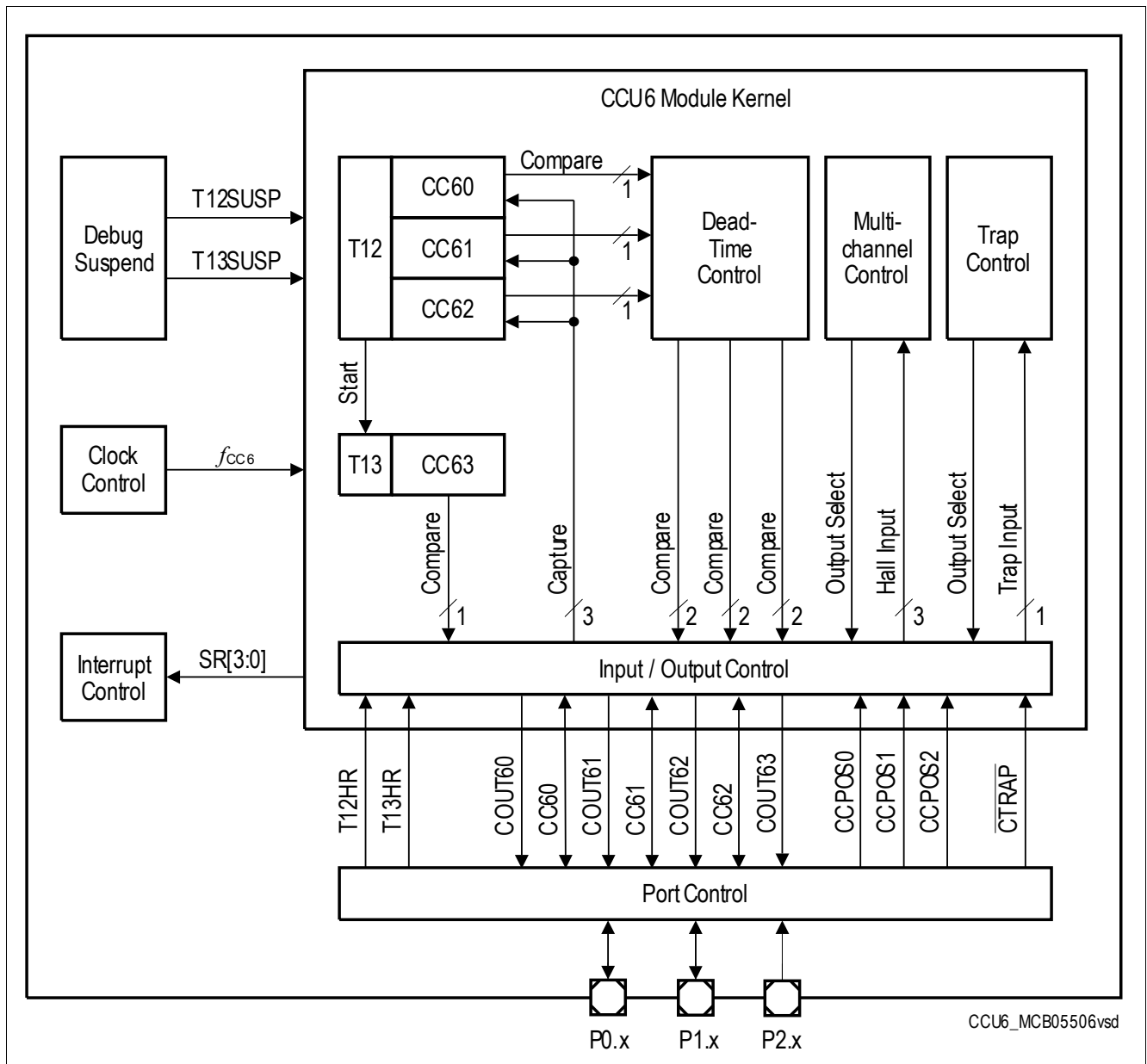


Figure 24 CCU6 Block Diagram

UART1/2**18 UART1/2****18.1 Features**

- Full-duplex asynchronous modes
 - 8-Bit or 9-Bit data frames, LSB first
 - fixed or variable baud rate
- Receive buffered (1 Byte)
- Multiprocessor communication
- Interrupt generation on the completion of a data transmission or reception
- Baud-rate generator with fractional divider for generating a wide range of baud rates, e.g. 9.6kBaud, 19.2kBaud, 115.2kBaud, 125kBaud, 250kBaud, 500kBaud
- Hardware logic for break and sync byte detection
- for UART1: LIN support: connected to timer channel for synchronization to LIN baud rate

In all modes, transmission is initiated by any instruction that uses SBUF as a destination register. Reception is initiated in the modes by the incoming start bit if REN = 1.

The serial interface also provides interrupt requests when transmission or reception of the frames has been completed. The corresponding interrupt request flags are TI or RI, respectively. If the serial interrupt is not used (i.e., serial interrupt not enabled), TI and RI can also be used for polling the serial interface.

18.2 Introduction

The UART1/2 provide a full-duplex asynchronous receiver/transmitter, i.e., it can transmit and receive simultaneously. They are also receive-buffered, i.e., they can commence reception of a second byte before a previously received byte has been read from the receive register. However, if the first byte still has not been read by the time reception of the second byte is complete, the previous byte will be lost. The serial port receive and transmit registers are both accessed at Special Function Register (SFR) SBUF. Writing to SBUF loads the transmit register, and reading SBUF accesses a physically separate receive register.

UART1/2

18.2.1 Block Diagram

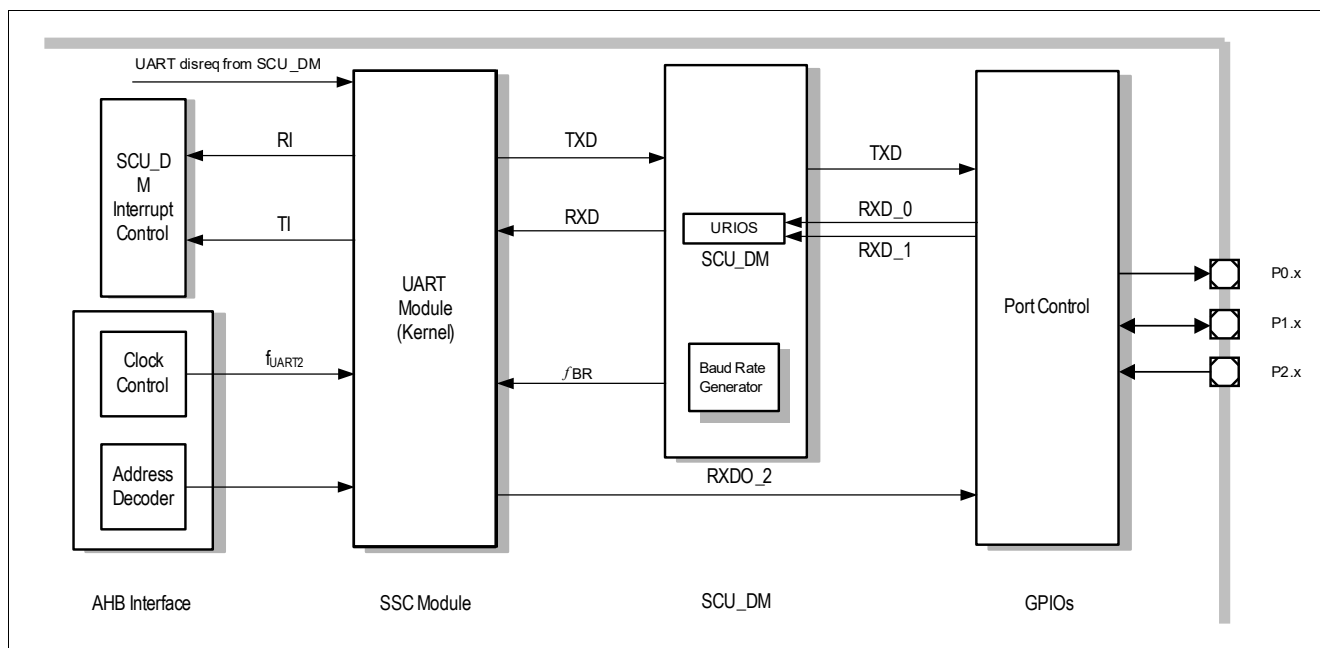


Figure 25 UART Block Diagram

18.3 UART Modes

The UART1/2 can be used in four different modes. In mode 0, it operates as an 8-Bit shift register. In mode 1, it operates as an 8-Bit serial port. In modes 2 and 3, it operates as a 9-Bit serial port. The only difference between mode 2 and mode 3 is the baud rate, which is fixed in mode 2 but variable in mode 3. The variable baud rate is set by the underflow rate on the dedicated baud-rate generator.

The different modes are selected by setting bits SM0 and SM1 to their corresponding values, as shown in Table 11.

Mode 1 example: 8 data bits, 1 start bit, 1 stop bit, no parity selection, 16 times oversampled, receive & transmit register double buffered, Tx/Rx IRQ(s).

Table 11 UART Modes

| SM0 | SM1 | Operating Mode | Baud Rate |
|-----|-----|------------------------------|------------------------------|
| 0 | 0 | Mode 0: 8-Bit shift register | $f_{sys}/2$ |
| 0 | 1 | Mode 1: 8-Bit shift UART | Variable |
| 1 | 0 | Mode 2: 9-Bit shift UART | $f_{sys}/64$ or $f_{sys}/32$ |
| 1 | 1 | Mode 3: 9-Bit shift UART | Variable |

19 LIN Transceiver

19.1 Features

General Functional Features

- Compliant to LIN2.2 Standard, backward compatible to LIN1.3, LIN2.0 and LIN 2.1
- Compliant to SAE J2602 (Slew Rate, Receiver hysteresis)

Special Features

- Measurement of LIN Master baudrate via Timer 2
- LIN can be used as Input/Output with SFR bits.
- TxD Timeout Feature (optional, on by default)
- Overcurrent limitation and overtemperature protection
- LIN module fully resettable via global enable bit

Operation Modes Features

- LIN Sleep Mode (LSLM)
- LIN Receive-Only Mode (LROM)
- LIN Normal Mode (LNM)
- High Voltage Input / Output Mode (LHVIO)

Slope Modes Features

- Normal Slope Mode (20 kbit/s)
- Low Slope Mode (10.4 kbit/s)
- Fast Slope Mode (62.5 kbit/s)
- Flash Mode (115 kbit/s, 250 kbit/s)

Wake-Up Features

- LIN Bus wake-up

19.2 Introduction

The LIN Module is a transceiver for the Local Interconnect Network (LIN) compliant to the LIN2.2 Standard, backward compatible to LIN1.3, LIN2.0 and LIN2.1. It operates as a bus driver between the protocol controller and the physical network. The LIN bus is a single wire, bi-directional bus typically used for in-vehicle networks, using baud rates between 2.4 kBaud and 20 kBaud. Additionally baud rates up to 62.5 kBaud are implemented.

The LIN Module offers several different operation modes, including a LIN Sleep Mode and the LIN Normal Mode. The integrated slope control allows to use several data transmission rates with optimized EMC performance. For data transfer at the end of line, a Flash Mode up to 115 kBaud is implemented. This Flash Mode can be used for data transfer under special conditions for up to 250 kbit/s (in production environment, point-to-point communication with reduced wire length and limited supply voltage).

LIN Transceiver

19.2.1 Block Diagram

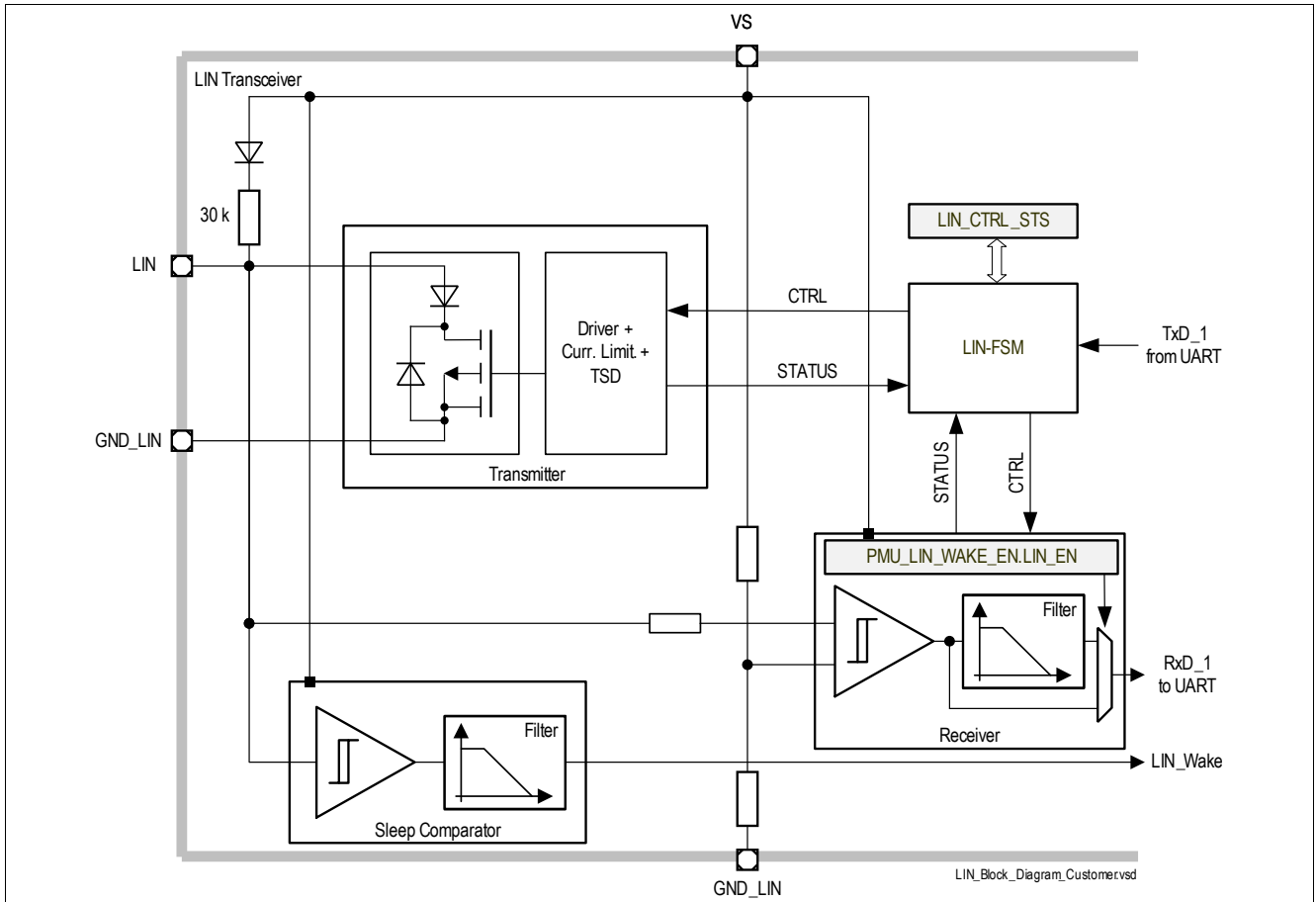


Figure 26 LIN Transceiver Block Diagram

20 High-Speed Synchronous Serial Interface SSC1/2

20.1 Features

- Master and Slave Mode operation
 - Full-duplex or half-duplex operation
- Transmit and receive double buffered
- Flexible data format
 - Programmable number of data bits: 2 to 16 bits
 - Programmable shift direction: Least Significant Bit (LSB) or Most Significant Bit (MSB) shift first
 - Programmable clock polarity: idle low or high state for the shift clock
 - Programmable clock/data phase: data shift with leading or trailing edge of the shift clock
- Variable baud rate, e.g. 250kBaude - 8MBaud
- Compatible with Serial Peripheral Interface (SPI)
- Interrupt generation
 - On a transmitter empty condition
 - On a receiver full condition
 - On an error condition (receive, phase, baud rate, transmit error)
 - On a transfer complete condition
- Port direction selection, see [Chapter 14](#)

20.2 Introduction

The High-Speed Synchronous Serial Interface (SSC) supports both full-duplex and half-duplex serial synchronous communication. The serial clock signal can be generated by the SSC internally (master mode), using its own 16-Bit baud-rate generator, or can be received from an external master (slave mode). Data width, shift direction, clock polarity, and phase are programmable. This allows communication with SPI-compatible devices or devices using other synchronous serial interfaces.

Data is transmitted or received on lines TXD and RXD, which are normally connected to the pins MTSR (Master Transmit/Slave Receive) and MRST (Master Receive/Slave Transmit). The clock signal is output via line MS_CLK (Master Serial Shift Clock) or input via line SS_CLK (Slave Serial Shift Clock). Both lines are normally connected to the pin SCLK. Transmission and reception of data are double-buffered.

High-Speed Synchronous Serial Interface SSC1/2

20.2.1 Block Diagram

Figure 27 shows all functional relevant interfaces associated with the SSC Kernel.

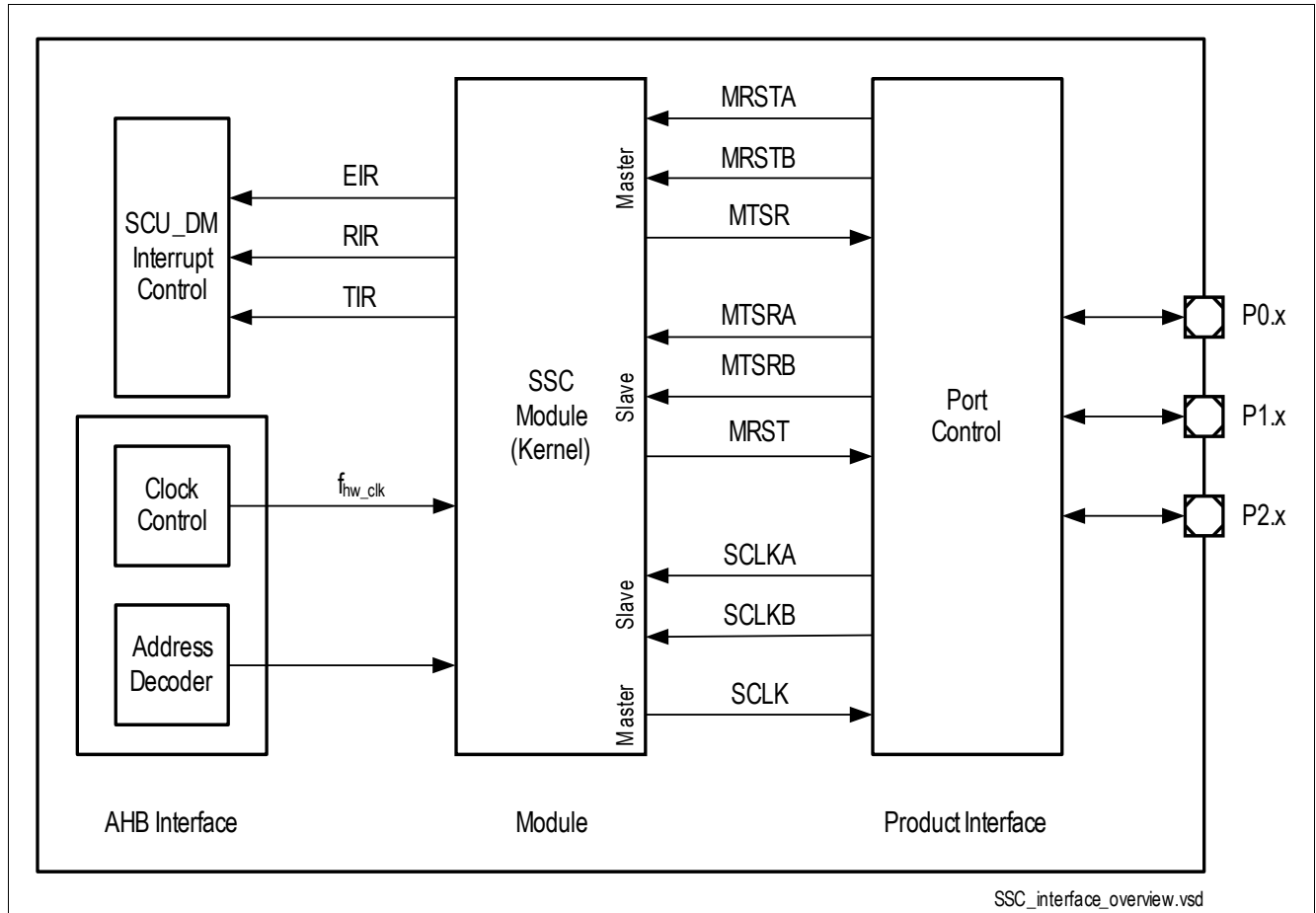


Figure 27 SSC Interface Diagram

Measurement Unit

21 Measurement Unit

21.1 Features

- 1 x 10-bit ADC with 11 inputs
- Supply Voltage Attenuators with attenuation of **VBAT_SENSE, VS, MONx, P2.x**.
- 1 x 8-bit ADC with 9 inputs
- Supply Voltage Attenuators with attenuation of **VS, VDDEXT, VSD, VCP, VDDP, VBG, VDDC, T_SENSE1 (Central Temperature Sensor), T_SENSE2 (Bridge Driver Charge Pump Temperature Sensor)**.
- Monitoring of PMU bandgap by 8-bit ADC to support functional safety requirements.
- Temperature Sensor to monitor the chip temperature and Bridge Driver Charge Pump temperature.
- Supplement Block with Reference Voltage Generation, Bias Current Generation, Voltage Buffer for NVM Reference Voltage, Voltage Buffer for Analog Module Reference Voltage and Test Interface.

21.2 Introduction

The measurement unit is a functional unit that comprises the following associated sub-modules:

Table 12 Measurement functions and associated modules

| Module Name | Modules | Functions |
|-------------------------|---|---|
| Central Functions Unit | Bandgap reference circuit + current reference circuit | The bandgap-reference sub-module provides two reference voltages 1. an accurate reference voltage for the 10-bit and 8-bit ADCs. A local dedicated bandgap circuit is implemented to avoid deterioration of the reference voltage caused e.g. by crosstalk or ground voltage shift. 2. the reference voltage for the NVM module |
| 10-bit ADC (ADC1) | 10-bit ADC module with 11 multiplexed analog inputs | VBAT_SENSE, VS and MONx measurement. Five (5V) analog inputs from Port 2.x |
| 8-bit ADC (ADC2) | 8-bit ADC module with 9 multiplexed inputs | VS/VDDEXT/VSD/VCP/VDDP/VBG/VDDC/BDrv CP Temperature Sensor and Central Temperature Sensor measurement. |
| Temperature Sensor | Temperature sensor readout amplifier with two multiplexed ΔV_{be} -sensing elements | Generates output voltage which is a linear function of the local chip (T_j) temperature. |
| Measurement Core Module | Digital signal processing and ADC control unit | 1. Generates the control signal for the 8-bit ADC 2 and the synchronous clock for the switched capacitor circuits (temperature sensor) 2. Performs digital signal processing functions and provides status outputs for interrupt generation. |

Measurement Unit

21.2.1 Block Diagram

The Structure of the Measurement Functions Module is shown in the following figure.

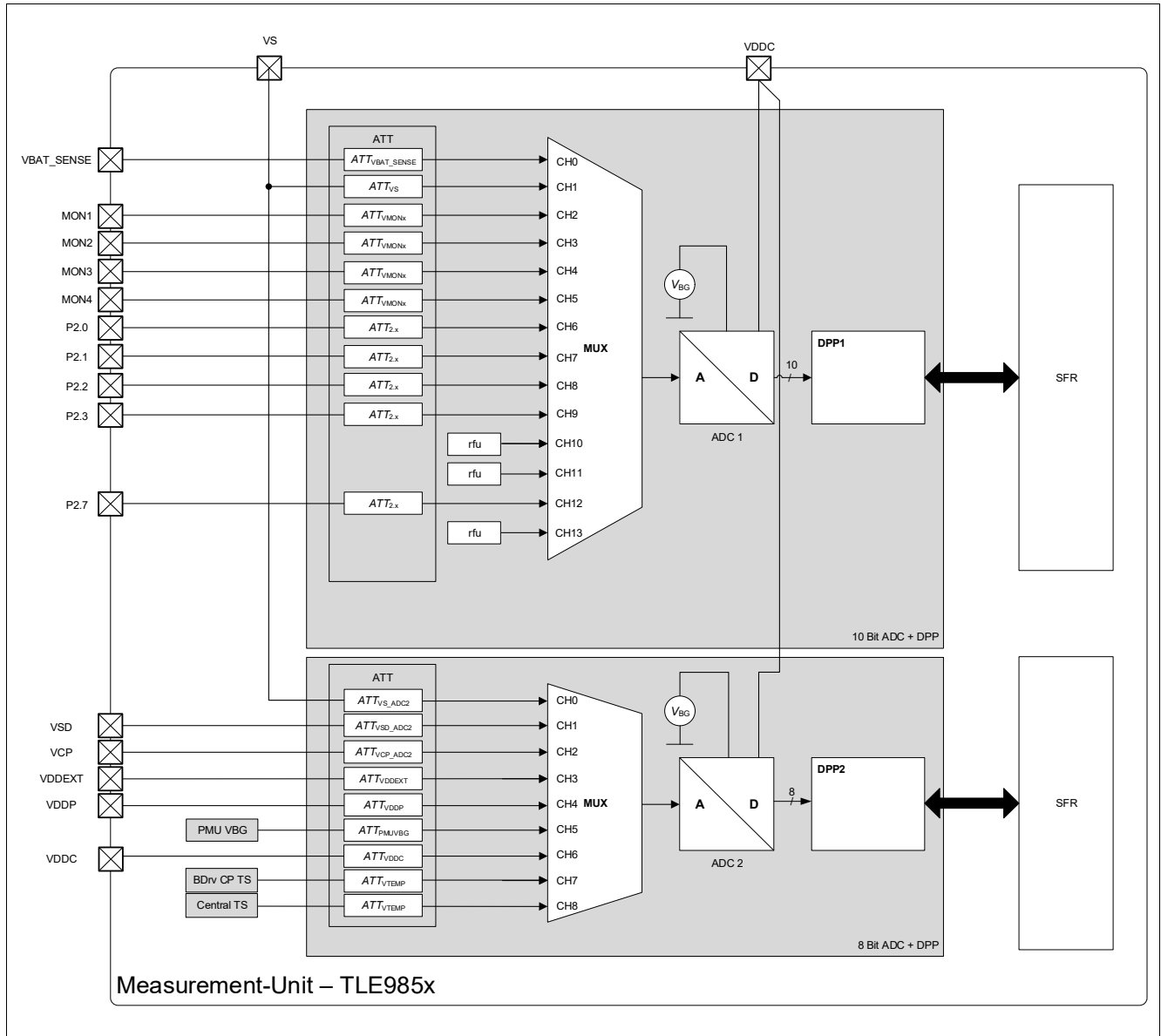


Figure 28 Measurement Unit-Overview

22 Measurement Core Module (incl. ADC2)

22.1 Features

- 9 individually programmable channels split into two groups of user configurable and non user configurable
- Individually programmable channel prioritization scheme for measurement unit
- Two independent filter stages with programmable low-pass and time filter characteristics for each channel
- Two channel configurations:
 - Programmable upper- and lower trigger thresholds comprising a fully programmable hysteresis
 - Two individually programmable trigger thresholds with limit hysteresis settings
- Status for all channel thresholds
- Operation down to reset threshold of entire system

22.2 Introduction

The basic function of this block is the digital postprocessing of several analog digitized measurement signals by means of filtering, level comparison and interrupt generation. The measurement postprocessing block is built of nine identical channel units attached to the outputs of the 9-channels 8-bit ADC (ADC2). It processes nine channels, where the channel sequence and prioritization is programmable within a wide range.

Measurement Core Module (incl. ADC2)

22.2.1 Block Diagram

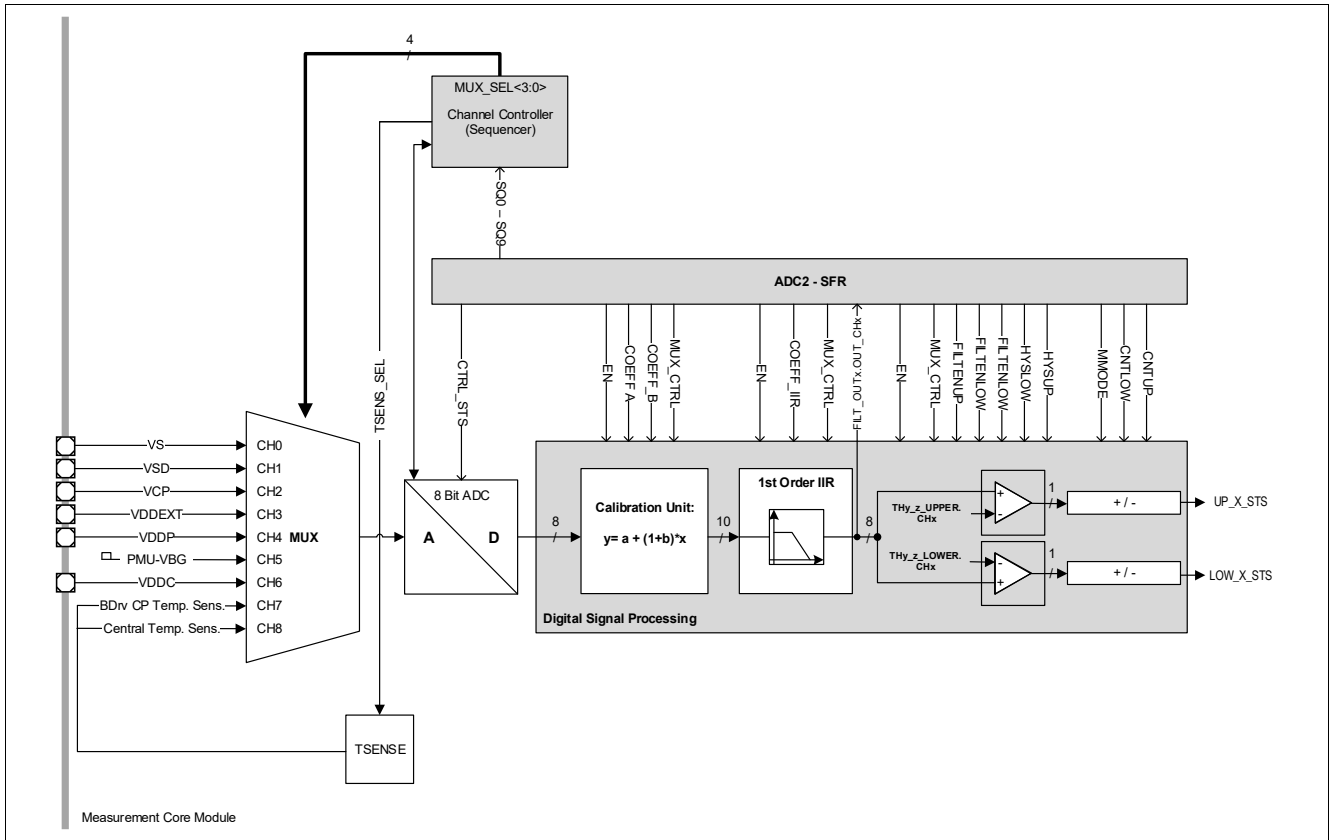


Figure 29 Module Block Diagram

23 Analog Digital Converter ADC10B (ADC1)

23.1 Features

The basic function of this block is the digital postprocessing of several analog digitized measurement signals by means of filtering, level comparison and interrupt generation. The measurement postprocessing block is built of the same number of identical channel units attached to the outputs of the 10-bit ADC. It processes all channels, where the channel sequence and prioritization is programmable within a wide range.

Functional Features

- 10 Bit SAR ADC with conversion time of 17 clock cycles
- programmable clock divider for sequencer and ADC
- 11 individually programmable channels:
 - 6 HV Channels: VS, VBAT_SENSE, MON1...MON4
 - 5 LV Channels: P2.0, P2.1, P2.2, P2.3, P2.7
- all channels are fully calibrated; calibration can be enabled/disabled by user
- individually programmable channel prioritization scheme for digital postprocessing (dpp)
- two independent filter stages with programmable low-pass and time filter characteristics for each channel
- two channel configurations:
 - programmable upper- and lower trigger thresholds comprising a fully programmable hysteresis
 - two individually programmable trigger thresholds with limit hysteresis settings
- individually programmable upper threshold and lower threshold interrupts and status for all channel thresholds
- one additional differential channel (MON1-MON2) with postprocessing and interrupt generation
- ADC voltage reference completely integrated

Note: In case the MONx should be evaluated by the ADC1, it is recommended to add 6.8nF capacitors close to the MONx pin of the device, in order to build an external RC filter to limit the bandwidth of the input signal.

Analog Digital Converter ADC10B (ADC1)

23.2 Introduction

23.2.1 Block Diagram

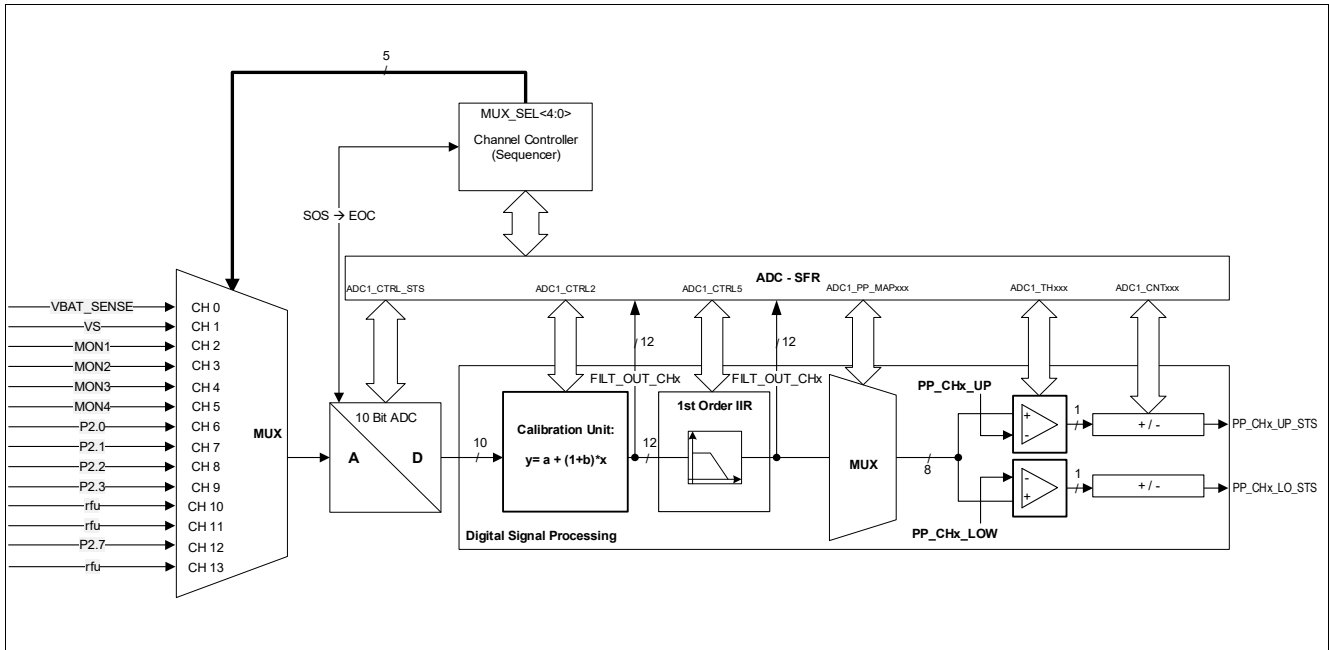


Figure 30 Module Block Diagram

High-Voltage Monitor Input

24 High-Voltage Monitor Input

24.1 Features

- Four High-voltage inputs with $V_S/2$ threshold voltage
- Wake capability for system stop mode and system sleep mode
- Edge sensitive wake-up feature configurable for transitions from low to high, high to low or both directions
- MON inputs can also be evaluated with ADC in Active Mode, using adjustable threshold values
- Selectable pull-up and pull-down current sources available

24.2 Introduction

This module is dedicated to monitor external voltage levels above or below a specified threshold. Each MONx pin can further be used to detect a wake-up event by detecting a level change by crossing the selected threshold. This applies to any power mode. Further more each MONx pin can be sampled by the ADC as analog input.

24.2.1 Block Diagram

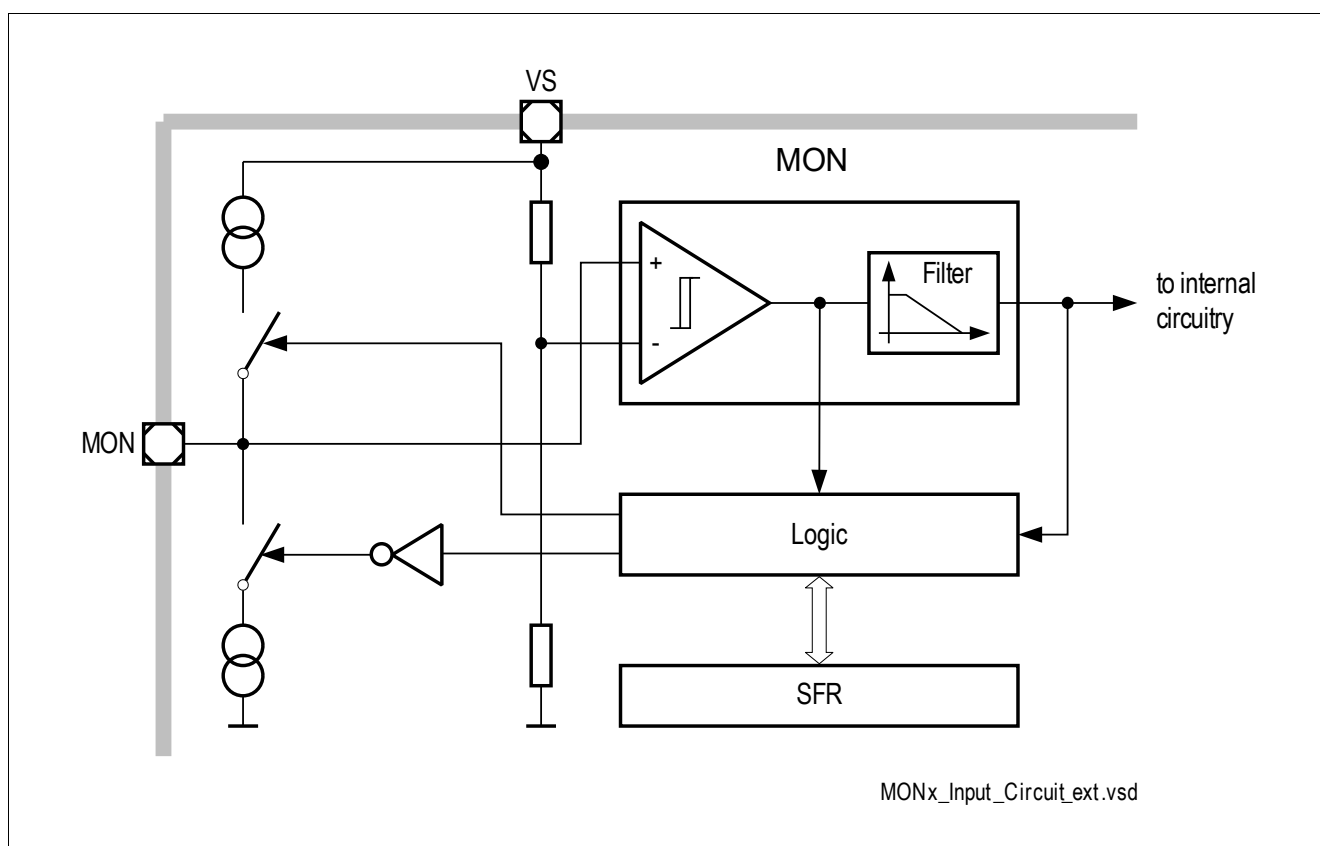


Figure 31 Monitoring Input Block Diagram

High-Side Switch**25 High-Side Switch****25.1 Features**

The high-side switch is optimized for driving resistive loads. Only small line inductances are allowed. Typical applications are single or multiple LEDs of a dashboard, switch illumination or other loads that require a high-side switch.

A cyclic switch activation during Sleep Mode or Stop Mode of the system is also available.

Functional Features

- Multi purpose high-side switch for resistive load connections (only small line inductances are allowed)
- Overcurrent limitation
- Selectable current capability (25 mA/50 mA/100 mA/150 mA) by adjustable overcurrent detection with automatic shutdown
- Overtemperature detection and automatic shutdown
- Open load detection in on mode with open load current of typ. 1.4 mA
- Interrupt signalling of overcurrent, overtemperature and open load condition
- Cyclic switch activation in Sleep Mode and Stop Mode with cyclic sense support and reduced driver capability: max. 40 mA
- PWM capability up to 25 kHz
- Internal connection to System-PWM Generator (CCU6)
- Slew rate control for low EMI characteristic

Applications hints

- The voltage at HSx must not exceed the supply voltage by more than 0.3V to prevent a reverse current from HSx to VS.

High-Side Switch

25.2 Introduction

25.2.1 Block Diagram

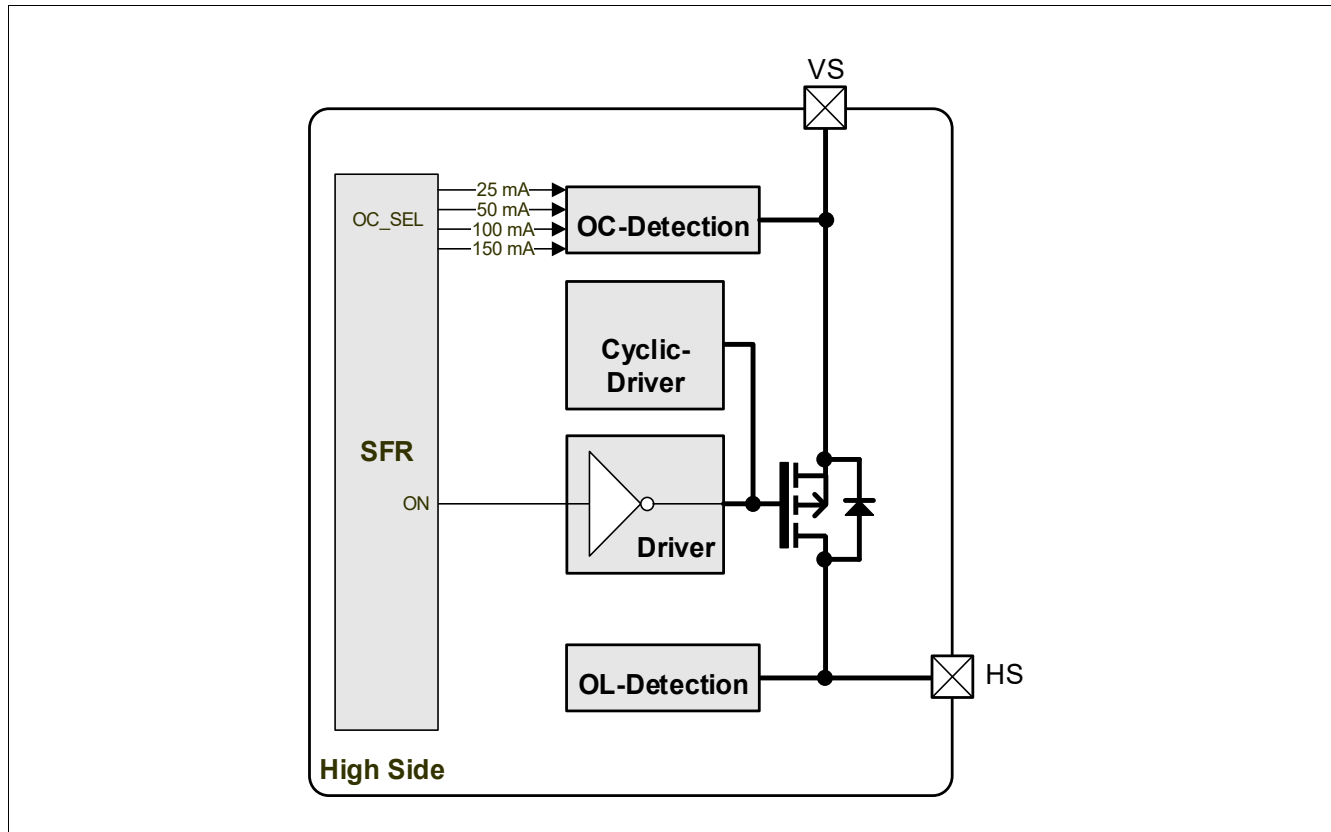


Figure 32 High-Side Module Block Diagram (incl. subblocks)

25.2.2 General

The high-side switch can generally be controlled in three different ways:

- In normal mode the output stage is fully controllable through the **SFR** Registers **HSx_CTRL**. Protection functions as overcurrent, overtemperature and open load detection are available.
- The PWM Mode can also be enabled by a **HSx_CTRL - SFR** bit. The PWM configuration has to be done in the corresponding PWM Module. All protection functions are also available in this mode. The maximum PWM frequency must not exceed 25 kHz (disabled slew rate control only).
- The high-side switch provides also the possibility of cyclic switch activation in all low power modes (Sleep Mode and Stop Mode). In this configuration it has limited functionality with limited current capability. Diagnostic functions are not available in this mode.

26 Bridge Driver (incl. Charge Pump)

26.1 Features

The Bridge Driver is intended to drive external normal-level MOSFETs in bridge configuration and provides many diagnostic possibilities to detect faults.

Functional Features

- **Flexible control** by SFRs of Bridge Driver module or PWM output signals of CCU6 module
- **Current-driven output stages** to control external n-channel MOSFET gates with flexibly programmable gate current profile
- **Adjustable cross-conduction protection**
- **High-current discharge mode** to reduce dead times and to keep external MOSFETs off during fast transients
- **Passive pull-down mode** to keep external MOSFETs off if the Bridge Driver is disabled
- **Brake mode** with reduced current consumption to statically switch on external MOSFETs
- **Hold mode** with low current consumption to switch on external low-side MOSFETs if the Bridge Driver is disabled
- **Timing measurements** of on/off delays and on/off slope durations
- **Adaptive control mode** with automatic adjustment of gate current values
- **Integrated 2-stage charge pump** for low-voltage operation and statical MOSFET gate control
- **Adjustable voltage monitoring** of Bridge Driver supply voltage (VSD) and charge pump output voltage (VCP)
- **Adjustable short-circuit detection** in on and off state
- **Open-load detection** in off state
- **Overtemperature** detection and shutdown

Bridge Driver (incl. Charge Pump)

26.2 Introduction

26.2.1 Block Diagram

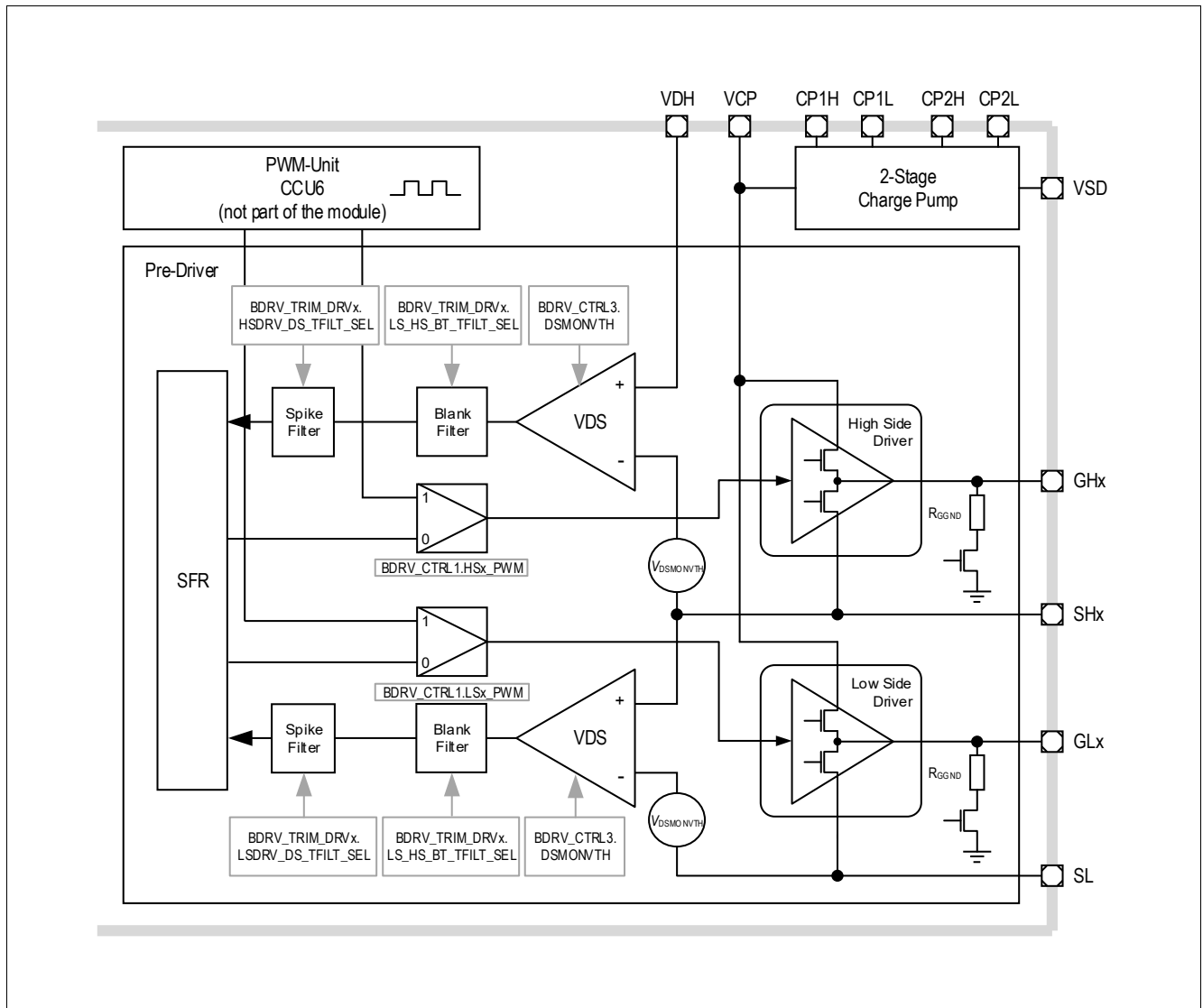


Figure 33 Driver Module Block Diagram (incl. System Connections)

26.2.2 Flexible Control

Each gate driver of the Bridge Driver module can be switched on and off in two different ways:

- Static Mode: The gate drivers are statically switched on or off by the Bridge Driver module SFRs.
- PWM Mode: The gate drivers are PWM-controlled by the System PWM Module (CCU6). The interconnection from the CCU6 output channels to the gate drivers is set up by the Bridge Driver module SFRs.

In both modes all diagnostic and protection functions (short-circuit, open-load, and overtemperature detection) are available.

Bridge Driver (incl. Charge Pump)

26.2.3 Current-Driven Output Stages

The Bridge Driver output stages generate source and sink currents to charge and discharge the gates of the external n-channel MOSFETs. The gate current values are programmable to vary the slew rate at the bridge output.

26.2.3.1 Overview

Figure 34 shows an overview of one switching cycle of an external MOSFET.

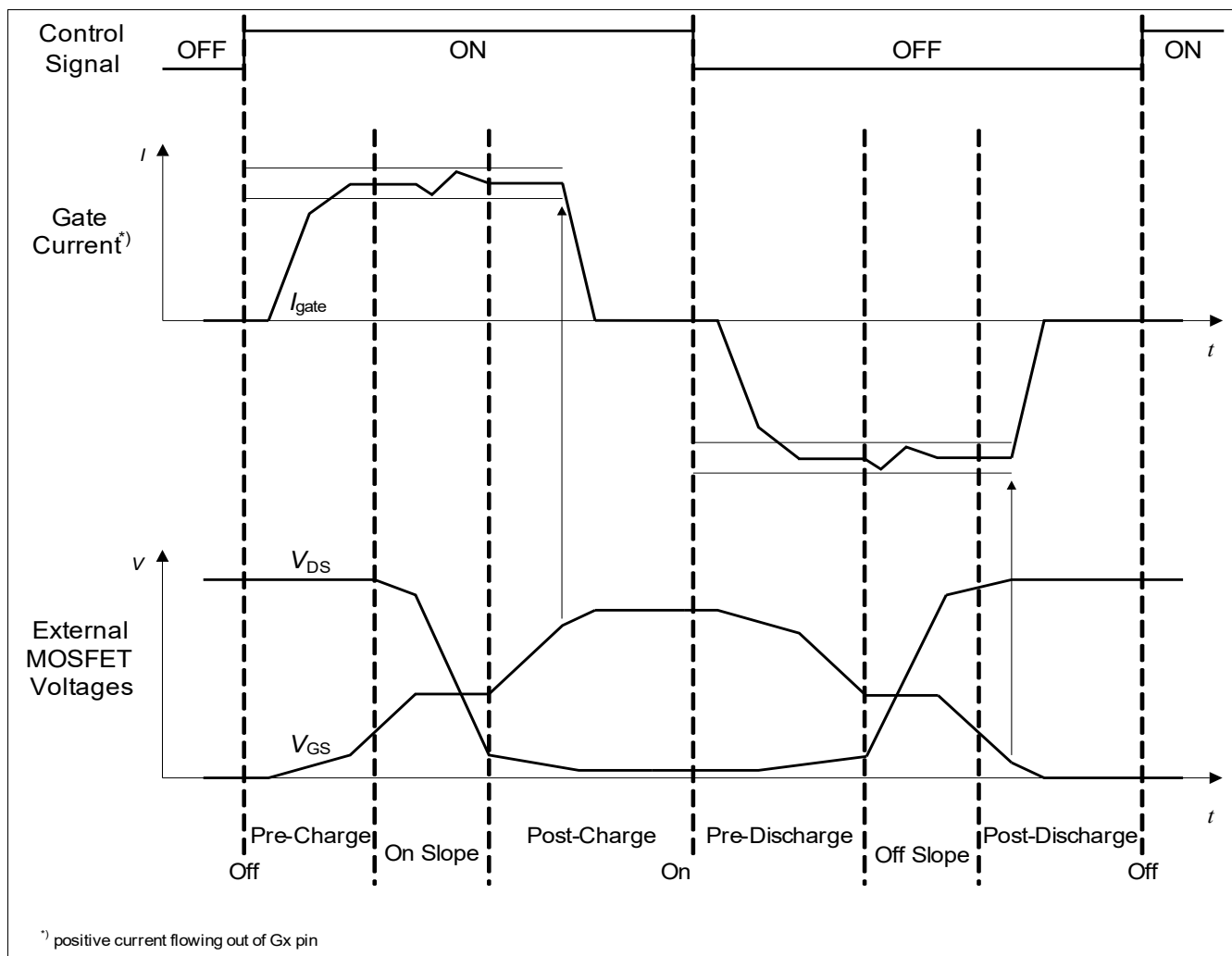


Figure 34 Switching cycle

The control input signal sets the gate driver either in charge or discharge mode, i.e. it generates a source current flowing out of the driver to charge the gate of an external MOSFET or a sink current flowing into the driver to discharge the gate of an external MOSFET.

Based on the changes on the drain-to-source voltage of the external MOSFET the charging and discharging phases can each be divided into three subphases.

Subphases of the charging phase:

- pre-charge subphase: the gate of the external MOSFET is pre-charged without change on V_{DS} ; the external MOSFET is still off
- on slope subphase: the gate of the external MOSFET is further charged while the external MOSFET turns on and generates the on slope at V_{DS}

Bridge Driver (incl. Charge Pump)

- post-charge subphase: the gate of the external MOSFET is post-charged until the maximum V_{GS} the gate driver is able to provide; the external MOSFET is on and its $R_{DS(on)}$ decreases to its minimum value

Subphases of the discharging phase:

- pre-discharge subphase: the gate of the external MOSFET is pre-discharged without significant change on V_{DS} ; the external MOSFET is still on, but its $R_{DS(on)}$ increases
- off slope subphase: the gate of the external MOSFET is further discharged while the external MOSFET turns off and generates the off slope at V_{DS}
- post-discharge subphase: the gate of the external MOSFET is post-charged until V_{GS} is equal to 0V; the external MOSFET is off and is kept off

26.2.3.2 Switch-On

Figure 35 shows the detailed behavior of the gate driver output stage in the switch-on phase and the corresponding electrical characteristic parameters.

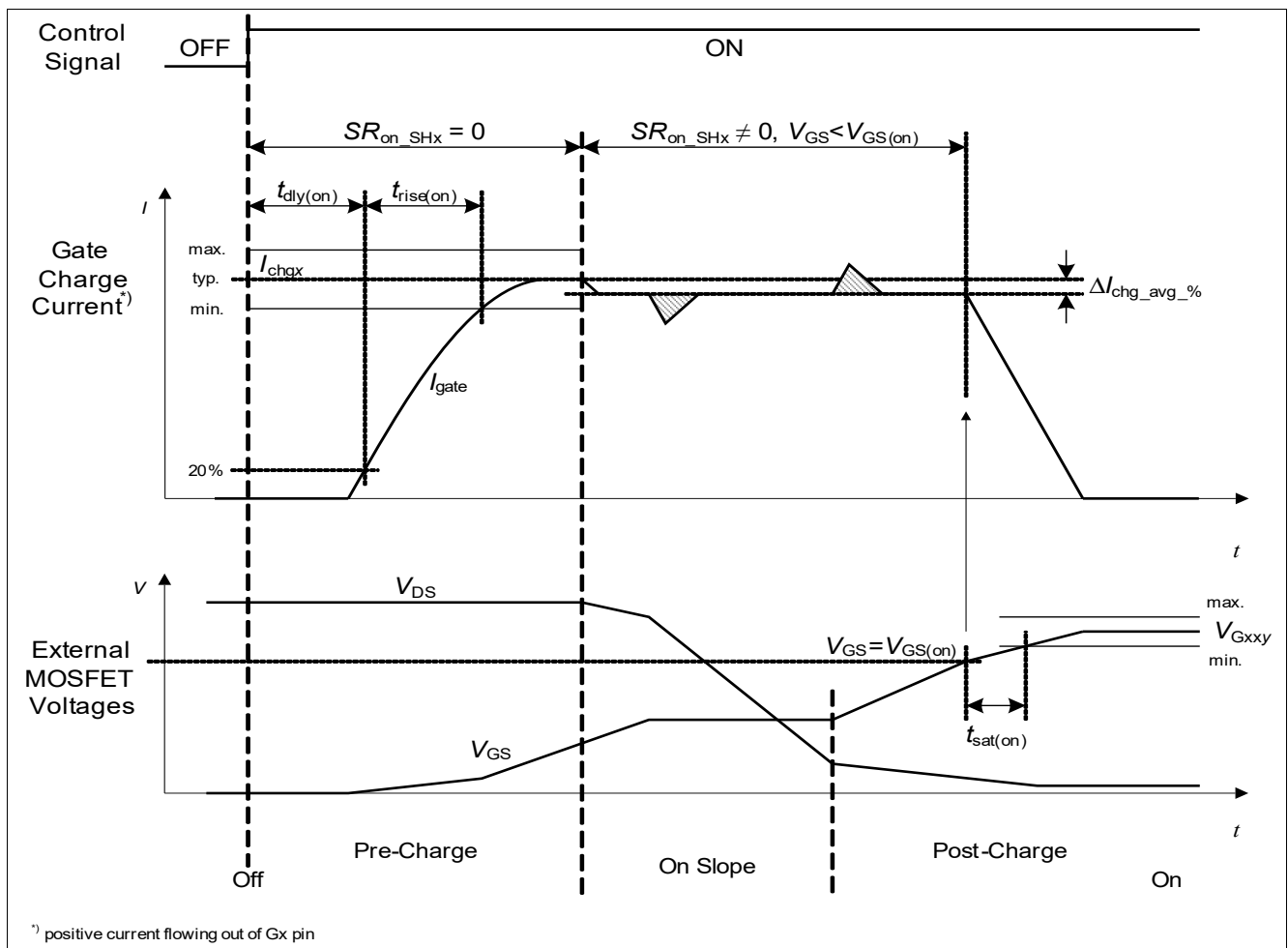


Figure 35 Detailed behavior of the gate driver output stage in the switch-on phase

After an initial turn-on delay time $t_{dly(on)}$ the gate charge current I_{gate} rises and after additional $t_{rise(on)}$ reaches its specified minimum limit $I_{chgx,min}$ and stays stable until the gate-to-source voltage of the external MOSFET reaches $V_{GS} = V_{GS(on)}$. During the slope at the corresponding SHx pin (i.e. $SR_{on_SHx} \neq 0$) the average gate current deviates less than $\Delta I_{chg_avg_ \%}$ from the original set point $I_{chgx,typ}$. The gate of the external MOSFET is further charged to the high-level output voltage of the gate driver $V_{Gxxy,max}$. The time from exceeding $V_{GS} = V_{GS(on)}$ and reaching $V_{Gxxy,min}$ is defined by $t_{sat(on)}$.

Bridge Driver (incl. Charge Pump)

26.2.3.3 Switch-Off

Figure 36 shows the detailed behavior of the gate driver output stage in the switch-off phase and the corresponding electrical characteristic parameters.

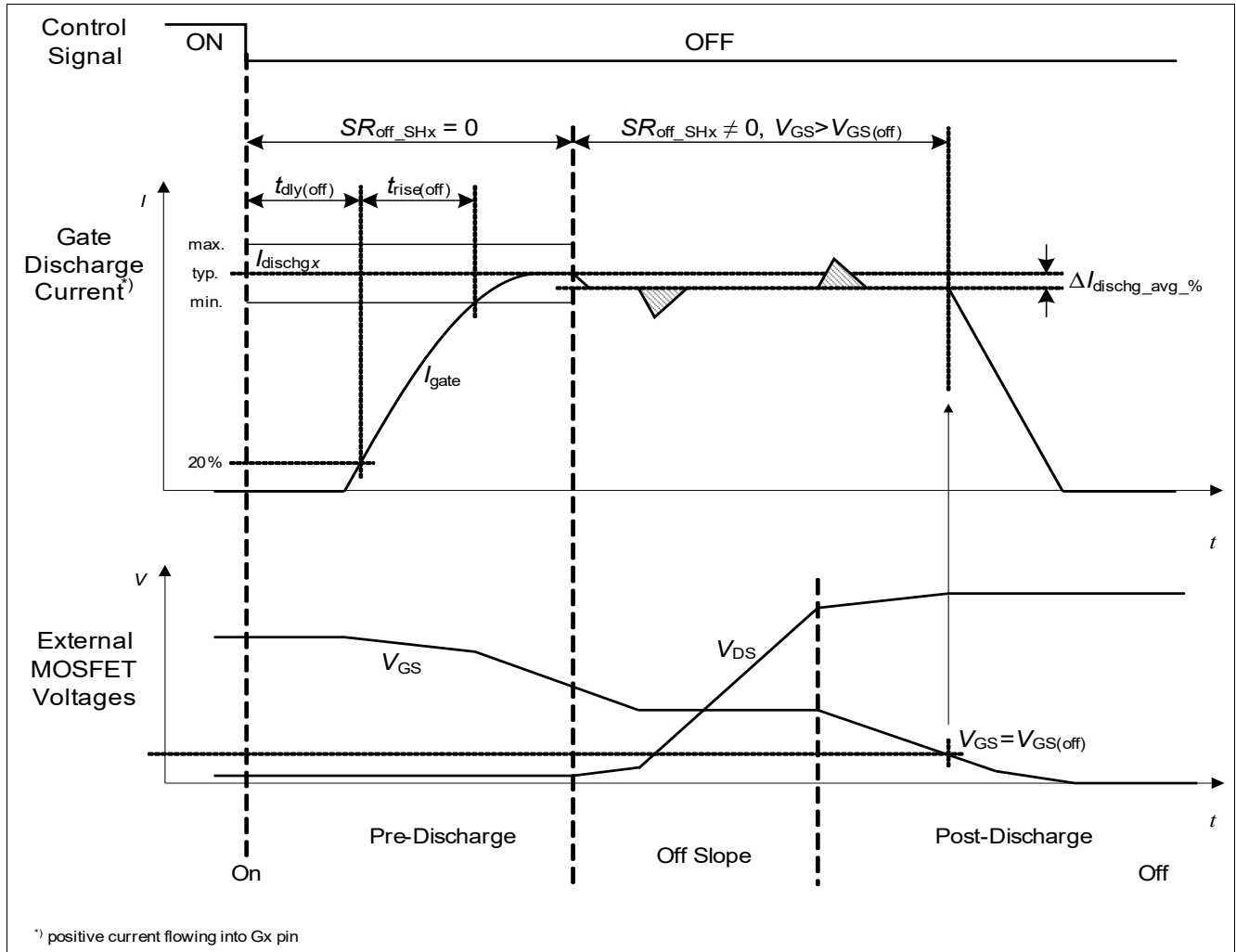


Figure 36 Detailed behavior of the gate driver output stage in the switch-off phase

After an initial turn-off delay time $t_{dly(off)}$ the gate discharge current I_{gate} rises and reaches its specified minimum limit $I_{dischg,min}$ after $t_{rise(off)}$ and stays stable until the gate-to-source voltage of the external MOSFET reaches $V_{GS} = V_{GS(off)}$. During the slope at the corresponding SHx pin (i.e. $SR_{off_SHx} \neq 0$) the average gate discharge current deviates less than $\Delta I_{dischg_avg_ \%}$ from the original set point I_{dischg} .

26.2.3.4 Control Modes

There are two basic modes to program the gate current set point values of the output stages: constant mode and sequencer mode.

- In constant mode a simple gate current profile is defined by SFRs where the gate charging phase and the gate discharging phase each have two current set point values and one duration value. The second current set point value remains valid until the driver changes from charge mode to discharge mode or vice versa and is intended to statically keep on or off the external MOSFET at a reduced gate current level to be robust against external shorts at the gate pin.

Bridge Driver (incl. Charge Pump)

- In sequencer mode an advanced gate current profile is defined by SFRs where the gate charging phase and the gate discharging phase each are split into consecutive sub phases with individual current set point values and duration values (see **Figure 37**):
 - For the gate charging phase 5 current set point values ($i_{x(on)}$) and 4 duration values ($t_{x(on)}$) are defined by SFRs.
 - The fifth current setpoint value $i_{5(on)}$ remains valid until the driver changes to discharge mode. This charge current is intended to statically keep on the external MOSFET (e.g. driving an external R_{GS}) at a reduced gate current level to be robust against external gate-to-source shorts.
 - For the gate discharging phase 5 current set point values ($i_{x(off)}$) and 4 duration values ($t_{x(off)}$) are defined by SFRs.
 - The fifth current setpoint value $i_{5(off)}$ remains valid until the driver changes to charge mode. This discharge current is intended to statically keep off the external MOSFET (e.g. during fast voltage transients or EMI) at a reduced gate current level to be robust against external gate-to-drain shorts.
 - At the transition between two gate current set points the actual gate driver output current settles within $t_{set(seq)}$ to the new gate current set point (see **Figure 38**).

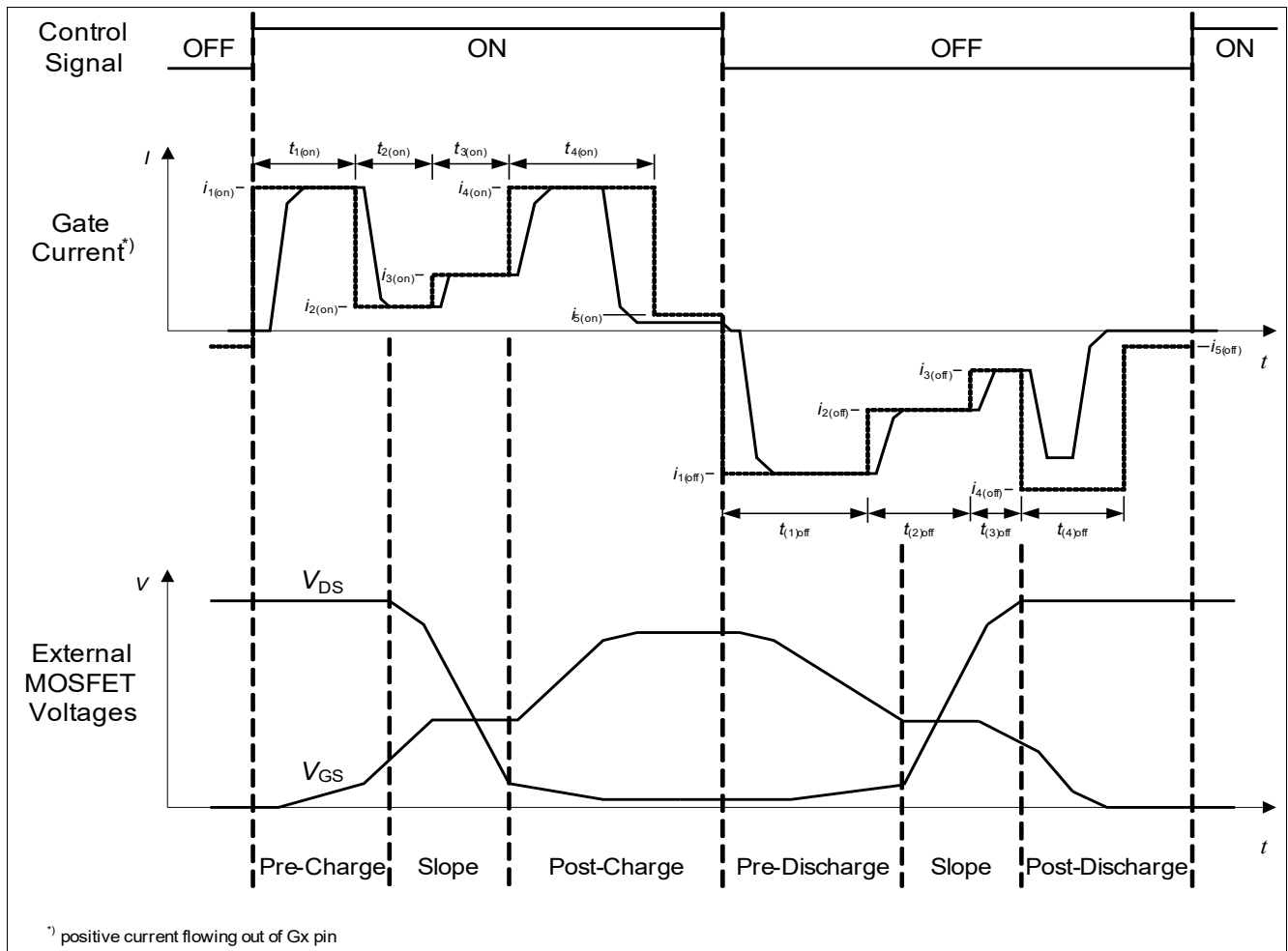
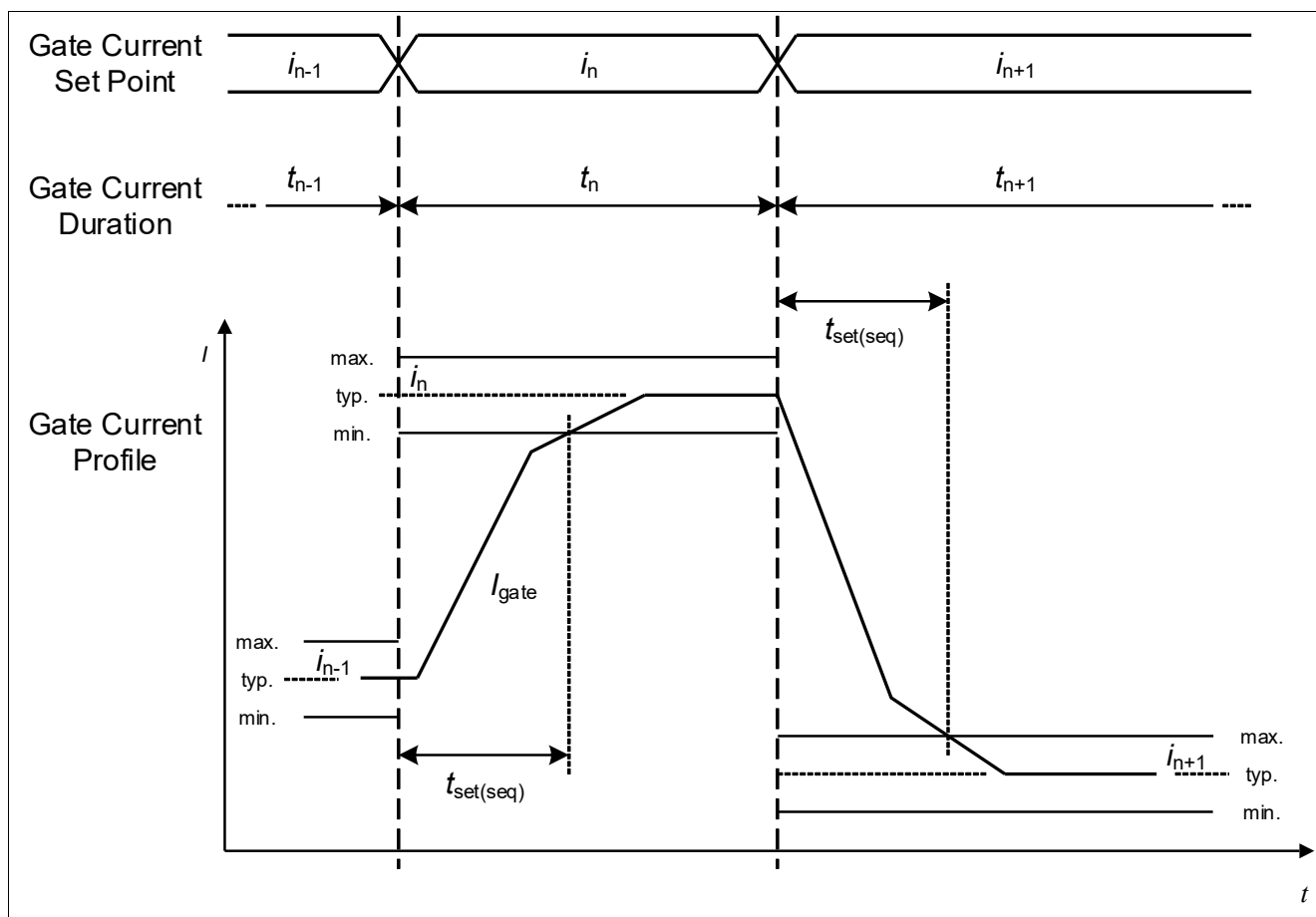


Figure 37 Gate current set point values generated by the sequencer

Bridge Driver (incl. Charge Pump)

Figure 38 Gate current settling time

26.2.4 Adjustable Cross-Conduction Protection

The Bridge Driver protects half bridges of external MOSFETs against cross conduction. After switching off one of the MOSFETs of a half bridge the complementary MOSFET cannot be switched on for an optionally programmable time defined by SFRs.

26.2.5 High-Current Discharge Mode

The high-current discharge mode provides a low-ohmic path between the Gx and Sx pins to do a fast discharge of the external MOSFET gate and keep the external MOSFET off during fast voltage transients at its drain or source terminals.

The high-current discharge mode is activated in the following situations:

- in the case of an emergency shutdown after detection of an error condition,
- if the complementary external MOSFET is switched on to avoid cross conduction in the external half bridge.

If the adjustable cross-conduction protection feature is enabled the high-current discharge mode is delayed and activated at the same time than the switch-on control signal of the complementary MOSFET.

26.2.6 Passive Pull-Down Mode

If the Bridge Driver module is disabled the passive pull-down mode activates resistors R_{GGND} between the Gx pins and ground to passively keep discharged the gates of the external MOSFETs. During normal operation these pull-down resistors are switched off.

Bridge Driver (incl. Charge Pump)

26.2.7 Brake Mode

In Brake Mode either both external high-side MOSFETs or both external low-side MOSFETs are statically switched on to short circuit the motor coil to brake the motor or keep it actively blocked during standstill. Since in brake mode no PWM capability is needed the charge pump is set into low-power mode to reduce the current consumption I_{VSD_BK} from the VSD pin.

26.2.8 Hold Mode

In Hold Mode the external low-side MOSFETs can be switched to an auxiliary gate voltage V_{Gxx_HM} to terminate the motor pins in all cases where the Bridge Driver and its charge pump is disabled (including stop mode and sleep mode where the Bridge Driver is disabled by default). This leads to low current consumption I_{VSD_SMHM} and I_{VSD_STPMHM} from the VSD pin. The Hold Mode is configured by SFRs in the Power Management Unit where the behavior during stop or sleep mode is defined. The configuration includes the channel-individual selection between static and cyclic activation of the Hold mode and programmable timing.

Note: In Hold Mode the monitoring and protection of the Bridge Driver is not available.

26.2.9 Timing Measurements

The Bridge Driver provides fast comparators with low propagation delay t_{cdly} at the SHx pins to measure on and off delays $t_{sdly(on)}$ and $t_{sdly(off)}$ between changes on the control signals and the corresponding slopes at the SHx pins. Additionally, these comparators are able to measure the on and off slope durations $t_{sdur(on)}$ and $t_{sdur(off)}$ at the SHx pins. The measured values are stored in SFRs for further evaluation by software or by the adaptive control mode (see [Chapter 26.2.10](#)).

Figure 39 shows the thresholds $V_{SH(high)}$ and $V_{SH(low)}$ and propagation delay t_{cdly} of the fast comparators and the measured slope timing parameters $t_{sdly(on)}$, $t_{sdur(on)}$, $t_{sdly(off)}$, and $t_{sdur(off)}$ during PWM actuation of the external low-side MOSFET.

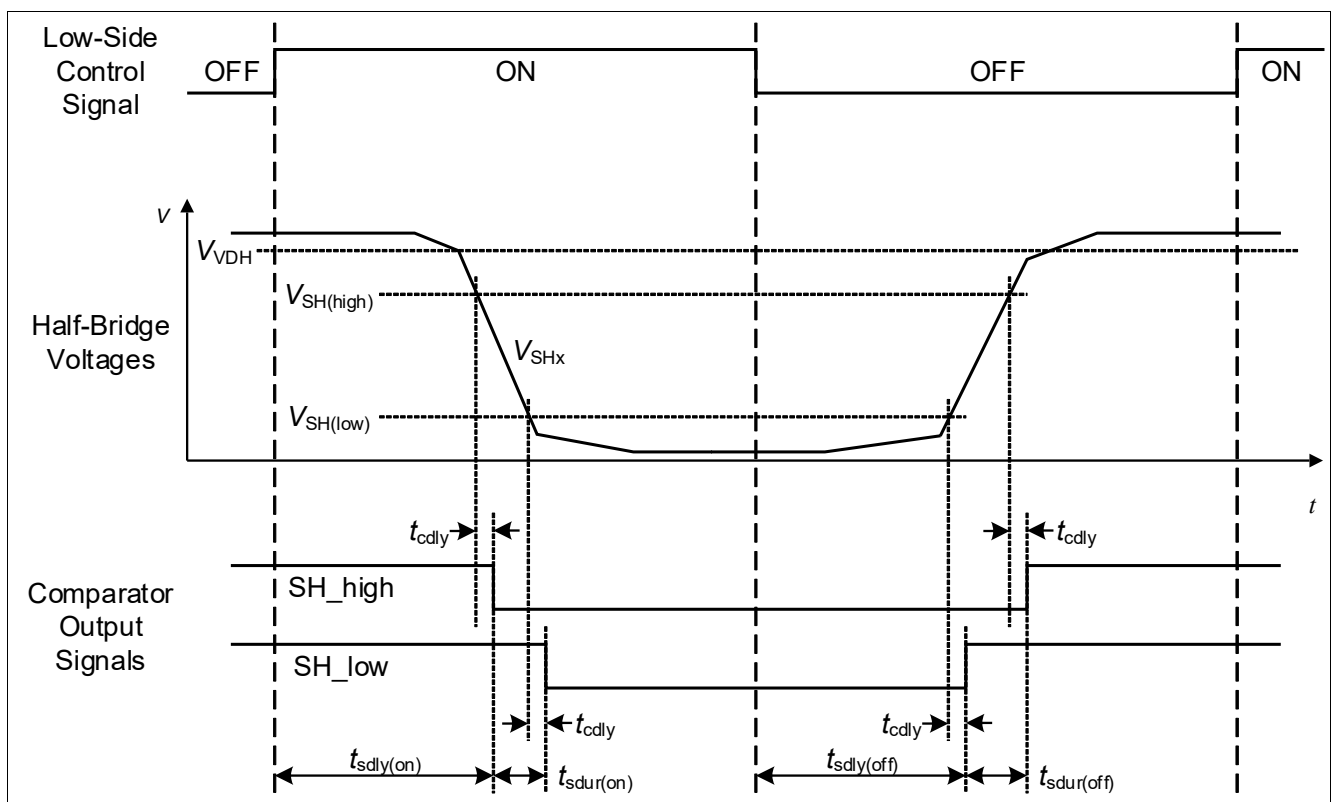


Figure 39 Comparator thresholds and timing parameters during low-side PWM

Bridge Driver (incl. Charge Pump)

Figure 40 shows the thresholds $V_{SH(high)}$ and $V_{SH(low)}$ and propagation delay t_{cdly} of the fast comparators and the measured slope timing parameters $t_{sdly(on)}$, $t_{sdur(on)}$, $t_{sdly(off)}$, and $t_{sdur(off)}$ during PWM actuation of the external high-side MOSFET.

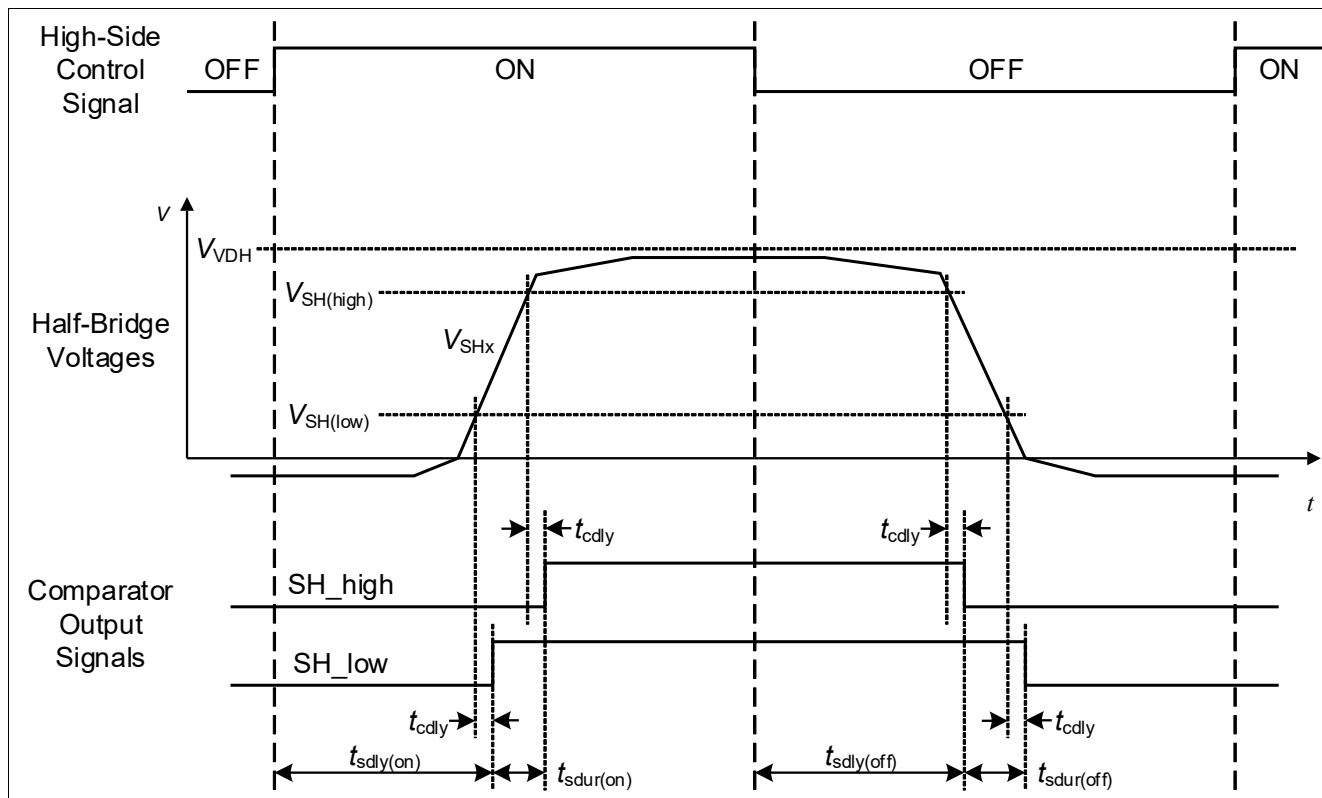


Figure 40 Comparator thresholds and timing parameters during high-side PWM

For plausibility checks of the fast comparators and the assigned timing measurement counters there is an additional channel on/off delay measurement counter which can be switched to each channel’s control signals and the corresponding drain-to-source voltage monitoring comparator outputs.

26.2.10 Adaptive Control Mode

The Bridge Driver provides an optional adaptive control mode if the output stages are controlled by the sequencer mode. The target values for on and off delays are defined by SFRs. In order to reach these target values, the adaptive control algorithm reads the results from the timing measurement and adjusts the current set point of the first gate charging sub phase $i_{1(on)}$ and the first gate discharging sub phase $i_{1(off)}$ accordingly.

26.2.11 Integrated 2-Stage Charge Pump

The Bridge Driver is supplied by an integrated 2-stage charge pump which provides a stable voltage V_{CP} above the battery voltage. This enables the Bridge Driver to operate down to low battery voltage values and to statically switch on the external MOSFETs.

The charge pump output voltage is programmable by SFRs. The charge pump frequency is continuously varied between two boundary frequencies defined by SFRs.

Bridge Driver (incl. Charge Pump)**26.2.12 Adjustable Voltage Monitoring**

The supply voltages of the Bridge Driver (VSD and VCP) are monitored by the Measurement Unit. The Bridge Driver including the charge pump can be optionally disabled at undervoltage or overvoltage of the monitored signals.

26.2.13 Adjustable Short Circuit Detection

For short circuit detection the drain-to-source comparators of the Bridge Driver are used to compare the voltage drops across the external MOSFETs to the programmable threshold voltage $V_{DSMONVTH}$. During transitions from off to on and vice versa the comparator output signals are ignored for a programmable blank time defined by SFRs.

In on state the external MOSFETs are switched off automatically if a stable short-circuit condition is detected for a SFR programmable filter time and an interrupt is generated. It can be selected by SFR if all MOSFETs are switched off or only the one where the short-circuit condition was detected.

In off state the motor phases can be pulled up or pulled down by the diagnostic currents I_{PUDiag} and I_{PDDiag} . The drain-to-source comparator output signals can be read by SFRs to check if the motor phase voltages change according to the activated diagnostic currents.

26.2.14 Open-Load Detection

For open-load detection in off state the pull-up diagnostic current I_{PUDiag} of one half bridge and the pull-down diagnostic current I_{PDDiag} of the other half bridge are activated. The pull-down diagnostic current I_{PDDiag} is able to overdrive the pull-up diagnostic current I_{PUDiag} (by I_{PDDiag_OD}). Therefore, in the case of a connected motor, both motor phase voltages are pulled-down. In the case of a disconnected motor, one motor phase voltage is pulled down while the other is pulled up according to the diagnostic current settings. The reaction of the motor phase voltages can be checked by the drain-to-source comparators of the Bridge Driver and their corresponding SFR status bits.

26.2.15 Overtemperature

The temperature of the Bridge Driver Charge Pump is monitored by a dedicated temperature sensor of the Measurement Unit for temperature warning signalling and overtemperature shutdown of the Bridge Driver.

Application Information

27 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

27.1 Window-Lift Application Diagram

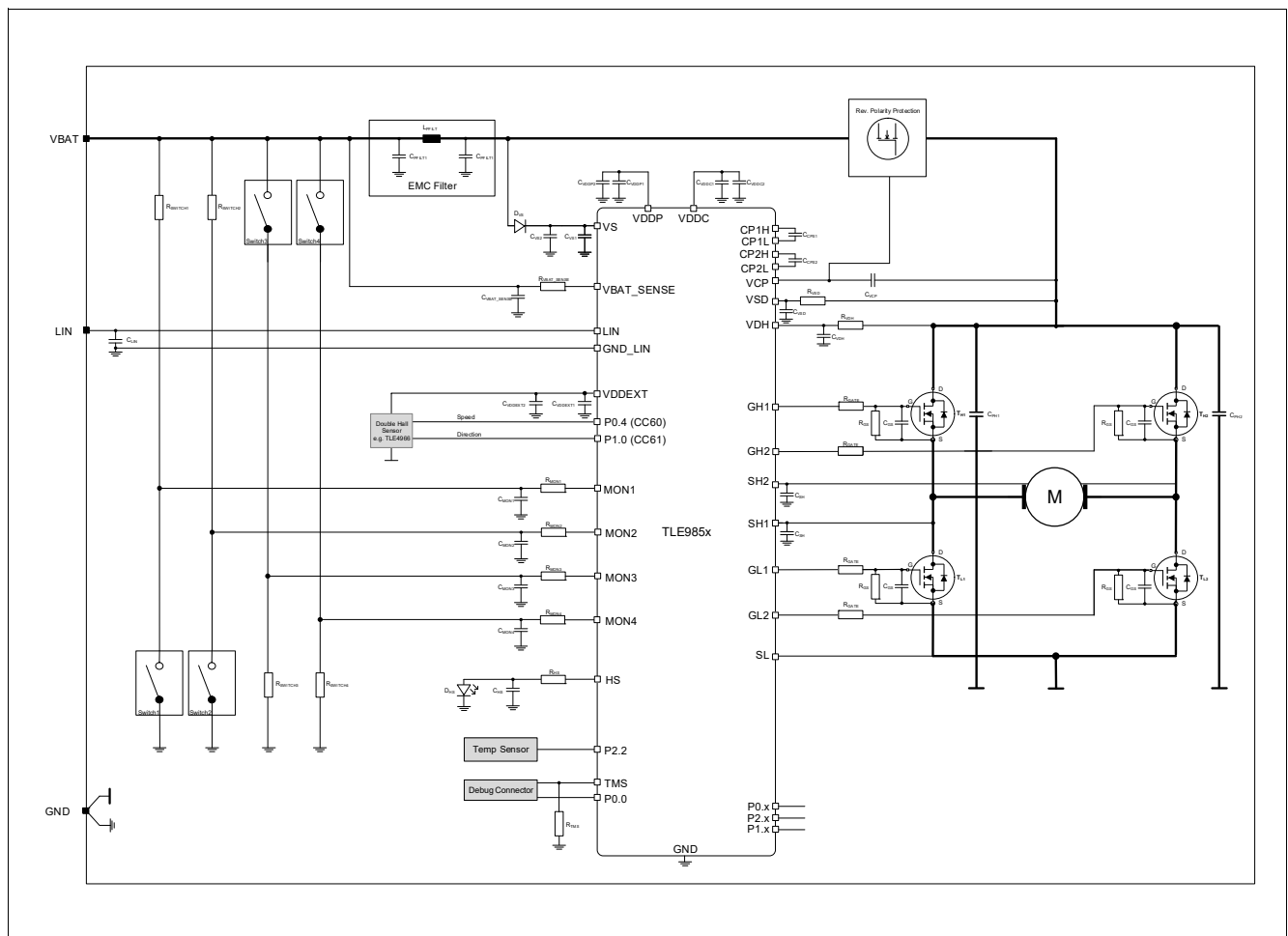


Figure 41 Simplified Application Diagram Example

Note: This is a very simplified example of an application circuit and bill of material. The function must be verified in the actual application.

Table 13 External Component (BOM)

| Symbol | Function | Component |
|------------------|-----------------------------------|------------------------|
| C _{VS1} | Capacitor 1 at VS pin | 22 μF ¹⁾ |
| C _{VS2} | Capacitor 2 at VS pin | 100 nF ²⁾³⁾ |
| D _{VS} | Reverse-polarity protection diode | |

Application Information

Table 13 External Component (BOM) (cont'd)

| Symbol | Function | Component |
|-------------------|---|---|
| $C_{VDDEXT1}$ | Capacitor 1 at VDDEXT pin | 470 nF ³⁾ |
| $C_{VDDEXT2}$ | Capacitor 2 at VDDEXT pin | 470 nF |
| C_{VDDC1} | Capacitor 1 at VDDC pin | 100 nF ³⁾ |
| C_{VDDC2} | Capacitor 2 at VDDC pin | 330nF |
| C_{VDDP1} | Capacitor 1 at VDDP pin | 470 nF ³⁾ |
| C_{VDDP2} | Capacitor 2 at VDDP pin | 470 nF |
| R_{MONx} | Resistor at MONx pin | 1 k Ω |
| C_{MONx} | Capacitor at MONx pin | 10 nF |
| R_{VBAT_SENSE} | Resistor at VBAT_SENSE pin | 1 k Ω |
| C_{VBAT_SENSE} | Capacitor at VBAT_SENSE pin | 10 nF |
| C_{LIN} | Capacitor at LIN pin | 220 pF |
| R_{HS} | Resistor at HS pin | 160 Ω ⁴⁾ |
| C_{HS} | Capacitor at HS pin | 6.8 nF or 33 nF (dependant on ESD GUN requirements) |
| D_{HS} | LED | |
| R_{VSD} | Limitation of reverse currents due to transients (-2V, 8ms) | 2 Ω |
| C_{VSD} | Filter C for charge pump and driver | 1 μ F |
| C_{CPS1} | Charge pump flying capacitor 1 | 220 nF |
| C_{CPS2} | Charge pump flying capacitor 2 | 220 nF |
| C_{VCP} | Charge pump storage capacitor | 470 nF |
| R_{VDH} | Resistor | 1 k Ω |
| C_{VDH} | Capacitor | 1 nF |
| C_{PH1} | DC-link buffer capacitor phase 1 | 220 μ F |
| C_{PH2} | DC-link buffer capacitor phase 2 | 220 μ F |
| C_{SH} | Capacitor | 1 nF |
| R_{GATE} | Resistor | optional |
| R_{GS} | Resistor | 100 k Ω |
| C_{GS} | Capacitor | 4.7 nF (depends on MOSFET C_{GS}) |
| L_{PFILT} | PI filter inductor | |
| C_{PFILT} | PI filter capacitor | 10 μ F |
| $R_{SWITCHx}$ | Resistor | |
| R_{TMS} | Resistor | |

1) to be dimensioned according to application requirements

2) to reduce the effect of fast voltage transients of V_s , these capacitors should be placed close to the device pin

3) ceramic capacitor

4) calculated for 24V (jump start)

Application Information

27.2 Connection of unused pins

Table 14 shows recommendations how to connect pins, in case they are not needed by the application.

Table 14 Recommendation for connecting unused pins

| type | pin number | recommendation 1 (if unused) | recommendation 2 (if unused) |
|-------------|--|---------------------------------|---|
| LIN | 48 | open | |
| HS | 2 | VS | open |
| MON | 17, 18, 19, 20 | GND | open + configure internal PU/PD |
| GPIO | 22, 24, 26, 27, 28, 29, 31, 32, 33, 34, 37, 38, 39, 40, 41 | GND | external PU/PD or open + configure internal PU/PD |
| TMS | 23 | GND | |
| RESET | 25 | open | |
| P2/XTAL out | 40 | open | |
| P2/XTAL in | 41 | GND | |
| VDDEXT | 45 | open | |
| VBAT_SENSE | 47 | VS | |
| N.U. | 35, 36 | GND | |

27.3 Connection of P0.2 for SWD debug mode

To enter the SWD debug mode, P0.2 needs to be 0 at the rising edge of the reset signal.

P0.2 has an internal pulldown, so it just needs to be ensured that there is no external 1 at P0.2 when the debug mode is entered.

27.4 Connection of TMS

For the debug mode, the TMS pin needs to be 1 at the rising edge of the reset signal. This is controlled by the debugger. The TMS pin has an internal PD.

To avoid the device entering the debug mode unintendedly in the final application, adding an external pull-down additionally is recommended.

27.5 ESD Tests

*Note: Tests for ESD robustness according to IEC61000-4-2 “gun test” (150pF, 330Ω) were performed. The results and test condition will be available in a test report. The target values for the test are listed in **Table 15** below.*

Application Information
Table 15 ESD “Gun Test”

| Performed Test | Result | Unit | Remarks |
|---|--------|------|--------------------------------|
| ESD at pin LIN, versus GND | >6 | kV | ¹⁾ positive pulse |
| ESD at pin LIN, versus GND | < -6 | kV | ¹⁾ negative pulse |
| ESD at pin VS, VBAT_SENSE, MONx, HS, versus GND | >6 | kV | ¹⁾²⁾ positive pulse |
| ESD at pin VS, VBAT_SENSE, MONx, HS, versus GND | < -6 | kV | ¹⁾²⁾ negative pulse |

- 1) ESD susceptibility “ESD GUN”, tested by external test house (IBEE Zwickau, EMC Test report Nr. 07-01-19), according to “LIN Conformance Test Specification Package for LIN 2.1, October 10th, 2008” and “Hardware Requirements for LIN, CAN and FlexRay Interfaces in Automotive Application - AUDI, BMW, Daimler, Porsche, Volkswagen - Revision 1.3 / 2012”
- 2) With external circuit as shown in [Figure 41](#).

Electrical Characteristics

28 Electrical Characteristics

This chapter includes all relevant Electrical Characteristics of the product TLE9852QX.

28.1 General Characteristics

28.1.1 Absolute Maximum Ratings

Table 16 Voltages Supply Pins

$T_j = -40^\circ\text{C}$ to $+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|----------------|----------------------------|--------|------|-------------|------|---|----------|
| | | Min. | Typ. | Max. | | | |
| VS voltage | $V_{S,max}$ | -0.3 | - | 40 | V | ¹⁾ Load dump | P_1.1.1 |
| VSD voltage | $V_{SD,max}$ | -0.3 | - | 48 | V | ¹⁾ | P_1.1.34 |
| VSD voltage | V_{SD,max_ext} ended | -2.8 | - | 48 | V | ^{2) 1)} Series resistor; $R_{VSD}=2.2\Omega$; $t=8\text{ms}$ | P_1.1.35 |
| VDDP voltage | $V_{DDP,max}$ | -0.3 | - | 5.5 | V | ¹⁾ | P_1.1.2 |
| VDDEXT voltage | $V_{DDEXT,max}$ | -0.3 | - | $V_S + 0.3$ | V | ¹⁾ | P_1.1.3 |
| VDDC voltage | $V_{DDC,max}$ | -0.3 | - | 1.6 | V | ¹⁾ | P_1.1.4 |

1) Not subject to production test, specified by design

2) Conditions and min. value is derived from application condition for reverse-polarity event.

Table 17 Voltages High Voltage Pins

$T_j = -40^\circ\text{C}$ to $+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|-----------------------------|----------------------|--------|------|-------------|------|------------------------|----------|
| | | Min. | Typ. | Max. | | | |
| Voltage at VBAT_SENSE pin | $V_{BAT_SENSE,max}$ | -28 | - | 40 | V | ^{1) 2)} | P_1.1.5 |
| Voltage at HS pin | $V_{HS,max}$ | -0.3 | - | $V_S + 0.3$ | V | ²⁾ | P_1.1.6 |
| Voltage at LIN pin | $V_{LIN,max}$ | -28 | - | 40 | V | ²⁾ | P_1.1.7 |
| Voltage at MONx pins | $V_{MON,max}$ | -28 | - | 40 | V | ^{1) 2)} | P_1.1.8 |
| Voltage at VDH pin | $V_{VDH,max}$ | -2.8 | - | 48 | V | ^{3) 2)} | P_1.1.36 |
| Voltage at GHx pins | V_{GH} | -8 | - | 48 | V | ^{4) 2)} | P_1.1.37 |
| Voltage at GHx vs. SHx pins | V_{GHvsSH} | - | - | 14 | V | ²⁾ | P_1.1.38 |
| Voltage at SHx pins | V_{SH} | -8 | - | 48 | V | ²⁾ | P_1.1.39 |
| Voltage at GLx pins | V_{GL} | -8 | - | 48 | V | ^{5) 2)} | P_1.1.40 |

Electrical Characteristics

Table 17 Voltages High Voltage Pins (cont'd)

$T_j = -40^\circ\text{C}$ to $+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|--------------|--------|------|------|------|------------------------|----------|
| | | Min. | Typ. | Max. | | | |
| Voltage at GLx vs. SL pins | V_{GLvsSL} | - | - | 14 | V | 2) | P_1.1.41 |
| Voltage at SL pin | V_{SL} | -8 | - | 48 | V | 2) | P_1.1.49 |
| Voltage at charge pump pins CP1H, CP1L, CP2H, CP2L, VCP | V_{CPx} | -0.3 | - | 48 | V | 6) 2) | P_1.1.42 |

- 1) For -28V, external 1 k Ω resistor is required to limit output current.
- 2) Not subject to production test, specified by design
- 3) For -2.8V, external 1 k Ω resistor is required to limit output current.
- 4) To achieve max. ratings on this pin, Parameter P_1.1.38 has to be taken into account resulting in the following dependency: $V_{GH} < V_{SH} + V_{GHvsSH_max}$ and additionally $V_{SH} < V_{GH} + 0.3\text{ V}$
- 5) To achieve max. ratings on this pin, Parameter P_1.1.41 has to be taken into account resulting in the following dependency: $V_{GL} < V_{SL} + V_{GLvsSL_max}$ and additionally $V_{SL} < V_{GL} + 0.3\text{ V}$
- 6) These limits can be kept if max current drawn out of pin does not exceed limit of 200 μA

Table 18 Voltages GPIOs

$T_j = -40^\circ\text{C}$ to $+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|--------------|--------|------|-----------------|------|---|----------|
| | | Min. | Typ. | Max. | | | |
| Voltage on port pin P0.x, P1.x, P2.x, TMS and RESET | $V_{IO,max}$ | -0.3 | - | $V_{DDP} + 0.3$ | V | 1) in consideration of $V_{IO,max} < V_{DDP@MAX}$ | P_1.1.10 |

- 1) Not subject to production test, specified by design

Table 19 Currents

$T_j = -40^\circ\text{C}$ to $+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|--|-----------|--------|------|------|------|--|----------|
| | | Min. | Typ. | Max. | | | |
| Injection current in Sleep Mode on P0.x, P1.x, P2.x, TMS and RESET | I_{xx} | - | - | 5 | mA | 1) maximum allowed injection current on single pin or sum of pins in Sleep Mode and unpowered device | P_1.1.11 |
| Injection current on HS | I_{HS} | - | - | 150 | mA | 1) current flowing into HS pin (back supply in case of short to battery) | P_1.1.12 |
| Max. current at VCP pin | I_{VCP} | -15 | - | - | mA | 1) | P_1.1.44 |

- 1) Not subject to production test, specified by design

Electrical Characteristics

Table 20 Temperatures

$T_j = -40^\circ\text{C}$ to $+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|----------------------|------------------|--------|------|------|------------------|------------------------|----------|
| | | Min. | Typ. | Max. | | | |
| Junction Temperature | T_j | -40 | - | 150 | $^\circ\text{C}$ | 1) | P_1.1.14 |
| Storage Temperature | T_{stg} | -55 | - | 150 | $^\circ\text{C}$ | 1) | P_1.1.15 |

1) Not subject to production test, specified by design

Table 21 ESD Susceptibility

$T_j = -40^\circ\text{C}$ to $+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|--|---|--------|------|------|------|---|----------|
| | | Min. | Typ. | Max. | | | |
| ESD Susceptibility HBM all pins | V_{ESD1} | -2 | - | 2 | kV | 1) 2) JEDEC HBM | P_1.1.16 |
| ESD Susceptibility HBM pins LIN vs. LINGND | V_{ESD3} | -6 | - | 6 | kV | 1) 2) JEDEC HBM | P_1.1.17 |
| ESD Susceptibility CDM | $V_{\text{ESD_CDM}}$ | -500 | - | 500 | V | 2) Charged device model, acc. JEDEC JESD22-C101 | P_1.1.18 |
| ESD Susceptibility CDM corner pins: 1, 12, 13, 24, 25, 36, 37, 48 | $V_{\text{ESD_CDM_C}}_{\text{orner}}$ | -750 | - | 750 | V | 2) Charged device model, acc. JEDEC JESD22-C101 | P_1.1.48 |

1) ESD susceptibility, "JEDEC HBM" according to ANSI/ESDA/JEDEC JS001 (1.5 k Ω , 100 pF).

2) Not subject to production test, specified by design

Notes

1. Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

28.1.2 Functional Range

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

Electrical Characteristics

Table 22 Functional Range

$T_j = -40^\circ\text{C}$ to $+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|-----------------------------|--------|------|------|------------------|---|----------|
| | | Min. | Typ. | Max. | | | |
| Supply voltage in Active Mode | V_{S_AM} | 5.5 | - | 28 | V | | P_1.2.1 |
| Extended Supply voltage in Active Mode-range 1 | $V_{S_AM_exten_d_1}$ | 28 | - | 40 | V | ¹⁾ Functional with parameter deviation | P_1.2.24 |
| Extended Supply voltage in Active Mode | $V_{S_AM_exten_d_2}$ | 3.0 | - | 28 | V | ²⁾ Functional with parameter deviation | P_1.2.2 |
| Supply voltage in Active Mode for MOSFET Driver Supply | V_{SD_AM} | 5.4 | - | 29 | V | | P_1.2.12 |
| Extended maximum supply voltage in Active Mode for MOSFET Driver Supply | $V_{SD_AM_max_extended}$ | 29 | - | 32 | V | ¹⁾ Functional with parameter deviation | P_1.2.13 |
| Supply voltage for LIN Transceiver | $V_{S_AM_LIN}$ | 5.5 | - | 18 | V | Parameter Specification | P_1.2.3 |
| Extended Supply voltage for LIN Transceiver and Monitoring Inputs (MONx) for all device modes | $V_{S_AM_LIN_e_xtend}$ | 4.0 | - | 28 | V | Functional with parameter deviation | P_1.2.4 |
| Supply voltage in Stop Mode | $V_{S_Stopmin}$ | 3.0 | - | - | V | | P_1.2.5 |
| Min. Supply voltage in Sleep Mode | $V_{S_Sleepmin}$ | 3.0 | - | - | V | | P_1.2.6 |
| Supply Voltage transients slew rate | dV_S/dt | -5 | - | 5 | V/ μs | ³⁾ | P_1.2.7 |
| Output current on any GPIO | I_{OH}, I_{OL} | -5 | - | 5 | mA | ³⁾ | P_1.2.8 |
| Output sum current for all GPIO pins | $I_{GPIO,sum}$ | -50 | - | 50 | mA | ³⁾ | P_1.2.9 |
| Junction Temperature | T_j | -40 | - | 150 | $^\circ\text{C}$ | | P_1.2.11 |

1) This operation voltage range is only allowed for a short duration: $t_{max} < 400$ ms

2) Hall-Supply, ADC, SPI, UART, NVM, RAM, CPU fully functional and in spec down to $V_S = 3$ V. Actuators (High-Side Switch, MOSFET Driver) in V_S range from $3 \text{ V} < V_S < 5.5 \text{ V}$ (High-Side Switch) or $3 \text{ V} < V_S < 4.4 \text{ V}$ (MOSFET Driver) functional but some parameters can be out of spec

3) Not subject to production test, specified by design

Electrical Characteristics

28.1.3 Current Consumption

Table 23 Current Consumption

$V_S = 5.5\text{ V to }28\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|-----------------------------|--------|------|------|---------------|--|----------|
| | | Min. | Typ. | Max. | | | |
| Current Consumption in Active Mode at pin VS | I_{VS_40M} | - | - | 30 | mA | all digital modules enabled and functional, ADCs converting in sequencer mode, PLL running, no loads on GPIOs, VDDEXT off, LIN in recessive state (no communication), HSx enabled but off, Charge Pump on, MOSFET Driver enabled and on (PWM running at 25kHz with a capacitive load of $C_{Load} = 10\text{ nF}$).; $3V \leq V_S \leq 28V$; $f_{sys} = 40\text{ MHz}$ | P_1.3.18 |
| Current consumption in Active Mode at pin VSD | I_{VSD} | - | - | 50 | mA | Charge Pump on, MOSFET Driver enabled and on (PWM running at 25kHz with a capacitive load of $C_{Load} = 10\text{ nF}$). | P_1.3.8 |
| Current consumption in Active Mode at pin VSD - Brake Mode | I_{VSD_BK} | - | - | 25 | mA | Charge Pump on and in single-stage mode, MOSFET Driver enabled and 2 Low-Side Drivers on, but not switching; $I_{CHARGE} = 15 I_D$ | P_1.3.33 |
| Current consumption in Sleep Mode at pin VSD - Hold Mode | I_{VSD_SMHM} | - | - | 16 | μA | Device in Sleep mode, but Low Side Gates are charged statically to keep low side MOSFETs on. Current does not include static Gate to Source current caused by external Gate to Source resistor.; $-40^\circ\text{C} \leq T_j \leq 85^\circ\text{C}$ | P_1.3.34 |
| Current consumption in Sleep Mode at pin VSD - Hold Mode (extended Temperature Range) | $I_{VSD_SMHM}(T_{extend})$ | - | - | 19 | μA | Device in Sleep mode, but Low Side Gates are charged statically to keep low side MOSFETs on. Current does not include static Gate to Source current caused by external Gate to Source resistor.; $85^\circ\text{C} < T_j \leq 150^\circ\text{C}$ | P_1.3.35 |

Electrical Characteristics

Table 23 Current Consumption (cont'd)

$V_S = 5.5\text{ V to }28\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|------------------------------------|--------|------|------|---------------|---|----------|
| | | Min. | Typ. | Max. | | | |
| Current consumption in Stop Mode at pin VSD - Hold Mode | $I_{VSD_STPMH_M}$ | - | - | 16 | μA | Device in Stop mode, but Low Side Gates are charged statically to keep low side MOSFETs on. Current does not include static Gate to Source current caused by external Gate to Source resistor.; $-40^\circ\text{C} \leq T_j \leq 85^\circ\text{C}$ | P_1.3.37 |
| Current consumption in Stop Mode at pin VSD - Hold Mode (extended Temperature Range) | $I_{VSD_STPMH_M(T_extend)}$ | - | - | 19 | μA | Device in Stop mode, but Low Side Gates are charged statically to keep low side MOSFETs on. Current does not include static Gate to Source current caused by external Gate to Source resistor.; $85^\circ\text{C} < T_j \leq 150^\circ\text{C}$ | P_1.3.38 |
| Current consumption in Sleep Mode at pin VS | I_{Sleep} | - | - | 25 | μA | System in Sleep Mode, microcontroller not powered, Wake capable via LIN and MON; GPIOs open (no loads) or connected to GND; $-40^\circ\text{C} \leq T_j \leq 25^\circ\text{C}$ | P_1.3.2 |
| Current consumption in Sleep Mode at pin VS (extended Temperature Range) | $I_{\text{Sleep}(T_extended)}$ | - | - | 35 | μA | ¹⁾ System in Sleep Mode, microcontroller not powered, Wake capable via LIN and MON; GPIOs open (no loads) or connected to GND; $25^\circ\text{C} < T_j \leq 85^\circ\text{C}$; $3\text{V} \leq V_S \leq 18\text{V}$ | P_1.3.3 |
| Current consumption in Sleep Mode at pin VS (extended Voltage and Temperature Range) | $I_{\text{Sleep}(V_T_extended)}$ | - | - | 40 | μA | ¹⁾ System in Sleep Mode, microcontroller not powered, Wake capable via LIN and MON; GPIOs open (no loads) or connected to GND; $25^\circ\text{C} < T_j \leq 85^\circ\text{C}$; $3\text{V} \leq V_S \leq 28\text{V}$ | P_1.3.4 |
| Current consumption in Sleep Mode at pin VS with cyclic wake | I_{Cyclic} | - | - | 30 | μA | during sleep period; $-40^\circ\text{C} \leq T_j \leq 25^\circ\text{C}$; $3\text{V} \leq V_S \leq 28\text{V}$ | P_1.3.5 |
| Current consumption in Sleep Mode at pin VS with cyclic wake (extended Temperature Range) | $I_{\text{Cyclic}(T_extended)}$ | - | - | 40 | μA | ¹⁾ during sleep period; $25^\circ\text{C} < T_j \leq 85^\circ\text{C}$; $3\text{V} \leq V_S \leq 28\text{V}$ | P_1.3.6 |

Electrical Characteristics

Table 23 Current Consumption (cont'd)

$V_S = 5.5\text{ V to }28\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|--------|------|------|---------------|--|----------|
| | | Min. | Typ. | Max. | | | |
| Current consumption in Stop Mode at pin VS | I_{Stop} | - | - | 60 | μA | System in Stop Mode, microcontroller not clocked, Wake capable via LIN and MON; GPIOs open (no loads) or connected to GND; $-40^\circ\text{C} \leq T_j \leq 25^\circ\text{C}$; $5.5\text{V} \leq V_S \leq 18\text{V}$ | P_1.3.22 |
| Current consumption in Stop Mode at pin VS (extended Temperature Range) | $I_{\text{Stop}(T_{\text{exte}}\text{nd})}$ | - | 90 | 110 | μA | ¹⁾ System in Stop Mode, microcontroller not clocked, Wake capable via LIN and MON; GPIOs open (no loads) or connected to GND; $25^\circ\text{C} < T_j \leq 85^\circ\text{C}$ | P_1.3.19 |
| Current consumption in Stop Mode at pin VS | $I_{\text{Stop}_V_{\text{exte}}\text{nd}}$ | - | - | 4.0 | mA | System in Stop Mode, microcontroller not clocked, Wake capable via LIN and MON; GPIOs open (no loads) or connected to GND; $-40^\circ\text{C} \leq T_j \leq 85^\circ\text{C}$; $3\text{V} \leq V_S < 5.5\text{V}$ | P_1.3.21 |
| Current consumption in Stop Mode at pin VS with cyclic sense | $I_{\text{Stop}_{\text{CS}}}$ | - | 95 | 115 | μA | ¹⁾ System in Stop Mode (during stop period), microcontroller not clocked, Wake capable via LIN and MON; VDDEXT off; High Side off; GPIOs open (no loads) or connected to GND or VDDP; $-40^\circ\text{C} \leq T_j \leq 85^\circ\text{C}$; $5.5\text{V} \leq V_S \leq 18\text{V}$ | P_1.3.20 |

1) Not subject to production test, specified by design

28.1.4 Thermal Resistance

Table 24 Thermal Resistance

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---------------------|---------------------|--------|------|------|------|---------------------------------------|---------|
| | | Min. | Typ. | Max. | | | |
| Junction to Case | $R_{\text{th}(JC)}$ | - | 6 | - | K/W | ¹⁾ measured to Exposed Pad | P_1.4.1 |
| Junction to Ambient | $R_{\text{th}(JA)}$ | - | 33 | - | K/W | ²⁾ | P_1.4.2 |

1) Not subject to production test, specified by design

2) According to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board . Board: $76.2 \times 114.3 \times 1.5\text{mm}^3$ with 2 inner copper layers ($35\mu\text{m}$ thick), with thermal via array under the exposed pad contacting the first inner copper layer and 300mm^2 cooling area on the bottom layer ($70\mu\text{m}$).

Electrical Characteristics

28.1.5 Timing Characteristics

The transition times between the system modes are specified here. Generally the timings are defined from the time when the corresponding bits in register PMCON0 are set until the sequence is terminated.

Table 25 System Timing

$V_S = 5.5\text{ V to }28\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|----------------------|----------------------------|--------|------|------|---------------|---|---------|
| | | Min. | Typ. | Max. | | | |
| Wake-up over battery | t_{start} | - | - | 2.5 | ms | ¹⁾ Battery ramp-up till MCU software is running. | P_1.5.1 |
| Sleep-Exit | $t_{\text{sleep - exit}}$ | - | - | 2.5 | ms | ¹⁾ rising/falling edge of any wake-up signal (LIN, MON) till MCU software running. | P_1.5.2 |
| Sleep-Entry | $t_{\text{sleep - entry}}$ | - | - | 330 | μs | ^{2) 1)} | P_1.5.3 |

1) Not subject to production test, specified by design

2) Wake events during Sleep-Entry are stored and lead to wake-up after Sleep Mode is reached.

Electrical Characteristics

28.2 Power Management Unit (PMU)

This chapter includes all electrical characteristics of the Power Management Unit.

28.2.1 PMU Input Voltage VS

Table 26 Electrical Characteristics

$V_S = 5.5\text{ V to }28\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|--|-----------|--------|------|------|---------------|------------------------|----------|
| | | Min. | Typ. | Max. | | | |
| Required decoupling capacitance | C_{VS1} | 0.1 | - | - | μF | ESR<1 Ω | P_2.1.12 |
| Required buffer capacitance for stability (load jumps) | C_{VS2} | 10 | - | - | μF | 1) | P_2.1.13 |

1) Not subject to production test, specified by design

28.2.2 PMU I/O Supply Parameters VDDP

Table 27 Electrical Characteristics

$V_S = 5.5\text{ V to }28\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|--|------------------|--------|------|------|---------------|---|---------|
| | | Min. | Typ. | Max. | | | |
| Specified Output Current | I_{VDDP} | 0 | - | 50 | mA | 1) | P_2.1.1 |
| Required decoupling capacitance | C_{VDDP1} | 0.47 | - | - | μF | 2) 3) ESR<1 Ω | P_2.1.2 |
| Total required buffer capacitance for stability (load jumps, line steps) | C_{VDDP2} | 0.47 | - | 2.2 | μF | 3) 4) | P_2.1.3 |
| Output Voltage including line and load regulation @ Active Mode | V_{DDPOUT} | 4.9 | 5.0 | 5.1 | V | 5) $I_{load}<90\text{mA}$; $V_S\geq 5.5\text{V}$ | P_2.1.4 |
| Output Voltage including line and load regulation @ Stop Mode | $V_{DDPOUTSTOP}$ | 4.5 | 5.0 | 5.25 | V | 5) $I_{load}=I_{load_internal}+I_{load_external}$; $I_{load_external}=5\text{mA}$; $I_{load_internal}=2\text{mA}$; $V_S\geq 5.5\text{V}$ | P_2.1.5 |
| Output Drop | $V_{SVDDPout}$ | - | 50 | +400 | mV | 6) $I_{VDDP}=50\text{mA}$; $V_S=3\text{V}$ | P_2.1.6 |
| Load Regulation | $V_{VDDPLOR}$ | -50 | - | 50 | mV | $2\text{mA}\leq I_{load}\leq 90\text{mA}$; $T_j\leq 150^\circ\text{C}$; $C=C_{VDDP1}+C_{VDDP2}$ | P_2.1.7 |
| Line Regulation | $V_{VDDPLIR}$ | -50 | - | 50 | mV | $5.5\text{V}\leq V_S\leq 28\text{V}$ | P_2.1.8 |
| Overshoot detection | V_{DDPOV} | 5.14 | - | 5.4 | V | Overshoot leads to SUPPLY_NMI; $V_S\geq 5.5\text{V}$ | P_2.1.9 |

Electrical Characteristics

Table 27 Electrical Characteristics (cont'd)

$V_S = 5.5\text{ V to }28\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|--|---------------------|--------|------|------|------|--|----------|
| | | Min. | Typ. | Max. | | | |
| Under Voltage Reset | V_{DDPUV} | 2.55 | 2.7 | 2.8 | V | | P_2.1.10 |
| Voltage stable detection range ⁷⁾ | ΔV_{DDPSTB} | -220 | - | +220 | mV | ⁴⁾ | P_2.1.15 |
| Over Current Diagnostic | I_{VDDPOC} | 90 | - | 220 | mA | current including VDDC current consumption | P_2.1.11 |
| Short-Circuit Diagnostic | I_{VDDPSC} | 270 | - | 600 | mA | ⁴⁾ | P_2.1.31 |
| Pull Down Strength in Sleep Mode | $I_{VDDPPDSL P}$ | 5.1 | - | 8.9 | mA | $V_{DDP}=5\text{V}$ | P_2.1.29 |

- 1) Specified output current for port supply and additional other external loads connected to VDDP, excluding on-chip current consumption.
- 2) only min. value is tested
- 3) The total capacitance on pin VDDP is specified by C_{VDDP2} including C_{VDDP1} .
- 4) Not subject to production test, specified by design
- 5) Load current includes internal supply.
- 6) Output drop for I_{VDDP} plus internal supply
- 7) The absolute voltage value is the sum of parameters $V_{VDDP} = V_{VDDP} + \Delta V_{VDDPSTB}$

Table 28 Timing Parameters

$V_S = 5.5\text{ V to }28\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|--|---------------------------|--------|------|------|---------------|------------------------|----------|
| | | Min. | Typ. | Max. | | | |
| Overvoltage detection filter time | t_{FILT_VDDPO} V | 465 | 665 | 865 | μs | ^{1) 2)} | P_2.1.16 |
| Overcurrent diagnostic filter time | t_{FILT_VDDPO} C | 21 | 30 | 39 | μs | ^{1) 2)} | P_2.1.17 |
| Overcurrent diagnostic shutdown time | t_{FILT_VDDPO} C_SD | 615 | 920 | 1250 | μs | ^{1) 2)} | P_2.1.18 |
| Short-circuit diagnostic filter time | t_{FILT_VDDPS} C | 5 | 10 | 13 | μs | ^{1) 2)} | P_2.1.34 |
| Short-circuit diagnostic shutdown time | t_{FILT_VDDPS} C_SD | 50 | 75 | 105 | μs | ^{1) 2)} | P_2.1.35 |

- 1) This filter time and its variation is derived from the time base $t_{LP_CK} = 1 / f_{LP_CLK}$
- 2) Not subject to production test, specified by design

Electrical Characteristics

28.2.3 PMU Core Supply Parameters VDDC

Table 29 Electrical Characteristics

$V_S = 5.5\text{ V to }28\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|--|-----------------------|--------|------|------|---------------|---|----------|
| | | Min. | Typ. | Max. | | | |
| Required decoupling capacitance | C_{VDDC1} | 0.1 | - | 1 | μF | ¹⁾ ESR<1 Ω | P_2.2.1 |
| Required buffer capacitance for stability (load jumps) | C_{VDDC2} | 0.33 | - | 1 | μF | ²⁾ | P_2.2.2 |
| Output Voltage including line regulation @ Active Mode | V_{DDCOUT} | 1.44 | 1.5 | 1.56 | V | $I_{load} < 40\text{mA}$ | P_2.2.3 |
| Output Voltage including line regulation @ Stop Mode | $V_{DDCOUT_st\ op1}$ | 1.44 | 1.5 | 1.56 | V | with setting of VDDC output voltage to 1.5V in Stop Mode; $I_{load_internal} < 2\text{mA}$ | P_2.2.26 |
| Output Voltage including line regulation @ Stop Mode - Reduced Core Supply Voltage | $V_{DDCOUT_st\ op2}$ | 0.8 | - | 1.3 | V | with setting of VDDC output voltage to 0.9V in Stop Mode; $I_{load_internal} < 2\text{mA}$ | P_2.2.25 |
| Load Regulation | V_{DDCLOR} | -50 | - | 50 | mV | $2\text{mA} \leq I_{load} \leq 40\text{mA}$; $C = C_{VDDC1} + C_{VDDC2}$ | P_2.2.4 |
| Line Regulation | V_{DDCLIR} | -25 | - | 25 | mV | $5.5\text{V} \leq V_S \leq 28\text{V}$ | P_2.2.5 |
| Over Voltage Detection | V_{DDCOV} | 1.58 | - | - | V | Overvoltage leads to SUPPLY_NMI | P_2.2.6 |
| Under Voltage Reset | V_{DDVUV} | 1.10 | - | 1.19 | V | | P_2.2.7 |
| Over Current Diagnostic | I_{VDDCOC} | 40 | - | 80 | mA | | P_2.2.8 |
| Short-Circuit Diagnostic | I_{VDDCSC} | 120 | - | 240 | mA | ²⁾ | P_2.2.28 |
| Pulldown Strength in Sleep Mode | $I_{VDDCPDPLP}$ | 0.75 | 1.5 | 2.7 | mA | $V_{DDC} = 1.5\text{V}$ | P_2.2.27 |

1) only min. value is tested

2) Not subject to production test, specified by design

Electrical Characteristics

Table 30 Timing Parameters

$V_S = 5.5\text{ V to }28\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|--|----------------------------------|--------|------|------|---------------|------------------------|----------|
| | | Min. | Typ. | Max. | | | |
| Overvoltage detection filter time | $t_{\text{FILT_VDDCO}}$ V | 465 | 665 | 865 | μs | 1) 2) | P_2.2.11 |
| Overcurrent diagnostic filter time | $t_{\text{FILT_VDDCO}}$ C | 21 | 30 | 39 | μs | 1) 2) | P_2.2.12 |
| Overcurrent diagnostic shutdown time | $t_{\text{FILT_VDDCO}}$ C_SD | 615 | 920 | 1250 | μs | 1) 2) | P_2.2.13 |
| Short-circuit diagnostic filter time | $t_{\text{FILT_VDDCS}}$ C | 5 | 10 | 13 | μs | 1) 2) | P_2.2.29 |
| Short-circuit diagnostic shutdown time | $t_{\text{FILT_VDDCS}}$ C_SD | 50 | 75 | 105 | μs | 1) 2) | P_2.2.30 |

1) This filter time and its variation is derived from the time base $t_{\text{LP_CLK}} = 1 / f_{\text{LP_CLK}}$.

2) Not subject to production test, specified by design

Electrical Characteristics

28.2.4 VDDEXT Voltage Regulator 5.0V

Table 31 VDDEXT Regulator Active Mode

$V_S = 5.5\text{ V to }28\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|--|----------------------------|--------|------|------|----------|---|----------|
| | | Min. | Typ. | Max. | | | |
| Specified Output Current | I_{VDDEXT} | 0 | - | 40 | mA | | P_2.3.1 |
| Required decoupling capacitance | $C_{VDDEXT1}$ | 330 | - | 1000 | nF | ESR<1Ω | P_2.3.2 |
| Required buffer capacitance for stability (load jumps) | $C_{VDDEXT2}$ | 100 | - | 1000 | nF | ¹⁾ | P_2.3.3 |
| Output voltage including line and load regulation - Load 1 | V_{DDEXT_LD1} | 4.9 | 5.0 | 5.1 | V | $I_{load} \leq 20\text{mA}$; $V_S \geq 5.5\text{V}$ | P_2.3.4 |
| Output voltage including line and load regulation - Load 2 | V_{DDEXT_LD2} | 4.9 | 5.0 | 5.1 | V | $I_{load} \leq 40\text{mA}$; $-40^\circ\text{C} \leq T_j \leq 150^\circ\text{C}$; $V_S \geq 5.5\text{V}$ | P_2.3.45 |
| Output Drop - Load 1 | V_{S-} $VDDEXT_L1$ | - | 50 | +300 | mV | ²⁾ $0\text{mA} \leq I_{load} \leq 20\text{mA}$; $3\text{V} \leq V_S \leq 5\text{V}$; $C = C_{VDDEXT1} + C_{VDDEXT2}$ | P_2.3.5 |
| Output Drop - Load 2 | V_{S-} $VDDEXT_L2$ | - | - | +600 | mV | $20\text{mA} < I_{load} \leq 40\text{mA}$; $3\text{V} \leq V_S \leq 5\text{V}$; $C = C_{VDDEXT1} + C_{VDDEXT2}$ | P_2.3.17 |
| Load Regulation | $V_{DDEXTLOR}$ | -100 | - | 10 | mV | ²⁾ $0\text{mA} \leq I_{load} \leq 40\text{mA}$; $V_S \geq 5.5\text{V}$; $C = C_{VDDEXT1} + C_{VDDEXT2}$ | P_2.3.6 |
| Line Regulation - Load 1 | $V_{DDEXTLIR}$ | -50 | - | 50 | mV | ²⁾ $0\text{mA} \leq I_{load} \leq 20\text{mA}$; $5.5\text{V} \leq V_S \leq 28\text{V}$ | P_2.3.7 |
| Line Regulation - Load 2 | $V_{DDEXTLIR}$ | -60 | - | 60 | mV | $20\text{mA} < I_{load} \leq 40\text{mA}$; $5.5\text{V} \leq V_S \leq 28\text{V}$ | P_2.3.50 |
| Power Supply Rejection Ratio | $PSRR_{VDDEX}$ $T1$ | 50 | - | - | dB | ¹⁾ $0\text{mA} \leq I_{load} \leq 20\text{mA}$; $V_r = 2\text{Vpp}$; $V_S = 13.5\text{V}$; $0\text{kHz} < f \leq 1\text{kHz}$ | P_2.3.8 |
| Under Voltage Shutdown | $V_{VDDEXTUV}$ | 1.55 | 1.9 | 2.1 | V | ³⁾ | P_2.3.9 |
| Over Current Limitation | $I_{VDDEXTOC}$ | 100 | 250 | 380 | mA | ¹⁾ | P_2.3.10 |
| VDDEXT output discharge resistance | R_{VDDEXT_DI} $SCHG$ | 16 | 20 | 24 | kOh m | | P_2.3.11 |

1) Not subject to production test, specified by design

2) Tested with 10 μA .

3) When condition is met, the bit $VDDEXT_CTRL.VDDEXT_UV_IS$ will be set.

Electrical Characteristics

Table 32 Thermal Shutdown (Junction Temperature)

$V_S = 5.5\text{ V to }28\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|------------------------|------------|--------|------|------|------------------|------------------------|----------|
| | | Min. | Typ. | Max. | | | |
| Thermal shutdown temp. | T_{jSD} | 180 | 200 | 215 | $^\circ\text{C}$ | 1) | P_2.3.48 |
| Thermal shutdown hyst. | ΔT | 5 | 10 | 15 | K | 1) | P_2.3.49 |

1) Not subject to production test, specified by design

Table 33 VDDEXT Regulator Low Current Mode

$V_S = 5.5\text{ V to }28\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|------------------------------|--------|------|------|------|---|----------|
| | | Min. | Typ. | Max. | | | |
| Specified Output Current | I_{VDDEXT_LCM} | 0 | - | 5 | mA | | P_2.3.28 |
| Output Voltage including line and load regulation | V_{DDEXT_LCM} | 4.6 | 5.0 | 5.1 | V | $I_{load} \leq 5\text{ mA}; V_S \geq 5.5\text{ V}$ | P_2.3.29 |
| Output Drop | V_{S-} V_{DDEXT_LCM} | - | 50 | +300 | mV | $I_{load} \leq 5\text{ mA}; 3\text{ V} \leq V_S \leq 5\text{ V};$ $C = C_{VDDEXT1} + C_{VDDEXT2}$ | P_2.3.30 |
| Load Regulation | $V_{DDEXTLOR_}$ LCM | -250 | - | 250 | mV | 1) $0\text{ mA} \leq I_{load} \leq 5\text{ mA}; V_S \geq 5.5\text{ V};$ $C = C_{VDDEXT1} + C_{VDDEXT2}$ | P_2.3.31 |
| Line Regulation | $V_{DDEXTLIR_}$ LCM | -300 | - | 300 | mV | 1) $0\text{ mA} \leq I_{load} \leq 5\text{ mA}; 5.5\text{ V} \leq V_S \leq 28\text{ V}$ | P_2.3.32 |
| Power Supply Rejection Ratio | $PSRR_{VDDEXT}$ T_LCM1 | 50 | - | - | dB | 2) $0\text{ mA} \leq I_{load} \leq 5\text{ mA}; V_r = 2\text{ Vpp};$ $V_S = 13.5\text{ V}; 0\text{ kHz} < f \leq 1\text{ kHz}$ | P_2.3.33 |

1) Tested with 10 μA .

2) Not subject to production test, specified by design

Electrical Characteristics

28.2.5 VPRE Voltage Regulator (PMU Subblock) Parameters

Table 34 Functional Range

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|--------------------------|------------|--------|------|------|------|------------------------|---------|
| | | Min. | Typ. | Max. | | | |
| Specified Output Current | I_{VPRE} | 0 | - | 90 | mA | ¹⁾ | P_2.4.1 |

1) Not subject to production test, specified by design

28.2.5.1 Load Sharing Scenario of VPRE Regulator

The figure below shows the possible load sharing scenario of VPRE regulator.

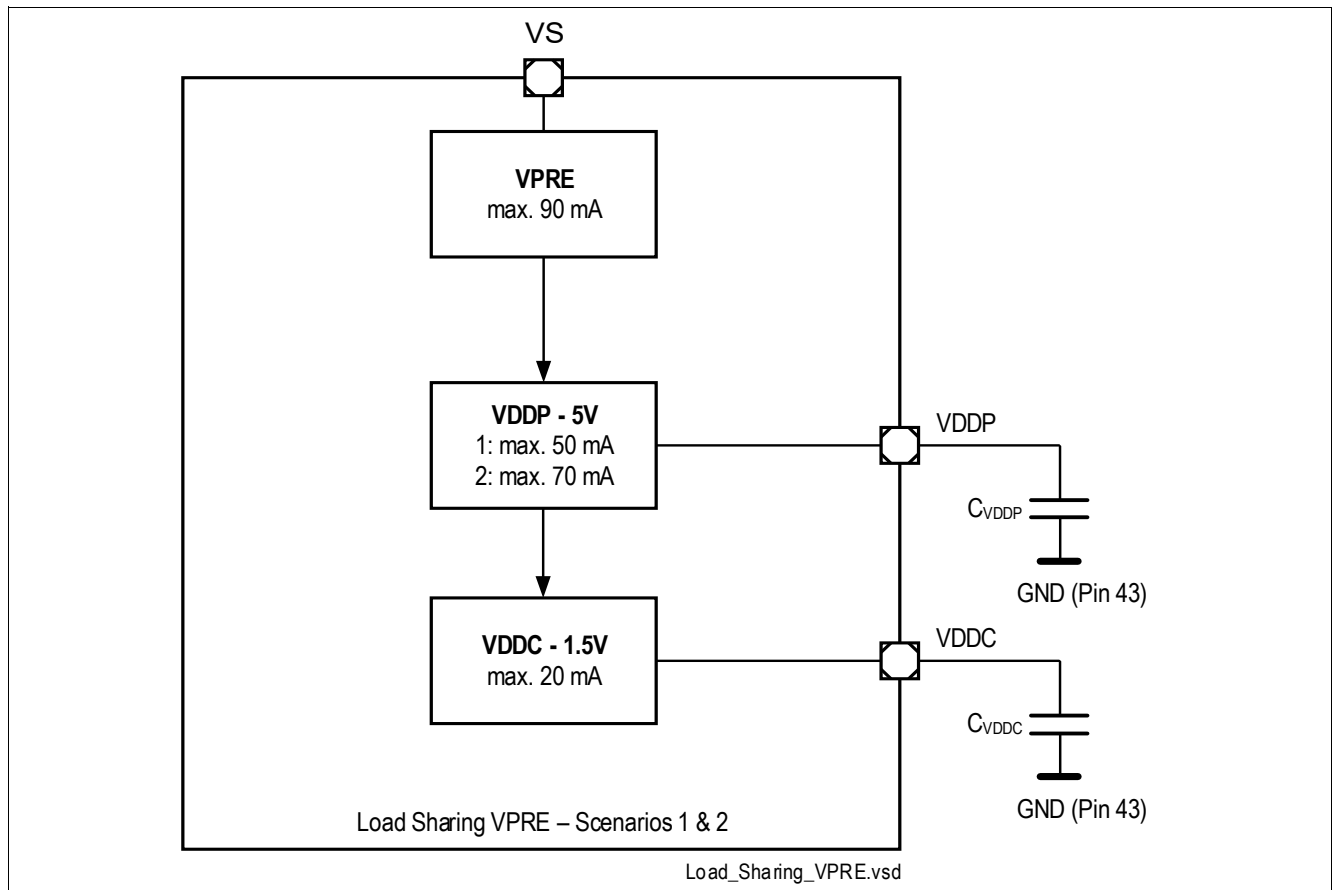


Figure 42 Load Sharing Scenario of VPRE and VDDP Regulator

Electrical Characteristics

28.2.6 Power Down Voltage Regulator (PMU Subblock) Parameters

The PMU Power Down voltage regulator consists of two subblocks:

- Power Down Pre regulator: VDD5VPD
- Power Down Core regulator: VDD1V5_PD (Supply used for GPUDATAx registers)

Both regulators are used as purely internal supplies. The following table contains all relevant parameter:

Table 35 Functional Range

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|--------------------------|------------------------|--------|------|------|------|--|---------|
| | | Min. | Typ. | Max. | | | |
| Power-On Reset Threshold | $V_{DD1V5_PD_RSTTH}$ | 1.2 | - | 1.5 | V | ¹⁾ I_{load} =internal load connected to VDD1V5_PD | P_2.5.1 |

1) Not subject to production test, specified by design

Electrical Characteristics

28.3 System Clocks

28.3.1 Electrical Characteristics Oscillators and PLL

Table 36 PMU Oscillators (Power Management Unit)

$V_S = 5.5\text{ V to }28\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|----------------------|----------------|--------|------|------|------|---|---------|
| | | Min. | Typ. | Max. | | | |
| Frequency of LP_CLK | f_{LP_CLK} | 17 | 20 | 23 | MHz | this clock is used at startup and can be used in case the PLL fails | P_3.1.1 |
| Frequency of LP_CLK2 | f_{LP_CLK2} | 70 | 100 | 130 | kHz | this clock is used for cyclic wake | P_3.1.2 |

Table 37 CGU Oscillator (Clock Generation Unit Microcontroller)

$V_S = 5.5\text{ V to }28\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|--------------------------------|----------------|---------|------|---------|---------------|---|---------|
| | | Min. | Typ. | Max. | | | |
| Short term frequency deviation | f_{TRIMST} | -0.4 % | - | +0.4 % | MHz | within any 100 ms, e.g. after synchronization to a LIN frame | P_3.1.3 |
| Absolute accuracy | $f_{TRIMABSA}$ | -1.49 % | - | +1.49 % | MHz | Including temperature and lifetime drift and supply variation; $T_j \leq 150^\circ\text{C}$ | P_3.1.4 |
| CGU-OSC Start-up time | t_{OSC} | - | - | 10 | μs | ¹⁾ startup time OSC from Sleep Mode, power supply stable | P_3.1.5 |

1) Not subject to production test, specified by design

Table 38 PLL (Clock Generation Unit Microcontroller)

$V_S = 5.5\text{ V to }28\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|-------------------------------|---------------|--------|------|------|------|---|----------|
| | | Min. | Typ. | Max. | | | |
| VCO reference frequency range | f_{REF} | 0.8 | 1 | 1.27 | MHz | ^{1) 2)} | P_3.1.25 |
| VCO frequency (tuning) range | f_{VCO} | 48 | - | 160 | MHz | ²⁾ | P_3.1.21 |
| Input frequency range | f_{OSC} | 4 | - | 40 | MHz | ^{3) 4) 2)} External input clock mode | P_3.1.6 |
| XTAL1 input freq. range | f_{OSCHP} | 4 | - | 16 | MHz | ^{3) 2)} External crystal mode | P_3.1.23 |
| Output freq. range | f_{PLL} | 5 | - | 40 | MHz | ^{3) 2)} | P_3.1.7 |
| Free-running frequency | $f_{VCOfree}$ | - | 21.5 | 38 | MHz | ²⁾ | P_3.1.24 |

Electrical Characteristics

Table 38 PLL (Clock Generation Unit Microcontroller) (cont'd)

$V_S = 5.5\text{ V to }28\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|-----------------------|--------|------|------|---------------|--|----------|
| | | Min. | Typ. | Max. | | | |
| Input clock high/low time | $t_{\text{high/low}}$ | 10 | - | - | ns | 2) | P_3.1.8 |
| Accumulated jitter with external oscillator | $j_{\text{acc_ext}}$ | - | - | 8 | ns | 2) for K2=2; this parameter value is only valid with the combination of an external quartz oscillator (e.g. 5 MHz) | P_3.1.10 |
| Lock-in time | t_L | - | - | 260 | μs | 2) this parameter represents the duration from module power-on to assertion of lock signal | P_3.1.11 |

- 1) oscillator or clock inaccuracy needs to be taken into account, do not select a nominal frequency and PDIV in a combination that fREF has exactly min or max value
- 2) Not subject to production test, specified by design
- 3) specified limits for fVCO and fREF need to be fulfilled, restrictions to PDIV, NDIV, K2DIV settings apply
- 4) Above 24MHz the hysteresis of the OSC_HP module needs to be switched off (see register SCU_XTAL_CTRL).

28.3.2 External Clock Parameters XTAL1, XTAL2

Table 39 Functional Range

$V_S = 5.5\text{ V to }28\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|------------------------|-------------------------------|------|------|---------------|--|----------|
| | | Min. | Typ. | Max. | | | |
| Input voltage range limits for signal on XTAL1 | $V_{\text{IX1_SR}}$ | -1.7 + V_{DDC} | - | 1.7 | V | 1) 2) | P_3.2.1 |
| Input voltage (amplitude) on XTAL1 | $V_{\text{AX1_SR}}$ | 0.3x V_{DDC} | - | - | V | 3) 4) Peak-to-peak voltage | P_3.2.2 |
| XTAL1 input current | I_{IL} | -20 | - | 20 | μA | $0\text{V} < V_{\text{IN}} < V_{\text{DDC}}$ | P_3.2.3 |
| Oscillator frequency - External input clock mode | $f_{\text{OSC_EXT}}$ | 4 | - | 16 | MHz | 5) 6) | P_3.2.4 |
| Oscillator frequency - External crystal (or resonator) mode | $f_{\text{OSC_XTAL}}$ | 4 | - | 16 | MHz | 4) | P_3.2.5 |
| High time | t_{H} | 6 | - | - | ns | 5) 7) 4) 2) | P_3.2.6 |
| Low time | t_{L} | 6 | - | - | ns | 5) 7) 4) 2) | P_3.2.7 |
| Rise time | t_{R} | - | 8 | 8 | ns | 5) 7) 4) 2) | P_3.2.8 |
| Fall time | t_{F} | - | 8 | 8 | ns | 5) 7) 4) 2) | P_3.2.9 |
| High time | $t_{\text{H_PLLNM}}$ | 12 | - | - | ns | 5) 8) 4) 2) | P_3.2.10 |

Electrical Characteristics

Table 39 Functional Range (cont'd)

$V_S = 5.5\text{ V to }28\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|-----------|----------------|--------|------|------|------|------------------------|----------|
| | | Min. | Typ. | Max. | | | |
| Low time | t_{L_PLLNM} | 12 | - | - | ns | 5) 8) 4) 2) | P_3.2.11 |
| Rise time | t_{R_PLLNM} | - | 7 | 7 | ns | 5) 8) 4) 2) | P_3.2.12 |
| Fall time | t_{F_PLLNM} | - | 7 | 7 | ns | 5) 8) 4) 2) | P_3.2.13 |

- 1) Overload conditions must not occur on pin XTAL1. This Parameter is not valid for stop mode.
- 2) Not subject to production test, specified by design
- 3) The amplitude voltage V_{AX1} refers to the offset voltage V_{OFF} . This offset voltage must be stable during the operation and the resulting voltage peaks must remain within the limits defined by V_{IX1} .
- 4) Default hysteresis settings ($SCU_XTAL_CTRL.XTALHYSEN = I_B$, $SCU_XTAL_CTRL.XTALHYSCTRL = 1I_B$)
- 5) Valid for rectangular full-swing input signals.
- 6) Hysteresis disabled ($SCU_XTAL_CTRL.XTALHYSEN=0_B$)
- 7) This performance is only valid for Prescaler Mode (VCO Bypass mode).
- 8) This performance is only valid for PLL Normal Mode.

Electrical Characteristics

28.4 Flash Parameters

This chapter includes the parameters for the 48 KB embedded flash module (incl. config sector).

28.4.1 Flash Characteristics

Table 40 Flash Characteristics

$V_S = 5.5\text{ V to }28\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|-----------------------|--------|------|------|---------|---|----------|
| | | Min. | Typ. | Max. | | | |
| Read time | $t_{\text{read_ac}}$ | - | - | 75 | ns | ¹⁾ $3\text{V} < V_S < 28\text{V}$ | P_4.1.22 |
| Programming time per 128 Byte page | t_{PR} | - | 3 | 3.5 | ms | ¹⁾ $3\text{V} < V_S < 28\text{V}$ | P_4.1.1 |
| Programming time per 128 Byte page incl. Firmware routine runtime for program operation | $t_{\text{PR_FW}}$ | - | - | 4 | ms | ¹⁾ $3\text{V} < V_S < 28\text{V}$ | P_4.1.20 |
| Erase time per sector/page | t_{ER} | - | 4 | 4.5 | ms | ¹⁾ $3\text{V} < V_S < 28\text{V}$ | P_4.1.2 |
| Erase time per sector/page incl. Firmware routine runtime for erase operation | $t_{\text{ER_FW}}$ | - | - | 5 | ms | ¹⁾ $3\text{V} < V_S < 28\text{V}$ | P_4.1.21 |
| Data retention time | t_{RET} | 20 | - | - | years | ¹⁾ 1,000 erase / program cycles | P_4.1.3 |
| Data retention time | t_{RET} | 50 | - | - | years | ^{2) 1)} 1,000 erase / program cycles; $T_j = 30^\circ\text{C}$ | P_4.1.4 |
| Flash erase endurance for user sectors | N_{ER} | 30 | - | - | kcycles | ¹⁾ Data retention time 5 years | P_4.1.5 |
| Flash erase endurance for security pages | N_{SEC} | 10 | - | - | cycles | ¹⁾ Data retention time 20 years; $T_j = 25^\circ\text{C}$ | P_4.1.6 |
| Drain disturb limit | N_{DD} | 32 | - | - | kcycles | ^{3) 1)} | P_4.1.7 |

1) Not subject to production test, specified by design

2) Derived by extrapolation of lifetime tests.

3) This parameter limits the number of subsequent programming operations within a physical sector without a given page in this sector being (re-)programmed. The drain disturb limit is applicable if wordline erase is used repeatedly. For normal sector erase/program cycles this limit will not be violated. For data sectors the integrated EEPROM emulation firmware routines handle this limit automatically, for wordline erases in code sectors (without EEPROM emulation) it is recommended to execute a software based refresh, which may make use of the integrated random number generator NVMBRNG to statistically start a refresh.

Electrical Characteristics

28.5 Parallel Ports (GPIO)

28.5.1 Description of Keep and Force Current

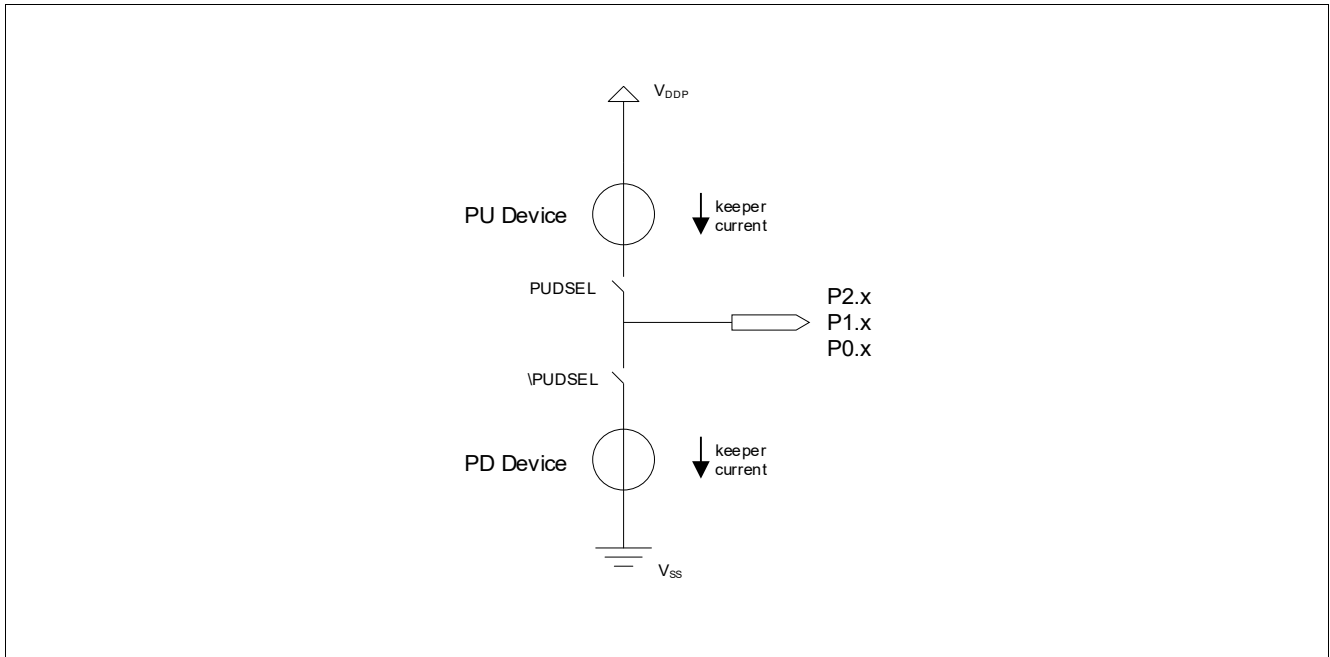


Figure 43 Pull-Up/Down Device

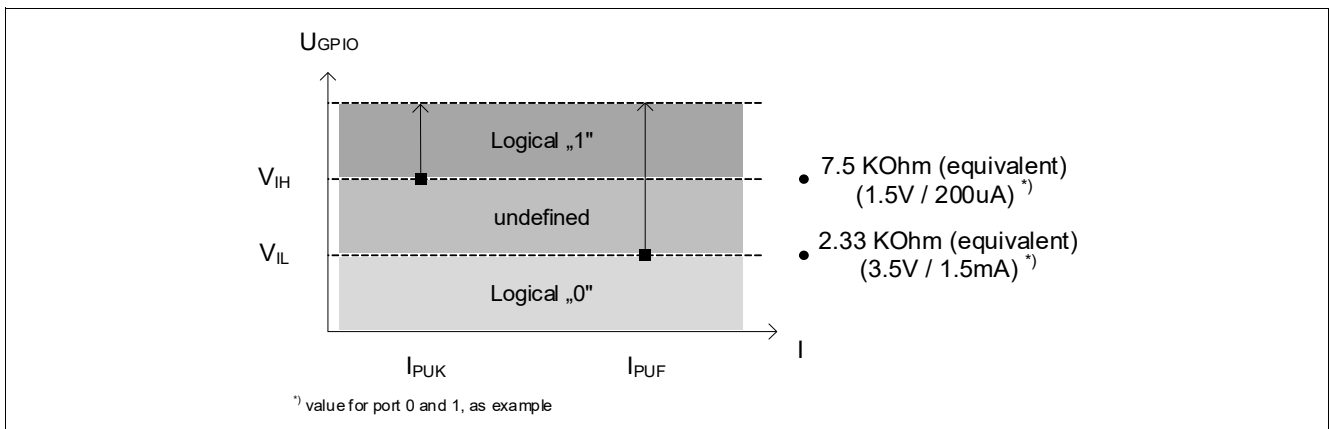


Figure 44 Pull-Up Keep and Forced Current

Electrical Characteristics

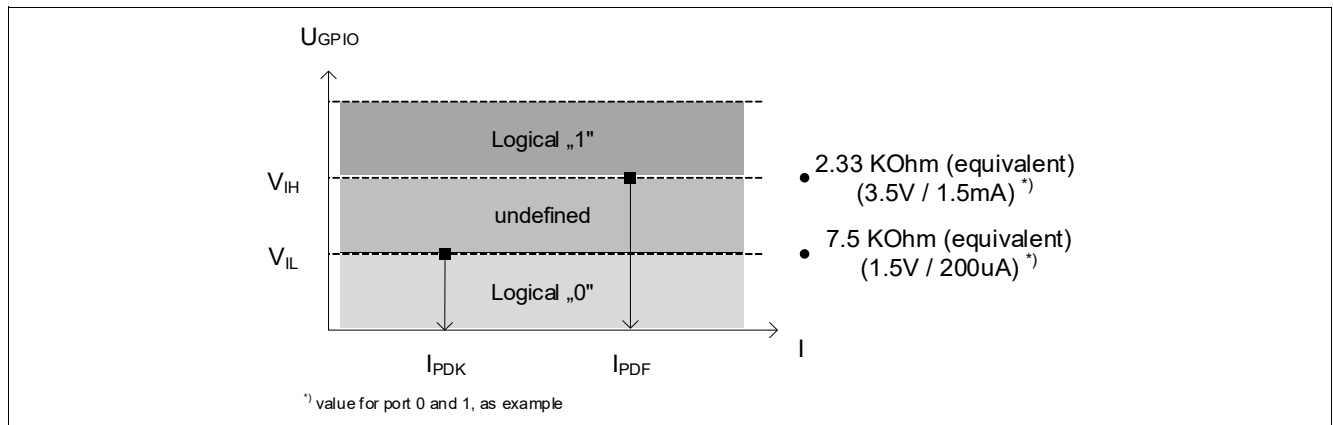


Figure 45 Pull-Down Keep and Force Current

28.5.2 DC Parameters Port 0, Port 1, TMS, Reset

Note: Operating Conditions apply.
 Keeping signal levels within the limits specified in this table ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the overload current I_{OV} .

Table 41 DC Characteristics Port0, Port1, TMS, Reset

$V_S = 5.5\text{ V to }28\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|-----------------------|----------------------|-----------------------|------|----------------------|------|--|----------|
| | | Min. | Typ. | Max. | | | |
| Input low voltage | V_{IL} | -0.3 | - | $0.3 \times V_{DDP}$ | V | $2.55\text{V} \leq V_{DDP} < 5.5\text{V}$ | P_5.2.1 |
| Input high voltage | V_{IH} | $0.7 \times V_{DDP}$ | - | $V_{DDP} + 0.3$ | V | $2.55\text{V} \leq V_{DDP} < 5.5\text{V}$ | P_5.2.2 |
| Input Hysteresis | HYS | $0.11 \times V_{DDP}$ | - | - | V | ¹⁾ $4.5\text{V} \leq V_{DDP} \leq 5.5\text{V}$; Series Resistance=0Ω | P_5.2.3 |
| Input Hysteresis | HYS_{extend} | $0.04 \times V_{DDP}$ | - | - | V | ¹⁾ $2.55\text{V} \leq V_{DDP} < 4.5\text{V}$; Series Resistance=0Ω | P_5.2.16 |
| Output low voltage | V_{OL} | - | - | 1.0 | V | ^{2) 3)} $I_{OL} \leq I_{OLmax}$; $2.55\text{V} \leq V_{DDP} < 5.5\text{V}$ | P_5.2.4 |
| Output low voltage | V_{OL} | - | - | 0.4 | V | ^{2) 3)} $I_{OL} \leq I_{OLnom}$; $2.55\text{V} \leq V_{DDP} < 5.5\text{V}$ | P_5.2.5 |
| Output high voltage | V_{OH} | $V_{DDP} - 1.0$ | - | - | V | ^{2) 3)} $I_{OH} \geq I_{OHmax}$; $2.55\text{V} \leq V_{DDP} < 5.5\text{V}$ | P_5.2.6 |
| Output high voltage | V_{OH} | $V_{DDP} - 0.4$ | - | - | V | ^{2) 3)} $I_{OH} \geq I_{OHnom}$; $2.55\text{V} \leq V_{DDP} < 5.5\text{V}$ | P_5.2.7 |
| Input leakage current | I_{OZ2} | -5 | - | +5 | μA | ⁴⁾ $T_j \leq 85^\circ\text{C}$; $0\text{V} < V_{IN} < V_{DDP}$ | P_5.2.8 |
| Input leakage current | $I_{OZ2_T_extend}$ | -15 | - | +15 | μA | ⁴⁾ $T_j \leq 150^\circ\text{C}$; $0\text{V} < V_{IN} < V_{DDP}$ | P_5.2.9 |

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Table 41 DC Characteristics Port0, Port1, TMS, Reset (cont'd)

$V_S = 5.5\text{ V to }28\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|-------------------------------|--------------------------|--------|------|------|---------------|-------------------------------------|----------|
| | | Min. | Typ. | Max. | | | |
| Pull-up level keep current | I_{PUK} | - | - | -200 | μA | ⁵⁾ $V_{PIN} \geq V_{IH}$ | P_5.2.10 |
| Pull-up level force current | I_{PUF} | -1.5 | - | - | mA | ⁵⁾ $V_{PIN} \leq V_{IL}$ | P_5.2.11 |
| Pull-down level keep current | I_{PDK} | 200 | - | - | μA | ⁵⁾ $V_{PIN} \leq V_{IL}$ | P_5.2.26 |
| Pull-down level force current | I_{PDF} | - | - | 1.5 | mA | ⁵⁾ $V_{PIN} \geq V_{IH}$ | P_5.2.27 |
| Pin capacitance | C_{IO} | - | - | 10 | pF | ¹⁾ | P_5.2.12 |
| Reset Pin Input Filter Time | $T_{\text{filt_RESET}}$ | 3 | 4.5 | 6 | μs | ⁶⁾ | P_5.2.13 |

1) Not subject to production test, specified by design

2) The values for I_{OLnom} , I_{OLmax} , I_{OHnom} , I_{OHmax} depend on the driver strength settings (see register bit fields SCU_Px_POCON0.Px_PDMy) and are defined by P_5.2.20 ... P_5.2.25

3) The maximum deliverable output current of a port driver depends on the selected output driver mode. The limit for pin groups must be respected (see P_1.2.9).

4) The given values are worst-case values. In production test, this leakage current is only tested at 150°C ; other values are ensured by correlation. For derating, please refer to the following descriptions:

Leakage derating depending on temperature ($T_j = \text{junction temperature } [^\circ\text{C}]$): $I_{OZ} = 0.05 \times e^{(1.5 + 0.028 \times T_j)}$ [μA]. For example, at a temperature of 95°C the resulting leakage current is $3.2\mu\text{A}$.

Leakage derating depending on voltage level ($DV = V_{DDP} - V_{PIN}$ [V]): $I_{OZ} = I_{OZtempmax} - (1.6 \times DV)$ [μA]
This voltage derating formula is an approximation which applies for maximum temperature.

5) Keep current: Limit the current through this pin to the indicated value so that the enabled pull device can keep the default pin level: $V_{PIN} \geq V_{IH}$ for a pull-up; $V_{PIN} \leq V_{IL}$ for a pull-down.

Force current: Drive the indicated minimum current through this pin to change the default pin level driven by the enabled pull device: $V_{PIN} \leq V_{IL}$ for a pull-up; $V_{PIN} \geq V_{IH}$ for a pull-down.

These values apply to the fixed pull-devices in dedicated pins and to the user-selectable pull-devices in general purpose IO pins.

6) This filter time and its variation is derived from the time base $t_{LP_CLK} = 1 / f_{LP_CLK}$.

Table 42 Current Limits for Port Output Drivers

$V_S = 5.5\text{ V to }28\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|-------------------------------|------------|--------|------|------|-------------|--|----------|
| | | Min. | Typ. | Max. | | | |
| Output Current, Strong Driver | I_{OLs5} | - | 1.6 | 5 | mA | ¹⁾ $V_{DDP} \geq 4.5\text{V}$ | P_5.2.20 |
| Output Current, Medium Driver | I_{OLm5} | - | 1.0 | 3 | mA | ¹⁾ $V_{DDP} \geq 4.5\text{V}$ | P_5.2.21 |
| Output Current, Weak Driver | I_{OLw5} | - | 0.25 | 0.5 | mA | ¹⁾ $V_{DDP} \geq 4.5\text{V}$ | P_5.2.22 |

Electrical Characteristics

Table 42 Current Limits for Port Output Drivers (cont'd)

$V_S = 5.5\text{ V to }28\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|-------------------------------|------------|--------|------|------|------|--|----------|
| | | Min. | Typ. | Max. | | | |
| Output Current, Strong Driver | I_{OLs3} | - | 1.0 | 3 | mA | ¹⁾ $2.55\text{V} < V_{DDP} < 4.5\text{V}$ | P_5.2.23 |
| Output Current, Medium Driver | I_{OLm3} | - | 0.8 | 1.8 | mA | ¹⁾ $2.55\text{V} < V_{DDP} < 4.5\text{V}$ | P_5.2.24 |
| Output Current, Weak Driver | I_{OLw3} | - | 0.15 | 0.3 | mA | ¹⁾ $2.55\text{V} < V_{DDP} < 4.5\text{V}$ | P_5.2.25 |

1) These values apply for P_5.2.4 ... P_5.2.7: typ. values represent the "Nominal Output Current" (I_{OLnom} , $-I_{OHnom}$), max. values represent the "Maximum Output Current" (I_{OLmax} , $-I_{OHmax}$)

28.5.3 DC Parameters Port 2

Note: Operating Conditions apply.

Keeping signal levels within the limits specified in this table ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the overload current I_{OV} .

Table 43 DC Characteristics Port 2

$V_S = 5.5\text{ V to }28\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|--|--------------------------|-----------------------|------|----------------------|---------------|--|----------|
| | | Min. | Typ. | Max. | | | |
| Input low voltage | V_{IL_P2} | -0.3 | - | $0.3 \times V_{DDP}$ | V | $2.55\text{V} \leq V_{DDP} < 5.5\text{V}$ | P_5.3.1 |
| Input high voltage | V_{IH_P2} | $0.7 \times V_{DDP}$ | - | $V_{DDP} + 0.3$ | V | $2.55\text{V} \leq V_{DDP} < 5.5\text{V}$ | P_5.3.2 |
| Input Hysteresis | HYS_{P2} | $0.11 \times V_{DDP}$ | - | - | V | ¹⁾ $4.5\text{V} \leq V_{DDP} \leq 5.5\text{V}$; Series Resistance=0 Ω | P_5.3.3 |
| Input Hysteresis | $HYS_{P2_exte_nd}$ | $0.04 \times V_{DDP}$ | - | - | V | ¹⁾ $2.55\text{V} \leq V_{DDP} < 4.5\text{V}$; Series Resistance=0 Ω | P_5.3.10 |
| Input leakage current | I_{OZ1_P2} | -400 | - | +400 | nA | ; $T_j \leq 85^\circ\text{C}$; $0\text{V} < V_{IN} < V_{DDP}$ | P_5.3.4 |
| Input leakage current (extended temperature range) | $I_{OZ1_P2_T_extend}$ | -1 | - | +1 | μA | ; $T_j \leq 150^\circ\text{C}$; $0\text{V} < V_{IN} < V_{DDP}$ | P_5.3.11 |
| Pull-up level keep current | I_{PUK_P2} | - | - | -30 | μA | ²⁾ $V_{PIN} \geq V_{IH}$ | P_5.3.5 |

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Table 43 DC Characteristics Port 2 (cont'd)

$V_S = 5.5\text{ V to }28\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|--|---------------|--------|------|------|---------------|-------------------------------------|----------|
| | | Min. | Typ. | Max. | | | |
| Pull-up level force current | I_{PUF_P2} | -750 | - | - | μA | ²⁾ $V_{PIN} \leq V_{IL}$ | P_5.3.6 |
| Pull-down level keep current | I_{PDK_P2} | 30 | - | - | μA | ²⁾ $V_{PIN} \leq V_{IL}$ | P_5.3.12 |
| Pull-down level force current | I_{PDF_P2} | - | - | 750 | μA | ²⁾ $V_{PIN} \geq V_{IH}$ | P_5.3.13 |
| Pin capacitance (digital inputs/outputs) | C_{IO_P2} | - | - | 10 | pF | ¹⁾ | P_5.3.7 |

1) Not subject to production test, specified by design

2) Keep current: Limit the current through this pin to the indicated value so that the enabled pull device can keep the default pin level: $V_{PIN} \geq V_{IH}$ for a pull-up; $V_{PIN} \leq V_{IL}$ for a pull-down.

Force current: Drive the indicated minimum current through this pin to change the default pin level driven by the enabled pull device: $V_{PIN} \leq V_{IL}$ for a pull-up; $V_{PIN} \geq V_{IH}$ for a pull-down.

Electrical Characteristics

28.6 LIN Transceiver

28.6.1 Electrical Characteristics

Table 44 Bus Receiver Interface

$V_S = 5.5\text{ V to }18\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|--|-------------------|--------------------|-------------------|--------------------|---------------|--|----------|
| | | Min. | Typ. | Max. | | | |
| Receiver threshold voltage, recessive to dominant edge | V_{th_dom} | $0.4 \times V_S$ | $0.45 \times V_S$ | $0.53 \times V_S$ | V | SAE J2602 | P_6.1.1 |
| Receiver dominant state | V_{BUSdom} | -27 | - | $0.4 \times V_S$ | V | LIN Spec 2.2 (Par. 17) | P_6.1.2 |
| Receiver threshold voltage, dominant to recessive edge | V_{th_rec} | $0.47 \times V_S$ | $0.55 \times V_S$ | $0.6 \times V_S$ | V | SAE J2602 | P_6.1.3 |
| Receiver recessive state | V_{BUSrec} | $0.6 \times V_S$ | - | $1.15 \times V_S$ | V | ¹⁾ LIN Spec 2.2 (Par. 18) | P_6.1.4 |
| Receiver center voltage | V_{BUS_CNT} | $0.475 \times V_S$ | $0.5 \times V_S$ | $0.525 \times V_S$ | V | ²⁾ LIN Spec 2.2 (Par. 19) | P_6.1.5 |
| Receiver hysteresis | V_{HYS} | $0.07 \times V_S$ | $0.12 \times V_S$ | $0.175 \times V_S$ | V | ³⁾ LIN Spec 2.2 (Par. 20) | P_6.1.6 |
| Wake-up threshold voltage | $V_{BUS,wk}$ | $0.4 \times V_S$ | $0.5 \times V_S$ | $0.6 \times V_S$ | V | | P_6.1.7 |
| Dominant analog filter time for bus wake-up | $t_{WK_ana,bus}$ | 3 | - | 15 | μs | analog filter time of transceiver | P_6.1.88 |
| Dominant time for bus wake-up | $t_{WK,bus}$ | 30 | - | 150 | μs | including analog and digital filter time. Digital filter time can be adjusted by PMU.CNF_WAKE_FILTER | P_6.1.8 |

1) Maximum limit specified by design.

2) $V_{BUS_CNT} = (V_{th_dom} + V_{th_rec})/2$

3) $V_{HYS} = V_{BUSrec} - V_{BUSdom}$

Electrical Characteristics

Table 45 Bus Transmitter Interface

$V_S = 5.5\text{ V to }18\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|------------------------------|----------------------|------------------|------|-------|---------------|--|----------|
| | | Min. | Typ. | Max. | | | |
| Bus recessive output voltage | $V_{BUS,ro}$ | $0.8 \times V_S$ | - | V_S | V | $V_{TxD} = \text{high Level}$ | P_6.1.9 |
| Bus short circuit current | $I_{BUS,sc}$ | 40 | 100 | 150 | mA | Current Limitation for driver dominant state driver on $V_{BUS}=18\text{V}$; LIN Spec 2.2 (Par. 12) | P_6.1.10 |
| Leakage current | $I_{BUS_NO_GN D}$ | -1000 | -450 | 0 | μA | LIN Spec 2.2 (Par. 15); $V_{BUS} = -12\text{V}$; $V_S = 0\text{V}$ | P_6.1.11 |
| Leakage current | $I_{BUS_NO_BA T}$ | - | 10 | 20 | μA | LIN Spec 2.2 (Par. 16); $V_{BUS} = 18\text{V}$; $V_S = 0\text{V}$ | P_6.1.12 |
| Leakage current | $I_{BUS_PAS_do m}$ | -1 | - | - | mA | LIN Spec 2.2 (Par. 13); $V_{BUS} = 0\text{V}$; $V_S = 18\text{V}$ | P_6.1.13 |
| Leakage current | $I_{BUS_PAS_re c}$ | - | - | 20 | μA | LIN Spec 2.2 (Par. 14); $V_{BUS} = 18\text{V}$; $V_S = 8\text{V}$ | P_6.1.14 |
| Bus pull-up resistance | R_{BUS} | 20 | 30 | 47 | kOhm | Normal mode LIN Spec 2.2 (Par. 26), also present in Sleep mode | P_6.1.15 |

Table 46 AC Characteristics - Transceiver Normal Slope Mode

$V_S = 5.5\text{ V to }18\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|--------------|--------|------|-------|---------------|---|----------|
| | | Min. | Typ. | Max. | | | |
| Propagation delay bus dominant to RxD LOW | $t_{d(L),R}$ | 0.1 | 1 | 6 | μs | LIN Spec 2.2 (Param. 31) | P_6.1.16 |
| Propagation delay bus recessive to RxD HIGH | $t_{d(H),R}$ | 0.1 | 1 | 6 | μs | LIN Spec 2.2 (Param. 31) | P_6.1.17 |
| Receiver delay symmetry | $t_{sym,R}$ | -2 | - | 2 | μs | LIN Spec 2.2 (Par. 32); $t_{sym,R} = t_{d(L),R} - t_{d(H),R}$ | P_6.1.18 |
| Duty cycle D1 Normal Slope Mode (for worst case at 20 kbit/s) | t_{duty1} | 0.396 | - | - | | ¹⁾ duty cycle 1, LIN Spec 2.2 (Par. 27); $D1 = t_{bus_rec(min)}/2 t_{bit}$; $TH_{Dom(max)} = 0.581 \times V_S$; $TH_{Rec(max)} = 0.744 \times V_S$; $5.5\text{V} \leq V_S \leq 18\text{V}$; $t_{bit} = 50\mu\text{s}$ | P_6.1.19 |
| Duty cycle D2 Normal Slope Mode (for worst case at 20 kbit/s) | t_{duty2} | - | - | 0.581 | | ¹⁾ duty cycle 2, LIN Spec 2.2 (Par. 28); $D2 = t_{bus_rec(max)}/2 t_{bit}$; $TH_{Dom(max)} = 0.284 \times V_S$; $TH_{Rec(max)} = 0.422 \times V_S$; $5.5\text{V} \leq V_S \leq 18\text{V}$; $t_{bit} = 50\mu\text{s}$ | P_6.1.20 |

Electrical Characteristics

1) Bus load concerning LIN Spec. 2.2: Load 1 = 1 nF / 1 k Ω = C_{BUS} / R_{BUS} , Load 2 = 6.8 nF / 660 Ω = C_{BUS} / R_{BUS} , Load 3 = 10 nF / 500 Ω = C_{BUS} / R_{BUS}

Table 47 AC Characteristics - Transceiver Low Slope Mode

$V_S = 5.5\text{ V to }18\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|--|-------------------|-----------|------|-------|---------------|---|----------|
| | | Min. | Typ. | Max. | | | |
| Propagation delay bus dominant to RxD LOW | $t_{d(L),R_LSM}$ | 0.1 | 1 | 6 | μs | LIN Spec 2.2 (Param. 31) | P_6.1.21 |
| Propagation delay bus recessive to RxD HIGH | $t_{d(H),R_LSM}$ | 0.1 | 1 | 6 | μs | LIN Spec 2.2 (Param. 31) | P_6.1.22 |
| Receiver delay symmetry | t_{sym,R_LSM} | -2 | - | 2 | μs | LIN Spec 2.2 (Par. 32); $t_{sym,R} = t_{d(L),R} - t_{d(H),R}$ | P_6.1.23 |
| Duty cycle D3(for worst case at 10.4 kbit/s) | t_{duty1_LSM} | 0.41 7 | - | - | | ¹⁾ duty cycle 3 LIN Spec 2.2 (Par. 29); $D3 = t_{bus_rec(min)}/2 t_{bit}$; $TH_{Dom}(max) = 0.616 \times V_S$; $TH_{Rec}(max) = 0.778 \times V_S$; $5.5V \leq V_S \leq 18V$; $t_{bit} = 96\mu\text{s}$ | P_6.1.24 |
| Duty cycle D4(for worst case at 10.4 kbit/s) | t_{duty2_LSM} | - | - | 0.590 | | ¹⁾ duty cycle 4 LIN Spec 2.2 (Par. 30); $D4 = t_{bus_rec(max)}/2 t_{bit}$; $TH_{Dom}(max) = 0.251 \times V_S$; $TH_{Rec}(max) = 0.389 \times V_S$; $5.5V \leq V_S \leq 18V$; $t_{bit} = 96\mu\text{s}$ | P_6.1.25 |

1) Bus load concerning LIN Spec. 2.2: Load 1 = 1 nF / 1 k Ω = C_{BUS} / R_{BUS} , Load 2 = 6.8 nF / 660 Ω = C_{BUS} / R_{BUS} , Load 3 = 10 nF / 500 Ω = C_{BUS} / R_{BUS}

Table 48 AC Characteristics - Transceiver Fast Slope Mode

$V_S = 5.5\text{ V to }18\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|--|----------------------------|--------|------|------|---------------|--|----------|
| | | Min. | Typ. | Max. | | | |
| Propagation delay bus dominant to RxD LOW | $t_{d(L),R_FSM}$ | 0.1 | 1 | 6 | μs | | P_6.1.26 |
| Propagation delay bus recessive to RxD HIGH | $t_{d(H),R_FSM}$ | 0.1 | 1 | 6 | μs | | P_6.1.27 |
| Receiver delay symmetry (LIN Spec V1.3 supply voltage range) | $t_{sym,R_VS_S pecV1.3}$ | -1.5 | - | 1.5 | μs | $7V \leq V_S \leq 18V$; $t_{sym,R} = t_{d(L),R} - t_{d(H),R}$ | P_6.1.28 |
| Receiver delay symmetry | t_{sym,R_FSM} | -2.0 | - | 2.0 | μs | $t_{sym,R} = t_{d(L),R} - t_{d(H),R}$ | P_6.1.42 |

Electrical Characteristics

Table 48 AC Characteristics - Transceiver Fast Slope Mode (cont'd)

$V_S = 5.5\text{ V to }18\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|-------------------------------------|-------------------------|-----------|------|-------|------|--|----------|
| | | Min. | Typ. | Max. | | | |
| Duty cycle D5(used for 62.5 kbit/s) | $t_{\text{duty1_FSM}}$ | 0.39 5 | - | - | | ¹⁾ duty cycle 5; $D1 = t_{\text{bus_rec(min)}/2} t_{\text{bit}}$; $TH_{\text{Dom(max)}} = 0.581 \times V_S$; $TH_{\text{Rec(max)}} = 0.744 \times V_S$; $5.5\text{V} \leq V_S \leq 18\text{V}$; $t_{\text{bit}} = 25\mu\text{s}$ | P_6.1.29 |
| Duty cycle D6(used for 62.5 kbit/s) | $t_{\text{duty2_FSM}}$ | - | - | 0.581 | | ¹⁾ duty cycle 6; $D2 = t_{\text{bus_rec(max)}/2} t_{\text{bit}}$; $TH_{\text{Dom(max)}} = 0.284 \times V_S$; $TH_{\text{Rec(max)}} = 0.422 \times V_S$; $t_{\text{bit}} = 25\mu\text{s}$ | P_6.1.30 |

1) Bus load concerning LIN Spec. 2.2: Load 1 = $1\text{ nF} / 1\text{ k}\Omega = C_{\text{BUS}} / R_{\text{BUS}}$, Load 2 = $6.8\text{ nF} / 660\ \Omega = C_{\text{BUS}} / R_{\text{BUS}}$, Load 3 = $10\text{ nF} / 500\ \Omega = C_{\text{BUS}} / R_{\text{BUS}}$

Table 49 AC Characteristics - Flash Mode

$V_S = 5.5\text{ V to }18\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|--|-----------------------------------|-----------|------|-------|---------------|--|----------|
| | | Min. | Typ. | Max. | | | |
| Propagation delay bus dominant to Rx D LOW | $t_{\text{d(L),R_FM}}$ | 0.1 | 0.5 | 6 | μs | | P_6.1.31 |
| Propagation delay bus recessive to Rx D HIGH | $t_{\text{d(H),R_FM}}$ | 0.1 | 0.5 | 6 | μs | | P_6.1.32 |
| Receiver delay symmetry (LIN Spec V1.3 supply voltage range) | $t_{\text{sym,R_VS_SpecV1_3}}$ | -1.0 | - | 1.5 | μs | $7\text{V} \leq V_S \leq 18\text{V}$; $t_{\text{sym,R}} = t_{\text{d(L),R}} - t_{\text{d(H),R}}$ | P_6.1.33 |
| Receiver delay symmetry | $t_{\text{sym,R_FM}}$ | -2.0 | - | 2.0 | μs | $t_{\text{sym,R}} = t_{\text{d(L),R}} - t_{\text{d(H),R}}$ | P_6.1.86 |
| Duty cycle D7(for worst case at 115 kbit/s)for +1 us Receiver delay symmetry (used for 250 kbit/s programming) | $t_{\text{duty1_FM}}$ | 0.39 5 | - | - | | ¹⁾ duty cycle D7; $D7 = t_{\text{bus_rec(min)}/(2 \times t_{\text{bit}})}$; $TH_{\text{Dom(max)}} = 0.581 \times V_S$; $TH_{\text{Rec(max)}} = 0.744 \times V_S$; $t_{\text{bit}} = 8.7\mu\text{s}$ | P_6.1.34 |
| Duty cycle D8(for worst case at 115 kbit/s)for +1 us Receiver delay symmetry (used for 250 kbit/s programming) | $t_{\text{duty2_FM}}$ | - | - | 0.578 | | ¹⁾ duty cycle 8; $D8 = t_{\text{bus_rec(max)}/(2 \times t_{\text{bit}})}$; $TH_{\text{Dom(max)}} = 0.284 \times V_S$; $TH_{\text{Rec(max)}} = 0.422 \times V_S$; $t_{\text{bit}} = 8.7\mu\text{s}$ | P_6.1.35 |
| LIN input capacity | $C_{\text{LIN_IN}}$ | - | 15 | 30 | pF | ²⁾ | P_6.1.36 |

1) Bus load: Load 1 = $1\text{ nF} / 500\ \Omega = C_{\text{BUS}} / R_{\text{BUS}}$

2) Not subject to production test, specified by design

Electrical Characteristics

Table 50 AC Characteristics - Other Timings

$V_S = 5.5\text{ V to }18\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|-----------------------|----------------------|--------|------|------|------|----------------------------|----------|
| | | Min. | Typ. | Max. | | | |
| TxD dominant time out | t_{timeout} | 6 | 12 | 20 | ms | $V_{\text{TxD}}=0\text{V}$ | P_6.1.37 |

Table 51 Thermal Shutdown (Junction Temperature)

$V_S = 5.5\text{ V to }18\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|------------------------|------------------|--------|------|------|------------------|------------------------|----------|
| | | Min. | Typ. | Max. | | | |
| Thermal shutdown temp. | T_{jSD} | 180 | 200 | 215 | $^\circ\text{C}$ | ¹⁾ | P_6.1.38 |
| Thermal shutdown hyst. | ΔT | - | 10 | - | K | ¹⁾ | P_6.1.39 |

¹⁾ Not subject to production test, specified by design

Electrical Characteristics

28.7 High-Speed Synchronous Serial Interface

28.7.1 SSC Timing

The table below provides the SSC timing in the TLE9852QX:

Table 52 SSC Master Mode Timing (Operating Conditions apply, CL = 50 pF)

$V_S = 5.5\text{ V to }28\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|----------------------|--------|--------------------|------|------|------|--|---------|
| | | Min. | Typ. | Max. | | | |
| SCLK clock period | t_0 | $2 \times T_{SSC}$ | - | - | | ^{1) 2)} $V_{DDP} > 2.7\text{V}$ | P_7.1.1 |
| MTSR delay from SCLK | t_1 | 10 | - | - | ns | ²⁾ $V_{DDP} > 2.7\text{V}$ | P_7.1.2 |
| MRST setup to SCLK | t_2 | 10 | - | - | ns | ²⁾ $V_{DDP} > 2.7\text{V}$ | P_7.1.3 |
| MRST hold from SCLK | t_3 | 15 | - | - | ns | ²⁾ $V_{DDP} > 2.7\text{V}$ | P_7.1.4 |

- 1) $T_{SSCmin} = T_{CPU} = 1/f_{CPU}$.
If $f_{CPU} = 20\text{ MHz}$, $t_0 = 100\text{ ns}$. T_{CPU} is the CPU clock period.
- 2) Not subject to production test, specified by design

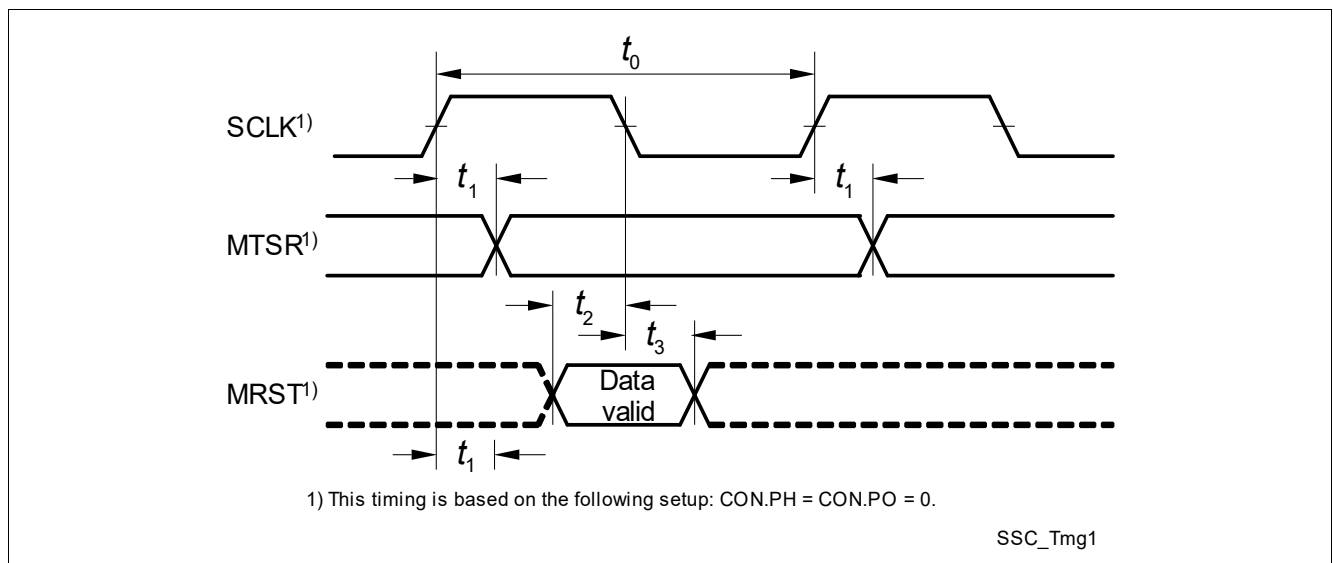


Figure 46 SSC Master Mode Timing

Electrical Characteristics

28.8 Measurement Unit

28.8.1 Electrical Characteristics

Table 53 ADC1 - Battery / Supply Voltage Measurement V_{BAT_SENSE} , V_S

$V_S = 5.5\text{ V to }28\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|--|---|--------|-------|-------|------|--|----------|
| | | Min. | Typ. | Max. | | | |
| Input to output voltage attenuation: V_{BAT_SENSE}/V_S | $ATT_{VBAT_SENSE}, ATT_{VS}$ | - | 0.047 | - | | | P_8.1.10 |
| Nominal operating input voltage range V_{BAT_SENSE}/V_S | $V_{BAT_SENSE, range}, V_{S, range}$ | 0 | - | 25.77 | V | ¹⁾ Max. value corresponds to typ. ADC full scale input; calculated: typ. V_{BG} / typ. ATT_{VBAT_SENSE} | P_8.1.11 |
| Accuracy of V_{BAT_SENSE}/V_S after calibration - with IIR filter | $\Delta V_{BAT_SENSE_IIR}, \Delta V_{S_IIR}$ | -200 | - | 200 | mV | $-40^\circ\text{C} \leq T_j \leq 150^\circ\text{C}$; $5.5\text{V} \leq V_S \leq 28\text{V}$; $ADC1_FILTCOEFF0_13.CHx=11_B$; $f_{ADC1}=f_{sys_max}$ | P_8.1.12 |
| Accuracy of V_{BAT_SENSE}/V_S after calibration | $\Delta V_{BAT_SENSE}, \Delta V_S$ | -300 | - | 300 | mV | $-40^\circ\text{C} \leq T_j \leq 150^\circ\text{C}$; $5.5\text{V} \leq V_S \leq 28\text{V}$; $f_{ADC1}=f_{sys_max}$ | P_8.1.49 |

1) Not subject to production test, specified by design

Table 54 ADC1 - Monitoring Input Voltage Measurement V_{MONx}

$V_S = 5.5\text{ V to }28\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|--|-------------------|--------|-------|-------|------|--|----------|
| | | Min. | Typ. | Max. | | | |
| Input to output voltage attenuation: V_{MONx} | $ATT_{V_{MONx}}$ | - | 0.039 | - | | | P_8.1.13 |
| Nominal operating input voltage range V_{MONx} | $V_{MONx, range}$ | 0 | - | 31.05 | V | ¹⁾ Max. value corresponds to typ. ADC full scale input; calculated: typ. V_{BG} / typ. $ATT_{V_{MONx}}$ | P_8.1.14 |

1) Not subject to production test, specified by design

Electrical Characteristics

Table 55 ADC1 - Port 2.x Voltage Measurement $V_{2,x}$

$V_S = 5.5\text{ V to }28\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|-------------------------|--------|-------|------------------|------|---|----------|
| | | Min. | Typ. | Max. | | | |
| Input to output voltage attenuation: $V_{Port2.x}$ | $ATT_{2,x}$ | - | 0.227 | - | | | P_8.1.15 |
| Nominal operating input voltage range $V_{Port2.x}$ | $V_{Port2.x,rang}$ e | 0 | - | V_{DDPOU} T | V | ¹⁾ Max. value corresponds to typ. ADC full scale input; calculated: typ. V_{BG} / typ. $ATT_{2,x}$ | P_8.1.16 |

1) Not subject to production test, specified by design

Table 56 ADC2 - Supply Voltage Measurement V_S

$V_S = 5.5\text{ V to }28\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|----------------------|--------|-------|-------|------|--|---------|
| | | Min. | Typ. | Max. | | | |
| Input to output voltage attenuation: V_S | ATT_{VS_ADC} 2 | - | 0.039 | - | | | P_8.1.1 |
| Nominal operating input voltage range V_S | $V_{S,ADC2}$ | 3 | - | 31.05 | V | ¹⁾ Max. value corresponds to typ. ADC full scale input; calculated: typ. V_{BG} / typ. ATT_{VS_ADC2} | P_8.1.2 |
| Accuracy of V_S after calibration | $\Delta V_{S,ADC2}$ | -320 | - | 320 | mV | $-40^\circ\text{C} \leq T_j \leq 150^\circ\text{C}$; $5.5\text{V} \leq V_S \leq 28\text{V}$ | P_8.1.3 |

1) Not subject to production test, specified by design

Table 57 ADC2 - Supply Voltage Measurement V_{SD}

$V_S = 5.5\text{ V to }28\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|--|-----------------------|--------|-------|-------|------|---|----------|
| | | Min. | Typ. | Max. | | | |
| Input to output voltage attenuation: V_{SD} | ATT_{VSD_AD} C2 | - | 0.039 | - | | | P_8.1.44 |
| Nominal operating input voltage range V_{SD} | $V_{SD,ADC2}$ | 3 | - | 31.05 | V | ¹⁾ Max. value corresponds to typ. ADC full scale input; calculated: typ. V_{BG} / typ. ATT_{VSD_ADC2} | P_8.1.39 |
| Accuracy of V_{SD} after calibration | $\Delta V_{SD,ADC2}$ | -320 | - | 320 | mV | $-40^\circ\text{C} \leq T_j \leq 150^\circ\text{C}$; $5.5\text{V} \leq V_S \leq 28\text{V}$ | P_8.1.40 |

1) Not subject to production test, specified by design

Electrical Characteristics

Table 58 ADC2 - Supply Voltage Measurement V_{CP}

$V_S = 5.5\text{ V to }28\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|--|-----------------------|--------|-------|-------|------|--|----------|
| | | Min. | Typ. | Max. | | | |
| Input to output voltage attenuation: V_{CP} | $ATT_{V_{CP_ADC2}}$ | - | 0.023 | - | | | P_8.1.41 |
| Nominal operating input voltage range V_{CP} | V_{CP_ADC2} | 3 | - | 52.65 | V | ^{1) 2)} Max. value corresponds to typ. ADC full scale input; calculated: typ. $V_{BG}/$ typ. $ATT_{V_{CP_ADC2}}$ | P_8.1.42 |
| Accuracy of V_{CP} after calibration | ΔV_{CP_ADC2} | -650 | - | 650 | mV | $-40^\circ\text{C} \leq T_j \leq 150^\circ\text{C}$; $5.5\text{V} \leq V_S \leq 28\text{V}$ | P_8.1.43 |

- 1) This is the theoretical nominal full-scale input range of the measurement chain. The allowed input voltage range at the pin is given in the "Absolute Maximum Ratings" section.
- 2) Not subject to production test, specified by design

Table 59 ADC2 - VDDEXT Voltage Measurement V_{DDEXT}

$V_S = 5.5\text{ V to }28\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|--|-------------------|--------|-------|------|------|---|----------|
| | | Min. | Typ. | Max. | | | |
| Input to output voltage attenuation: VDDEXT | ATT_{VDDEXT} | - | 0.195 | - | | | P_8.1.17 |
| Nominal operating input voltage range VDDEXT | $V_{DDEXT,range}$ | 0 | - | 5.97 | V | ¹⁾ Max. value corresponds to typ. ADC full scale input; calculated: typ. $V_{BG}/$ typ. $ATT_{V_{CP_VDDEXT}}$ | P_8.1.18 |

- 1) Not subject to production test, specified by design

Table 60 ADC2 - Pad Supply Voltage Measurement V_{VDDP}

$V_S = 5.5\text{ V to }28\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|--|-----------------|--------|-------|---------------------|------|---|---------|
| | | Min. | Typ. | Max. | | | |
| Input-to-output voltage attenuation: VDDP | ATT_{VDDP} | - | 0.195 | - | | | P_8.1.4 |
| Nominal operating input voltage range VDDP | $V_{DDP,range}$ | 0 | - | $V_{DDPOU_T} + 0.3$ | V | ¹⁾ Max. value corresponds to typ. ADC full scale input; calculated: typ. $V_{BG}/$ typ. ATT_{VDDP} | P_8.1.5 |

- 1) Not subject to production test, specified by design

Electrical Characteristics

Table 61 ADC2 - Reference Voltage Measurement V_{PMUBG}

$V_S = 5.5\text{ V to }28\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|--|-------------------|--------|------|-----------------|------|--|----------|
| | | Min. | Typ. | Max. | | | |
| Input-to-output voltage attenuation: VBG | ATT_{PMUVBG} | - | 0.75 | - | | ¹⁾ | P_8.1.6 |
| Nominal operating input voltage range VBG | $V_{PMUBG,range}$ | 0.8 | - | $V_{DDC} - 0.1$ | V | ¹⁾ Max. value corresponds to typ. ADC full scale input; calculated: typ. $V_{BG}/$ typ. ATT_{VBG} | P_8.1.7 |
| Value of ADC2- V_{PMUBG} measurement after calibration | V_{PMUBG} | 0.9 | 1.0 | 1.1 | V | | P_8.1.45 |

¹⁾ Not subject to production test, specified by design

Table 62 ADC2 - Core supply Voltage Measurement V_{DDC}

$V_S = 5.5\text{ V to }28\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|--|-----------------|--------|------|-----------------|------|---|---------|
| | | Min. | Typ. | Max. | | | |
| Input-to-output voltage attenuation: VDDC | ATT_{VDDC} | - | 0.75 | - | | | P_8.1.8 |
| Nominal operating input voltage range VDDC | $V_{DDC,range}$ | 0.6 | - | $V_{DDC} + 0.1$ | V | ¹⁾ Max. value corresponds to typ. ADC full scale input; calculated: typ. $V_{BG}/$ typ. ATT_{VDDC} | P_8.1.9 |

¹⁾ Not subject to production test, specified by design

Electrical Characteristics

28.8.2 Central Temperature Sensor Module

28.8.2.1 Electrical Characteristics

Table 63 Temperature Sensor Specifications

$V_S = 5.5\text{ V}$ to 28 V , $T_j = -40^\circ\text{C}$ to $+150^\circ\text{C}$; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|--|----------|--------|-------|------|------------------|---|---------|
| | | Min. | Typ. | Max. | | | |
| Output voltage V_{TEMP} at $T_0=0^\circ\text{C}$ (273 K) | a | - | 0.628 | - | V | ¹⁾ $T_0=0^\circ\text{C}$ | P_8.2.1 |
| Temperature sensitivity b | b | - | 2.31 | - | mV/ K | ¹⁾ | P_8.2.2 |
| Accuracy_1 | Acc_1 | -10 | - | 10 | $^\circ\text{C}$ | ²⁾ $-40^\circ\text{C} < T_j < 85^\circ\text{C}$ | P_8.2.3 |
| Accuracy_2 | Acc_2 | -10 | - | 10 | $^\circ\text{C}$ | ¹⁾ $125^\circ\text{C} < T_j < 150^\circ\text{C}$ | P_8.2.4 |
| Accuracy_3 | Acc_3 | -5 | - | 5 | $^\circ\text{C}$ | $85^\circ\text{C} < T_j < 125^\circ\text{C}$ | P_8.2.5 |

1) Not subject to production test, specified by design

2) Accuracy with reference to on-chip temperature calibration measurement, valid for Mode1

Electrical Characteristics

28.9 ADC1 (10-Bit)

28.9.1 Electrical Characteristics ADC1 (10-Bit)

These parameters describe the conditions for optimum ADC performance.

Note: Operating Conditions apply.

Table 64 Timing and AC Specification

$V_S = 5.5\text{ V to }28\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|------------------------|-------------------|--------|------|------|------|------------------------|---------|
| | | Min. | Typ. | Max. | | | |
| Analog clock frequency | f_{ADCI} | 5 | - | | MHz | ¹⁾ | P_9.2.1 |

1) The limit values for f_{ADCI} must not be exceeded when selecting the peripheral frequency and the prescaler setting.

Table 65 DC Specification

$V_S = 5.5\text{ V to }28\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|--|------------------------|--------|------|------|----------|---|----------|
| | | Min. | Typ. | Max. | | | |
| DNL error | EA_{DNL} | -2 | - | 2 | LSB | | P_9.2.8 |
| INL error | EA_{INL} | -2 | - | 2 | LSB | $T_j \leq 150^\circ\text{C}$ | P_9.2.9 |
| Gain error | EA_{GAIN} | -1.2 | - | 1.2 | % of FSR | ^{1) 2)} Already calibrated by implemented calibration unit | P_9.2.10 |
| Offset error | EA_{OFF} | -2.5 | - | 2.5 | LSB | ²⁾ already calibrated | P_9.2.11 |
| Total unadjusted error | EA_{TUE} | -10 | - | 10 | LSB | ²⁾ already calibrated | P_9.2.33 |
| Cross-coupling Attenuation between LV Channels | EA_{CCOUP} | -2 | - | 2 | LSB | ²⁾ | P_9.2.12 |
| Input capacitance of a HV analog input | $C_{\text{AINT_HVI}}$ | - | - | 200 | fF | ²⁾ | P_9.2.13 |
| Input capacitance of a LV analog input | $C_{\text{AINT_LVI}}$ | - | - | 200 | fF | ²⁾ | P_9.2.19 |

1) This Gain error is calibrated by IFX end of line

2) Not subject to production test, specified by design

Electrical Characteristics

28.10 High-Voltage Monitoring Input

28.10.1 Electrical Characteristics

Table 66 Electrical Characteristics Monitoring Input

$V_S = 5.5\text{ V to }28\text{ V}$; $T_j = -40^\circ\text{C to }+150^\circ\text{C}$; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|--------------------------------------|------------------------|-------------------|-------------------|-------------------|---------------|--|----------|
| | | Min. | Typ. | Max. | | | |
| Wake-up/monitoring threshold voltage | V_{MONth} | $0.4 \times V_S$ | $0.5 \times V_S$ | $0.6 \times V_S$ | V | without external serial resistor R_S (with $R_S: dV = I_{\text{PD/PU}} * R_S$); | P_10.1.1 |
| Threshold hysteresis | $V_{\text{MONth,hys}}$ | $0.02 \times V_S$ | $0.06 \times V_S$ | $0.12 \times V_S$ | V | in all modes; without external serial resistor R_S (with $R_S: dV = I_{\text{PD/PU}} * R_S$); | P_10.1.2 |
| Pull-up current | $I_{\text{PU,MON}}$ | -20 | -10 | -5 | μA | $V_{\text{MON_IN}} = 0.6 * V_S$ | P_10.1.3 |
| Pull-down current | $I_{\text{PD,MON}}$ | 5 | 10 | 20 | μA | $V_{\text{MON_IN}} = 0.4 * V_S$ | P_10.1.4 |
| Input leakage current | $I_{\text{LK,MON}}$ | -2 | - | 2 | μA | ¹⁾ $T_j < 150^\circ\text{C}$; $0\text{V} < V_{\text{MON_IN}} < 28\text{V}$ | P_10.1.5 |
| Wake-up filter time | $t_{\text{FT,MON}}$ | - | 20 | - | μs | ²⁾ | P_10.1.6 |

1) Valid for enabled module. Pull-up and pull down current functionality disabled; ADC1 off.

2) With pull-up, pull down current disabled.

Electrical Characteristics

28.11 High Side Switch

28.11.1 Electrical Characteristics

Table 67 Operating areas

$V_S = 5.5\text{ V to }28\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|-------------------------------|--------|------|------|------|---|----------|
| | | Min. | Typ. | Max. | | | |
| PWM frequency of HS with Slew Rate Control | $f_{\text{PWM_W_SR}}$ | 0 | - | 10 | kHz | ¹⁾ Frequency must be configured in the PWM Generator | P_11.1.1 |
| PWM frequency of HS without Slew Rate Control | $f_{\text{PWM_W/O_S}}$ R | 0 | - | 25 | kHz | ^{2) 1)} Frequency must be configured in the PWM Generator (minimum ON / OFF time 5 μs) | P_11.1.2 |

1) Not subject to production test, specified by design

2) Referring to a 470 Ω series resistor to charge an external power mos gate.

Table 68 Output HS

$V_S = 5.5\text{ V to }28\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|--|--------------------------|--------|------|------|------------------------|--|----------|
| | | Min. | Typ. | Max. | | | |
| ON-State Resistance | R_{ON} | 3.5 | 10 | 15 | Ohm | $V_S=13.5\text{V}$; $I_{\text{ds}}=100\text{mA}$ | P_11.1.3 |
| Output leakage Current | I_{leakage} | -1.5 | - | - | μA | Output OFF; $-0.3\text{V} < V_{\text{HS}} < V_S$ | P_11.1.4 |
| Output Slew Rate (rising) with slow Slew Rate setting (Slew Rate 1) | $SR_{\text{raise_SR1}}$ | 1.5 | - | 7 | $\text{V}/\mu\text{s}$ | 20% to 80% of V_S ; $C_L=1\text{nF}$; $R_L=300\Omega$ | P_11.1.5 |
| Output Slew Rate (falling) with slow Slew Rate setting (Slew Rate 1) | $SR_{\text{fall_SR1}}$ | -7 | - | -1.5 | $\text{V}/\mu\text{s}$ | 80% to 20% of V_S ; $C_L=1\text{nF}$; $R_L=300\Omega$ | P_11.1.6 |
| Output Slew Rate (rising) with fast Slew Rate setting (Slew Rate 2) | $SR_{\text{raise_SR2}}$ | 21 | - | 80 | $\text{V}/\mu\text{s}$ | 20% to 80% of V_S ; $C_L=1\text{nF}$; $R_L=300\Omega$ | P_11.1.7 |
| Output Slew Rate (falling) with fast Slew Rate setting (Slew Rate 2) | $SR_{\text{fall_SR2}}$ | -30 | - | -3 | $\text{V}/\mu\text{s}$ | 80% to 20% of V_S ; $C_L=1\text{nF}$; $R_L=300\Omega$ | P_11.1.8 |

Electrical Characteristics

Table 68 Output HS (cont'd)

$V_S = 5.5\text{ V to }28\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|--|--------------------------|--------|------|------|------------------|--|-----------|
| | | Min. | Typ. | Max. | | | |
| Output Slew Rate (rising) with Slew Rate setting for low Emission (Slew Rate 3) | $SR_{\text{raise_SR3}}$ | 0.3 | - | 1.8 | V/ μs | 20% to 80% of V_S ; $C_L=1\text{nF}$; $R_L=300\Omega$ | P_11.1.59 |
| Output Slew Rate (falling) with Slew Rate setting for low Emission (Slew Rate 3) | $SR_{\text{fall_SR3}}$ | -1.8 | - | -0.3 | V/ μs | 80% to 20% of V_S ; $C_L=1\text{nF}$; $R_L=300\Omega$ | P_11.1.60 |
| Turn ON Delay time (Slew Rate 1) | $t_{\text{IN-HS_SR1}}$ | 1.1 | 2.2 | 3.6 | μs | ON=1 to 20% of V_S ; $C_L=1\text{nF}$; $R_L=300\Omega$ | P_11.1.9 |
| Turn ON time (Slew Rate 1) | $t_{\text{ON_SR1}}$ | 2.1 | - | 8.8 | μs | HS_ON=1 to 80% of V_S ; $C_L=1\text{nF}$; $R_L=300\Omega$ | P_11.1.10 |
| Turn OFF time (Slew Rate 1) | $t_{\text{OFF_SR1}}$ | 5 | - | 16 | μs | HS_ON=0 to 20% of V_S ; $C_L=1\text{nF}$; $R_L=300\Omega$ | P_11.1.11 |
| Turn ON Delay time (Slew Rate 2) | $t_{\text{IN-HS_SR2}}$ | 0.08 | 0.22 | 0.38 | μs | ON=1 to 20% of V_S ; $C_L=1\text{nF}$; $R_L=300\Omega$ | P_11.1.55 |
| Turn ON time (Slew Rate 2) | $t_{\text{ON_SR2}}$ | 0.2 | - | 1.2 | μs | HS_ON=1 to 80% of V_S ; $C_L=1\text{nF}$; $R_L=300\Omega$ | P_11.1.56 |
| Turn OFF time (Slew Rate 2) | $t_{\text{OFF_SR2}}$ | 1.1 | - | 2.7 | μs | HS_ON=0 to 20% of V_S ; $C_L=1\text{nF}$; $R_L=300\Omega$ | P_11.1.57 |
| Turn ON Delay time (Slew Rate 3) | $t_{\text{IN-HS_SR3}}$ | 3.5 | 8.2 | 13.5 | μs | ON=1 to 20% of V_S ; $C_L=1\text{nF}$; $R_L=300\Omega$ | P_11.1.61 |
| Turn ON time (Slew Rate 3) | $t_{\text{ON_SR3}}$ | 7.8 | - | 36 | μs | HS_ON=1 to 80% of V_S ; $C_L=1\text{nF}$; $R_L=300\Omega$ | P_11.1.62 |
| Turn OFF time (Slew Rate 3) | $t_{\text{OFF_SR3}}$ | 18 | - | 64 | μs | HS_ON=0 to 20% of V_S ; $C_L=1\text{nF}$; $R_L=300\Omega$ | P_11.1.63 |

Table 69 Overcurrent detection

$V_S = 5.5\text{ V to }28\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|------------------------------------|-------------------------|--------|------|------|------|------------------------------------|-----------|
| | | Min. | Typ. | Max. | | | |
| Overcurrent threshold 0, trimmed | I_{octh0} | 26 | 40.5 | 56 | mA | $V_S=13.5\text{V}$; HSx_OC_SEL=00 | P_11.1.12 |
| Overcurrent threshold 0 hysteresis | $I_{\text{octh0,hyst}}$ | 2.5 | 5 | 12 | mA | ¹⁾ HSx_OC_SEL=00 | P_11.1.13 |
| Overcurrent threshold 1, trimmed | I_{octh1} | 51 | 65 | 86 | mA | $V_S=13.5\text{V}$; HSx_OC_SEL=01 | P_11.1.14 |

Electrical Characteristics

Table 69 Overcurrent detection (cont'd)

$V_S = 5.5\text{ V to }28\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|------------------------------------|-------------------------------|--------|------|------|---------------|---|-----------|
| | | Min. | Typ. | Max. | | | |
| Overcurrent threshold 1 hysteresis | $I_{\text{oct}1,\text{hyst}}$ | 4 | 8 | 17 | mA | ¹⁾ HSx_OC_SEL=01 | P_11.1.15 |
| Overcurrent threshold 2, trimmed | $I_{\text{oct}2}$ | 101 | 134 | 180 | mA | $V_S=13.5\text{V}$; HSx_OC_SEL=10 | P_11.1.16 |
| Overcurrent threshold 2 hysteresis | $I_{\text{oct}2,\text{hyst}}$ | 11 | 17 | 33 | mA | ¹⁾ HSx_OC_SEL=10 | P_11.1.17 |
| Overcurrent threshold 3, trimmed | $I_{\text{oct}3}$ | 151 | 201 | 270 | mA | $V_S=13.5\text{V}$; HSx_OC_SEL=11 | P_11.1.18 |
| Overcurrent threshold 3 hysteresis | $I_{\text{oct}3,\text{hyst}}$ | 22 | 35 | 67 | mA | ¹⁾ HSx_OC_SEL=11 | P_11.1.19 |
| Overcurrent shutdown response time | t_{oct} | 8 | - | 80 | μs | ¹⁾ HS_ON to OC_SD (including switch-on time); $R_L=100\Omega$; $V_S=13.5\text{V}$ | P_11.1.20 |

1) Not subject to production test, specified by design

Table 70 ON-state open load detection

$V_S = 5.5\text{ V to }28\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---------------------|----------------------|-----------|------|------|------|------------------------|-----------|
| | | Min. | Typ. | Max. | | | |
| Open load threshold | I_{OLONth} | 0.35 | - | 2.15 | mA | | P_11.1.21 |
| Hysteresis | I_{OLONhys} | 0.01 5 | - | 0.3 | mA | | P_11.1.22 |

Table 71 Cyclic sense mode

$V_S = 5.5\text{ V to }28\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|----------------------------|---------------------------------|--------|------|------|------------------------|---|-----------|
| | | Min. | Typ. | Max. | | | |
| Current capability | $I_{\text{HS max}}$ sleep_pd | 40 | - | - | mA | Sleep Mode / Stop Mode Cyclic Operation | P_11.1.23 |
| ON-State Resistance | $R_{\text{ON,static}}$ | - | - | 105 | Oh m | $I_{\text{ds}}=40\text{mA}$ | P_11.1.24 |
| Output Slew Rate (rising) | $SR_{\text{rise_cyc}}$ | 0.9 | - | 18 | $\text{V}/\mu\text{s}$ | 20% to 80% of V_S ; $R_L=300\Omega$; $V_S \leq 18\text{V}$ | P_11.1.25 |
| Output Slew Rate (falling) | $SR_{\text{fal_cycl}}$ | -34 | - | -2.5 | $\text{V}/\mu\text{s}$ | 80% to 20% of V_S ; $R_L=300\Omega$; $V_S \leq 18\text{V}$ | P_11.1.26 |

Electrical Characteristics
Table 71 **Cyclic sense mode** (cont'd)

$V_S = 5.5\text{ V to }28\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|-------------------------|----------------|--------|------|------|---------------|--|-----------|
| | | Min. | Typ. | Max. | | | |
| Delay Time CYCLIC_ON-HS | t_{IN_cyc} | 0.2 | - | 5.6 | μs | ON=1 to 20% of V_S ; $R_L=300\Omega$; $V_S \leq 18\text{V}$ | P_11.1.27 |
| Turn-ON time | t_{ON_cyc} | 1.5 | - | 15 | μs | ON=1 to 80%; $R_L=300\Omega$; $V_S \leq 18\text{V}$ | P_11.1.28 |
| Turn-OFF time | t_{OFF_cyc} | 0.8 | - | 3.4 | μs | ON=0 to 20% of V_S ; $R_L=300\Omega$; $V_S \leq 18\text{V}$ | P_11.1.29 |

Electrical Characteristics

28.12 MOSFET Driver

28.12.1 Electrical Characteristics

Table 72 MOSFET Driver Output

$V_S = 4.4\text{ V to }28\text{ V}$, $V_{SD} = 5.4\text{ V to }29\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin
(unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|--|-------------------------------------|--------|------|-------|------|---|-----------|
| | | Min. | Typ. | Max. | | | |
| Gate charge current | I_{chg0} | 3 | 7 | 12 | mA | ¹⁾ $C_L=10\text{nF}$; $I_{\text{CHARGE}}=0_D$; $V_{\text{GSx}} \leq V_{\text{GS(on)}}$; $V_{\text{SD}} \geq 7.4\text{V}$ | P_12.1.80 |
| Gate charge current | I_{chg3} | 8 | 15 | 23 | mA | ¹⁾ $C_L=10\text{nF}$; $I_{\text{CHARGE}}=3_D$; $V_{\text{GSx}} \leq V_{\text{GS(on)}}$; $V_{\text{SD}} \geq 7.4\text{V}$ | P_12.1.81 |
| Gate charge current | I_{chg7} | 16 | 26 | 36 | mA | ¹⁾ $C_L=10\text{nF}$; $I_{\text{CHARGE}}=7_D$; $V_{\text{GSx}} \leq V_{\text{GS(on)}}$; $V_{\text{SD}} \geq 7.4\text{V}$ | P_12.1.82 |
| Gate charge current | I_{chg15} | 38 | 53 | 68 | mA | ¹⁾ $C_L=10\text{nF}$; $I_{\text{CHARGE}}=15_D$; $V_{\text{GSx}} \leq V_{\text{GS(on)}}$; $V_{\text{SD}} \geq 7.4\text{V}$ | P_12.1.83 |
| Gate charge current | I_{chg31} | 96 | 125 | 154 | mA | ¹⁾ $C_L=10\text{nF}$; $I_{\text{CHARGE}}=31_D$; $V_{\text{GSx}} \leq V_{\text{GS(on)}}$; $V_{\text{SD}} \geq 7.4\text{V}$ | P_12.1.84 |
| Gate charge current | I_{chg63} | 260 | 320 | 380 | mA | $C_L=10\text{nF}$; $I_{\text{CHARGE}}=63_D$; $V_{\text{GSx}} \leq V_{\text{GS(on)}}$; $V_{\text{SD}} \geq 7.4\text{V}$ | P_12.1.44 |
| Gate charge current dynamic average deviation | $\Delta I_{\text{chg_avg_}}\%$ | -25 % | - | +25 % | | ¹⁾ Reference: typ. $I_{\text{chg}}\%$; $C_L=10$, 33nF ; $SR_{\text{on_SHx}}=165\text{V}/\mu\text{s}$; $V_{\text{GSx}} \leq V_{\text{GS(on)}}$ | P_12.1.85 |
| Gate discharge current | I_{dischg0} | 3 | 7 | 12 | mA | ¹⁾ $C_L=10\text{nF}$; $I_{\text{DISCHARGE}}=0_D$; $V_{\text{GSx}} \geq V_{\text{GS(off)}}$; $V_{\text{SD}} \geq 7.4\text{V}$ | P_12.1.86 |
| Gate discharge current | I_{dischg3} | 8 | 15 | 23 | mA | ¹⁾ $C_L=10\text{nF}$; $I_{\text{DISCHARGE}}=3_D$; $V_{\text{GSx}} \geq V_{\text{GS(off)}}$; $V_{\text{SD}} \geq 7.4\text{V}$ | P_12.1.87 |
| Gate discharge current | I_{dischg7} | 16 | 26 | 36 | mA | ¹⁾ $C_L=10\text{nF}$; $I_{\text{DISCHARGE}}=7_D$; $V_{\text{GSx}} \geq V_{\text{GS(off)}}$; $V_{\text{SD}} \geq 7.4\text{V}$ | P_12.1.88 |
| Gate discharge current | I_{dischg15} | 38 | 53 | 68 | mA | ¹⁾ $C_L=10\text{nF}$; $I_{\text{DISCHARGE}}=15_D$; $V_{\text{GSx}} \geq V_{\text{GS(off)}}$; $V_{\text{SD}} \geq 7.4\text{V}$ | P_12.1.89 |
| Gate discharge current | I_{dischg31} | 96 | 125 | 154 | mA | ¹⁾ $C_L=10\text{nF}$; $I_{\text{DISCHARGE}}=31_D$; $V_{\text{GSx}} \geq V_{\text{GS(off)}}$; $V_{\text{SD}} \geq 7.4\text{V}$ | P_12.1.90 |
| Gate discharge current | I_{dischg63} | 260 | 320 | 380 | mA | $C_L=10\text{nF}$; $I_{\text{DISCHARGE}}=63_D$; $V_{\text{GSx}} \geq V_{\text{GS(off)}}$; $V_{\text{SD}} \geq 7.4\text{V}$ | P_12.1.45 |
| Gate discharge current dynamic average deviation | $\Delta I_{\text{dischg_avg_}}\%$ | -28 % | - | +28 % | | ¹⁾ Reference: typ. $I_{\text{dischg}}\%$; $C_L=10$, 33nF ; $SR_{\text{off_SHx}}=165\text{V}/\mu\text{s}$; $V_{\text{GSx}} \geq V_{\text{GS(off)}}$; $V_{\text{SD}} \geq 7.4\text{V}$ | P_12.1.91 |
| High level output voltage Gxx vs. Sxx | V_{Gxx1} | 10 | - | 12 | V | ²⁾ all other Drivers enabled but not ON; $C_L=10\text{nF}$; $I_{\text{CP}}=6\text{mA}$; $V_{\text{SD}} \geq 7.4\text{V}$ | P_12.1.3 |

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Table 72 MOSFET Driver Output (cont'd)

$V_S = 4.4\text{ V to }28\text{ V}$, $V_{SD} = 5.4\text{ V to }29\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin
(unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|--|------------------|--------|------|------|------|---|------------|
| | | Min. | Typ. | Max. | | | |
| High level output voltage GHx vs. SHx | V_{Gxx2} | 8 | - | - | V | ^{2) 1)} all other Drivers enabled but not ON; $C_L=10\text{nF}$; $I_{CP}=6\text{mA}$; $V_{SD}=6.4\text{V}$ | P_12.1.4 |
| High level output voltage GHx vs. SHx | V_{Gxx3} | 7 | - | - | V | ²⁾ all other Drivers enabled but not ON; $C_L=10\text{nF}$; $I_{CHARGE} \leq 3I_D$; $I_{CP}=6\text{mA}$; $V_{SD}=5.4\text{V}$ | P_12.1.5 |
| High level output voltage GLx vs. GND | V_{Gxx6} | 8 | - | - | V | ^{2) 1)} all other Drivers enabled but not ON; $C_L=10\text{nF}$; $I_{CP}=6\text{mA}$; $V_{SD}=6.4\text{V}$ | P_12.1.6 |
| High level output voltage GLx vs. GND | V_{Gxx7} | 7 | - | - | V | ²⁾ all other Drivers enabled but not ON; $C_L=10\text{nF}$; $I_{CP}=6\text{mA}$; $V_{SD}=5.4\text{V}$ | P_12.1.7 |
| High level output voltage GLx vs. GND / GHx vs. SHx - Brake Mode | V_{Gxx_BM} | 7 | - | - | V | all other Drivers enabled but not ON; $C_L=10\text{nF}$; $R_{GS}=100\text{k}\Omega$; $V_{SD}=5.4\text{V}$ | P_12.1.66 |
| High level output voltage GLx vs. GND - Hold Mode | V_{Gxx_HM} | 2.5 | - | 7.1 | V | $C_L=10\text{nF}$; $R_{GS}=100\text{k}\Omega$; $V_{SD} \geq 5.4\text{V}$ | P_12.1.67 |
| | | 4.2 | - | 7.4 | V | ¹⁾ ; $C_L=10\text{nF}$; $R_{GS}=100\text{k}\Omega$; $V_{SD} \geq 7.4\text{V}$ | P_12.1.102 |
| External MOSFET gate-to-source voltage - MOSFET on | $V_{GS(on)}$ | 5 | - | - | V | ¹⁾ $V_{SD}=5.4\text{V}$ | P_12.1.103 |
| | | 7 | - | - | V | ¹⁾ $V_{SD}=7.4\text{V}$ | P_12.1.95 |
| External MOSFET gate-to-source voltage - MOSFET off | $V_{GS(off)}$ | - | - | 2 | V | ¹⁾ $I_{DISCHARGE} < 3I_D$ | P_12.1.104 |
| | | - | - | 3.5 | V | ¹⁾ $I_{DISCHARGE} \geq 3I_D$ | P_12.1.96 |
| Rise time | t_{rise3_3nf} | 65 | 100 | 130 | ns | ¹⁾ 25-75% of V_{Gxx1} ; $C_L=3.3\text{nF}$; $I_{CHARGE}=\text{max}$; $I_{DISCHARGE}=\text{max}$; $V_{SD} \geq 7.4\text{V}$ | P_12.1.8 |
| Fall time | t_{fall3_3nf} | 65 | 100 | 130 | ns | ¹⁾ 75-25% of V_{Gxx1} ; $C_L=3.3\text{nF}$; $I_{CHARGE}=\text{max}$; $I_{DISCHARGE}=\text{max}$; $V_{SD} \geq 7.4\text{V}$ | P_12.1.9 |
| Rise time | $t_{risemax}$ | 100 | 250 | 450 | ns | 25-75% of V_{Gxx1} ; $C_L=10\text{nF}$; $I_{CHARGE}=\text{max}$; $I_{DISCHARGE}=\text{max}$; $V_{SD} \geq 7.4\text{V}$ | P_12.1.57 |
| Fall time | $t_{fallmax}$ | 100 | 250 | 450 | ns | 75-25% of V_{Gxx1} ; $C_L=10\text{nF}$; $I_{CHARGE}=\text{max}$; $I_{DISCHARGE}=\text{max}$; $V_{SD} \geq 7.4\text{V}$ | P_12.1.58 |

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Table 72 MOSFET Driver Output (cont'd)

$V_S = 4.4\text{ V to }28\text{ V}$, $V_{SD} = 5.4\text{ V to }29\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin
(unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|--|---------------------------|--------|------|------|---------------|--|-----------|
| | | Min. | Typ. | Max. | | | |
| Rise time | t_{risemin} | 4 | - | 15 | μs | ¹⁾ 25-75% of V_{Gxx1} ; $C_L=10\text{nF}$; $I_{\text{CHARGE}}=\text{min}$; $I_{\text{DISCHARGE}}=\text{min}$; $V_{\text{SD}}\geq 7.4\text{V}$ | P_12.1.14 |
| Fall time | t_{fallmin} | 3.5 | - | 12 | μs | ¹⁾ 75-25% of V_{Gxx1} ; $C_L=10\text{nF}$; $I_{\text{CHARGE}}=\text{min}$; $I_{\text{DISCHARGE}}=\text{min}$; $V_{\text{SD}}\geq 7.4\text{V}$ | P_12.1.15 |
| Absolute rise - fall time difference for all LSx | $t_{\text{r-f(diff)LSx}}$ | - | - | 100 | ns | 25-75% of V_{Gxx1} ; $C_L=10\text{nF}$; $I_{\text{CHARGE}}=\text{max}$; $I_{\text{DISCHARGE}}=\text{max}$; $V_{\text{SD}}\geq 7.4\text{V}$ | P_12.1.35 |
| Absolute rise - fall time difference for all HSx | $t_{\text{r-f(diff)HSx}}$ | - | - | 100 | ns | 25-75% of V_{Gxx1} ; $C_L=10\text{nF}$; $I_{\text{CHARGE}}=\text{max}$; $I_{\text{DISCHARGE}}=\text{max}$; $V_{\text{SD}}\geq 7.4\text{V}$ | P_12.1.36 |
| Resistor between GHx/GLx and GND | R_{GGND} | 30 | 40 | 50 | kOh m | | P_12.1.11 |
| Resistor between SHx and GND | R_{SHGN} | 30 | 40 | 50 | kOh m | ³⁾ This resistance is the resistance between GHx and GND connected through a diode to SHx. As a consequence the voltage at SHx can rise up to 0,6V typ. before it gets discharged through the resistor. | P_12.1.10 |
| Effective discharge RDSON | R_{ONCCP} | - | 9 | 12 | Oh m | 50mA forced into Gx, Sx grounded; $I_{\text{DISCHARGE}}=63_{\text{D}}$; $V_{\text{VCP}}=V_{\text{VSD}}+14.0\text{V}$; $V_{\text{VSD}}=13.5\text{V}$ | P_12.1.50 |
| Input propagation time (LS on) | $t_{\text{P(ILN)min}}$ | - | 3 | 8 | μs | ¹⁾ "ON"=1 to 25% of V_{Gxx1} ; $C_L=10\text{nF}$; $I_{\text{CHARGE}}=\text{min}$ | P_12.1.37 |
| Input propagation time (LS off) | $t_{\text{P(ILF)min}}$ | - | 3 | 8 | μs | ¹⁾ "ON"=0 to 75% of V_{Gxx1} ; $C_L=10\text{nF}$; $I_{\text{DISCHARGE}}=\text{min}$ | P_12.1.38 |
| Input propagation time (HS on) | $t_{\text{P(IHN)min}}$ | - | 3 | 8 | μs | ¹⁾ "ON"=1 to 25% of V_{Gxx1} ; $C_L=10\text{nF}$; $I_{\text{CHARGE}}=\text{min}$ | P_12.1.39 |
| Input propagation time (HS off) | $t_{\text{P(IHF)min}}$ | - | 3 | 8 | μs | ¹⁾ "ON"=0 to 75% of V_{Gxx1} ; $C_L=10\text{nF}$; $I_{\text{DISCHARGE}}=\text{min}$ | P_12.1.40 |
| Input propagation time (LS on) | $t_{\text{P(ILN)max}}$ | - | 200 | 350 | ns | "ON"=1 to 25% of V_{Gxx1} ; $C_L=10\text{nF}$; $I_{\text{CHARGE}}=\text{max}$ | P_12.1.26 |
| Input propagation time (LS off) | $t_{\text{P(ILF)max}}$ | - | 200 | 300 | ns | "ON"=0 to 75% of V_{Gxx1} ; $C_L=10\text{nF}$; $I_{\text{DISCHARGE}}=\text{max}$ | P_12.1.27 |
| Input propagation time (HS on) | $t_{\text{P(IHN)max}}$ | - | 200 | 350 | ns | "ON"=1 to 25% of V_{Gxx1} ; $C_L=10\text{nF}$; $I_{\text{CHARGE}}=\text{max}$ | P_12.1.28 |

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Table 72 MOSFET Driver Output (cont'd)

$V_S = 4.4\text{ V to }28\text{ V}$, $V_{SD} = 5.4\text{ V to }29\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin
(unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|--|---------------------|--------|------|------|------|--|-----------|
| | | Min. | Typ. | Max. | | | |
| Input propagation time (HS off) | $t_{P(IHF)max}$ | - | 200 | 300 | ns | "ON"=0 to 75% of V_{Gxx1} ; $C_L=10\text{nF}$; $I_{DISCHARGE}=\text{max}$ | P_12.1.29 |
| Absolute input propagation time difference between propagation times for all LSx (LSx on) | $t_{Pon(diff)LSx}$ | - | - | 100 | ns | "ON"=1 to 25% of V_{Gxx1} ; $C_L=10\text{nF}$; $I_{CHARGE}=\text{max}$ | P_12.1.30 |
| Absolute input propagation time difference between propagation times for all LSx (LSx off) | $t_{Poff(diff)LSx}$ | - | - | 100 | ns | "ON"=0 to 75% of V_{Gxx1} ; $C_L=10\text{nF}$; $I_{CHARGE}=\text{max}$ | P_12.1.41 |
| Absolute input propagation time difference between propagation times for all HSx (HSx on) | $t_{Pon(diff)HSx}$ | - | - | 100 | ns | "ON"=1 to 25% of V_{Gxx1} ; $C_L=10\text{nF}$; $I_{CHARGE}=\text{max}$ | P_12.1.42 |
| Absolute input propagation time difference between propagation times for all HSx (HSx off) | $t_{Poff(diff)HSx}$ | - | - | 100 | ns | "ON"=0 to 75% of V_{Gxx1} ; $C_L=10\text{nF}$; $I_{CHARGE}=\text{max}$ | P_12.1.43 |

- 1) Not subject to production test, specified by design
- 2) The condition $I_{CP} = 6\text{ mA}$ emulates H-Bridge Drive with 2 MOSFET switching at 25 kHz and $C_L = 10\text{ nF}$.
- 3) This resistance is connected through a diode between SHx and GHx to ground.

Table 73 Charge-Discharge Current Timing Characteristics

$V_S = 4.4\text{ V to }28\text{ V}$, $V_{SD} = 5.4\text{ V to }29\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin
(unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|-------------------------------------|----------------|--------|------|------|------|---|-----------|
| | | Min. | Typ. | Max. | | | |
| Charge current delay time | $t_{dly(on)}$ | - | 35 | 90 | ns | ¹⁾ from "ON"=1 to 20% of I_{chgX} ($x=0\dots63$); $C_L=10\text{nF}$ | P_12.1.63 |
| Charge current rise time | $t_{rise(on)}$ | - | 35 | 70 | ns | ¹⁾ from 20% of I_{chgX} to $I_{chgX,min}$ ($x=0\dots63$); $C_L=10\text{nF}$ | P_12.1.64 |
| Gate Source Voltage Saturation Time | $t_{sat(on)}$ | - | 50 | 100 | ns | ¹⁾ from $V_{GS}=V_{GS(on)}$ to $V_{Gxy,min}$; $C_L=10\text{nF}$; $I_{CHARGE}=63$ | P_12.1.68 |

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Table 73 Charge-Discharge Current Timing Characteristics (cont'd)

$V_S = 4.4\text{ V to }28\text{ V}$, $V_{SD} = 5.4\text{ V to }29\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin
(unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|--|-------------------------------|--------|------|------|------|--|-----------|
| | | Min. | Typ. | Max. | | | |
| Charge current settling time - sequencer mode | $t_{\text{set_chg(seq)}}$ | - | - | 150 | ns | ^{2) 1)} from any $I_{\text{CHARGE}(n)}$ to $I_{\text{CHARGE}(n+1)} = 0_D$ or 63_D ; $C_L=10\text{nF}$ | P_12.1.69 |
| Discharge current settling time - sequencer mode | $t_{\text{set_dischg(seq)}}$ | - | - | 75 | ns | ^{3) 1)} from any $I_{\text{DISCHARGE}(n)}$ to $I_{\text{DISCHARGE}(n+1)} = 0_D$ or 63_D ; $C_L=10\text{nF}$ | P_12.1.70 |
| Discharge current delay time | $t_{\text{dly(off)}}$ | - | 25 | 80 | ns | ¹⁾ from "ON"=0 to 20% of $I_{\text{dischg}x}$ ($x=0\dots63$); $C_L=10\text{nF}$ | P_12.1.71 |
| Discharge current rise time | $t_{\text{rise(off)}}$ | - | 25 | 50 | ns | ¹⁾ from 20% of $I_{\text{dischg}x}$ to $I_{\text{dischg}x,\text{min}}$ ($x=0\dots63$); $C_L=10\text{nF}$ | P_12.1.72 |

1) Not subject to production test, specified by design

2) $I_{\text{CHARGE}(n)}$ and $I_{\text{CHARGE}(n+1)}$ are consecutive gate charge current set points in sequencer mode.

3) $I_{\text{DISCHARGE}(n)}$ and $I_{\text{DISCHARGE}(n+1)}$ are consecutive gate discharge current set points in sequencer mode.

Table 74 Timing Measurement Comparators

$V_S = 4.4\text{ V to }28\text{ V}$, $V_{SD} = 5.4\text{ V to }29\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin
(unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|-------------------------|------------------------|------|----------------------|------|------------------------|-----------|
| | | Min. | Typ. | Max. | | | |
| Low-side timing measurement comparator threshold | $V_{\text{SH}(low)}$ | 2 | - | 2.5 | V | | P_12.1.73 |
| High-side timing measurement comparator threshold | $V_{\text{SH}(high)}$ | $V_{SD} - 2.5\text{V}$ | - | $V_{SD} - 2\text{V}$ | V | | P_12.1.74 |
| Delay of low-side timing measurement comparator | $t_{\text{cdly}(low)}$ | 5 | - | 20 | ns | | P_12.1.75 |
| Delay of high-side timing measurement comparator | $t_{\text{cdly}(high)}$ | 5 | - | 25 | ns | | P_12.1.76 |

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Table 75 Drain source monitoring

$V_S = 4.4\text{ V to }28\text{ V}$, $V_{SD} = 5.4\text{ V to }29\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin
(unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|-----------------------------------|----------------|--------|-------|-------|------|---|------------|
| | | Min. | Typ. | Max. | | | |
| Drain source monitoring threshold | $V_{DSMONVTH}$ | 0.11 | 0.145 | 0.178 | V | BDRV_CTRL3.DSMONVTH<2:0>=000 _B | P_12.1.146 |
| | | 2 | | | | | |
| | | 0.22 | 0.27 | 0.311 | V | BDRV_CTRL3.DSMONVTH<2:0>=001 _B | P_12.1.105 |
| | | 9 | | | | | |
| | | 0.42 | 0.5 | 0.575 | V | BDRV_CTRL3.DSMONVTH<2:0>=010 _B | P_12.1.106 |
| | | 5 | | | | | |
| | | 0.63 | 0.75 | 0.863 | V | BDRV_CTRL3.DSMONVTH<2:0>=011 _B | P_12.1.107 |
| | | 7 | | | | | |
| | | 0.85 | 1.00 | 1.15 | V | BDRV_CTRL3.DSMONVTH<2:0>=100 _B | P_12.1.108 |
| | | 1.06 | 1.25 | 1.44 | V | BDRV_CTRL3.DSMONVTH<2:0>=101 _B | P_12.1.109 |
| | | 1.27 | 1.5 | 1.73 | V | BDRV_CTRL3.DSMONVTH<2:0>=110 _B | P_12.1.110 |
| | | 1.48 | 1.75 | 2.02 | V | BDRV_CTRL3.DSMONVTH<2:0>=111 _B | P_12.1.111 |

Table 76 Open load diagnosis currents

$V_S = 4.4\text{ V to }28\text{ V}$, $V_{SD} = 5.4\text{ V to }29\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin
(unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|------------------|--------|------|------|---------------|--|------------|
| | | Min. | Typ. | Max. | | | |
| Pull-Up diagnosis current | I_{PUDiag} | -700 | - | -300 | μA | $I_{DISCHARGE}=0$; $V_{SD} \geq 6.4\text{V}$; $V_{SHX}=5\text{V}$; $V_S \geq 5.4\text{V}$ | P_12.1.147 |
| Pull-Down diagnosis current | I_{PDDiag} | 800 | - | 1450 | μA | $I_{DISCHARGE}=0$; $V_{SD} \geq 6.4\text{V}$; $V_{SHX}=5\text{V}$; $V_S \geq 5.4\text{V}$ | P_12.1.148 |
| Effective Pull-Down diagnosis current overdrive | I_{PDDiag_OD} | 200 | - | - | μA | $I_{DISCHARGE}=0$; $V_{SD} \geq 6.4\text{V}$; $V_{SHX}=5\text{V}$; $V_S \geq 5.4\text{V}$ | P_12.1.100 |

Electrical Characteristics

Table 77 Charge pump

$V_S = 4.4\text{ V to }28\text{ V}$, $V_{SD} = 5.4\text{ V to }29\text{ V}$, $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin
(unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|--|-----------------|--------|------|------|---------------|---|------------|
| | | Min. | Typ. | Max. | | | |
| Output voltage VCP vs. VSD | V_{CPmin1} | 7.7 | - | 10.1 | V | ¹⁾ Bridge Driver enabled but not ON; $C_{CP1}=220\text{nF}$; $C_{CP2}=220\text{nF}$; $100\mu\text{A} \leq I_{CP} \leq 6\text{mA}$; $V_{SD}=5.4\text{V}$; $f_{CP}=250\text{kHz}$ | P_12.1.53 |
| Single-Stage Mode Output voltage VCP vs. VSD | $V_{CPsingle}$ | 10.5 | - | 12.5 | V | ¹⁾ Bridge Driver enabled but not ON, Charge Pump in single-stage mode; $C_{CP1}=220\text{nF}$; $C_{CP2}=220\text{nF}$; $100\mu\text{A} \leq I_{CP} \leq 6\text{mA}$; $V_{SD}=13.5\text{V}$; $f_{CP}=250\text{kHz}$ | P_12.1.101 |
| Regulated output voltage VCP vs. VSD | V_{CP} | 11.8 | 14.8 | 16.8 | V | ¹⁾ Bridge Driver enabled but not ON; $C_{CP1}=220\text{nF}$; $C_{CP2}=220\text{nF}$; $I_{CP}=6\text{mA}$; $V_{SD} \geq 7.4\text{V}$; $f_{CP}=250\text{kHz}$ | P_12.1.49 |
| Regulated output voltage VCP vs. VSD | V_{CP9V} | 7.4 | 9.4 | 11.4 | V | ¹⁾ Bridge Driver enabled but not ON; $C_{CP1}=220\text{nF}$; $C_{CP2}=220\text{nF}$; $I_{CP}=6\text{mA}$; $V_{SD} \geq 7.4\text{V}$; $f_{CP}=250\text{kHz}$; $V_{CP9V_SET}=1$ | P_12.1.98 |
| Turn ON Time | t_{ON_VCP} | 27 | - | 90 | μs | ^{2) 1) 3)} from CPCLK_EN='1' to 25% of V_{CP} ; $C_{CP1}=220\text{nF}$; $C_{CP2}=220\text{nF}$; $C_{VCP}=470\text{nF}$; $V_{SD} \geq 7.4\text{V}$; $f_{CP}=250\text{kHz}$ | P_12.1.59 |
| Rise time | t_{rise_VCP} | 55 | - | 130 | μs | ^{2) 1) 3)} from 25% to 75% of V_{CP} ; $C_{CP1}=220\text{nF}$; $C_{CP2}=220\text{nF}$; $C_{VCP}=470\text{nF}$; $V_{SD} \geq 7.4\text{V}$; $f_{CP}=250\text{kHz}$ | P_12.1.60 |

1) $I_{chg} = 63\text{d}$, $I_{dischg} = 63\text{d}$, BDRV_CTRL3.DSMONVTH<2:0>=111B

2) This time applies when bit DRV_CP_CLK_CTRL.CPCLK_EN is set

3) Not subject to production test, specified by design

Abbreviations

30 Abbreviations

The following acronyms and terms are used within this document. List see in [Table 78](#).

Table 78 Acronyms

| Acronyms | Name |
|----------|---|
| AHB | Arm® Advanced High-Performance Bus |
| CCU6 | Capture Compare Unit 6 |
| CGU | Clock Generation Unit |
| CLKMU | Clock Management Unit |
| CMU | Cyclic Management Unit |
| DPP | Data Post Processing |
| ECC | Error Correction Code |
| EEPROM | Electrically Erasable Programmable Read Only Memory |
| GPIO | General Purpose Input Output |
| HV | High Voltage |
| ICU | Interrupt Control Unit |
| LDO | Low DropOut voltage regulator |
| LIN | Local Interconnect Network |
| LSB | Least Significant Bit |
| LTI | Lead Tip Inspection |
| LV | Low Voltage |
| MCU | Memory Control Unit |
| MF | Measurement Functions |
| MPU | Memory Protection Unit |
| MRST | Master Receive / Slave Transmit, corresponds to MISO in SPI |
| MSB | Most Significant Bit |
| MTRSR | Master Transmit / Slave Receive, corresponds to MOSI in SPI |
| MU | Measurement Unit |
| NMI | Non Maskable Interrupt |
| NVIC | Nested Vector Interrupt Controller |
| OSC | Oscillator |
| OTP | One Time Programmable |
| PBA | Peripheral Bridge |
| PC | Program Counter |
| PCU | Power Control Unit |
| PD | Pull Down |
| PGU | Power supply Generation Unit |
| PLL | Phase Locked Loop |
| PMU | Power Management Unit |

Abbreviations
Table 78 Acronyms

| Acronyms | Name |
|-----------------|--|
| PPB | Private Peripheral Bus |
| PSW | Program Status Word |
| PU | Pull Up |
| PWM | Pulse Width Modulation |
| RAM | Random Access Memory |
| RCU | Reset Control Unit |
| rfu | reserved for future use |
| RMU | Reset Management Unit |
| ROM | Read Only Memory |
| SCU | System Control Unit |
| SOW | Short Open Window (for WDT1) |
| SPI | Serial Peripheral Interface |
| SSC | Synchronous Serial Channel |
| SWD | Arm® Serial Wire Debug |
| TCCR | Temperature Compensation Control Register |
| TMS | Test Mode Select |
| TSD | Thermal Shut Down |
| UART | Universal Asynchronous Receiver Transmitter |
| VBG | Voltage reference Band Gap |
| VCO | Voltage Controlled Oscillator |
| WDT | Watchdog timer in SCU-DM (System Control Unit - Digital Modules) |
| WDT1 | Watchdog timer in SCU-PM (System Control Unit - Power Modules) |
| WMU | Wake-up Management Unit |
| 100TP | 100 Times Programmable |

Revision History**31 Revision History**

| Revision | Date | Changes |
|-----------------|-------------|-----------------------------|
| 1.0 | 2019-07-26 | Initial version for AD-Step |

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Edition 2019-07-26

Published by

Infineon Technologies AG

81726 Munich, Germany

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Document reference

Z8F65189480

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