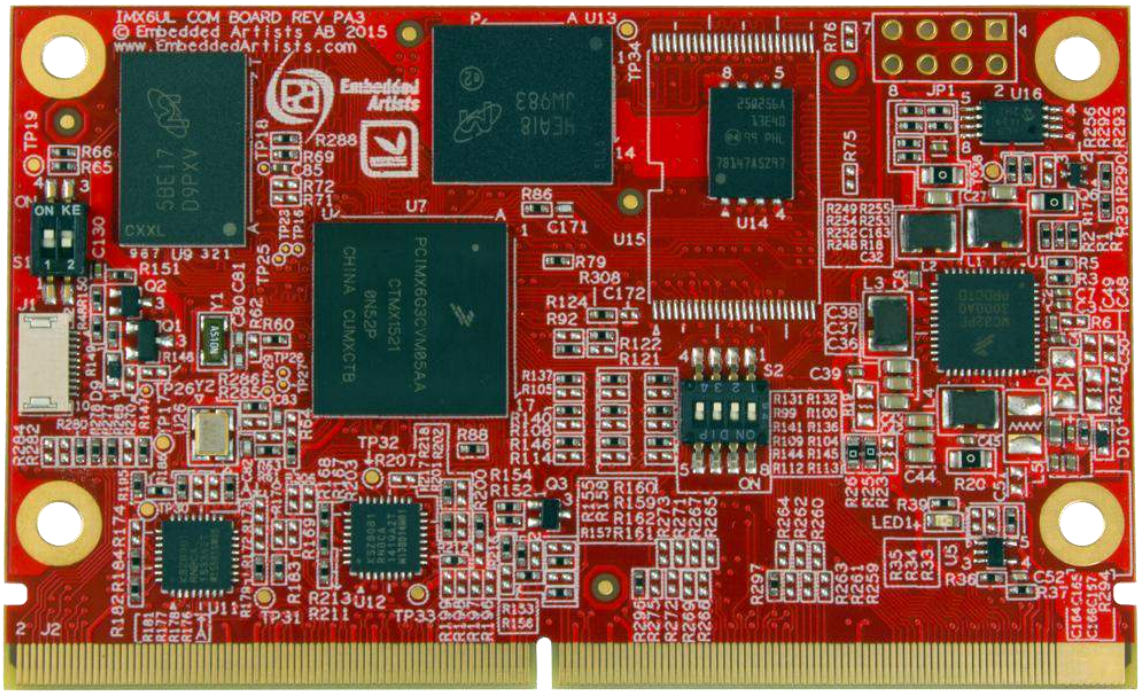
iMX6 UltraLite COM Board Datasheet



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1 Document Revision History

Revision	*Date*	*Description*
PA1	2016-08-04	First version.
PA2	2017-07-31	Added information about boot pins.
PA3	2018-03-07	Added current consumption information.

2 Introduction

This document is a datasheet that specifies and describes the *iMX6 UltraLite COM Board* mainly from a hardware point of view. Some basic software related issues are also addressed, like booting and functional verification, but there are separate software development manuals that should also be consulted.

2.1 Hardware

The *iMX6 UltraLite COM Board* is a Computer-on-Module (COM) based on NXP's ARM Cortex-A7 i.MX 6UltraLite System-on-Chip (SoC) application processor. The board provides a quick and easy solution for implementing a high-performance, low-power ARM Cortex-A7 based design. The Cortex-A7 cores runs at up to 528 MHz.

The *iMX6 UltraLite COM Board* delivers high computational and graphical performance at very low power consumption. The on-board PMIC, supporting DVFS (Dynamic Voltage and Frequency Scaling), together with a DDR3L memory sub-system reduce the power consumption to a minimum.

The SoC is part of the scalable i.MX 6 product family. There is a range of i.MX 6 (and i.MX 7) COM Boards from Embedded Artists with single, dual and UltraLite Cortex-A9/A7 cores, with or without a heterogeneous Cortex-M4 core. All boards share the same basic pinning for maximum flexibility and performance scalability.

The *iMX6 UltraLite COM Board* has a very small form factor and shields the user from a lot of complexity of designing a high performance system. It is a robust and proven design that allows the user to focus the product development, shorten time to market and minimize the development risk.

The *iMX6 UltraLite COM Board* targets a wide range of applications, such as:

- Industrial automation
- HVAC Building and Control Systems
- Smart Grid and Smart Metering
- HMI/GUI solutions
- Smart Toll Systems
- Connected vending machines
- Digital signage
- Point-of-Sale (POS) applications
- Data acquisition
- Communication gateway solutions
- Connected real-time systems
- Portable systems
- ...and much more

The picture below illustrates the block diagram of the *iMX6 UltraLite COM Board*.

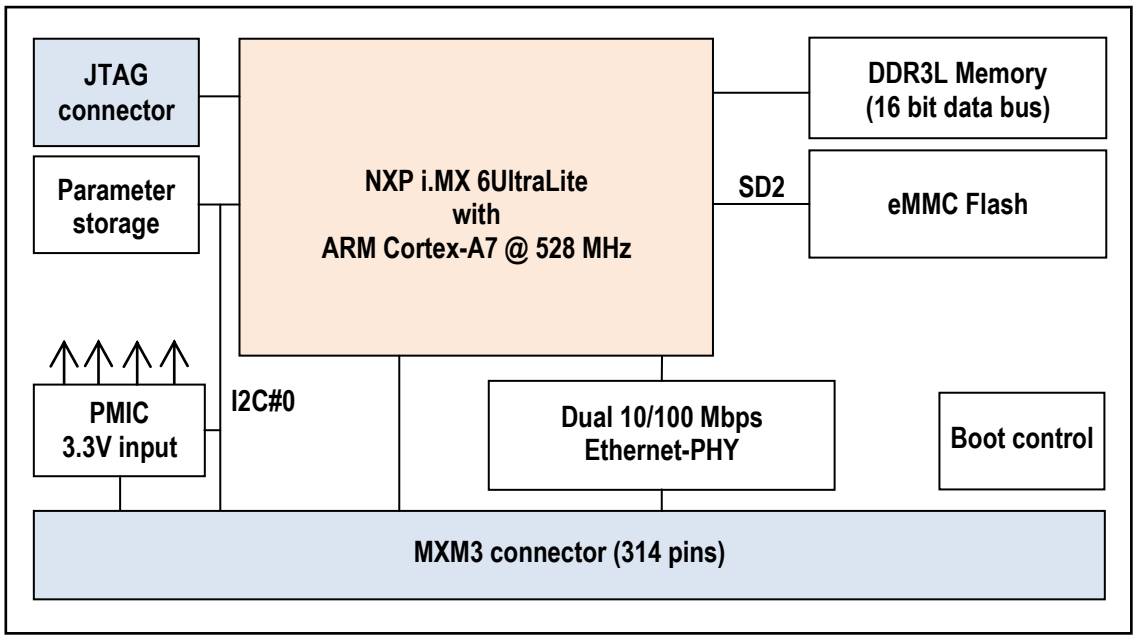


Figure 1 – iMX6 UltraLite COM Board Block Diagram

The *iMX6 UltraLite COM Board* pin assignment focus on direct connection to (carrier board) interface connectors and minimize trace and layer crossing. This is important for high speed, serial interfaces with impedance controlled differential pairs. As a result, carrier boards can be designed with few routing layers. In many cases, a four layer pcb is enough to implement advanced and compact carrier boards. The pin assignment is common for the *iMX6/7 COM Boards* from Embedded Artists and the general, so called, *EACOM Board Specification* is found in separate document.

2.2 Software

The *iMX6 UltraLite COM Board* has Board Support Packages (BSPs) for Embedded Linux. Precompiled images are available. Embedded Artists works with partners that can provide support for other operating systems (OS). For more information contact Embedded Artists support.

This document has a hardware focus and does not cover software development. See other documents related to the *iMX6 UltraLite COM Board* for more information about software development.

2.3 Features and Functionality

The i.MX 6UltraLite is a powerful SoC. The full specification can be found in NXP's *iMX6 UltraLite Datasheet* and *iMX6UltraLite Reference Manual*. The table below lists the main features and functions of the *iMX6 UltraLite COM Board* - which represents Embedded Artists integration of the i.MX 6UltraLite SoC. Due to pin configuration some functions and interfaces of the i.MX 6UltraLite are not available on the *iMX6 UltraLite COM Board*.

Group	Feature	iMX6 UltraLite COM Board Commercial temp. range
CPU	NXP SoC	MCIMX6G2CVM05AA
	CPU Core	Cortex-A7
	L1 Instruction cache	32 KByte
	L1 Data cache	32 KByte
	Unified I/D L2 Cache	128 KByte

	NEON SIMD media accelerator	✓
	Maximum CPU frequency	528 MHz
Security Functions	ARM TrustZone	✓
	Advanced High Assurance Boot	✓
	Cryptographic Acceleration and Assurance Module	✓
	Secure Non-Volatile Storage, incl. Secure Real-Time Clock	✓
	System JTAG controller	✓
Memory	DDR3L RAM Size	0.5 GByte
	DDR3L RAM Speed	400 MT/s
	DDR3L RAM Memory Width	16 bit
	eMMC NAND Flash (8 bit)	4 GByte
Graphical Processing	PiXel Processing Pipeline (PXP)	✓
Graphical Output	RGB, 24-bit parallel interface	✓
Graphical Input	CMOS sensor interface (camera), digital 24-bit parallel interface	✓
Interfaces (all functions are not available at the same time)	Dual 10/100 Mbps Gigabit Ethernet controllers	✓ with on-board PHYs
	12-bit ADC	✓
	2x USB OTG 2.0 ports	✓
	1x SD/MMC 5	✓ SD2 interface used on-board
	4x SPI, 8x UART, 4x I²C, 3x I²S/SSI, S/PDIF TX/RX	✓
	Dual FlexCAN, CAN bus 2.0B	✓
Other	PMIC (MMPF3000) supporting DVFS techniques for low power modes	✓
	On-board boot configuration to select either eMMC or USB OTG boot source	✓
	E2PROM storing board information including Ethernet MAC addresses and memory bus setup parameters	✓
	i.MX6 UltraLite on-chip RTC	✓
	On-board watchdog functionality	✓

2.4 Interface Overview

The table below lists the interfaces that are specified in the EACOM specification (see separate document for details) and what is supported by the *iMX6 UltraLite COM board*.

Interface	EACOM specification	iMX6 UltraLite COM Board	Note
UART	3 ports (two 4 wire and one 2 wire)	3 ports	More ports available as alternative pin functions
SPI	2 ports	1 port	More ports available as alternative pin functions
I2C	3 ports	2 ports	More ports available as alternative pin functions
SD/MMC	2 ports (one 4 databits and one 8 databits)	1 port	
Parallel LCD	24 databits and CLK/HS/VS/DE	Full support	
LCD support	LCD power ctrl, Backlight power/contrast control, touch panel ctrl (RST and IRQ)	Full support	1 PWM and 4 GPIO
LVDS LCD	2 ports (18/24 bit LVDS data)	-	
HDMI (TDMS)		-	
Parallel Camera		1 port	
Serial Camera	CSI, 4 lane	-	
Gigabit Ethernet	2 ports	2 ports	10/100Mbps capable
PCIe	1 post, 1 lane	-	
SATA	1 port	-	
USB	1 USB3.0 OTG 1 USB3.0 Host 1 USB2.0 Host	2 USB2.0 OTG	
SPDIF	1 TX/RX port	1 output port	Only output
CAN	2 ports	2 ports	
I2S/SSI/AC97	1 port (4 wire synchronous plus MCLK)	1 port	Shared pins are used. More ports available as alternative pin functions.
Analog audio	Stereo output	-	
GPIO	9 pins	5 pins	More GPIO pins are available as alternative pin functions.
PWM	1 pin	1 pin	More pins are available as alternative pin functions.
ADC	8 inputs	4 inputs	Shared pins are used.

Type specific	39 pins	7 pins	All type specific pins connected to i.MX 6UltraLite pins.
Power	10 VIN, VBAT and 47 GND	10 VIN, VBAT and 47 GND	About 15% of the pins are ground pins.

2.5 Reference Documents

The following documents are important reference documents and should be consulted when integrating the *iMX6 UltraLite COM board*:

- EACOM Board Specification
- EACOM Board Integration Manual

The following NXP documents are also important reference documents and should be consulted for functional details:

- IMX6ULCEC, i.MX 6UltraLite Applications Processors for Consumer Products - Data Sheet, latest revision
- IMX6ULIEC, i.MX 6UltraLite Applications Processors for Industrial Products - Data Sheet, latest version
- IMX6ULRM, i.MX 6UltraLite Applications Processor Reference Manual, latest revision
- IMX6ULCE, Chip Errata for the i.MX 6UltraLite, latest revision
  Note: It is the user's responsibility to make sure all errata published by the manufacturer are taken note of. The manufacturer's advice should be followed.
- AN5170, i.MX 6UltraLite Power Consumption Measurement, latest revision
- AN5198, i.MX 6UltraLite Product Usage Lifetime Estimates, latest revision

The following documents are external industry standard reference documents and should also be consulted when applicable:

- eMMC (Embedded Multi-Media Card) the eMMC electrical standard is defined by JEDEC JESD84-B45 and the mechanical standard by JESD84-C44 (www.jedec.org)
- The I2C Specification, Version 2.1, January 2000, Philips Semiconductor (now NXP) (www.nxp.com)
- I2S Bus Specification, Feb. 1986 and Revised June 5, 1996, Philips Semiconductor (now NXP) (www.nxp.com)
- JTAG (Joint Test Action Group) defined by IEEE 1149.1-2001 - IEEE Standard Test Access Port and Boundary Scan Architecture (www.ieee.org)
- MXM3 Graphics Module Mobile PCI Express Module Electromechanical Specification, Version 3.0, Revision 1.1, © 2009 NVIDIA Corporation (www.mxm-sig.org)
- SD Specifications Part 1 Physical Layer Simplified Specification, Version 3.01, May 18, 2010, © 2010 SD Group and SD Card Association (Secure Digital) (www.sdcard.org)
- SPDIF (aka S/PDIF) (Sony Philips Digital Interface) - IEC 60958-3

- SPI Bus – “Serial Peripheral Interface” – de-facto serial interface standard defined by Motorola. A good description may be found on Wikipedia (http://en.wikipedia.org/wiki/Serial_Peripheral_Interface_Bus)
- USB Specifications (www.usb.org)

3 EACOM Board Pinning

Embedded Artists has defined the EACOM board standard that is based on the SMARC form factor; module size 82 x 50 mm. Note that pinning is different from the SMARC standard. See the *EACOM Board specification* document for details and background information. Hereafter this standard will be referred to as **EACOM**.

The carrier board connector has 314 pins with 0.5 mm pitch and the EACOM board is inserted in a right angle (R/A) style. The connector is originally defined for use with MXM3 graphics cards. There are multiple sources for carrier board (MXM3) connectors due to the popular standard. The signal integrity is excellent and suitable for data rates up to 5 GHz.

Overall assembly height of the EACOM board/Carrier board connector can be as low as 6 mm. There are different stack height options available, including 2.7 mm (resulting in overall 6 mm height), 5 mm and 8 mm.

3.1 Pin Numbering

The figures below show the pin numbering for EACOM. Top side edge fingers are numbered P1-P156. Bottom side edge fingers are numbered S1-S158. There is an alternative pin numbering that follows the MXM3 standard with even numbers on the bottom and odd numbers on the top. This numbering is from 1-321, with 7 numbers/pins (150-156) removed due to the keying.

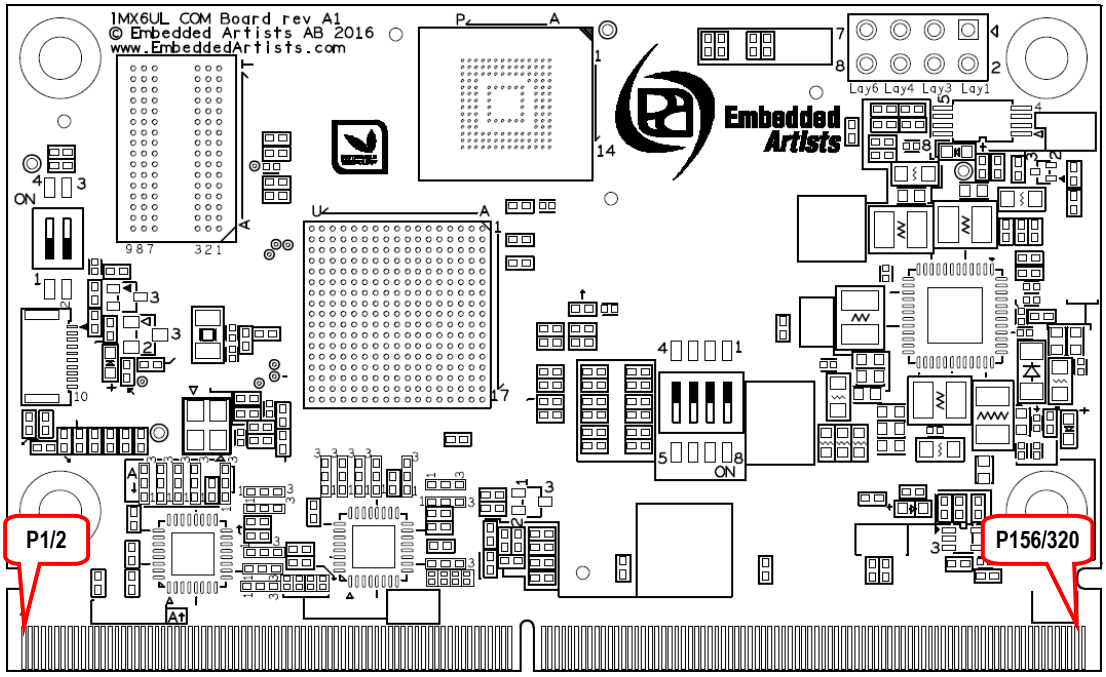


Figure 2 – EACOM Board Pin Numbering, Top Side

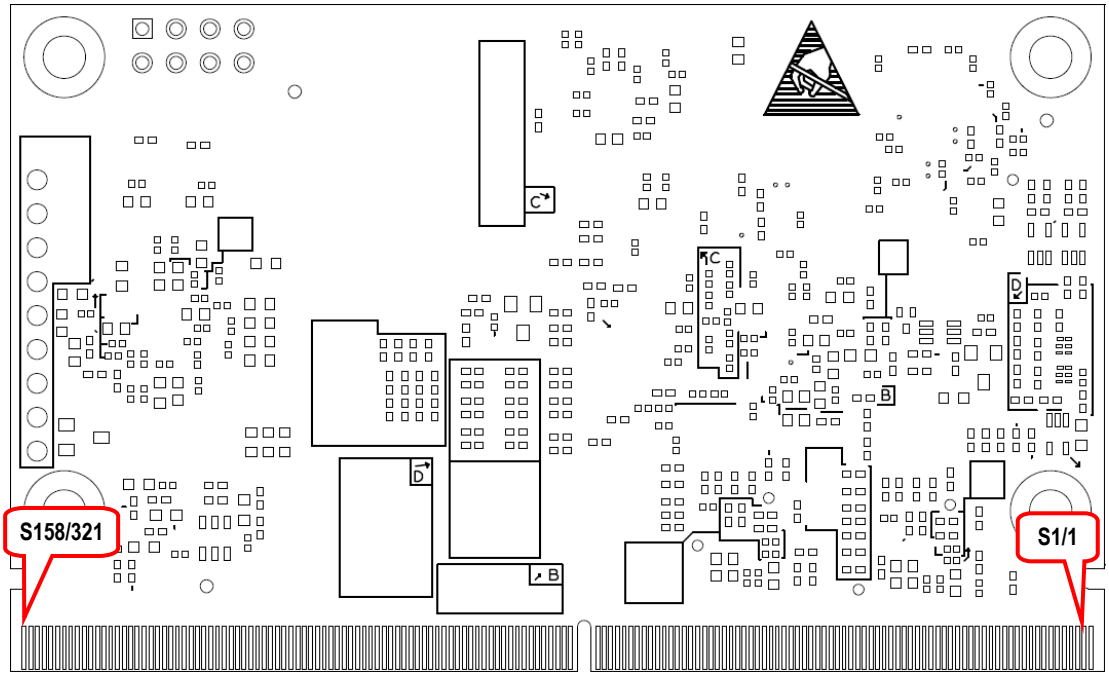


Figure 3 – EACOM Board Pin Numbering, Bottom Side

3.2 Pin Assignment

This section describes the pin assignment of the board, with the following columns:

Pin number	**Px** are top side edge fingers. **Sx** are bottom side edge fingers. An alternative, consecutive, numbering is also shown with odd numbers on the top and even numbers on the bottom side.
EACOM Board	Describe the typical usage of the pin according to EACOM. This pin usage should be followed to get compatibility between different EACOM boards. If this is not needed, then any of the alternative functions on the pin can also be used.
i.MX 6UltraLite Ball Name	The name of the ball of the i.MX 6UltraLite SoC (or other component on the EACOM board) that is connected to this pin.
Notes	When relevant, the preferred pin function is listed.

There are 47 ground pins, which equal to about 15%, and 10 input voltage supply pins.

Note that some pins are EACOM board *type specific*, meaning that these pins might not be compatible with other EACOM boards. Using these may result in lost compatibility between EACOM boards, but not always. Check details between EACOM boards of interest.

The table below lists the top side pins, P1-P156, odd numbers.

Top Side Pin Number	EACOM Board	i.MX 6UltraLite Ball Name	Alternative pin functions?	Notes
P1/2	GPIO6	SNVS_TAMPER1	Yes	GPIO6 controlled by alternative pin function GPIO5_IO01
P2/4	GPIO5			
P3/6	GPIO4	GPIO1_IO03	Yes	GPIO4 controlled by alternative pin function GPIO1_IO03 **Note:** Signal also connected to AIN2
P4/8	GPIO3	GPIO1_IO09	Yes	GPIO3 controlled by alternative pin function GPIO1_IO09

P5/10	SD_D1	SD1_DATA1	Yes	
P6/12	SD_D0	SD1_DATA0	Yes	
P7/14	SD_CLK	SD1_CLK	Yes	
P8/16	SD_CMD	SD1_CMD	Yes	
P9/18	SD_D3	SD1_DATA3	Yes	
P10/20	SD_D2	SD1_DATA2	Yes	
P11/22	SD_VCC			Supply voltage for SD interface (3.3V). Should only supply the SD interface.
P12/24	MMC_D1			
P13/26	MMC_D0			
P14/28	MMC_D7			
P15/30	MMC_D6			
P16/32	MMC_CLK			
P17/34	MMC_D5			
P18/36	MMC_CMD			
P19/38	MMC_D4			
P20/40	MMC_D3			
P21/42	MMC_D2			
P22/44	GND			
P23/46	HDMI_TXC_N			
P24/48	HDMI_TXC_P			
P25/50	GND			
P26/52	HDMI_TXD0_N			
P27/54	HDMI_TXD0_P			
P28/56	HDMI_HPD			
P29/58	HDMI_TXD1_N			
P30/60	HDMI_TXD1_P			
P31/62	GND			
P32/64	HDMI_TXD2_N			
P33/66	HDMI_TXD2_P			
P34/68	HDMI_CEC			
P35/70	GND			
P36/72	ETH1_MD1_P			Connects to Ethernet-PHY KSZ8081 #1, pin 5
P37/74	ETH1_MD1_N			Connects to Ethernet-PHY KSZ8081 #1, pin 4
P38/76	GND			
P39/78	ETH1_MD0_P			Connects to Ethernet-PHY KSZ8081 #1, pin 7
P40/80	ETH1_MD0_N			Connects to Ethernet-PHY KSZ8081 #1, pin 6
P41/82	ETH1_LINK1000			
P42/84	ETH1_ACT			Connects to Ethernet-PHY KSZ8081 #1, pin 30
P43/86	ETH1_LINK			Connects to Ethernet-PHY KSZ8081 #1, pin 31
P44/88	ETH1_MD3_N			
P45/90	ETH1_MD3_P			

P46/92	GND			
P47/94	ETH1_MD2_N			
P48/96	ETH1_MD2_P			
P49/98	GND			
P50/100	ETH2_MD1_P			Connects to Ethernet-PHY KSZ8081 #2, pin 5
P51/102	ETH2_MD1_N			Connects to Ethernet-PHY KSZ8081 #2, pin 4
P52/104	GND			
P53/106	ETH2_MD0_P			Connects to Ethernet-PHY KSZ8081 #2, pin 7
P54/108	ETH2_MD0_N			Connects to Ethernet-PHY KSZ8081 #2, pin 6
P55/110	ETH2_LINK1000			
P56/112	ETH2_ACT			Connects to Ethernet-PHY KSZ8081 #2, pin 30
P57/114	ETH2_LINK			Connects to Ethernet-PHY KSZ8081 #2, pin 31
P58/116	ETH2_MD3_N			
P59/118	ETH2_MD3_P			
P60/120	GND			
P61/122	ETH2_MD2_N			
P62/124	ETH2_MD2_P			
P63/126	GND			
P64/128	USB_O1_DN	USB_OTG1_DN	No	
P65/130	USB_O1_DP	USB_OTG1_DP	No	
P66/132	USB_O1_OTG_ID	GPIO1_IO00	Yes	Controlled by alternative pin function USB_OTG1_ID
P67/134	USB_O1_SSTXN			USB OTG port #1 on i.MX 6UltraLite does not support USB 3.0 so this pin is unconnected.
P68/136	USB_O1_SSTXP			USB OTG port #1 on i.MX 6UltraLite does not support USB 3.0 so this pin is unconnected.
P69/138	GND			
P70/140	USB_O1_SSRXN			USB OTG port #1 on i.MX 6UltraLite does not support USB 3.0 so this pin is unconnected.
P71/142	USB_O1_SSRXP			USB OTG port #1 on i.MX 6UltraLite does not support USB 3.0 so this pin is unconnected.
P72/144	USB_O1_VBUS	USB_OTG1_VBUS	No	
P73/146	USB_O1_PWR_EN	-	No	Connected to 4.7Kohm pull-up resistor to 3.3V, meaning that the power control for this USB interface is always on. Signal is also controlled by pin USB_O1_OTG_ID. If this pin is pulled high externally, this pin (USB_O1_PWR_EN) will be pulled low.
P74/148	USB_O1_OC	-	No	Pin is connected directly to pin USB_O1_PWR_EN. If signal is pulled low externally, pin USB_O1_PWR_EN will also be pulled low.
150	Non existing pin			
152	Non existing pin			
154	Non existing pin			
156	Non existing pin			
P75/158	USB_H1_PWR_EN	-	No	Connected to 4.7Kohm pull-up resistor to 3.3V, meaning that the power control for this USB interface is always on.
P76/160	USB_H1_OC	-	No	Pin is connected directly to pin USB_H1_PWR_EN. If signal is pulled low externally, pin USB_H1_PWR_EN will also be

				pulled low.
P77/162	GND			
P78/164	USB_H1_DN	USB_OTG2_DN	No	
P79/166	USB_H1_DP	USB_OTG2_DP	No	
P80/168	USB_H1_SSTXN			USB Host port #1 on i.MX 6UltraLite does not support USB 3.0 so this pin is unconnected.
P81/170	USB_H1_SSTXP			USB Host port #1 on i.MX 6UltraLite does not support USB 3.0 so this pin is unconnected.
P82/172	GND			
P83/174	USB_H1_SSRXN			USB Host port #1 on i.MX 6UltraLite does not support USB 3.0 so this pin is unconnected.
P84/176	USB_H1_SSRXP			USB Host port #1 on i.MX 6UltraLite does not support USB 3.0 so this pin is unconnected.
P85/178	USB_H1_VBUS	USB_OTG2_VBUS	No	
P86/180	USB_H2_PWR_EN	SNVS_TAMPER0	No	USB Host port #2 on i.MX 6UltraLite does not exist. Non-standard pin allocation. Pin carry signal SNVS_TAMPER, i.MX 6UltraLite ball R10.
P87/182	USB_H2_OC	ONOFF	No	USB Host port #2 on i.MX 6UltraLite does not exist. Non-standard pin allocation. Pin carry signal ONOFF, i.MX 6UltraLite ball R8.
P88/184	GND			
P89/186	USB_H2_DN	GPIO1_IO05	Yes	USB Host port #2 on i.MX 6UltraLite does not exist. Non-standard pin allocation. Note that pin GPIO1_IO05 function as signal SD1_VSELECT and is connected to SD_VSEL on PF3000 PMIC. The signal can be used if the SD1 interface is not used.
P90/188	USB_H2_DP			
P91/190	GND			
P92/192	COM board specific	(ENET1_TX_CLK)	(Yes)	**Note:** Only available if ENET1 not mounted.
P93/194	COM board specific	(ENET1_TXEN)	(Yes)	**Note:** Only available if ENET1 not mounted.
P94/196	COM board specific	(ENET1_TXD1)	(Yes)	**Note:** Only available if ENET1 not mounted.
P95/198	COM board specific	(ENET1_TXD0)	(Yes)	**Note:** Only available if ENET1 not mounted.
P96/200	COM board specific	(ENET1_RXER)	(Yes)	**Note:** Only available if ENET1 not mounted.
P97/202	COM board specific	(ENET1_CRS_DV)	(Yes)	**Note:** Only available if ENET1 not mounted.
P98/204	COM board specific	(ENET1_RXD1)	(Yes)	**Note:** Only available if ENET1 not mounted.
P99/206	COM board specific	(ENET1_RXD0)	(Yes)	**Note:** Only available if ENET1 not mounted.
P100/208	COM board specific	(GPIO1_IO07)	(Yes)	**Note:** Only available if ENET1 and ENET2 are not mounted
P101/210	COM board specific	(GPIO1_IO06)	(Yes)	**Note:** Only available if ENET1 and ENET2 are not mounted
P102/212	COM board specific	(ENET2_CRS_DV)	(Yes)	**Note:** Only available if ENET2 not mounted.
P103/214	COM board specific	(ENET2_RXER)	(Yes)	**Note:** Only available if ENET2 not mounted.
P104/216	COM board specific	(ENET2_RXD1)	(Yes)	**Note:** Only available if ENET2 not mounted.
P105/218	COM board specific	(ENET2_RXD0)	(Yes)	**Note:** Only available if ENET2 not mounted.
P106/220	COM board specific	(ENET2_TX_CLK)	(Yes)	**Note:** Only available if ENET2 not mounted.
P107/222	COM board specific	(ENET2_TXEN)	(Yes)	**Note:** Only available if ENET2 not mounted.
P108/224	COM board specific	(ENET2_TXD1)	(Yes)	**Note:** Only available if ENET2 not mounted.
P109/226	COM board specific	(ENET2_TXD0)	(Yes)	**Note:** Only available if ENET2 not mounted.

P110/228	COM board specific	BOOT_MODE1	Yes	This pin is sampled just after reset and determines the boot mode of the processor. This pin is normally pulled high by a 10K pull-up resistor internally on the board. It is left floating (pulled low by the i.MX6 UltraLite SoC) if pin E2PROM_WP is pulled low. This pin can be configured as GPIO5_IO12 and if so, make sure boot mode control is still valid.
P111/230	COM board specific	BOOT_MODE0	Yes	This pin is sampled just after reset and determines the boot mode of the processor. This pin is normally left floating (pulled low by the i.MX6 UltraLite SoC). It is pulled high by a 10K pull-up resistor if pin E2PROM_WP is pulled low. This pin can be configured as GPIO5_IO11 and if so, make sure boot mode control is still valid.
P112/232	COM board specific			
P113/234	COM board specific	NAND_WP	Yes	
P114/236	COM board specific			
P115/238	COM board specific			
P116/240	COM board specific			
P117/242	COM board specific			
P118/244	GND			
P119/246	SPI-B_SSEL			
P120/248	SPI-B_MOSI			
P121/250	SPI-B_MISO			
P122/252	SPI-B_CLK			
P123/254	SPI-A_SSEL	NAND_READY	Yes	Controlled by alternative pin function ECSPI3_SS0
P124/256	SPI-A_MOSI	NAND_CE1	Yes	Controlled by alternative pin function ECSPI3_MOSI
P125/258	SPI-A_MISO	NAND_CLE	Yes	Controlled by alternative pin function ECSPI3_MISO
P126/260	SPI-A_CLK	NAND_CE0	Yes	Controlled by alternative pin function ECSPI3_SCLK
P127/262	GND			
P128/264	UART-C_RXD	UART3_RX	Yes	Controlled by alternative pin function UART3_RX_DATA
P129/266	UART-C_TXD	UART3_TX	Yes	Controlled by alternative pin function UART3_TX_DATA
P130/268	UART-B_RXD	UART2_RX	Yes	Controlled by alternative pin function UART2_RX_DATA
P131/270	UART-B_CTS	UART2_CTS	Yes	Controlled by alternative pin function UART2_CTS_B **Note:** Signal also connected to CAN2_TX
P132/272	UART-B_RTS	UART2_RTS	Yes	Controlled by alternative pin function UART2_RTS_B **Note:** Signal also connected to CAN2_RX
P133/274	UART-B_TXD	UART2_TX	Yes	Controlled by alternative pin function UART2_TX_DATA
P134/276	UART-A_RXD	UART1_RX	Yes	Controlled by alternative pin function UART1_RX_DATA
P135/278	UART-A_CTS	UART1_CTS	Yes	Controlled by alternative pin function UART1_CTS_B
P136/280	UART-A_RTS	UART1_RTS	Yes	Controlled by alternative pin function UART1_RTS_B
P137/282	UART-A_TXD	UART1_TX	Yes	Controlled by alternative pin function UART1_TX_DATA
P138/284	PWM	GPIO1_IO08	Yes	Controlled by alternative pin function PWM1_OUT. **Note:** Signal also connected to BL_PWM
P139/286	GPIO2	GPIO1_IO02	Yes	GPIO2 controlled by alternative pin function GPIO1_IO02 **Note:** Signal also connected to DISP_PWR_EN and AIN1
P140/288	GPIO1	GPIO1_IO01	Yes	GPIO1 controlled by alternative pin function GPIO1_IO01

				Note: Signal also connected to BL_PWR_EN and AIN0
P141/290	PERI_PWR_EN	SNVS_TAMPER2	Yes	Enable signal (active high) for carrier board peripheral power supplies. More information about carrier board design can be found in *EACOM Board specification*.
P142/292	RESET_IN			Reset input, active low. Pull signal low to activate reset. No need to pull signal high externally.
P143/294	RESET_OUT			Reset (open drain) output, active low. Driven low during reset. 1.5K pull-up resistor to VIN.
P144/296	GND			
P145/298	VBAT			Supply voltage from coin cell battery for keeping PMIC and RTC functioning during standby.
P146/300	E2PROM_WP			Should be left open (will write protect the on-board parameter storage E2PROM), or connected to GND (will enable writes to the on-board parameter storage E2PROM AND place the i.MX 6UltraLite SoC in USB OTG boot mode after a power cycle).
P147/302	VIN			Main input voltage supply (3.3V)
P148/304	VIN			Main input voltage supply (3.3V)
P149/306	VIN			Main input voltage supply (3.3V)
P150/308	VIN			Main input voltage supply (3.3V)
P151/310	VIN			Main input voltage supply (3.3V)
P152/312	VIN			Main input voltage supply (3.3V)
P153/314	VIN			Main input voltage supply (3.3V)
P154/316	VIN			Main input voltage supply (3.3V)
P155/318	VIN			Main input voltage supply (3.3V)
P156/320	VIN			Main input voltage supply (3.3V)

The table below lists the bottom side pins, S1-S158, even numbers.

Bottom Side Pin Number	EACOM Board	i.MX 6UltraLite Ball Name	Alternative pin functions?	Notes
S1/1	MQS_RIGHT	JTAG_TDO	Yes	Controlled by alternative pin function MQS_RIGHT **Note:** Signals also connected to JTAG interface and signal AUDIO_TXFS
S2/3	MQS_LEFT	JTAG_TDI	Yes	Controlled by alternative pin function MQS_LEFT **Note:** Signals also connected to JTAG interface and signal AUDIO_TXC
S3/5	GND			
S4/7	AUDIO_TXFS	JTAG_TDO	Yes	Controlled by alternative pin function SAI2_TX_SYNC **Note:** Signals also connected to JTAG interface and signal MQS_RIGHT
S5/9	AUDIO_RXD	JTAG_TCK	Yes	Controlled by alternative pin function SAI2_RX_DATA **Note:** Signals also connected to JTAG interface
S6/11	AUDIO_TXC	JTAG_TDI	Yes	Controlled by alternative pin function SAI2_TX_BCLK **Note:** Signals also connected to JTAG interface and signal MQS_LEFT
S7/13	AUDIO_TXD	JTAG_TRST	Yes	Controlled by alternative pin function SAI2_TX_DATA **Note:** Signals also connected to JTAG interface
S8/15	AUDIO_MCLK	JTAG_TMS	Yes	Controlled by alternative pin function SAI2_MCLK

				Note: Signals also connected to JTAG interface
S9/17	GND			
S10/19	SPDIF_IN			
S11/21	SPDIF_OUT	JTAG_MOD	Yes	Controlled by alternative pin function SPDIF_OUT **Note:** Signals also connected to JTAG interface
S12/23	CAN2_TX	UART2_CTS	Yes	Controlled by alternative pin function CAN2_TX **Note:** Signals also connected to UART-B_CTS
S13/25	CAN2_RX	UART2_RTS	Yes	Controlled by alternative pin function CAN2_RX **Note:** Signals also connected to UART-B_RTS
S14/27	CAN1_TX	UART3_CTS	Yes	Controlled by alternative pin function CAN1_TX
S15/29	CAN1_RX	UART3_RTS	Yes	Controlled by alternative pin function CAN1_RX
S16/31	GND			
S17/33	LVDS1_D3_P			
S18/35	LVDS1_D3_N			
S19/37	GPIO9			
S20/39	LVDS1_D2_P			
S21/41	LVDS1_D2_N			
S22/43	GND			
S23/45	LVDS1_D1_P			
S24/47	LVDS1_D1_N			
S25/49	GND			
S26/51	LVDS1_D0_P			
S27/53	LVDS1_D0_N			
S28/55	GND			
S29/57	LVDS1_CLK_P			
S30/59	LVDS1_CLK_N			
S31/61	GND			
S32/63	LVDS0_D3_P			
S33/65	LVDS0_D3_N			
S34/67	GPIO8			
S35/69	LVDS0_D2_P			
S36/71	LVDS0_D2_N			
S37/73	GND			
S38/75	LVDS0_D1_P			
S39/77	LVDS0_D1_N			
S40/79	GND			
S41/81	LVDS0_D0_P			
S42/83	LVDS0_D0_N			
S43/85	GND			
S44/87	LVDS0_CLK_P			
S45/89	LVDS0_CLK_N			
S46/91	I2C-A_SDA	UART4_RX	Yes	Controlled by alternative pin function I2C1_SDA

S47/93	I2C-A_SCL	UART4_TX	Yes	Controlled by alternative pin function I2C1_SCL
S48/95	I2C-B_SDA	UART5_RX	Yes	Controlled by alternative pin function I2C2_SDA
S49/97	I2C-B_SCL	UART5_TX	Yes	Controlled by alternative pin function I2C2_SCL
S50/99	HDMI/I2C-C_SDA			
S51/101	HDMI/I2C-C_SCL			
S52/103	TP_RST	NAND_DQS	Yes	Controlled by alternative pin function GPIO4_IO16
S53/105	TP_IRQ	GPIO1_IO04	Yes	Controlled by alternative pin function GPIO1_IO04 **Note:** Signals also connected to AIN3
S54/107	DISP_PWR_EN	GPIO1_IO02	Yes	Controlled by alternative pin function GPIO1_IO02 **Note:** Signals also connected to AIN1 and GPIO2
S55/109	BL_PWR_EN	GPIO1_IO01	Yes	Controlled by alternative pin function GPIO1_IO01 **Note:** Signals also connected to AIN0 and GPIO1
S56/111	BL_PWM	GPIO1_IO08	Yes	Controlled by alternative pin function PWM1_OUT **Note:** Signals also connected to PWM
S57/113	GND			
S58/115	LCD_R0	LCD_DATA16	Yes	Controlled by alternative pin function LCD_DATA16
S59/117	LCD_R1	LCD_DATA17	Yes	Controlled by alternative pin function LCD_DATA17
S60/119	LCD_R2	LCD_DATA18	Yes	Controlled by alternative pin function LCD_DATA18
S61/121	LCD_R3	LCD_DATA19	Yes	Controlled by alternative pin function LCD_DATA19
S62/123	LCD_R4	LCD_DATA20	Yes	Controlled by alternative pin function LCD_DATA20
S63/125	LCD_R5	LCD_DATA21	Yes	Controlled by alternative pin function LCD_DATA21
S64/127	LCD_R6	LCD_DATA22	Yes	Controlled by alternative pin function LCD_DATA22
S65/129	LCD_R7	LCD_DATA23	Yes	Controlled by alternative pin function LCD_DATA23
S66/131	LCD_G0	LCD_DATA08	Yes	Controlled by alternative pin function LCD_DATA08
S67/133	LCD_G1	LCD_DATA09	Yes	Controlled by alternative pin function LCD_DATA09
S68/135	LCD_G2	LCD_DATA10	Yes	Controlled by alternative pin function LCD_DATA10
S69/137	LCD_G3	LCD_DATA11	Yes	Controlled by alternative pin function LCD_DATA11
S70/139	LCD_G4	LCD_DATA12	Yes	Controlled by alternative pin function LCD_DATA12
S71/141	LCD_G5	LCD_DATA13	Yes	Controlled by alternative pin function LCD_DATA13
S72/143	LCD_G6	LCD_DATA14	Yes	Controlled by alternative pin function LCD_DATA14
S73/145	LCD_G7	LCD_DATA15	Yes	Controlled by alternative pin function LCD_DATA15
S74/147	GND			
S75/149	LCD_B0	LCD_DATA00	Yes	Controlled by alternative pin function LCD_DATA00
151	Non existing pin			
153	Non existing pin			
155	Non existing pin			
S76/157	LCD_B1	LCD_DATA01	Yes	Controlled by alternative pin function LCD_DATA01
S77/159	LCD_B2	LCD_DATA02	Yes	Controlled by alternative pin function LCD_DATA02
S78/161	LCD_B3	LCD_DATA03	Yes	Controlled by alternative pin function LCD_DATA03
S79/163	LCD_B4	LCD_DATA04	Yes	Controlled by alternative pin function LCD_DATA04
S80/165	LCD_B5	LCD_DATA05	Yes	Controlled by alternative pin function LCD_DATA05
S81/167	LCD_B6	LCD_DATA06	Yes	Controlled by alternative pin function LCD_DATA06

S82/169	LCD_B7	LCD_DATA07	Yes	Controlled by alternative pin function LCD_DATA07
S83/171	LCD_CLK	LCD_PCLK	Yes	Controlled by alternative pin function LCD_PCLK
S84/173	GPIO7			
S85/175	LCD_HSYNC	LCD_HSYNC	Yes	Controlled by alternative pin function LCD_HSYNC
S86/177	LCD_VSYNC	LCD_VSYNC	Yes	Controlled by alternative pin function LCD_VSYNC
S87/179	LCD_ENABLE	LCD_DE	Yes	Controlled by alternative pin function LCD_DE
S88/181	GND			
S89/183	AIN_VREF	VDDA_ADC_3P3	Yes	Signal connected to ADC reference input, i.MX 6UltraLite ball L13 and M13.
S90/185	AIN7			
S91/187	AIN6			
S92/189	AIN5			
S93/191	AIN4			
S94/193	AIN3	GPIO1_IO4	Yes	**Note:** Signals also connected to TP_IRQ
S95/195	AIN2	GPIO1_IO3	Yes	**Note:** Signals also connected to GPIO4
S96/197	AIN1	GPIO1_IO2	Yes	**Note:** Signals also connected to GPIO2 and DISP_PWR_EN
S97/199	AIN0	GPIO1_IO1	Yes	**Note:** Signals also connected to GPIO1 and BL_PWR_EN
S98/201	GND			
S99/203	COM board specific			
S100/205	COM board specific			
S101/207	GND			
S102/209	COM board specific			
S103/211	COM board specific			
S104/213	GND			
S105/215	COM board specific			
S106/217	COM board specific			
S107/219	COM board specific	SNVS_TAMPER9	No	
S108/221	COM board specific	SNVS_TAMPER8	Yes	
S109/223	COM board specific	SNVS_TAMPER7	Yes	
S110/225	COM board specific	(SNVS_TAMPER6)	(Yes)	**Note:** Only available if ENET2 not mounted
S111/227	COM board specific	(SNVS_TAMPER5)	(Yes)	**Note:** Only available if ENET1 not mounted
S112/229	COM board specific	SNVS_TAMPER1	Yes	**Note:** Signals also connected to GPIO6
S113/231	COM board specific	SNVS_TAMPER0	Yes	**Note:** Signals also connected to pin P86/180
S114/233	CSI_HSYNC	CSI_HSYNC	Yes	Controlled by alternative pin function CSI_HSYNC
S115/235	CSI_VSYNC	CSI_VSYNC	Yes	Controlled by alternative pin function CSI_VSYNC
S116/237	CSI_MCLK	CSI_MCLK	Yes	Controlled by alternative pin function CSI_MCLK
S117/239	CSI_PCLK	CSI_PIXCLK	Yes	Controlled by alternative pin function CSI_PIXCLK
S118/241	GND			
S119/243	CSI_D0	CSI_DATA0	Yes	Controlled by alternative pin function CSI_DATA0
S120/245	CSI_D1	CSI_DATA1	Yes	Controlled by alternative pin function CSI_DATA1
S121/247	CSI_D2	CSI_DATA2	Yes	Controlled by alternative pin function CSI_DATA2
S122/249	CSI_D3	CSI_DATA3	Yes	Controlled by alternative pin function CSI_DATA3

S123/251	CSI_D4	CSI_DATA4	Yes	Controlled by alternative pin function CSI_DATA4
S124/253	CSI_D5	CSI_DATA5	Yes	Controlled by alternative pin function CSI_DATA5
S125/255	CSI_D6	CSI_DATA6	Yes	Controlled by alternative pin function CSI_DATA6
S126/257	CSI_D7	CSI_DATA7	Yes	Controlled by alternative pin function CSI_DATA7
S127/259	GND			
S128/261	CSI_D3_M			
S129/263	CSI_D3_P			
S130/265	GND			
S131/267	CSI_D2_M			
S132/269	CSI_D2_P			
S133/271	GND			
S134/273	CSI_D1_M			
S135/275	CSI_D1_P			
S136/277	GND			
S137/279	CSI_D0_M			
S138/281	CSI_D0_P			
S139/283	GND			
S140/285	CSI_CLK_M			
S141/287	CSI_CLK_P			
S142/289	GND			
S143/291	SATA_TX_P			
S144/293	SATA_TX_N			
S145/295	GND			
S146/297	SATA_RX_N			
S147/299	SATA_RX_P			
S148/301	GND			
S149/303	GND			
S150/305	PCIE_CLK_P	CCM_CLK1_P	No	Non-standard pin allocation. Is a general differential clock output, positive signal
S151/307	PCIE_CLK_N	CCM_CLK1_N	No	Non-standard pin allocation. Is a general differential clock output, negative signal
S152/309	GND			
S153/311	PCIE_TX_P			
S154/313	PCIE_TX_N			
S155/315	GND			
S156/317	PCIE_RX_P			
S157/319	PCIE_RX_N			
S158/321	GND			

4 Pin Mapping

4.1 Functional Multiplexing on I/O Pins

There are a lot of different peripherals inside the i.MX 6UltraLite SoC. Many of these peripherals are connected to the IOMUX block, that allows the I/O pins to be configured to carry one of many (up to nine different) alternative functions. This leave great flexibility to select a function multiplexing scheme for the pins that satisfy the interface need for a particular application.

Some interfaces with specific voltage levels/drivers/transceivers have dedicated pins, like USB. i.MX 6UltraLite pins carrying these signals do not have any functional multiplexing possibilities. These interfaces are fixed.

To keep compatibility between EACOM boards the EACOM specified pinning should be followed, but in general there are no restrictions to select alternative pin multiplexing schemes on the *iMX6 UltraLite COM Board*. Note that all EACOM-defined pins are not connected on some EACOM boards, typically because an interface is not supported or there are not enough free pins in the SoC. Further, some EACOM board pins are *type specific*, meaning that these pins might not be compatible with other EACOM boards. Using *type specific* pins may result in lost compatibility between EACOM boards, but not always. Always check details between EACOM boards of interest.

If switching between EACOM board is not needed, then pin multiplexing can be done without considering the EACOM pin allocation. A custom carrier board design is needed in this case.

Functional multiplexing is normally controlled via the Linux BSP. It can also be done directly via register IOMUXC_SW_MUX_CTL_PAD_xxx where xxx is the name of the i.MX 6UltraLite pin. For more information about the register settings, see the *iMX6UltraLite Reference Manual* from NXP.

Note that input functions that are available on multiple pins will require control of an input multiplexer. This is controlled via register IOMUXC_xxx_SELECT_INPUT where xxx is the name of the input function. Again, for more information about the register settings, see the *iMX6UltraLite Reference Manual* from NXP.

4.1.1 Alternative I/O Function List

There is an accompanying Excel document that lists all alternative functions for each available I/O pin. Reset state (typically GPIO, ALT5 function, except for two pins) is shown as well as the EACOM function allocation.

4.2 I/O Pin Control

Each pin also has an additional control register for configuring input hysteresis, pull up/down resistors, push-pull/open-drain driving, drive strength and more. Also in this case, configuration is normally done via the Linux BSP but it is possible to directly access the control registers, which are called IOMUXC_SW_PAD_CTL_PAD_xxx where xxx is the name of the i.MX 6UltraLite pin. For more information about the register settings, see the *iMX6UltraLite Reference Manual* from NXP.

Note that most pins are configured as GPIO inputs, with a 100Kohm pull-down resistor, after reset. When the bootloader (typically u-boot) executes it is possible to reconfigure the pins.

5 Interface Description

This chapter lists details about the different EACOM interfaces. The **i.MX 6UltraLite datasheet and user manual should always be consulted** for details about different functions and interfaces. Many interfaces are multiplexed on different pins and not available simultaneously.

Note that this chapter do not list all peripheral functions available on the i.MX6 UltraLite SoC. Only the ones related to the EACOM specification. For all available interfaces, consult *Chapter 4 - External Signals and Pin Multiplexing* in NXP's *i.MX 6UltraLite Applications Processor Reference Manual* (document id: IMX6ULRM).

Example of peripheral blocks **not** listed in this chapter are listed below (see document IMX6ULRM for details). Some of the blocks have multiple instances.

- CCM - Clock Controller Module
  Besides internal clocks, this peripheral can generate external clocks.
- EIM - External Interface Module
  This peripheral provides asynchronous access to devices with SRAM-like interface and synchronous access to devices with NOR-Flash-like or PSRAM-like interface.
- EPIT - Enhanced Periodic Interrupt Timer
  This peripheral is a 32-bit timer that provides precise interrupts.
- GPT - General Purpose Timer
  This peripheral is a 32-bit general purpose timer with capture and trigger functions.
- KPP - Keypad Port
  This peripheral provides a keypad matrix interface.
- QSPI - Quad Serial Peripheral Interface
  This peripheral provides an interface to serial flash devices with up to 4 bidirectional data lines.
- SDMA - Smart Direct Memory Access Controller
  This peripheral provides fast data transfers between peripheral I/O devices and internal/external memories
- SIM - Subscriber Identification Module
  This peripheral provides communication to SIM cards or Eurochip pre-paid phone cards that are compatible with ISO/IEC 7816-3 standards.
- TSC - Touch Screen Controller
  This peripheral use the ADC inputs to provide a 4-wire of 5-wire touch screen interface.
- WDOG - Watchdog Timer
  This peripheral implements a watchdog timer.

There is an accompanying Excel document that lists all alternative functions for each available I/O pin.

5.1 Analogue Inputs

This section lists signals related to analog inputs.

The i.MX 6UltraLite SoC has two 10 (single-ended input) channel 12-bit resolution ADC modules that shares the same 10 pins, channel for channel. This can be useful for setting up different sample rates. A sample rate of up to about 1MHz can be configured. Input voltage range is from ground to ADC_VREFH voltage.

Not only do the two ADC blocks inputs overlap pin for pin. The analog inputs overlap GPIO1_IO00-GPIO1_IO09. Four of the analogue inputs have been allocated to EACOM pins, see table below.

EACOM Board Pin	EACOM Board Name	i.MX 6UltraLite Ball Name	I/O	Description	Remarks
S97/199 (P140/288) (S55/109)	AIN0 (GPIO1) (BL_PWR_EN)	GPIO1_IO01	AI	Analog input #1 to ADC#1 and ADC#2	**Note:** Signal is also connected to EACOM signals GPIO1 and BL_PWR_EN
S96/197 (P139/286) (S54/107)	AIN1 (GPIO2) (DISP_PWR_EN)	GPIO1_IO02	AI	Analog input #2 to ADC#1 and ADC#2	**Note:** Signal is also connected to EACOM signals GPIO2 and DISP_PWR_EN
S95/195 (P3/6)	AIN2 (GPIO4)	GPIO1_IO03	AI	Analog input #3 to ADC#1 and ADC#2	**Note:** Signal is also connected to EACOM signal GPIO4
S94/193 (S53/105)	AIN3 (TP_IRQ)	GPIO1_IO04	AI	Analog input #4 to ADC#1 and ADC#2	**Note:** Signal is also connected to EACOM signal TP_IRQ
S93/191	AIN4				Not connected
S92/189	AIN5				Not connected
S91/187	AIN6				Not connected
S90/185	AIN7				Not connected
S89/183	AIN_VREF		AO	Positive reference voltage for ADC inputs (not related to VADC inputs)	Signal connected to ADC reference input, i.MX 6UltraLite ball L13 and M13. **Note**: this is not an input voltage, but rather an observation of internal reference voltage.

Note that the GPIO default configuration is to have the pin keeper functionality enabled. The keeper causes an undesired jump behavior in ADC. To avoid the problem, disable keeper before starting the ADC.

The rest of the analogue inputs are available on the following EACOM pins.

EACOM Board Pin	EACOM Board Name	i.MX 6UltraLite Ball Name	I/O	Description	Remarks
P66/132	USB_O1_OTG_ID	GPIO1_IO00	AI	Analog input #0 to ADC#1 and ADC#2	
P89/186	USB_H2_DN	GPIO1_IO05	AI	Analog input #5 to ADC#1 and ADC#2	Note that pin GPIO1_IO05 function as signal SD1_VSELECT and is connected to SD_VSEL on PF3000 PMIC. The signal can be used if the SD1 interface is not used.
P101/210	COM board specific	(GPIO1_IO06)	AI	Analog input #6 to ADC#1 and ADC#2	**Note**: Only available if ENET1 and ENET2 are not mounted.
P100/208	COM board specific	(GPIO1_IO07)	AI	Analog input #7 to ADC#1 and ADC#2	**Note**: Only available if ENET1 and ENET2 are not mounted.
P138/284 S56/111	PWM BL_PWM	GPIO1_IO08	AI	Analog input #8 to ADC#1 and ADC#2	**Note:** Signals also connected to EACOM signal PWM and BL_PWM
P4/8	GPIO3	GPIO1_IO09	AI	Analog input #9 to ADC#1 and ADC#2	

5.2 CSI - Parallel Camera Interface

This section lists signals related to CMOS Sensor Interface (CSI) functions.

The i.MX 6UltraLite SoC has one CSI interfaces that allows direct connection to CMOS image sensors, or camera, for short. The interface provides a standard parallel CSI camera interface port. The CSI parallel data ports are up to 24 bits. It is designed to support 24-bit RGB888/YUV444, CCIR656 video interface, 8/16/24-bit YCbCr, YUV or RGB, and 8/10/16-bit Bayer (also called "raw") data input.

The *EACOM Board specification* defines an 8-bit parallel camera interface. Note the difference in pin numbering and internal data bus numbering. The table below lists the pin assignment according to *EACOM Board specification*.

EACOM Board Pin	EACOM Board Name	i.MX 6UltraLite Ball Name	I/O	Description	Remarks
S116/237	CSI_MCLK	CSI_MCLK	O	CMOS Sensor Master Clock	
S117/239	CSI_PCLK	CSI_PIXCLK	I	Pixel Clock	
S114/233	CSI_HSYNC	CSI_HSYNC	I	Horizontal Sync	
S115/235	CSI_VSYNC	CSI_VSYNC	I	Vertical Sync (Start Of Frame)	
S119/243	CSI_D0	CSI_DATA00	I	Data Sensor Signal	Signal called csi.DATA[2] internally.
S120/245	CSI_D1	CSI_DATA01	I	Data Sensor Signal	Signal called csi.DATA[3] internally.
S121/247	CSI_D2	CSI_DATA02	I	Data Sensor Signal	Signal called csi.DATA[4] internally.
S122/249	CSI_D3	CSI_DATA03	I	Data Sensor Signal	Signal called csi.DATA[5] internally.
S123/251	CSI_D4	CSI_DATA04	I	Data Sensor Signal	Signal called csi.DATA[6] internally.
S124/253	CSI_D5	CSI_DATA05	I	Data Sensor Signal	Signal called csi.DATA[7] internally.
S125/255	CSI_D6	CSI_DATA06	I	Data Sensor Signal	Signal called csi.DATA[8] internally.
S126/257	CSI_D7	CSI_DATA07	I	Data Sensor Signal	Signal called csi.DATA[9] internally.

The table below lists these the alternative pin locations are.

EACOM Board Pin	EACOM Board Name	i.MX 6UltraLite Ball Name	I/O	Description	Remarks
S59/117	LCD_R1	LCD_DATA17	I	Data Sensor Signal	Alternative location for csi.DATA[0]
P128/264	UART-C_RXD	UART3_RX	I	Data Sensor Signal	Alternative location for csi.DATA[0]
S58/115	LCD_R0	LCD_DATA16	I	Data Sensor Signal	Alternative location for csi.DATA[1]
P129/266	UART-C_TXD	UART3_TX	I	Data Sensor Signal	Alternative location for csi.DATA[1]
S75/149	LCD_B0	LCD_DATA00	I	Data Sensor Signal	Alternative location for csi.DATA[2]
P137/282	UART-A_TXD	UART1_TX	I	Data Sensor Signal	Alternative location for csi.DATA[2]
S76/157	LCD_B1	LCD_DATA01	I	Data Sensor Signal	Alternative location for csi.DATA[3]
P134/276	UART-A_RXD	UART1_RX	I	Data Sensor Signal	Alternative location for csi.DATA[3]
S77/159	LCD_B2	LCD_DATA02	I	Data Sensor Signal	Alternative location for csi.DATA[4]
P135/278	UART-A_CTS	UART1_CTS	I	Data Sensor Signal	Alternative location for csi.DATA[4]
S78/161	LCD_B3	LCD_DATA03	I	Data Sensor Signal	Alternative location for csi.DATA[5]
P136/280	UART-A_RTS	UART1_RTS	I	Data Sensor Signal	Alternative location for csi.DATA[5]
S79/163	LCD_B4	LCD_DATA04	I	Data Sensor Signal	Alternative location for csi.DATA[6]
P133/274	UART-B_TXD	UART2_TX	I	Data Sensor Signal	Alternative location for csi.DATA[6]

S80/165	LCD_B5	LCD_DATA05	I	Data Sensor Signal	Alternative location for csi.DATA[7]
P130/268	UART-B_RXD	UART2_RX	I	Data Sensor Signal	Alternative location for csi.DATA[7]
S81/167	LCD_B6	LCD_DATA06	I	Data Sensor Signal	Alternative location for csi.DATA[8]
P131/270 **S12/23**	UART-B_CTS CAN2_TX	UART2_CTS	I	Data Sensor Signal	Alternative location for csi.DATA[8]
S82/169	LCD_B7	LCD_DATA07	I	Data Sensor Signal	Alternative location for csi.DATA[9]
P132/272 **S13/25**	UART-B_RTS CAN2_RX	UART2_RTS	I	Data Sensor Signal	Alternative location for csi.DATA[9]
S60/119	LCD_R2	LCD_DATA18	I	Data Sensor Signal	Alternative location for csi.DATA[10]
S14/27	CAN1_TX	UART3_CTS	I	Data Sensor Signal	Alternative location for csi.DATA[10]
S61/121	LCD_R3	LCD_DATA19	I	Data Sensor Signal	Alternative location for csi.DATA[11]
S15/29	CAN1_RX	UART3_RTS	I	Data Sensor Signal	Alternative location for csi.DATA[11]
S62/123	LCD_R4	LCD_DATA20	I	Data Sensor Signal	Alternative location for csi.DATA[12]
S63/125	LCD_R5	LCD_DATA21	I	Data Sensor Signal	Alternative location for csi.DATA[13]
S64/127	LCD_R6	LCD_DATA22	I	Data Sensor Signal	Alternative location for csi.DATA[14]
S49/97	I2C-B_SCL	UART5_TX	I	Data Sensor Signal	Alternative location for csi.DATA[14] Note:
S65/129	LCD_R7	LCD_DATA23	I	Data Sensor Signal	Alternative location for csi.DATA[15]
S48/95	I2C-B_SDA	UART5_RX	I	Data Sensor Signal	Alternative location for csi.DATA[15] Note:
P99/206	COM board specific	(ENET1_RXD0)	I	Data Sensor Signal	Alternative location for csi.DATA[16] **Note:** Only available if ENET1 not mounted.
S66/131	LCD_G0	LCD_DATA08	I	Data Sensor Signal	Alternative location for csi.DATA[16]
P98/204	COM board specific	(ENET1_RXD1)	I	Data Sensor Signal	Alternative location for csi.DATA[17] **Note:** Only available if ENET1 not mounted.
S67/133	LCD_G1	LCD_DATA09	I	Data Sensor Signal	Alternative location for csi.DATA[17]
P97/202	COM board specific	(ENET1_CRS_DV)	I	Data Sensor Signal	Alternative location for csi.DATA[18] **Note:** Only available if ENET1 not mounted.
S68/135	LCD_G2	LCD_DATA10	I	Data Sensor Signal	Alternative location for csi.DATA[18]
P95/198	COM board specific	(ENET1_TXD0)	I	Data Sensor Signal	Alternative location for csi.DATA[19] **Note:** Only available if ENET1 not mounted.
S69/137	LCD_G3	LCD_DATA11	I	Data Sensor Signal	Alternative location for csi.DATA[19]
P94/196	COM board specific	(ENET1_TXD1)	I	Data Sensor Signal	Alternative location for csi.DATA[20] **Note:** Only available if ENET1 not mounted.
S70/139	LCD_G4	LCD_DATA12	I	Data Sensor Signal	Alternative location for csi.DATA[20]
P93/194	COM board specific	(ENET1_TXEN)	I	Data Sensor Signal	Alternative location for csi.DATA[21] **Note:** Only available if ENET1 not mounted.
S71/141	LCD_G5	LCD_DATA13	I	Data Sensor Signal	Alternative location for csi.DATA[21]
P92/192	COM board specific	(ENET1_TX_CLK)	I	Data Sensor Signal	Alternative location for csi.DATA[22] **Note:** Only available if ENET1 not mounted.
S72/143	LCD_G6	LCD_DATA14	I	Data Sensor Signal	Alternative location for csi.DATA[22]
P96/200	COM board specific	(ENET1_RXER)	I	Data Sensor Signal	Alternative location for csi.DATA[23] **Note:** Only available if ENET1 not mounted.
S73/145	LCD_G7	LCD_DATA15	I	Data Sensor Signal	Alternative location for csi.DATA[23]

P89/186	USB_H2_DN	GPIO1_IO05	I	CSI Field Signal	Alternative location for csi.FIELD Note that pin GPIO1_IO05 function as signal SD1_VSELECT and is connected to SD_VSEL on PF3000 PMIC. The signal can be used if the SD1 interface is not used.
S52/103	TP_RST	NAND_DQS	I	CSI Field Signal	Alternative location for csi.FIELD
P4/8	GPIO3	GPIO1_IO09	I	Horizontal Sync	Alternative location for csi.HSYNC
P101/210	COM board specific	(GPIO1_IO06)	O	CMOS Sensor Master Clock	Alternative location for csi.MCLK **Note:** Only available if ENET1 and ENET2 are not mounted
P100/208	COM board specific	(GPIO1_IO07)	I	Pixel Clock	Alternative location for csi.PIXCLK **Note:** Only available if ENET1 and ENET2 are not mounted
P138/284 **S56/111**	PWM BL_PWM	GPIO1_IO08	I	Vertical Sync (Start Of Frame)	Alternative location for csi.VSYNC

The CSI can support connection with the sensor as follows.

- To connect with one 8-bit sensor, the sensor data interface should connect to CSI_DATA[9:2]. This is the method that is supported by the *EACOM Board specification*.
- To connect with one 10-bit sensor, the sensor data interface should connect to CSI_DATA[9:0].
- To connect with one 16-bit sensor, the sensor data interface should connect to CSI_DATA[15:0].
- To connect with one 24-bit data, either video pass-through or TV Decoder input, the sensor data interface should connect to CSI_DATA[23:0].

The CSI input data format mapping is shown in the table below.

Internal CSI Signal Name	EACOM Board Name	CCIR656	Generic 10 bit	YCbCr422 2 Cycle	YCbCr422 1 Cycle	RGB565 1 Cycle	RGB666 1 Cycle	RGB888/ YUV4444 3 Cycle	RGB888 1 Cycle	TVdecoder YCbCr 1 Cycle
CSI1_DATA00			Ge0		C0	B0	B4		B0	Cr0
CSI1_DATA01			Ge1		C1	B1	B5		B1	Cr1
CSI1_DATA02	**CSI_D0**	C0/Y0	Ge2	Y0/C0	C2	B2	B0	R0/G0/B0	B2	Cr2
CSI1_DATA03	**CSI_D1**	C1/Y1	Ge3	Y1/C1	C3	B3	B1	R1/G1/B1	B3	Cr3
CSI1_DATA04	**CSI_D2**	C2/Y2	Ge4	Y2/C2	C4	B4	B2	R2/G2/B2	B4	Cr4
CSI1_DATA05	**CSI_D3**	C3/Y3	Ge5	Y3/C3	C5	G0	B3	R3/G3/B3	B5	Cr5
CSI1_DATA06	**CSI_D4**	C4/Y4	Ge6	Y4/C4	C6	G1	B4	R4/G4/B4	B6	Cr6
CSI1_DATA07	**CSI_D5**	C5/Y5	Ge7	Y5/C5	C7	G2	B5	R5/G5/B5	B7	Cr7
CSI1_DATA08	**CSI_D6**	C6/Y6	Ge8	Y6/C6	Y0	G3	G4	R6/G6/B6	G0	Cb0
CSI1_DATA09	**CSI_D7**	C7/Y7	Ge9	Y7/C7	Y1	G4	G5	R7/G7/B7	G1	Cb1
CSI1_DATA10					Y2	G5	G0		G2	Cb2
CSI1_DATA11					Y3	R0	G1		G3	Cb3
CSI1_DATA12					Y4	R1	G2		G4	Cb4
CSI1_DATA13					Y5	R2	G3		G5	Cb5
CSI1_DATA14					Y6	R3	G4		G6	Cb6
CSI1_DATA15					Y7	R4	G5		G7	Cb7

CSI1_DATA16	R4	R0	Y0
CSI1_DATA17	Y5	R1	Y1
CSI1_DATA18	R0	R2	Y2
CSI1_DATA19	R1	R3	Y3
CSI1_DATA20	R2	R4	Y4
CSI1_DATA21	R3	R5	Y5
CSI1_DATA22	R4	R6	Y6
CSI1_DATA23	R5	R7	Y7

5.3 Display Interface - Parallel RGB LCD

This section presents signals related to the Enhanced LCD Interface (eLCDIF).

The i.MX 6UltraLite SoC has a display and graphics subsystem with dedicated components:

- PXP pixel pipeline: pixel/image processing engine for LCD display
- LCD interface (LCDIF), which is 24-bit parallel RGB LCD interface
- CSI interface with up to 24-bit parallel interface for image sensor

The picture below shows the high-level structure of the display and graphics subsystem in the i.MX 6UltraLite.

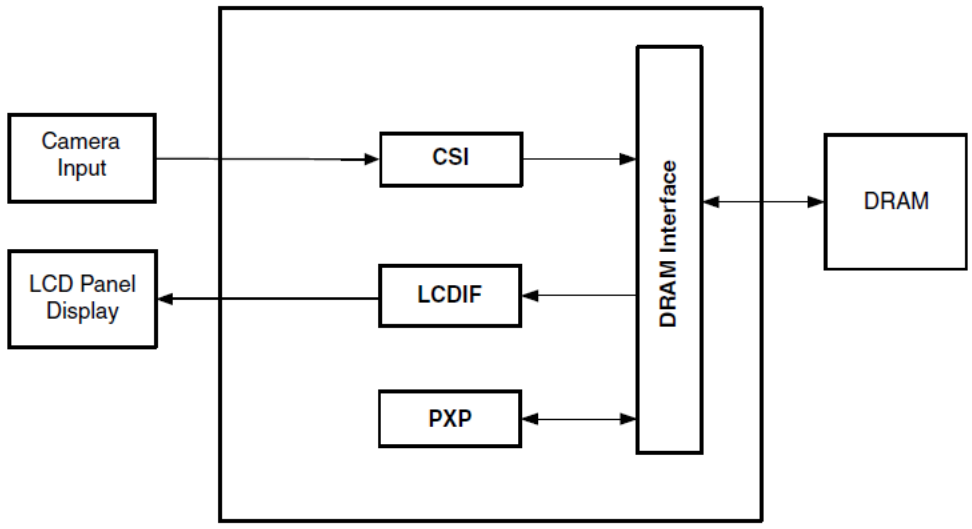


Figure 4 – Structure of Display and Graphics Subsystem

The *i.MX 6UltraLite COM board* has allocated pins (according to the *EACOM Board specification*) for one parallel camera input and a parallel RGB LCD output. The EACOM pins for LVDS, HDMI and MIPI-DSI output interfaces are not allocated since the i.MX 6UltraLite SoC does not support these interfaces. The parallel camera interface is presented in section 5.2 .

This section lists signals for the parallel RGB LCD interface.

The LCDIF supports one display with up to 1366x768 pixel resolution (WXGA), 24-bit color and 60Hz update rate.

The *EACOM Board specification* defines a 24-bit parallel LCD interface. The table below lists the pin assignment according to *EACOM Board specification*. For best portability it is recommended to always have the LCD interface running in 24-bit mode. If less bits are needed in a specific LCD implementation the LSB bits of each color is just ignored, see the three rightmost columns.

EACOM Board Pin	EACOM Board Name	i.MX 6UltraLite Ball Name	I/O	Color Config. for 16-bit 565RGB	Color Config. for 18-bit 666RGB	Color Config. for 16-bit 565RGB if interface set to 24-bit	Color Config. for 18-bit 666RGB if interface set to 24-bit	Color Config. for 24-bit 888RGB
S75/149	LCD_DATA00	LCD_DATA00	O	B0	B0			B0
S76/157	LCD_DATA01	LCD_DATA01	O	B1	B1			B1
S77/159	LCD_DATA02	LCD_DATA02	O	B2	B2		B2	B2
S78/161	LCD_DATA03	LCD_DATA03	O	B3	B3	B3	B3	B3
S79/163	LCD_DATA04	LCD_DATA04	O	B4	B4	B4	B4	B4
S80/165	LCD_DATA05	LCD_DATA05	O	G0	B5	B5	B5	B5
S81/167	LCD_DATA06	LCD_DATA06	O	G1	G0	B6	B6	B6
S82/169	LCD_DATA07	LCD_DATA07	O	G2	G1	B7	B7	B7
S66/131	LCD_DATA08	LCD_DATA08	O	G3	G2			G0
S67/133	LCD_DATA09	LCD_DATA09	O	G4	G3			G1
S68/135	LCD_DATA10	LCD_DATA10	O	G7	G4	G2	G2	G2
S69/137	LCD_DATA11	LCD_DATA11	O	R0	G5	G3	G3	G3
S70/139	LCD_DATA12	LCD_DATA12	O	R1	R0	G4	G4	G4
S71/141	LCD_DATA13	LCD_DATA13	O	R2	R1	G5	G5	G5
S72/143	LCD_DATA14	LCD_DATA14	O	R3	R2	G6	G6	G6
S73/145	LCD_DATA15	LCD_DATA15	O	R4	R3	G7	G7	G7
S58/115	LCD_DATA16	LCD_DATA16	O		R4			R0
S59/117	LCD_DATA17	LCD_DATA17	O		R5			R1
S60/119	LCD_DATA18	LCD_DATA18	O				R2	R2
S61/121	LCD_DATA19	LCD_DATA19	O			R3	R3	R3
S62/123	LCD_DATA20	LCD_DATA20	O			R4	R4	R4
S63/125	LCD_DATA21	LCD_DATA21	O			R5	R5	R5
S64/127	LCD_DATA22	LCD_DATA22	O			R6	R6	R6
S65/129	LCD_DATA23	LCD_DATA23	O			R7	R7	R7
S85/175	LCD_HSYNC	LCD_HSYNC	O	Horizontal (line) synchronization				
S86/177	LCD_VSYNC	LCD_VSYNC	O	Vertical (frame) synchronization				
S87/179	LCD_ENABLE	LCD_DE	O	Data enable				
S83/171	LCD_CLK	LCD_CLK	O	Pixel (dot) clock				

The *EACOM Board specification* has allocated some additional signals that are typically needed to implement an LCD interface. The table below list these signals.

EACOM Board Pin	EACOM Board Name	i.MX 6UltraLite Ball Name	I/O	Description	Remarks
S56/111 (P138/284)	BL_PWM (PWM)	GPIO1_IO08	O	PWM signal to control backlight contrast.	Signal is connected to PWM1_OUT
S55/109 (P140/288) (S97/199)	BL_PWR_EN GPIO1 AIN0	GPIO1_IO01	O	Power control for backlight. Active high	
S54/107 (P139/286) (S96/197)	DISP_PWR_EN (GPIO2) (AIN1)	GPIO1_IO02	O	Power control for LCD power supply. Active high	Signal is connected to GPIO1_IO02

S53/105 (S94/193)	TP_IRQ (AIN3)	GPIO1_IO04	I	Interrupt from touch controller	Signal is connected to GPIO1_IO04
S52/103	TP_RST	NAND_DQS	O	Reset signal to touch controller. Active low	Signal is connected to GPIO4_IO16
S47/93	I2C-A_SCL	UART4_TX	I/O	Clock signal of I2C channel A	It is recommended to connect the RGB LCD touch controller (if I2C interface) to this channel.
S46/91	I2C-A_SDA	UART4_RX	I/O	Data signal of I2C channel A	It is recommended to connect the RGB LCD touch controller (if I2C interface) to this channel.
S49/97	I2C-B_SCL	UART5_TX	I/O	Clock signal of I2C channel B	
S48/95	I2C-B_SDA	UART5_RX	I/O	Data signal of I2C channel B	

Note that the eLCDIF peripheral in the i.MX 6UltraLite SoC also supports MPU-like display interfaces. See chapter 34 in IMX6ULRM for more details.

5.4 Digital Audio Interface: Synchronous Audio Interface (SAI)

This section presents the audio subsystem component modules. It also lists signals related to the Synchronous Audio Interface (SAI). Subsequent sections lists the other audio interfaces (SPDIF and MQS).

The picture below provides an overview of each of the audio subsystem component modules.

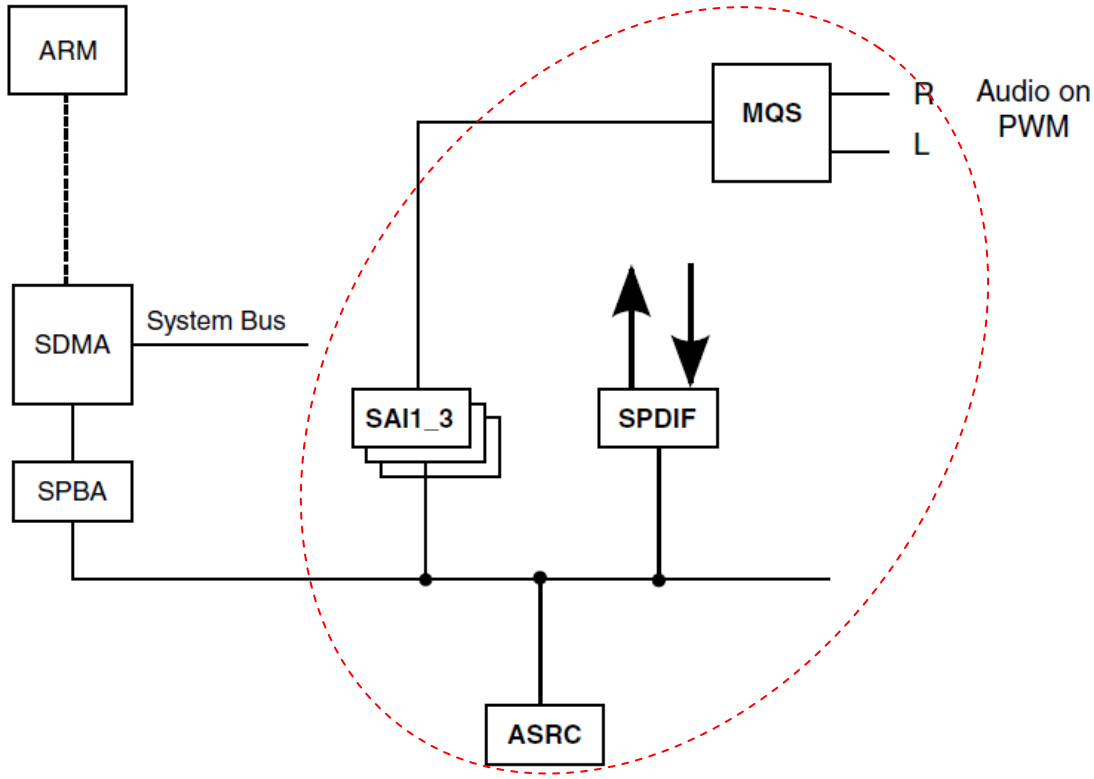


Figure 5 – Audio Subsystem Block Diagram

The key blocks are:

- The synchronous audio interface (SAI) supports full-duplex serial interfaces with frame synchronization such as I2S, AC97, TDM and codec/DSP interfaces. The SAI consists of independent transmitter and receiver sections, each section with its own clock generator. It is the three instances of this interface that is presented in this section.
- The Sony/Philips Digital Interface (SPDIF)audio module is a stereo that allows the processor transmit digital audio over it using the IEC60958 standard (a consumer market format). See section 5.5 for more details about this interface.
- ASRC (asynchronous sample rate converter) converts the sampling rate of a signal associated to an input clock into a signal associated to a different output clock. See chapter 16 in IMX6ULRM for more details.
- MQS is used to generate medium quality audio via a standard GPIO, via the SAI1 interface. See section 5.6 for more details about this interface.

The table below lists pins that have been allocated according to the *EACOM Board specification*. The SAI2 port is used with **synchronous** transmit and receive sections (meaning that transmit and receive share the clock and frame synch signals).

EACOM Board Pin	EACOM Board Name	i.MX 6UltraLite Ball Name	I/O	Description	Remarks
S5/9	AUDIO_RXD	JTAG_TCK	I	Data receive signal Ch#3	Alternative function SAI2_RXD

					Note: Signal is also connected to JTAG interface
S6/11 (S2/3)	AUDIO_TXC (MQS_LEFT)	JTAG_TDI	O	Transmit clock signal Ch#3. Also work as Receive clock signal Ch#3	Alternative function SAI2_TXC **Note:** Signal is also connected to JTAG interface and signal MQS_LEFT
S7/13	AUDIO_TXD	JTAG_TRST	O	Data transmit signal Ch#3	Alternative function SAI2_TXD **Note:** Signal is also connected to JTAG interface
S4/7 (S1/1)	AUDIO_TXFS (MQS_RIGHT)	JTAG_TDO	O	Transmit Frame sync signal Ch#3. Also work as Receive Frame sync signal Ch#3	Alternative function SAI2_TXFS **Note:** Signal is also connected to JTAG interface and signal MQS_RIGHT
S8/15	AUDIO_MCLK	JTAG_TMS	O	Clock output signal	Alternative function SAI2_MCLK **Note:** Signal is also connected to JTAG interface

The table below lists pins available for the SAI1 interface.

EACOM Board Pin	EACOM Board Name	i.MX 6UltraLite Ball Name	I/O	Description	Remarks
S120/245	CSI_D1	CSI_DATA1	I/O	Audio Master Clock	Alternative function SAI1_MCLK
S75/149	LCD_B0	LCD_DATA00	I/O	Audio Master Clock	Alternative function SAI1_MCLK
S122/249	CSI_D3	CSI_DATA3	I/O	Receive Bit Clock	Alternative function SAI1_RX_BCLK
S125/255	CSI_D6	CSI_DATA6	I	Receive Data	Alternative function SAI1_RX_DATA
S78/161	LCD_B3	LCD_DATA03	I	Receive Data	Alternative function SAI1_RX_DATA
S121/247	CSI_D2	CSI_DATA2	I/O	Receive Frame Sync	Alternative function SAI1_RX_SYNC
S124/253	CSI_D5	CSI_DATA5	I/O	Transmit Bit Clock	Alternative function SAI1_TX_BCLK
S77/159	LCD_B2	LCD_DATA02	I/O	Transmit Bit Clock	Alternative function SAI1_TX_BCLK
S126/257	CSI_D7	CSI_DATA7	O	Transmit Data	Alternative function SAI1_TX_DATA
S79/163	LCD_B4	LCD_DATA04	O	Transmit Data	Alternative function SAI1_TX_DATA
S123/251	CSI_D4	CSI_DATA4	I/O	Transmit Frame Sync	Alternative function SAI1_TX_SYNC
S76/157	LCD_B1	LCD_DATA01	I/O	Transmit Frame Sync	Alternative function SAI1_TX_SYNC

Besides the SAI port #2 signals allocated in the *EACOM Board specification* there are more (alternative) pins for the SAI2 interface. The table below lists these pins.

EACOM Board Pin	EACOM Board Name	i.MX 6UltraLite Ball Name	I/O	Description	Remarks
P7/14	SD_CLK	SD1_CLK	I/O	Audio Master Clock	Alternative function SAI2_MCLK
P10/20	SD_D2	SD1_DATA2	I	Receive Data	Alternative function SAI2_RX_DATA
P8/16	SD_CMD	SD1_CMD	I/O	Receive Frame Sync	Alternative function SAI2_RX_SYNC
P5/10	SD_D1	SD1_DATA1	I/O	Transmit Bit Clock	Alternative function SAI2_TX_BCLK
P9/18	SD_D3	SD1_DATA3	O	Transmit Data	Alternative function SAI2_TX_DATA
P6/12	SD_D0	SD1_DATA0	I/O	Transmit Frame Sync	Alternative function SAI2_TX_SYNC

The table below lists pins available for the SAI3 interface.

EACOM Board Pin	EACOM Board Name	i.MX 6UltraLite Ball Name	I/O	Description	Remarks

S83/171	LCD_CLK	LCD_PCLK	I/O	Audio Master Clock	Alternative function SAI3_MCLK
S67/133	LCD_G1	LCD_DATA09	I/O	Audio Master Clock	Alternative function SAI3_MCLK
S69/137	LCD_G3	LCD_DATA11	I/O	Receive Bit Clock	Alternative function SAI3_RX_BCLK
S72/143	LCD_G6	LCD_DATA14	I	Receive Data	Alternative function SAI3_RX_DATA
S86/177	LCD_VSYNC	LCD_VSYNC	I/O	Receive Frame Sync	Alternative function SAI3_RX_SYNC
S68/135	LCD_G2	LCD_DATA10	I/O	Receive Frame Sync	Alternative function SAI3_RX_SYNC
S71/141	LCD_G5	LCD_DATA13	I/O	Transmit Bit Clock	Alternative function SAI3_TX_BCLK
S85/175	LCD_HSYNC	LCD_HSYNC	I/O	Transmit Bit Clock	Alternative function SAI3_TX_BCLK
S73/145	LCD_G7	LCD_DATA15	O	Transmit Data	Alternative function SAI3_TX_DATA
S70/139	LCD_G4	LCD_DATA12	I/O	Transmit Frame Sync	Alternative function SAI3_TX_SYNC
S87/179	LCD_ENABLE	LCD_DE	I/O	Transmit Frame Sync	Alternative function SAI3_TX_SYNC

5.5 Digital Audio Interface: S/PDIF

This section lists signals related to the Sony/Philips Digital Interface (SPDIF) function.

The i.MX 6UltraLite SoC has one SPDIF interface, which is a stereo transceiver that allows the processor to receive and transmit digital audio according to the AES/EBU IEC 60958 standard.

The *EACOM Board specification* defines one input and one output SPDIF interface. Only the output pin has been allocated. The table below lists the pin assignment according to *EACOM Board specification*.

EACOM Board Pin	EACOM Board Name	i.MX 6UltraLite Ball Name	I/O	Description	Remarks
S10/19	SPDIF_IN		I	Input line	Not connected
S11/21	SPDIF_OUT	JTAG_MOD	O	Output line signal	**Note:** This pin is also connected to the JTAG interface

There are alternative locations for the SPDIF pins as well as some clock signals that are not used very often. The table below lists these alternative pin locations.

EACOM Board Pin	EACOM Board Name	i.MX 6UltraLite Ball Name	I/O	Description	Remarks
P4/8	GPIO3	GPIO1_IO09	I	Input line	Alternative function SPDIF_IN
S66/131	LCD_G0	LCD_DATA08	I	Input line	Alternative function SPDIF_IN
P7/14	SD_CLK	SD1_CLK	I	Input line	Alternative function SPDIF_IN
P134/276	UART-A_RXD	UART1_RX	I	Input line	Alternative function SPDIF_IN
S56/111 P138/284	BL_PWM PWM	GPIO1_IO08	O	Output line signal	Alternative function SPDIF_OUT
S80/165	LCD_B5	LCD_DATA05	O	Output line signal	Alternative function SPDIF_OUT
P8/16	SD_CMD	SD1_CMD	O	Output line signal	Alternative function SPDIF_OUT
P137/282	UART-A_TXD	UART1_TX	O	Output line signal	Alternative function SPDIF_OUT
S79/163	LCD_B4	LCD_DATA04	O	SR clock signal	Alternative function SPDIF_SR_CLK
S81/167	LCD_B6	LCD_DATA06	O	Lock signal	Alternative function SPDIF_LOCK
S82/169	LCD_B7	LCD_DATA07	I	External clock signal	Alternative function SPDIF_EXT_CLK
S52/103	TP_RST	NAND_DQS	I	External clock signal	Alternative function SPDIF_EXT_CLK

5.6 Digital Audio Interface: MQS

This section lists signals related to the Medium Quality Sound (MQS) function.

The i.MX 6UltraLite SoC has one MQS block that can generate audio via PWM modulation on digital output pins. MQS provides only simple audio reproduction. No internal pop, click or distortion artifact reduction methods are provided.

The *EACOM Board specification* defines a stereo output for MQS sound signals. The table below lists the pin assignment according to *EACOM Board specification*.

EACOM Board Pin	EACOM Board Name	i.MX 6UltraLite Ball Name	I/O	Description	Remarks
S2/3 (S6/11)	MQS_LEFT (AUDIO_TXC)	JTAG_TDI	O	Left signal output	**Note:** Signal is also connected to EACOM signal AUDIO_TXC.
S1/1 (S4/7)	MQS_RIGHT (AUDIO_TXFS)	JTAG_TDO	O	Right signal output	**Note:** Signal is also connected to EACOM signal AUDIO_TXFS.

The table below lists these the alternative pin locations are.

EACOM Board Pin	EACOM Board Name	i.MX 6UltraLite Ball Name	I/O	Description	Remarks
S97/199 P140/288 S55/109	AIN0 GPIO1 BL_PWR_EB	GPIO1_IO1	O	Left signal output	Alternative function MQS_LEFT
S65/129	LCD_R7	LCD_DATA23	O	Left signal output	Alternative function MQS_LEFT
P66/132	USB_O1_OTG_ID	GPIO1_IO00	O	Right signal output	Alternative function MQS_RIGHT
S64/127	LCD_R6	LCD_DATA22	O	Right signal output	Alternative function MQS_RIGHT

5.7 Ethernet

This section lists signals related to the Ethernet interface.

The i.MX 6UltraLite has two 10/100 Mbps Ethernet controllers that are IEEE1588 compliant. Both are connected in the default configuration of the board. The Microchip/Micrel KSZ8081RNB 10Base-T/100Base-TX Physical Layer Transceivers are used as external PHYs and are connected via the RMII interfaces to the i.MX 6UltraLite SoC.

The *EACOM Board Specification* defines two Ethernet interfaces, named ETH1 and ETH2. The i.MX 6UltraLite SoC Ethernet interface #1 is assigned to ETH2 and interface #2 is assigned to ETH2.

Each Ethernet interface consists of 2 pairs of low voltage differential pair signals plus two link indicator activity signals. These signals can be used to connect to a 10/100BaseT RJ45 connector with integrated or external isolation magnetics on the carrier board. MDI2 and MDI3 are left unconnected since these are 10/100Mbps Ethernet interfaces, as opposed to Gigabit interfaces.

EACOM Board Pin	EACOM Board Name	KSZ8081 Pin	I/O	Description	Remarks
P39/78	ETH1_TRXP0	KSZ8081 #1, pin 7	I/O	Media Dependent Interface	
P40/80	ETH1_TRXN0	KSZ8081 #1, pin 6	I/O	Media Dependent Interface	
P36/72	ETH1_TRXP1	KSZ8081 #1, pin 5	I/O	Media Dependent Interface	
P37/74	ETH1_TRXN1	KSZ8081 #1, pin 4	I/O	Media Dependent Interface	
P48/96	ETH1_TRXP2				
P47/94	ETH1_TRXN2				
P45/90	ETH1_TRXP3				
P44/88	ETH1_TRXN3				
P42/84	ETH1_LED_ACT	KSZ8081 #1, pin304	O	LED indicator output	Signal toggles during TX/RX activity.

P43/86	ETH1_LED_LINK	KSZ8081 #1, pin 31	O	LED indicator output	Signal high when 100M link is active.
P41/82	ETH1_LED_LINK1000				
P53/106	ETH2_TRXP0	KSZ8081 #2, pin 7	I/O	Media Dependent Interface	
P54/108	ETH2_TRXN0	KSZ8081 #2, pin 6	I/O	Media Dependent Interface	
P50/100	ETH2_TRXP1	KSZ8081 #2, pin 5	I/O	Media Dependent Interface	
P51/102	ETH2_TRXN1	KSZ8081 #2, pin 4	I/O	Media Dependent Interface	
P62/124	ETH2_TRXP2				
P61/122	ETH2_TRXN2				
P59/118	ETH2_TRXP3				
P58/116	ETH2_TRXN3				
P56/112	ETH2_LED_ACT	KSZ8081 #2, pin304	O	LED indicator output	Signal toggles during TX/RX activity.
P57/114	ETH2_LED_LINK100	KSZ8081 #2, pin 31	O	LED indicator output	Signal high when 100M link is active.
P55/110	ETH2_LED_LINK1000				

The external PHYs can be powered down in order to lower the power consumption to a minimum.

Below is a list of suggested magnetics for 10/100Mbps Ethernet operation:

Vendor	P/N	Magnetic + RJ45	Temp
Bel Fuse	S558-5999-U7	No	0 - 70° Celsius
Bel Fuse	SI-46001-F	Yes	0 - 70° Celsius
Bel Fuse	SI-50170-F	Yes	0 - 70° Celsius
Delta	LF8505	No	0 - 70° Celsius
Halo	HFJ11-2450E	Yes	0 - 70° Celsius
Halo	TG110-E055N5	No	-40 - 85° Celsius
Pulse	H1102	No	0 - 70° Celsius
Pulse	H1260	No	0 - 70° Celsius
Pulse	HX1188	No	-40 - 85° Celsius
Pulse	J00-0014	Yes	0 - 70° Celsius
Pulse	JX0011D21NL	Yes	-40 - 85° Celsius
TDK	TLA-6T718A	Yes	0 - 70° Celsius
Wurth/Midcom	000-7090-37R-LF1	No	-40 - 85° Celsius

5.8 FLEXCAN

This section lists signals related to the Controller Area Network (CAN) interface.

The i.MX 6UltraLite SoC has two Flexible Controller Area Network (FlexCAN) interfaces that supports bitrates of up to 1Mbps each. The FlexCAN module is a communication controller implementing the CAN protocol according to the CAN 2.0B protocol specification, which supports both standard and extended message frames.

EACOM Board Pin	EACOM Board Name	i.MX 6UltraLite Ball Name	I/O	Description	Remarks
S15/29	CAN1_RX	UART3_RTS	I	CAN port 1 receive signal	Default location for EACOM Board spec.

S14/27	CAN1_TX	UART3_CTS	O	CAN port 1 transmit signal	Default location for EACOM Board spec.
S13/25	CAN2_RX	UART2_RTS	I	CAN port 2 receive signal	Default location for EACOM Board spec.
S12/23	CAN2_TX	UART2_CTS	O	CAN port 2 transmit signal	Default location for EACOM Board spec.
S67/133	LCD_G1	LCD_DATA09	I	CAN port 1 receive signal	Alternative location for CAN1_RX signal
P5/10	SD_D1	SD1_DATA1	I	CAN port 1 receive signal	Alternative location for CAN1_RX signal
P98/204	COM specific	(ENET1_RX_DATA1)	I	CAN port 1 receive signal	Alternative location for CAN1_RX signal
S66/131	LCD_G0	LCD_DATA08	O	CAN port 1 transmit signal	Alternative location for CAN1_TX signal
P6/12	SD_D0	SD1_DATA0	O	CAN port 1 transmit signal	Alternative location for CAN1_TX signal
P99/206	COM specific	(ENET1_RX_DATA0)	O	CAN port 1 transmit signal	Alternative location for CAN1_TX signal
S69/137	LCD_G3	LCD_DATA11	I	CAN port 2 receive signal	Alternative location for CAN2_RX signal
P9/18	SD_D3	SD1_DATA3	I	CAN port 2 receive signal	Alternative location for CAN2_RX signal
P95/198	COM specific	(ENET1_TX_DATA0)	I	CAN port 2 receive signal	Alternative location for CAN2_RX signal
S68/135	LCD_G2	LCD_DATA10	O	CAN port 2 transmit signal	Alternative location for CAN2_TX signal
P10/20	SD_D2	SD1_DATA2	O	CAN port 2 transmit signal	Alternative location for CAN2_TX signal
P97/202	COM specific	(ENET1_RX_EN)	O	CAN port 2 transmit signal	Alternative location for CAN2_TX signal

5.9 GPIOs

This section lists signals related to General Purpose Input/Output (GPIO) functionality.

Many pins have GPIO functionality that can be enabled (via pin multiplexing). All GPIO pins can be used to generate interrupts as well as be wakeup sources.

The *EACOM Board specification* defines only a few GPIOs and they are listed in the table below. The pins that cannot be configured as GPIOs are for example Ethernet and USB. I2C pins can be GPIOs but are unsuitable since I2C-A is used on-board and I2C-B has 2.2Kohm on-board pull-up resistors.

EACOM Board Pin	EACOM Board Name	i.MX 6UltraLite Ball Name	I/O	Description	Remarks
P140/288 (S55/109) (S97/199)	GPIO1 (BL_PWR_EN) (AIN0)	GPIO1_IO01	I/O	GPIO	GPIO1 controlled by alternative pin function GPIO1_IO01
P139/286 (S54/107) (S96/197)	GPIO2 (DISP_PWR_EN) (AIN1)	GPIO1_IO02	I/O	GPIO	GPIO2 controlled by alternative pin function GPIO1_IO02
P4/8	GPIO3	GPIO1_IO09	I/O	GPIO	GPIO3 controlled by alternative pin function GPIO1_IO09
P3/6	GPIO4	GPIO1_IO03	I/O	GPIO	GPIO4 controlled by alternative pin function GPIO1_IO03
P2/4	GPIO5				Not connected
P1/2	GPIO6	SNVS_TAMPER1	I/O	GPIO	GPIO6 controlled by alternative pin function GPIO5_IO01
S84/173	GPIO7				Not connected
S34/67	GPIO8				Not connected
S19/37	GPIO9				Not connected

5.10 I2C

This section lists signals related to the Inter-Integrated Circuit (I2C) interface.

The i.MX 6UltraLite SoC has four I2C interfaces. Two of these are assigned in the *EACOM Board Specification*. i.MX 6UltraLite I2C channel #1 is assigned to EACOM I2C channel A. i.MX 6UltraLite I2C channel #2 is assigned to EACOM I2C channel B.

Pin assignment for EACOM I2C channel A cannot be changed since this channel is used on the *iMX6 UltraLite COM board* (for PMIC and E2PROM communication). It is recommended not to change pin assignment for EACOM I2C channel B (I2C channel #2) since these pins have 2.2Kohm pull-up resistors.

The table below lists the pin assignment as well as alternative pin locations.

EACOM Board Pin	EACOM Board Name	i.MX 6UltraLite Ball Name	I/O	Description	Remarks
S47/93	I2C-A_SCL	UART4_TX	I/O	Clock signal of I2C channel A	Signal has on-board 2.2Kohm pullup resistor. Signal is connected to on-board I2C channel to PMIC and E2PROM.
S46/91	I2C-A_SDA	UART4_RX	I/O	Data signal of I2C channel A	Signal has on-board 2.2Kohm pullup resistor. Signal is connected to on-board I2C channel to PMIC and E2PROM.
S49/97	I2C-B_SCL	UART5_TX	I/O	Clock signal of I2C channel B	Signal has on-board 2.2Kohm pullup resistor.
S48/95	I2C-B_SDA	UART5_RX	I/O	Data signal of I2C channel B	Signal has on-board 2.2Kohm pullup resistor.
S51/101	I2C-C_SCL		I/O	Clock signal of I2C channel C	Not connected
S50/99	I2C-C_SDA		I/O	Data signal of I2C channel C	Not connected

Note that the following positions for I2C interfaces are not allowed:

- I2C1_SCL on i.MX 6UltraLite pin CSI_PIXCLK and GPIO1_IO02 should not be used. I2C channel #1 is allocated on another pin (UART4_TX)
- I2C1_SDA on i.MX 6UltraLite pin CSI_MCLK and GPIO1_IO03 should not be used. I2C channel #1 is allocated on another pin (UART4_RX).

i.MX 6UltraLite I2C interface #2 are located on the following pins (as alternative functions), but note that these locations are not recommended since the *EACOM Board specification* has allocated this function on another pin, see above.

EACOM Board Pin	EACOM Board Name	i.MX 6UltraLite Ball Name	I/O	Description	Remarks
S114/233	CSI_HSYNC	CSI_HSYNC	I/O	Clock signal of I2C channel #2	I2C2_SCL
P66/132	USB_O1_OTG_ID	GPIO1_IO00	I/O	Clock signal of I2C channel #2	I2C2_SCL
S115/235	CSI_VSYNC	CSI_VSYNC	I/O	Data signal of I2C channel #2	I2C2_SDA
S97/199 **P140/288** **S55/109**	AIN0 GPIO1 BL_PWR_EN	GPIO1_IO1	I/O	Data signal of I2C channel #2	I2C2_SDA

i.MX 6UltraLite I2C interface #3 are located on the following pins (as alternative functions).

EACOM Board Pin	EACOM Board Name	i.MX 6UltraLite Ball Name	I/O	Description	Remarks
P105/218	COM board specific	(ENET2_RXD0)	I/O	Clock signal of I2C channel #3	I2C3_SCL **Note**: pin only available of Ethernet

					interface #2 is not mounted.
S76/157	LCD_B1	LCD_DATA01	I/O	Clock signal of I2C channel #3	I2C3_SCL
P137/282	UART-A_TXD	UART1_TX	I/O	Clock signal of I2C channel #3	I2C3_SCL
P104/216	COM board specific	(ENET2_RXD1)	I/O	Data signal of I2C channel #3	I2C3_SDA **Note**: pin only available of Ethernet interface #2 is not mounted.
S75/149	LCD_B0	LCD_DATA00	I/O	Data signal of I2C channel #3	I2C3_SDA
P134/276	UART-A_RXD	UART1_RX	I/O	Data signal of I2C channel #3	I2C3_SDA

i.MX 6UltraLite I2C interface #4 can are located on the following pins (as alternative functions).

EACOM Board Pin	EACOM Board Name	i.MX 6UltraLite Ball Name	I/O	Description	Remarks
P102/212	COM board specific	(ENET2_CRS_DV)	I/O	Clock signal of I2C channel #4	I2C4_SCL **Note**: pin only available of Ethernet interface #2 is not mounted.
S78/161	LCD_B3	LCD_DATA03	I/O	Clock signal of I2C channel #4	I2C4_SCL
P133/274	UART-B_TXD	UART2_TX	I/O	Clock signal of I2C channel #4	I2C4_SCL
P109/226	COM board specific	(ENET2_TXD0)	I/O	Data signal of I2C channel #4	I2C4_SDA **Note**: pin only available of Ethernet interface #2 is not mounted.
S77/159	LCD_B2	LCD_DATA02	I/O	Data signal of I2C channel #4	I2C4_SDA
P130/268	UART-B_RXD	UART2_RX	I/O	Data signal of I2C channel #4	I2C4_SDA

5.11 JTAG

This section lists signals related to the JTAG debug interface.

The i.MX 6UltraLite SoC has a module called System JTAG Controller (SJC) that provides a JTAG interface to internal logic, including the four ARM Cortex-A9 cores. The SJC complies with JTAG TAP standards. The i.MX 6UltraLite SoC use the JTAG port for production, testing, and system debugging.

The JTAG signals are not available on the MXM3 edge connector. Instead the signals are available via a 10 pos FPC connector, see picture below for location and orientation.

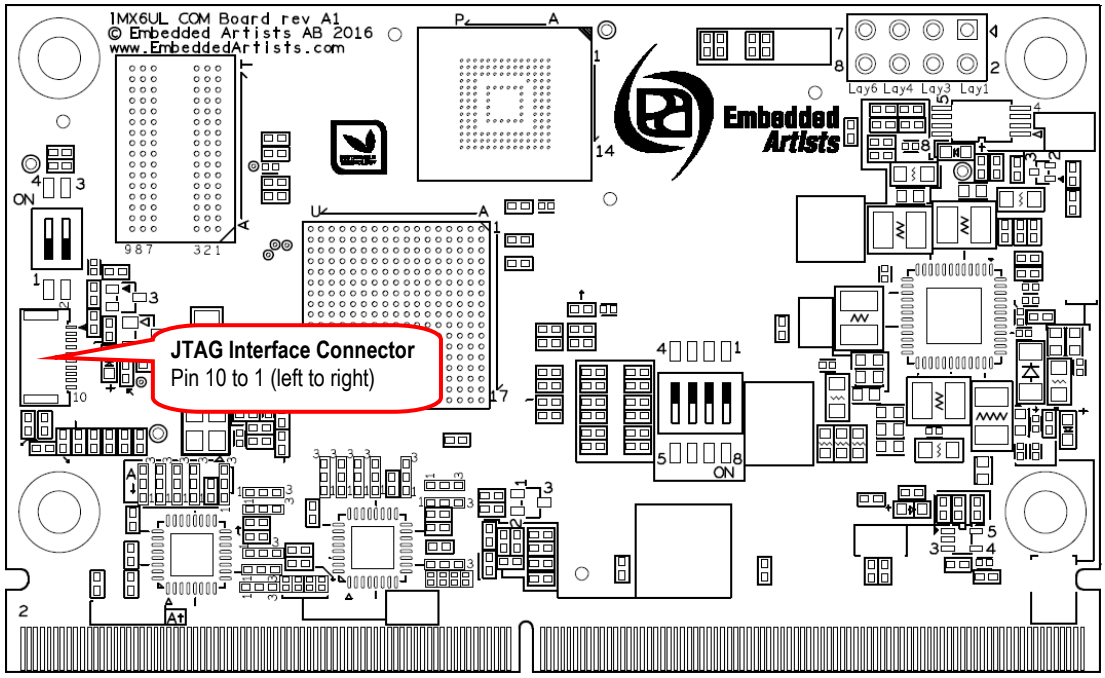


Figure 6 – iMX6 UltraLite COM Board, Top Side

The table below lists the 10 signals on the JTAG connector.

J1 Pin Number	Connected to i.MX 6UltraLite Ball Name	I/O	Description	Remarks
1	NVCC_JTAG	O	Logic level supply voltage	Used by external debugger to detect logic level to use for signaling. Typically 3.3V.
2	JTAG_TMS	I	JTAG signal TMS	
3			Ground	
4	JTAG_TCK	I	JTAG signal TCK	
5			Ground	
6	JTAG_TDO	O	JTAG signal TDO	
7	JTAG_MOD	I		Signal shall always be connected to ground. Signal has a 1Kohm pulldown resistor and can be left floating.
8	JTAG_TDI	I	JTAG signal TDI	
9	JTAG_TRST	I	JTAG signal TRST	Signal has a 10Kohm pullup resistor.
10	JTAG_SRST	I	System reset	Signal is active low and controls internal system, reset via buffer. Signal has a 10K ohm pullup resistor.

The *iMX6 UltraLite Developer's Kit* contains an adapter board for connection to common debug connectors. The 10 pos connector is Molex 512811094 and has 0.5 mm (20 mil) pitch. FPC length should be kept less than 7 cm.

5.12 Power Management

This section lists signals related to power management, i.e., reset and external power supplies.

EACOM Board Pin	EACOM Board Name	I/O	Description	Remarks
P143/294	RESET_OUT	O	Reset output, active low	Open drain output. Driven low during reset. 1.5K pull-up resistor to VIN.

P142/292	RESET_IN	I	Reset input, active low	Pull signal low to activate reset. No need to pull signal high externally. Connected to cathode of series diode, so logic level of driving signal can be anywhere between 1.5-5 V.
P141/290	PERI_PWR_EN	O	Enable signal (active high) for carrier board peripheral power supplies.	Uses pin SNVS_TAMPER2 (controlled as GPIO5_IO02) on the i.MX 6UltraLite. More information about carrier board design can be found in *EACOM Board specification*.

5.13 Power Supply Signals

This section lists signals related to power supply.

EACOM Board Pin	EACOM Board Name	I/O	Description	Remarks
P147/302, P148/304, P149/306, P150/308, P151/310, P152/312, P153/314, P154/316, P155/318, P156/320	VIN	A	3.3V supply voltage	See technical specification for details about valid range.
P22/44, P25/50, P31/62, P35/70, P38/76, P46/92, P49/98, P52/104, P60/120, P63/126, P69/138, P77/162, P82/172, P88/184, P91/190, P118/244, P127/262, P144/296, S3/5, S9/17, S16/31, S22/43, S25/49, S28/55, S31/61, S37/73, S40/79, S43/85, S57/113, S74/147, S88/181, S98/201, S101/207, S104/213, S118/241, S127/259, S130/265, S133/271, S136/277, S139/283, S142/289, S145/295, S148/301, S149/303, S152/309, S155/315, S158/321	GND	A	Ground	
P145/298	VBAT	AI/AO	Power supply for MMPF3000 PMIC and i.MX 6UltraLite on-chip RTC. Connect to external primary (= non rechargeable) or secondary (= rechargeable) coin cell battery.	Connected to MMPF3000 PMIC, pin 36, LICELL. PMIC can be programmed to charge a secondary coin cell.

5.14 PWM

This section lists signals related to Pulse Wide Modulators (PWM).

The i.MX 6UltraLite SoC has eight PWM channels that are available via pin multiplexing. The generated signals has 16-bit resolution. PWM signals can be used to for example generate analogue signals (emulate a DAC) and control intensity / brightness in display applications.

There are two PWM signals defined in the *EACOM Board specification*. One general PWM signal and one that is intended for backlight intensity control for displays. Due to limited number of available signals, the same PWM signal is connected to both these EACOM defined pins.

The table below lists the pin assignment as well as alternative pin locations.

EACOM	EACOM	i.MX 6UltraLite	I/O	Description	Remarks

Board Pin	Board Name	Ball Name			
P138/284 **S56/111**	PWM1 BL_PWM	GPIO1_IO08	O	PWM1_OUT signal	
P99/206	COM board specific	(ENET1_RXD0)	O	PWM1_OUT signal	Available as alternative signal. **Note:** Only available if ENET1 not mounted.
S75/149	LCD_B0	LCD_DATA00	O	PWM1_OUT signal	Available as alternative signal.
P98/204	COM board specific	(ENET1_RXD1)	O	PWM2_OUT signal	Available as alternative signal. **Note:** Only available if ENET1 not mounted.
P4/8	GPIO3	GPIO1_IO09	O	PWM2_OUT signal	Available as alternative signal.
S76/157	LCD_B1	LCD_DATA01	O	PWM2_OUT signal	Available as alternative signal.
S53/105 **S94/193**	TP_IRQ AIN3	GPIO1_IO04	O	PWM3_OUT signal	Available as alternative signal.
S77/159	LCD_B2	LCD_DATA02	O	PWM3_OUT signal	Available as alternative signal.
P89/186	USB_H2_DN	GPIO1_IO05	O	PWM4_OUT signal	Note that pin GPIO1_IO05 function as signal SD1_VSELECT and is connected to SD_VSEL on PF3000 PMIC. The signal can be used if the SD1 interface is not used.
S78/161	LCD_B3	LCD_DATA03	O	PWM4_OUT signal	Available as alternative signal.
P113/234	COM board specific	NAND_WP	O	PWM4_OUT signal	Available as alternative signal.
P94/196	COM board specific	(ENET1_TXD1)	O	PWM5_OUT signal	Available as alternative signal. **Note:** Only available if ENET1 not mounted..
S60/119	LCD_R2	LCD_DATA18	O	PWM5_OUT signal	Available as alternative signal.
S52/103	TP_RST	NAND_DQS	O	PWM5_OUT signal	Available as alternative signal.
P93/194	COM board specific	(ENET1_TXEN)	O	PWM6_OUT signal	Available as alternative signal. **Note:** Only available if ENET1 not mounted.
S2/3 **S6/11**	MQS_LEFT AUDIO_TXC	JTAG_TDI	O	PWM6_OUT signal	Available as alternative signal. **Note:** Signals also connected to JTAG interface
S61/121	LCD_R3	LCD_DATA19	O	PWM6_OUT signal	Available as alternative signal.
S86/177	LCD_VSYNC	LCD_VSYNC	O	PWM7_OUT signal	Available as alternative signal.
P92/192	COM board specific	(ENET1_TX_CLK)	O	PWM7_OUT signal	Available as alternative signal. **Note:** Only available if ENET1 not mounted.
S5/9	AUDIO_RXD	JTAG_TCK	O	PWM7_OUT signal	Available as alternative signal. **Note:** Signals also connected to JTAG interface
S85/175	LCD_HSYNC	LCD_HSYNC	O	PWM8_OUT signal	Available as alternative signal.
P96/200	COM board specific	(ENET1_RXER)	O	PWM8_OUT signal	Available as alternative signal. **Note:** Only available if ENET1 not mounted.
S7/13	AUDIO_TXD	JTAG_TRST	O	PWM8_OUT signal	Available as alternative signal. **Note:** Signals also connected to JTAG interface

5.15 SD/MMC

This section lists signals related to Ultra Secured Digital Host Controller (uSDHC) functions.

The i.MX 6UltraLite SoC has 2 uSDHC interfaces. One, uSDHC2, is allocated (on-board) for interface to eMMC Flash (8-bit MMC interface).

The uSDHC interface is capable of interfacing with SD Memory Cards, SDIO, MMC, CE-ATA cards and eMMC devices. The features of the uSDHC module include the following:

- Conforms to the SD Host Controller Standard Specification version 3.0
- Compatible with the MMC System Specification version 4.2/4.3/4.4/4.41

- Compatible with the SD Memory Card Specification version 3.0 and supports the Extended Capacity SD Memory Card
- Compatible with the SDIO Card Specification version 3.0
- Designed to work with SD Memory, miniSD Memory, SDIO, miniSDIO, SD Combo, MMC, MMC plus, and MMC RS cards
- Supports 1-bit / 4-bit SD and SDIO modes, 1-bit / 4-bit / 8-bit MMC modes

The *EACOM Board specification* defines one 4-databit uSDHC interface (uSDHC1) and one 8-databit uSDHC interface (not allocated since there are no more uSDHC interfaces).

The table below lists the pin assignment according to *EACOM Board specification*.

EACOM Board Pin	EACOM Board Name	i.MX 6UltraLite Ball Name	I/O	Description	Remarks
P7/14	SD_CLK	SD1_CLK	O	Clock for MMC/SD/SDIO card	
P8/16	SD_CMD	SD1_CMD	I/O	CMD line connect to card	
P6/12	SD_D0	SD1_DATA0	I/O	DATA0 line in all modes. Also used to detect busy status	
P5/10	SD_D1	SD1_DATA1	I/O	DATA1 line in 4/8-bit mode. Also used to detect interrupt in 1/4-bit mode	
P10/20	SD_D2	SD1_DATA2	I/O	DATA2 line or Read Wait in 4-bit mode, Read Wait in 1-bit mode	
P9/18	SD_D3	SD1_DATA3	I/O	DATA3 line in 4/8-bit mode or configured as card detection pin. May be configured as card detection pin in 1-bit mode	
P11/22	SD_VCC		PWR	Supply voltage for SD interface (3.3V). Should only supply the SD interface.	
P16/32	MMC_CLK				Not connected
P18/36	MMC_CMD				Not connected
P13/26	MMC_D0				Not connected
P12/24	MMC_D1				Not connected
P10/20	MMC_D2				Not connected
P20/40	MMC_D3				Not connected
P19/38	MMC_D4				Not connected
P17/34	MMC_D5				Not connected
P15/30	MMC_D6				Not connected
P14/28	MMC_D7				Not connected

The table below lists of alternative pin locations for uSDHC1 signals as well as data signals 4-7 (for full 8-bit MMC interface).

EACOM Board Pin	EACOM Board Name	i.MX 6UltraLite Ball Name	I/O	Description	Remarks
P123/254	SPI-A_SSEL	NAND_READY	I/O	DATA4 line in 8-bit mode, not used in other modes	Alternative function SD1_DATA4
P126/260	SPI-A_CLK	NAND_CE0	I/O	DATA5 line in 8-bit mode, not used in other modes	Alternative function SD1_DATA5
P124/256	SPI-A_MOSI	NAND_CE1	I/O	DATA6 line in 8-bit mode, not used in other modes	Alternative function SD1_DATA6
P125/258	SPI-A_MISO	NAND_CLE	I/O	DATA7 line in 8-bit mode, not used in other modes	Alternative function SD1_DATA7
S124/253	CSI_D5	CSI_DATA5	I	Card detection pin	Alternative function SD1_CD_B
S95/195 **P3/6**	AIN2 GPIO4	GPIO1_IO3	I	Card detection pin	Alternative function SD1_CD_B

P136/280	UART-A_RTS	UART1_RTS_B	I	Card detection pin	Alternative function SD1_CD_B
P89/186	USB_H2_DN	GPIO1_IO05	O	IO power voltage selection signal	Alternative function SD1_VSELECT **Note** that pin GPIO1_IO05 is connected to SD_VSEL on PF3000 PMIC.
P99/206	COM board specific	(ENET1_RXD0)	O	LED control used to drive an external LED Active high	Alternative function SD1_LCTL **Note:** Only available if ENET1 not mounted.
S123/251	CSI_D4	CSI_DATA4	I	Card write protect detect	Alternative function SD1_WP.
P139/286 **S96/197**	GPIO2 AIN1	GPIO1_IO02	I	Card write protect detect	Alternative function SD1_WP.
P135/278	UART-A_CTS	UART1_CTS_B	I	Card write protect detect	Alternative function SD1_WP.
S125/255	CSI_D6	CSI_DATA6	O	Card hardware reset signal, active LOW	Alternative function SD1_RESET_B
S94/193 **S53/105**	AIN3 TP_IRQ	GPIO1_IO4	O	Card hardware reset signal, active LOW	Alternative function SD1_RESET_B
P4/8	GPIO3	GPIO1_IO09	O	Card hardware reset signal, active LOW	Alternative function SD1_RESET_B
P113/234	COM board specific	NAND_WP	O	Card hardware reset signal, active LOW	Alternative function SD1_RESET_B

There are no accessible pins for uSDHC2 signals since these are connected to the on-board eMMC Flash.

5.16 ECSPI / SPI

This section lists signals related to Enhanced Configurable Serial Peripheral Interface (ECSPI) functions.

The i.MX 6UltraLite SoC has four ECSPI block that are capable of full-duplex, synchronous, four-wire serial communication. The *EACOM Board specification* defines two 4-signal SPI interfaces. Only one of these (ECSPI3) has been allocated due to limited number of available pins on the i.MX 6UltraLite SoC. The remaining ECSPI signals are available as alternative functions on certain pins.

The table below lists the pin assignment according to *EACOM Board specification*.

EACOM Board Pin	EACOM Board Name	i.MX 6UltraLite Ball Name	I/O	Description	Remarks
P125/258	SPI-A_MISO	NAND_CLE	I/O	Master data in, slave data out	ECSPI3_MISO
P124/256	SPI-A_MOSI	NAND_CE1	I/O	Master data out, slave data in	ECSPI3_MOSI
P126/260	SPI-A_SCLK	NAND_CE0	I/O	SPI clock signal	ECSPI3_SCLK
P123/254	SPI-A_SS0	NAND_READY	I/O	Chip select signal	ECSPI3_SS0
P121/250	SPI-B_MISO				Not connected
P120/248	SPI-B_MOSI				Not connected
P122/252	SPI-B_SCLK				Not connected
P119/246	SPI-B_SS0				Not connected

The table below lists of alternative pin locations for ECSPI1 signals.

EACOM Board Pin	EACOM Board Name	i.MX 6UltraLite Ball Name	I/O	Description	Remarks

S126/257	CSI_D7	CSI_DATA7	I/O	Master data in, slave data out	ECSPI1_MISO
S65/129	LCD_R7	LCD_DATA23	I/O	Master data in, slave data out	ECSPI1_MISO
S125/255	CSI_D6	CSI_DATA6	I/O	Master data out, slave data in	ECSPI1_MOSI
S64/127	LCD_R6	LCD_DATA22	I/O	Master data out, slave data in	ECSPI1_MOSI
S70/139	LCD_G4	LCD_DATA12	I/O	SPI data ready signal	ECSPI1_RDY
S123/251	CSI_D4	CSI_DATA4	I/O	SPI clock signal	ECSPI1_SCLK
S62/123	LCD_R4	LCD_DATA20	I/O	SPI clock signal	ECSPI1_SCLK
S124/253	CSI_D5	CSI_DATA5	I/O	Chip select signal	ECSPI1_SS0
S63/125	LCD_R5	LCD_DATA21	I/O	Chip select signal	ECSPI1_SS0
S80/165	LCD_B5	LCD_DATA05	I/O	Chip select signal	ECSPI1_SS1
S81/167	LCD_B6	LCD_DATA06	I/O	Chip select signal	ECSPI1_SS2
S82/169	LCD_B7	LCD_DATA07	I/O	Chip select signal	ECSPI1_SS3

The table below lists of alternative pin locations for ECSPI2 signals.

EACOM Board Pin	EACOM Board Name	i.MX 6UltraLite Ball Name	I/O	Description	Remarks
S122/249	CSI_D3	CSI_DATA3	I/O	Master data in, slave data out	ECSPI2_MISO
S48/95	I2C-B_SDA	UART5_RX	I/O	Master data in, slave data out	ECSPI2_MISO **Note**: This pin allocation is not recommended since there is a 2.2Kohm pull-up resistor on this signal. It is allocated as an I2C signal.
S121/247	CSI_D2	CSI_DATA2	I/O	Master data out, slave data in	ECSPI2_MOSI
S49/97	I2C-B_SCL	UART5_TX	I/O	Master data out, slave data in	ECSPI2_MOSI **Note**: This pin allocation is not recommended since there is a 2.2Kohm pull-up resistor on this signal. It is allocated as an I2C signal.
S87/179	LCD_ENABLE	LCD_DE	I/O	SPI data ready signal	ECSPI2_RDY
S119/243	CSI_D0	CSI_DATA0	I/O	SPI clock signal	ECSPI2_SCLK
S120/245	CSI_D1	CSI_DATA1	I/O	Chip select signal	ECSPI2_SS0
S85/175	LCD_HSYNC	LCD_HSYNC	I/O	Chip select signal	ECSPI2_SS1
S86/177	LCD_VSYNC	LCD_VSYNC	I/O	Chip select signal	ECSPI2_SS2

The table below lists of alternative pin locations for ECSPI3 signals. Note that this interface is allocation to the EACOM defined pins, see above.

EACOM Board Pin	EACOM Board Name	i.MX 6UltraLite Ball Name	I/O	Description	Remarks
S13/25 P132/272	CAN2_RX UART-B_RTS	UART2_RTS	I/O	Master data in, slave data out	ECSPI3_MISO
S12/23 P131/270	CAN2_TX UART-B_CTS	UART2_CTS	I/O	Master data out, slave data in	ECSPI3_MOSI
P113/234	COM board specific	NAND_WP	I/O	SPI data ready signal	ECSPI3_RDY
P134/276	UART-A_RXD	UART1_RX	I/O	SPI clock signal	ECSPI3_SCLK
P133/274	UART-B_TXD	UART2_TX	I/O	Chip select signal	ECSPI3_SS0

The table below lists of alternative pin locations for ECSPI4 signals.

EACOM Board Pin	EACOM Board Name	i.MX 6UltraLite Ball Name	I/O	Description	Remarks
P106/220	COM board specific	(ENET2_TX_CLK)	I/O	Master data in, slave data out	ECSPI4_MISO **Note:** Only available if ENET2 not mounted.
P107/222	COM board specific	(ENET2_TXEN)	I/O	Master data out, slave data in	ECSPI4_MOSI **Note:** Only available if ENET2 not mounted.
P108/224	COM board specific	(ENET2_TXD1)	I/O	SPI clock signal	ECSPI4_SCLK **Note:** Only available if ENET2 not mounted.
P103/214	COM board specific	(ENET2_RXER)	I/O	Chip select signal	ECSPI4_SS0 **Note:** Only available if ENET2 not mounted.

5.17 UART

This section lists signals related to Universal Asynchronous Receiver/Transmitter (UART) functions.

The i.MX 6UltraLite SoC has eight UARTs, supporting bitrates up to 5Mbps each. The *EACOM Board specification* defines two 4-signal UARTs and one 2-signal UART. The remaining UART signals are available as alternative functions on certain pins.

Note that the chip-level IOMUX modifies the direction and routing of the UART signals based on whether the UART is operating in DCE mode or DTE mode. See section 53.2 in IMX6ULRM for details.

The table below lists the pin assignment according to *EACOM Board specification*.

EACOM Board Pin	EACOM Board Name	i.MX 6UltraLite Ball Name	I/O	Description	Remarks
P137/282	UART-A_TXD	UART1_TX	I/O	UART4 Transmit Data	
P134/276	UART-A_RXD	UART1_RX	I/O	UART4 Receive Data	
P136/280	UART-A_RTS	UART1_RTS	I/O	UART4 Request to Send	
P135/278	UART-A_CTS	UART1_CTS	I/O	UART4 Clear to Send	
P133/274	UART-B_TXD	UART2_TX	I/O	UART5 Transmit Data	
P130/268	UART-B_RXD	UART2_RX	I/O	UART5 Receive Data	
P132/272 **S13/25**	UART-B_RTS CAN2_RX	UART2_RTS	I/O	UART5 Request to Send	**Note:** Signals also connected to two EACOM pins
P131/270 **S12/23**	UART-B_CTS CAN2_TX	UART2_CTS	I/O	UART5 Clear to Send	**Note:** Signals also connected to two EACOM pins
P129/266	UART-C_TXD	UART3_TX	I/O	UART1 Transmit Data	
P128/264	UART-C_RXD	UART3_RX	I/O	UART1 Receive Data	

The table below lists of alternative pin locations for UART1 signals.

EACOM Board Pin	EACOM Board Name	i.MX 6UltraLite Ball Name	I/O	Description	Remarks
P139/286 **S54/107** **S96/197**	GPIO2 DISP_PWR_EN AIN1	GPIO1_IO02	I/O	UART1 Transmit Data	Alternative function is UART1_TXD
P3/6	GPIO4	GPIO1_IO03	I/O	UART1 Receive Data	Alternative function is UART1_RXD
P100/208	COM board specific	(GPIO1_IO07)	I/O	UART1 Request to Send	Alternative function is UART1_RTS_B **Note**: Only available if ENET1 and ENET2 are not mounted.
P101/210	COM board specific	(GPIO1_IO06)	I/O	UART1 Clear to Send	Alternative function is UART1_CTS_B **Note**: Only available if ENET1 and ENET2 are not mounted.

The table below lists of alternative pin locations for UART2 signals.

EACOM Board Pin	EACOM Board Name	i.MX 6UltraLite Ball Name	I/O	Description	Remarks
P128/264	UART-C_RXD	UART3_RX	I/O	UART2 Request to Send	Alternative function is UART2_RTS_B.
P129/266	UART-C_TXD	UART3_TX	I/O	UART2 Clear to Send	Alternative function is UART2_CTS_B.

The table below lists of alternative pin locations for UART3 signals.

EACOM Board Pin	EACOM Board Name	i.MX 6UltraLite Ball Name	I/O	Description	Remarks
P123/254	SPI-A_SSEL	NAND_READY	I/O	UART3 Transmit Data	Alternative function is UART3_TXD.
P126/260	SPI-A_CLK	NAND_CE0	I/O	UART3 Receive Data	Alternative function is UART3_RXD.
P125/258	SPI-A_MISO	NAND_CLE	I/O	UART3 Request to Send	Alternative function is UART3_RTS_B.
S15/29	CAN1_RX	UART3_RTS	I/O	UART3 Request to Send	Alternative function is UART3_RTS_B.
P124/256	SPI-A_MOSI	NAND_CE1	I/O	UART3 Clear to Send	Alternative function is UART3_CTS_B.
S14/27	CAN1_TX	UART3_CTS	I/O	UART3 Clear to Send	Alternative function is UART3_CTS_B.

The table below lists of alternative pin locations for UART4 signals.

EACOM Board Pin	EACOM Board Name	i.MX 6UltraLite Ball Name	I/O	Description	Remarks
S83/171	LCD_CLK	LCD_PCLK	I/O	UART4 Transmit Data	Alternative function is UART4_TXD.
S87/179	LCD_ENABLE	LCD_DE	I/O	UART4 Receive Data	Alternative function is UART4_RXD.
P99/206	COM board specific	(ENET1_RXD0)	I/O	UART4 Request to Send	Alternative function is UART4_RTS_B. **Note:** Only available if ENET1 not mounted
S86/177	LCD_VSYNC	LCD_VSYNC	I/O	UART4 Request to Send	Alternative function is UART4_RTS_B.
P98/204	COM board specific	(ENET1_RXD1)	I/O	UART4 Clear to Send	Alternative function is UART4_CTS_B. **Note:** Only available if ENET1 not mounted
S85/175	LCD_HSYNC	LCD_HSYNC	I/O	UART4 Clear to Send	Alternative function is UART4_CTS_B.

The table below lists of alternative pin locations for UART5 signals.

EACOM Board Pin	EACOM Board Name	i.MX 6UltraLite Ball Name	I/O	Description	Remarks
S119/243	CSI_D0	CSI_DATA0	I/O	UART5 Transmit Data	Alternative function is UART5_TXD.
S53/105 **S94/193**	TP_IRQ AIN3	GPIO1_IO04	I/O	UART5 Transmit Data	Alternative function is UART5_TXD.
S49/97	I2C-B_SCL	UART5_TX	I/O	UART5 Transmit Data	Alternative function is UART5_TXD. **Note**: This pin allocation is not recommended since there is a 2.2Kohm pull-up resistor on this signal. It is allocated as an I2C signal.
S120/245	CSI_D1	CSI_DATA1	I/O	UART5 Receive Data	Alternative function is UART5_RXD.
P89/186	USB_H2_DN	GPIO1_IO05	I/O	UART5 Receive Data	Alternative function is UART5_RXD. **Note** that pin GPIO1_IO05 is connected to SD_VSEL on PF3000 PMIC. It can only be used if interface SD1 is not used.
S48/95	I2C-B_SDA	UART5_RX	I/O	UART5 Receive Data	Alternative function is UART5_RXD.

					Note: This pin allocation is not recommended since there is a 2.2Kohm pull-up resistor on this signal. It is allocated as an I2C signal.
S121/247	CSI_D2	CSI_DATA2	I/O	UART5 Request to Send	Alternative function is UART5_RTS_B.
P97/202	COM board specific	(ENET1_CRS_DV)	I/O	UART5 Request to Send	Alternative function is UART5_RTS_B. **Note:** Only available if ENET1 not mounted.
P138/284 S56/111	PWM BL_PWM	GPIO1_IO08	I/O	UART5 Request to Send	Alternative function is UART5_RTS_B.
S122/249	CSI_D3	CSI_DATA3	I/O	UART5 Clear to Send	Alternative function is UART5_CTS_B.
P95/198	COM board specific	(ENET1_TXD0)	I/O	UART5 Clear to Send	Alternative function is UART5_CTS_B. **Note:** Only available if ENET1 not mounted.
P4/8	GPIO3	GPIO1_IO09	I/O	UART5 Clear to Send	Alternative function is UART5_CTS_B.

The table below lists of alternative pin locations for UART6 signals.

EACOM Board Pin	EACOM Board Name	i.MX 6UltraLite Ball Name	I/O	Description	Remarks
S116/237	CSI_MCLK	CSI_MCLK	I/O	UART6 Transmit Data	Alternative function is UART6_TXD.
P105/218	COM board specific	(ENET2_RXD0)	I/O	UART6 Transmit Data	Alternative function is UART6_TXD. **Note:** Only available if ENET2 not mounted.
S117/239	CSI_PCLK	CSI_PIXCLK	I/O	UART6 Receive Data	Alternative function is UART6_RXD.
P104/216	COM board specific	(ENET2_RXD1)	I/O	UART6 Receive Data	Alternative function is UART6_RXD. **Note:** Only available if ENET2 not mounted.
S115/235	CSI_VSYNC	CSI_VSYNC	I/O	UART6 Request to Send	Alternative function is UART6_RTS_B.
P93/194	COM board specific	(ENET1_TXEN)	I/O	UART6 Request to Send	Alternative function is UART6_RTS_B. **Note:** Only available if ENET1 not mounted.
S114/233	CSI_HSYNC	CSI_HSYNC	I/O	UART6 Clear to Send	Alternative function is UART6_CTS_B.
P94/196	COM board specific	(ENET1_TXD1)	I/O	UART6 Clear to Send	Alternative function is UART6_CTS_B. **Note:** Only available if ENET1 not mounted.

The table below lists of alternative pin locations for UART7 signals.

EACOM Board Pin	EACOM Board Name	i.MX 6UltraLite Ball Name	I/O	Description	Remarks
P102/212	COM board specific	(ENET2_CRS_DV)	I/O	UART7 Transmit Data	Alternative function is UART7_TXD. **Note:** Only available if ENET2 not mounted.
S58/115	LCD_R0	LCD_DATA16	I/O	UART7 Transmit Data	Alternative function is UART7_TXD.
P109/226	COM board specific	(ENET2_TXD0)	I/O	UART7 Receive Data	Alternative function is UART7_RXD. **Note:** Only available if ENET2 not mounted.
S59/117	LCD_R1	LCD_DATA17	I/O	UART7 Receive Data	Alternative function is UART7_RXD.
P96/200	COM board specific	(ENET1_RXER)	I/O	UART7 Request to Send	Alternative function is UART7_RTS_B. **Note:** Only available if ENET1 not mounted.
S82/169	LCD_B7	LCD_DATA07	I/O	UART7 Request to Send	Alternative function is UART7_RTS_B.
P92/192	COM board	(ENET1_TX_CLK)	I/O	UART7 Clear to Send	Alternative function is UART7_CTS_B. **Note:** Only available if ENET1 not

	specific				mounted.
S81/167	LCD_B6	LCD_DATA06	I/O	UART7 Clear to Send	Alternative function is UART7_CTS_B.

The table below lists of alternative pin locations for UART8 signals.

EACOM Board Pin	EACOM Board Name	i.MX 6UltraLite Ball Name	I/O	Description	Remarks
P108/224	COM board specific	(ENET2_TXD1)	I/O	UART8 Transmit Data	Alternative function is UART8_TXD. **Note:** Only available if ENET2 not mounted.
S62/123	LCD_R4	LCD_DATA20	I/O	UART8 Transmit Data	Alternative function is UART8_TXD.
P107/222	COM board specific	(ENET2_TXEN)	I/O	UART8 Receive Data	Alternative function is UART8_RXD. **Note:** Only available if ENET2 not mounted.
S63/125	LCD_R5	LCD_DATA21	I/O	UART8 Receive Data	Alternative function is UART8_RXD.
P103/214	COM board specific	(ENET2_RXER)	I/O	UART8 Request to Send	Alternative function is UART8_RTS_B. **Note:** Only available if ENET2 not mounted.
S80/165	LCD_B5	LCD_DATA05	I/O	UART8 Request to Send	Alternative function is UART8_RTS_B.
P106/220	COM board specific	(ENET2_TX_CLK)	I/O	UART8 Clear to Send	Alternative function is UART8_CTS_B. **Note:** Only available if ENET2 not mounted.
S79/163	LCD_B4	LCD_DATA04	I/O	UART8 Clear to Send	Alternative function is UART8_CTS_B.

5.18 USB

This section lists signals related to the USB interfaces.

The *EACOM Board Specification* has one USB 3.0 OTG port, one USB 3.0 Host port and one USB 2.0 Host port. The i.MX 6UltraLite has two USB 2.0 OTG ports. Further, USB 3.0 is backward compatible with USB 2.0. The pins that are specific for USB 3.0 are just left unconnected and are for future upgrade.

The carrier board must provide a +5V supply (with enable and over-current functionality) for USB Host interfaces.

EACOM Board Pin	EACOM Board Name	i.MX 6UltraLite Ball Name	I/O	Description	Remarks
P64/128	USB_O1_DN	USB_OTG1_DN	I/O	Negative Differential USB Signal, OTG compatible	
P65/130	USB_O1_DP	USB_OTG1_DP	I/O	Positive Differential USB Signal, OTG compatible	
P66/132	USB_O1_OTG_ID	GPIO1_IO00	I	USB OTG ID pin	
P67/134	USB_O1_SSTXN				Not connected
P68/136	USB_O1_SSTXP				Not connected
P70/140	USB_O1_SSRXN				Not connected
P71/142	USB_O1_SSRXP				Not connected
P72/144	USB_O1_VBUS	USB_OTG_VBUS	I	+5V USB VBUS detect input	This pin is +5V tolerant.
P73/146	USB_O1_PWR_EN		O	Enable external USB voltage supply. Active high output.	Connected to 4.7Kohm pull-up resistor to 3.3V, meaning that the power control for this USB interface is always on. Signal is also controlled by pin USB_O1_OTG_ID. If this pin is

					pulled high externally, this pin (USB_O1_PWR_EN) will be pulled low.
P74/148	USB_O1_OC		I	Signals an over-current condition on the USB voltage supply. Active low input.	Pin is connected directly to pin USB_O1_PWR_EN. If signal is pulled low externally, pin USB_O1_PWR_EN will also be pulled low.
P75/158	USB_H1_PWR_EN		O	Enable external USB voltage supply. Active high output.	Connected to 4.7Kohm pull-up resistor to 3.3V, meaning that the power control for this USB interface is always on.
P76/160	USB_H1_OC		I	Signals an over-current condition on the USB voltage supply. Active low input.	Pin is connected directly to pin USB_H1_PWR_EN. If signal is pulled low externally, pin USB_H1_PWR_EN will also be pulled low.
P78/164	USB_H1_DN	USB_OTG2_DN	I/O	Negative Differential USB Signal	
P79/166	USB_H1_DP	USB_OTG2_DP	I/O	Positive Differential USB Signal	
P80/168	USB_H1_SSTXN				Not connected
P81/170	USB_H1_SSTXP				Not connected
P83/174	USB_H1_SSRXN				Not connected
P84/176	USB_H1_SSRXP				Not connected
P85/178	USB_H1_VBUS	USB_OTG2_VBUS	I	+5V USB VBUS detect input	This pin is +5V tolerant.

The table below lists of alternative pin locations for USB OTG1 signals.

EACOM Board Pin	EACOM Board Name	i.MX 6UltraLite Ball Name	I/O	Description	Remarks
P6/12	SD_D0	SD1_DATA0	I	USB OTG1 ID	
P128/264	UART-C_RXD	UART3_TX	I	USB OTG1 ID	
P104/216	COM board specific	(ENET2_RXD1)	I	USB OTG1 OC	Signals an over-current condition on the USB voltage supply. Active low input. **Note:** Only available if ENET2 not mounted.
P140/288 **S55/109** **S97/199**	GPIO1 BL_PWR_EN AIN0	GPIO1_IO01	I	USB OTG1 OC	Signals an over-current condition on the USB voltage supply. Active low input.
P7/14	SD_CLK	SD1_CLK	I	USB OTG1 OC	Signals an over-current condition on the USB voltage supply. Active low input.
P105/218	COM board specific	(ENET2_RXD0)	O	USB OTG PWR EN	Enable external USB voltage supply. Active high output. **Note:** Only available if ENET2 not mounted.
S53/105 **S94/193**	TP_IRQ AIN3	GPIO1_IO04	O	USB OTG PWR EN	Enable external USB voltage supply. Active high output.
P8/16	SD_CMD	SD1_CMD	O	USB OTG PWR EN	Enable external USB voltage supply. Active high output.

The table below lists of alternative pin locations for USB OTG2 signals.

EACOM Board Pin	EACOM Board Name	i.MX 6UltraLite Ball Name	I/O	Description	Remarks

P106/220	COM board specific	(ENET2_TX_CLK)	I	USB OTG2 ID	**Note:** Only available if ENET2 not mounted.
P89/186	USB_H2_DN	GPIO1_IO05	I	USB OTG2 ID	**Note** that pin GPIO1_IO05 function as signal SD1_VSELECT and is connected to SD_VSEL on PF3000 PMIC. The signal can be used if the SD1 interface is not used.
P9/18	SD_D3	SD1_DATA3	I	USB OTG2 ID	
P107/222	COM board specific	(ENET2_TXEN)	I	USB OTG2 OC	Signals an over-current condition on the USB voltage supply. Active low input. **Note:** Only available if ENET2 not mounted.
P3/6 **S95/195**	GPIO4 AIN2	GPIO1_IO03	I	USB OTG2 OC	Signals an over-current condition on the USB voltage supply. Active low input.
P10/20	SD_D2	SD1_DATA2	I	USB OTG2 OC	Signals an over-current condition on the USB voltage supply. Active low input.
P108/224	COM board specific	(ENET2_TXD1)	O	USB OTG2 PWR EN	Enable external USB voltage supply. Active high output. **Note:** Only available if ENET2 not mounted.
P139/286 **S54/107** **S96/197**	GPIO2 DISP_PWR_EN AIN1	GPIO1_IO02	O	USB OTG2 PWR EN	Enable external USB voltage supply. Active high output.
P5/10	SD_D1	SD1_DATA1	O	USB OTG2 PWR EN	Enable external USB voltage supply. Active high output.

Note that EACOM USB Host port #2 is not connected to a USB port on the i.MX 6UltraLite. Some other signals are connected to these pins in a non-standard way, see table below.

EACOM Board Pin	EACOM Board Name	i.MX 6UltraLite Ball Name	I/O	Description	Remarks
P86/180	USB_H2_PWR_EN	SNVS_TAMPER0	I/O	Not connected for USB functionality	
P87/182	USB_H2_OC	ONOFF signal, i.MX 6UltraLite ball R8	I	Not connected for USB functionality	
P89/186	USB_H2_DN	GPIO1_IO05	I/O	Not connected for USB functionality	Note that pin GPIO1_IO05 function as signal SD1_VSELECT and is connected to SD_VSEL on PF3000 PMIC. The signal can be used if the SD1 interface is not used.
P90/188	USB_H2_DP				Not connected

6 Boot Options

This chapter presents the different boot settings that the *iMX6 UltraLite COM Board* supports. This chapter will only present how the different options are controlled. Other documents discuss the pros and cons with different options and what general system architectures (with different booting phases) that are suitable in different situations.

The *iMX6 UltraLite COM Board* supports booting (i.e., from where the i.MX 6UltraLite SoC starts downloading code to start executing from) from different sources:

- On-board eMMC Flash (signal E2PROM_WP high/floating - default)
- USB OTG download (also called 'serial download'), (signal E2PROM_WP low)
- Other sources, like external SD/MMC memory cards, QSPI, SPI, etc.
  Note that the OTP fuses must be programmed to set these sources, see below.

Signal E2PROM_WP controls the booting source. If signal E2PROM_WP is high/floating, which is the default, booting takes place from eMMC. If Signal EPROM_WP is low, the i.MX 6UltraLite SoC boots into USB OTG mode. This latter mode it typically only used during production when the program images shall be downloaded the first time.

There are three main boot **modes** that controls which boot **source** to use.

- Boot according to on-board configuration pull-up/pull-down resistors
  - eMMC is set as default boot source.
  - **Note that signals LCD1_DATA00 - LCD1_DATA23 (EACOM pins LCD_B0-B7, LCD_G0-G7, LCD_R0-R7) must not be driven externally**. This is normally not a problem since these signals are typically used for a parallel RGB display output. There are often driving buffers between these pins and an external display.
    The reason why the pins must not be driven externally is that on-board resistors pull these signals high/low to select eMMC booting. Driving any of these signals can change this default behavior.
    If any of the signals are driven externally the on-chip OTP fuses must be programmed to force eMMC booting instead.
- Boot according to how internal (i.MX 6UltraLite on-chip) OTP fuses have been programmed
  - Any boot mode supported by the i.MX 6UltraLite SoC and the hardware connected to it can be selected. See i.MX 6UltraLite Reference Manual for details about available sources and OTP fuse settings.
  - Note that OTP fuse BT_FUSE_SEL must be set to 1 in order to override the default setting to boot from eMMC and to have OTP fuse settings controlling boot source instead.
  - Note that the ***iMX6 UltraLite COM Boards* have not programmed the on-chip OTP fuses**. Users have full control over these. This mode can only be used after having programmed the OTP fuses.
  - Programming OTP fuses is a critical operation. If wrong fuses are programmed boards will likely become unusable and there is no recovery.
- Boot from USB OTG interface
  - This mode is used in production to download the first stage bootloader and is typically not used by *iMX6 UltraLite COM Board* integrators. Sometimes this mode is called "Recovery mode".
  - This mode is activated by pulling signal E2PROM_WP low.

To summarize, the *iMX6 UltraLite COM board* is setup to boot from eMMC as default. If another source is needed, program the OTP fuses.

If using the default setup (boot from eMMC), make sure the boot control pins (LCD1_DATA00 - LCD1_DATA23, which are the EACOM pins LCD_B0-B7, LCD_G0-G7, LCD_R0-R7) are not driven externally.

An optional USB OTG boot mode can be enables by pulling signal E2PROM_WP low.

7 Technical Specification

7.1 Absolute Maximum Ratings

All voltages are with respect to ground, unless otherwise noted. Stress above these limits may cause malfunction or permanent damage to the board.

Symbol	Description	Min	Max	Unit
VIN	Main input supply voltage	-0.3	3.6	V
VBAT	Coin cell voltage	-0.3	3.4	V
VIO	Vin/Vout (I/O VDD + 0.3)	-0.5	3.6	V
VADCIN	Analog input voltage on ADC inputs	-0.3	3.6	V
USB_xx_VBUS	USB VBUS signals	-0.3	5.35	V
USB_xx_DP/DN	USB data signal pairs	-0.3	3.63	V

7.2 Recommended Operating Conditions

All voltages are with respect to ground, unless otherwise noted.

Symbol	Description	Min	Typical	Max	Unit
VIN	Main input supply voltage Ripple with frequency content < 10 MHz Ripple with frequency content ≥ 10 MHz	3.2	3.3	3.4 50 10	V mV mV
VBAT	Coin cell voltage **Note:** This voltage must remain valid at all times for correct operation of the board (including, but not limited to the RTC). **Note:** if the backup battery is rechargeable, the board provides a backup battery charger function.	2.8	3.3	3.4	V
USB_xx_VBUS	USB VBUS signals	4.4	5	5.25	V

7.3 Power Ramp-Up Time Requirements

Input supply voltages (VIN and VBAT) shall have smooth and continuous ramp from 10% to 90% of final set-point. Input supply voltages shall reach recommended operating range in 1-20 ms.

7.4 Electrical Characteristics

For DC electrical characteristics, see iMX6UltraLite Datasheet. Depending on internal VDD operating point, OVDD is 3.25V (50 mV under typical recommended VIN, 3.3V).

7.4.1 Reset Output Voltage Range

The reset output is an open drain output with a 1500 ohm pull-up resistor to VIN.

7.4.2 Reset Input

The reset input is triggered by pulling the reset input low (0.2 V max) for 20 uS minimum. The internal reset pulse will be 140-280 mS long, before the i.MX 6UltraLite boot process starts.

7.5 Power Consumption

There are several factors that determine power consumption of the *iMX6 UltraLite COM Board*, like input voltage, operating temperature, DDR3L activity, operating frequencies for the different cores, DVFS levels and software executed (i.e., Linux distribution).

The values presented are typical values and should be regarded as an estimate. Always measure current consumption in the real system to get a more accurate estimate.

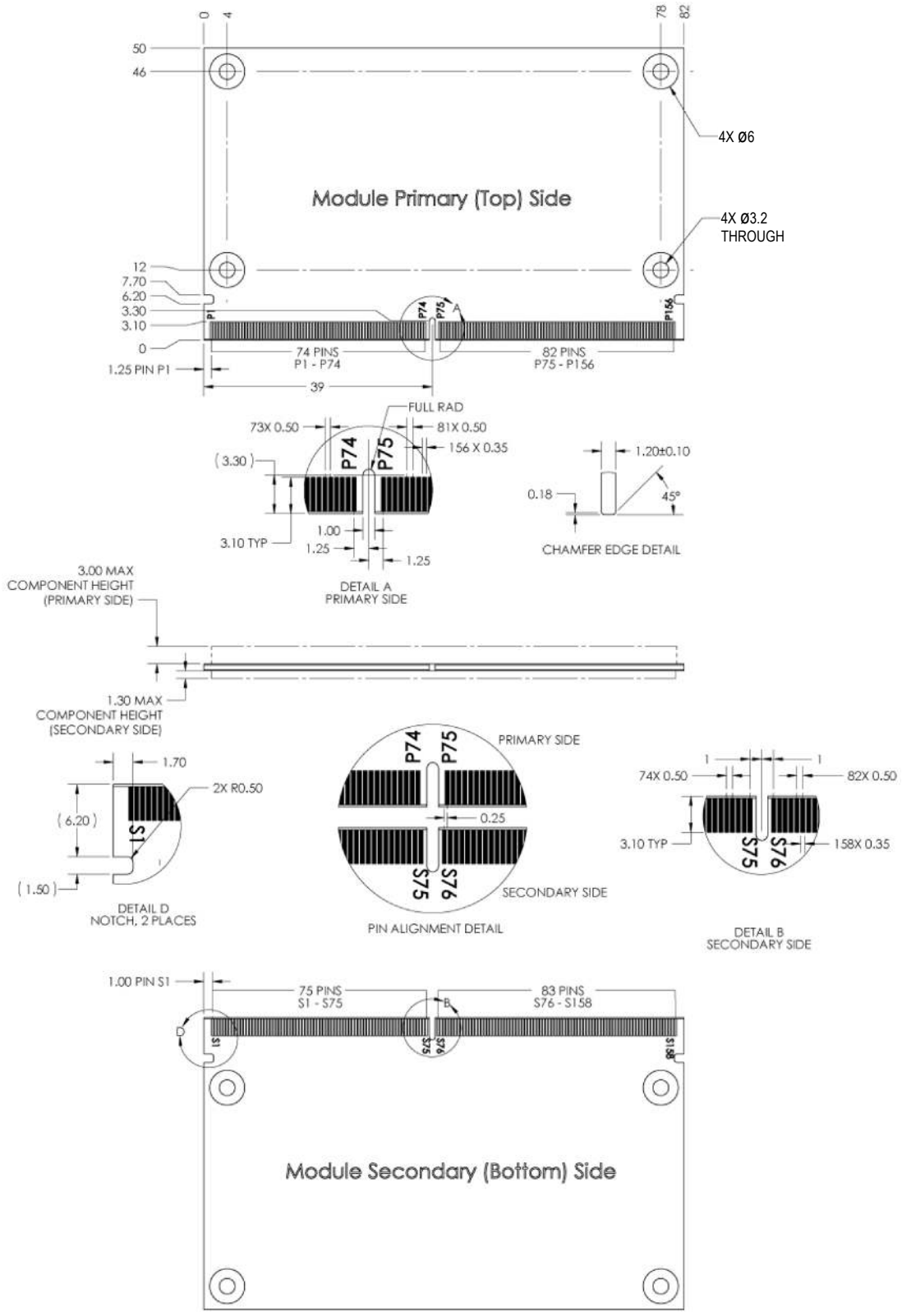
Symbol	Description (VIN = 3.3V, Toperating = 25°C)	Typical	Max observed over 1 sec period	Unit
I_{VIN}_MAX	Maximum CPU load, 528 MHz core frequency, without Ethernet	160	260	mA
I_{VIN}_IDLE	System idle state, uBoot prompt Linux prompt, without Ethernet Linux prompt, with Ethernet		132 105 250	mA
I_{VIN}_DSM	Deep-Sleep mode (DSM), aka "Dormant mode" or "Suspend-to-RAM" in Linux BSP	23		mA
I_{VIN}_STB	Linux standby	31		mA
I_{VBAT}_BACKUP	Current consumption to keep internal i.MX6 UltraLite RTC running	106		uA

7.6 Mechanical Dimensions

The board use the SMARC mechanical form factor.

Dimension	Value (±0.1 mm)	Unit
Module width	82	mm
Module height	50	mm
Module top side height	3.0	mm
Module bottom side height	1.3	mm
PCB thickness	1.2	mm
Mounting hole diameter **Note:** This measurement is not identical with SMARC specification.	3.2	mm
Module weight	16 ±1 gram	gram

The picture below show the mechanical details of the 82 x 50 mm module, including the pin numbering and edge finger pattern. The picture comes from the SMARC HW specification and show pin numbering in the Px and Sx format.



Picture source: SMARC HW Specification V1.1 © 2014 SGeT e.V.

Figure 7 – iMX6 UltraLite COM Board Mechanical Outline

7.6.1 MXM3 Socket

The board has 314 edge fingers that mates with an MXM3 connection, which is a low profile 314 pos, 0.5mm pitch right angle connector on the carrier board. This connector is available from different manufacturers in different board to board stacking heights, starting from 1.5 mm.

The AS0B821 and AS0B826 connector families from Foxconn are recommended.

Note that connector series MM70 (e.g., MM70-314-310B1) from JAE should not be used since this specific connector lack some of the pins. It is however possible to use the connector if it is acceptable for the project to not use the following pins:

- P146/300 E2PROM_WP This pin is also used to select USB OTG as boot mode (when pulled low), also known as "factory recovery" mode. Not having access to this pin means that USB OTG mode cannot be enabled from the carrier board.
- P147/302 VIN This is not any problem since there are many VIN pins.
- S149/303 GND This is not any problem since there are many GND pins.
- S148/301 GND This is not any problem since there are many GND pins.

Embedded Artists use connector AS0B826-S78B from Foxconn on the COM Carrier board. This connector gives a board to board stacking height of 5.0 mm. This space allows some components to also be placed right under the COM board.

Always check available component height before placing components on the carrier board under the COM board, see picture below.

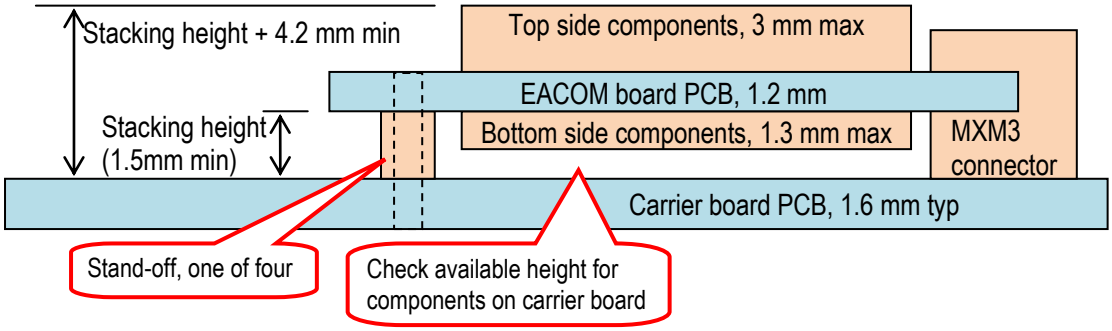


Figure 8 – COM Board Mounting in MXM3 Connector, Stacking Height

7.6.2 Module Assembly Hardware

The carrier board shall have four M3 threaded stand-offs for securing the EACOM board to the MXM3 connector and carrier board. Penn Engineering and Manufacturing (PEM, http://www.pemnet.com) makes surface mount spacers with M3 internal threads. Their product line is called "SMTSO". 5 mm height is standard so for simplicity select an MXM3 connector with 5 mm stacking height.

6-8 mm M3 screws are typically used.

7.7 Environmental Specification

7.7.1 Operating Temperature

Ambient temperature (T_A)

Parameter	Min	Max	Unit
Operating temperature range: commercial temperature range	0	70[1]	°C
Storage temperature range	-40	85	°C
Junction temperature i.MX 6UltraLite SoC, operating: comm. temp. range	0	105	°C

[1] Depends on cooling solution.

7.7.2 Relative Humidity (RH)

Parameter	Min	Max	Unit
Operating: 0°C ≤ T_A ≤ 60°C, non-condensing	10	90	%
Non-operating/Storage: -40°C ≤ T_A ≤ 85°C, non-condensing	5	90	%

7.8 Thermal Design Considerations

Heat dissipation from the i.MX 6UltraLite SoC depending on many operating conditions, like operating frequency, operating voltage, activity type, activity cycle duration and duty cycle. Dissipated heat is in the region of 0.5 Watt max. The DDR3L memory can account for another 0.15 Watt, also increasing ambient temperature.

If external cooling is needed, or not, depends on dissipated heat and ambient temperature range. In many cases it is possible to operate the *iMX6 UltraLite COM board* without external cooling, at least with ambient temperature up to +50° Celsius. Above this, care must be taken not to exceed max junction temperature of the i.MX 6UltraLite SoC.

The i.MX 6UltraLite SoC and PMIC (MMPF0100) together implement DVFS (Dynamic Voltage and Frequency Scaling) and Thermal Throttling. This enables the system to continuously adjust operating frequency and voltage in response to changes in workload and temperature. In general this result in higher performance at lower average power consumption.

The i.MX 6UltraLite SoC has an integrated temperature sensor for monitoring the junction (i.e., die) temperature, which affect several factors:

- A lower junction temperature, Tj, will result in longer SoC lifetime. See the following document for details: AN5198, i.MX 6UltraLite Product Usage Lifetime Estimates.
- A lower die temperature will result in lower power consumption due to lower leakage current.

7.8.1 Thermal Management

Embedded Artists provides a general heat spreader solution for EACOM boards. Note that a heat spreader is not a complete thermal solution. It provides a standardized surface for mounting a heat sink or for transporting heat to the housing.

The cooling solution must maintain an ambient air and heat spreader temperature of 60° Celsius, or less.

7.8.2 Thermal Parameters

The i.MX 6UltraLite SoC thermal parameters are listed in the table below.

Parameter	Typical	Unit
Thermal Resistance, CPU Junction to ambient ($R_{\theta JA}$)	37.6	°C/W
Thermal Resistance, CPU Junction to case, top ($R_{\theta JCtop}$)	19.3	°C/W

7.9 Product Compliance

Visit Embedded Artists' website at http://www.embeddedartists.com/product_compliance for up to date information about product compliances such as CE, RoHS2, Conflict Minerals, REACH, etc.

8 Functional Verification and RMA

There is a separate document that presents a number of functional tests that can be performed on the *iMX6 UltraLite Board* to verify correct operation on the different interfaces. Note that these tests must be performed on the carrier board that is supplied with the *iMX6 UltraLite Developer's Kit* and with a precompiled kernel from Embedded Artists.

The tests can also be done to troubleshoot a board that does not seem to operate properly. It is strongly advised to read through the list of tests and actions that can be done before contacting Embedded Artists. The different tests can help determine if there is a problem with the board, or not. For return policy, please read Embedded Artists' General Terms and Conditions document (http://www.embeddedartists.com/sites/default/files/docs/General_Terms_and_Conditions.pdf).

9 Things to Note

This chapter presents a number of issues and considerations that users must note.

9.1 Shared Pins and Multiplexing

The i.MX 6UltraLite SoC has multiple on-chip interfaces that are multiplexed on the external pins. It is not possible to use all interfaces simultaneously and some interface usage is prohibited by the i.MX 6UltraLite on-board design. Check if the needed interfaces are available to allocation before starting a design. See section 3.2 and chapter 5 for details.

9.2 Only Use EA Board Support Package (BSP)

The *iMX6 UltraLite COM board* use multiple on-board interfaces for the internal design, for example PMIC, eMMC, Ethernet and watchdog. Only use the BSP that is delivered from Embedded Artists. Do not change interface initialization and/or pin assignment for the on-board interfaces. Changing BSP settings can result in permanent board failure.

Note that Embedded Artists does not replace iMX6 UltraLite COM Boards because of improper interface initialization and/or improper pin assignment.

9.3 OTP Fuse Programming

The i.MX 6UltraLite SoC has on-chip OTP fuses that can be programmed, see NXP documents *iMX 6UltraLite Datasheet* and *iMX 6UltraLite Reference Manual* for details. Once programmed, there is no possibility to reprogram them.

iMX6UltraLite COM Boards are delivered without any OTP fuse programming. It is completely up to the COM board user to decide if OTP fuses shall be programmed and in that case, which ones.

Note that Embedded Artists does not replace iMX6 UltraLite COM Boards because of wrong OTP programming. It's the user's responsibility to be absolutely certain before OTP programming and not to program the fuses by accident.

9.4 Write Protect on Parameter Storage E2PROM

The parameter storage E2PROM contains important system data like DDR memory calibration settings and Ethernet MAC addresses. The content should not be erased or overwritten. The E2PROM is write protected if signal E2PROM_WR (pin P146/300) is left unconnected, i.e. floating. This should always be the case.

Note that all carrier board design should include the possibility to ground this pin.

The signal E2PROM_WR has dual functions. By pulling the signal low, the i.MX 6UltraLite SoC will boot into USB OTG boot mode (also called 'serial download' or 'factory recovery' mode).

9.5 Integration - Contact Embedded Artists

It is strongly recommended to contact Embedded Artists at an early stage in your project. A wide range of support during evaluation and the design-in phase are offered, including but not limited to:

- Developer's Kit to simplify evaluation
- Custom Carrier board design, including 'ready-to-go' standard carrier boards

- Display solutions
- Mechanical solutions
- Schematic review of customer carrier board designs
- Driver and application development

The *iMX6 UltraLite COM Board* targets a wide range of applications, such as:

- Industrial controllers and HMI systems
- Home automation and facility management
- Audiovisual equipment
- Instrumentation and measuring equipment
- Vending machines
- Industrial automation
- HVAC Building and Control Systems
- Smart Grid and Smart Metering
- HMI/GUI solutions
- Smart Toll Systems
- Connected vending machines
- Digital signage
- Point-of-Sale (POS) applications
- Data acquisition
- Communication gateway solutions
- Connected real-time systems
- Portable systems
- ...and much more

For more harsh use and environments, and where fail-safe operation, redundancy or other strict reliability or safety requirements exists, always contact Embedded Artists for a discussion about suitability.

There are application areas that the *iMX6 UltraLite COM Board* is not designed for (and such usage is strictly prohibited), for example:

- Military equipment
- Aerospace equipment
- Control equipment for nuclear power industry
- Medical equipment related to life support, etc.
- Gasoline stations and oil refineries

If not before, **it is essential to contact Embedded Artists before production begins**. In order to ensure a reliable supply for you, as a customer, we need to know your production volume estimates and forecasts. Embedded Artists can typically provide smaller volumes of the *iMX6 UltraLite COM Board* directly from stock (for evaluation and prototyping), but **larger volumes need to be planned**.

The more information you can share with Embedded Artists about your plans, estimates and forecasts the higher the likelihood is that we can provide a reliable supply to you of the *iMX6 UltraLite COM Board*.

9.6 ESD Precaution when Handling iMX6 UltraLite COM Board

Please note that the *iMX6 UltraLite COM Board* come without any case/box and all components are exposed for finger touches – and therefore extra attention must be paid to ESD (electrostatic discharge) precaution, for example use of static-free workstation and grounding strap. Only qualified personnel shall handle the product.

Make it a habit always to first touch one of the four mounting holes (these are grounded) for a few seconds with both hands before touching any other parts of the boards. That way, you will have the same potential as the board and therefore minimize the risk for ESD.

In general touch as little as possible on the boards in order to minimize the risk of ESD damage. The only reasons to touch the board are when mounting/unmounting it on a carrier board, connecting the JTAG cable or when changing boot slider switches.

Note that Embedded Artists does not replace boards that have been damaged by ESD.

9.7 EMC / ESD

The *iMX6 UltraLite COM Board* has been developed according to the requirements of electromagnetic compatibility (EMC). Nevertheless depending on the target system, additional anti-interference measurement may still be necessary to adherence to the limits for the overall system.

The *iMX6 UltraLite COM Board* must be mounted on carrier board (typically an application specific board) and therefore EMC and ESD tests only makes sense on the complete solution.

No specific ESD protection has been implemented on the *iMX6 UltraLite COM Board*, except on the JTAG interface signals, which all have suppressor diodes. ESD protection on board level is the same as what is specified in the i.MX 6UltraLite SoC datasheet. **It is strongly advised to implement protection against electrostatic discharges (ESD) on the carrier board** on all signals to and from the system. Such protection shall be arranged directly at the inputs/outputs of the system.

10 Custom Design

This document specify the standard *iMX6 UltraLite COM Board* design. Embedded Artists offers many custom design services. Contact Embedded Artists for a discussion about different options.

Examples of custom design services are:

- Different memory sizes on DDR3L SDRAM and eMMC Flash.
- Different mounting options, for example mount QSPI-flash and remove Ethernet interface.
- Different pinning on MXM3 edge pins, including but not limited to, SMARC compatible pinning.
- Different I/O voltage levels on all or parts of the pins.
- Different board form factor, for example SODIMM-200, high-density connectors on bottom side or MXM3 compatible boards that are higher (>50 mm).
- Different input supply voltage range, for example 5V input.
- Single Board Computer solutions, where the core design of the *iMX6 UltraLite COM Board* is integrated together with selected interfaces.
- Replace eMMC Flash with (unmanaged) MLC/SLC NAND Flash.
- Changed internal pinning to make certain pins available.

Embedded Artists also offers a range of services to shorten development time and risk, such as:

- Standard Carrier boards ready for integration
- Custom Carrier board design
- Display solutions
- Mechanical solutions

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