XR77103-A1R0

Universal PMIC 3-Output Buck Regulator

Description

The XR77103-A1R0 universal PMIC features three 2A synchronous high-efficiency, buck regulators with integrated power switches. They can operate in 5V, 9V and 12V powered systems with minimal required external component thus providing the smallest size solution possible. Two of the outputs may be paralleled for output currents up to 5A peak with steady state current of up to 4A.

The output voltage of each converter can be adjusted by external resistor divider down to voltage as low as 0.8V. With a nominal switching frequency of 1MHz, the regulators can also be synchronized to an external clock in applications where EMI control is critical.

XR77103-A1R0 features a supervisor circuit that monitors each converter output. PGOOD pin is asserted once sequencing is done, outputs are reported in regulation and the reset timer expires. The polarity of the signal is active high. A pulse skipping mode (PSM) reduces switching losses maintaining high efficiency when the system is unloaded or in standby mode.

FEATURES

- 4.5V to 14V wide input supply voltage range
- Built-in MOSFET and synchronous rectifier
- 0.8V, high accuracy reference (1%)
- Current-mode control with simple compensation circuit
- External synchronization
- Power good
- Protection
  - Thermal shutdown
  - Overvoltage transient protection
  - Overcurrent protection
- 32-pin 4mm x 4mm TQFN package

APPLICATIONS

- FPGA and DSP supplies
- Video processor supplies
- Applications processor power

Typical Application

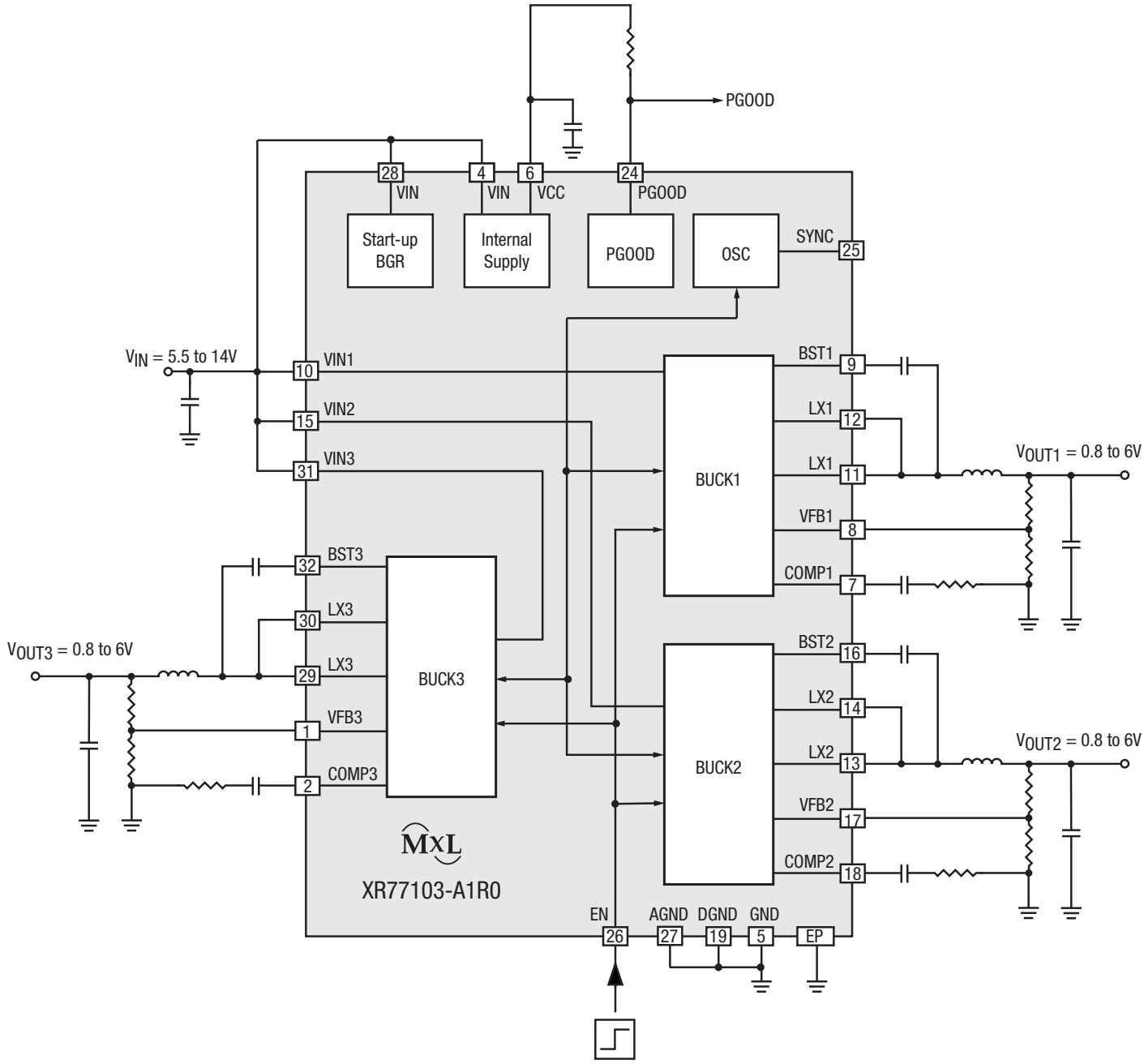


Figure 1. Typical Application

Absolute Maximum Ratings

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. Exposure to any absolute maximum rating condition for extended periods may affect device reliability and lifetime.

V_{IN1}, V_{IN2}, V_{IN3}, LX1, LX2, LX3 ..... -0.3V to 18V

EN, V_{CC} ..... -0.3V to 7V

PGOOD, SYNC ..... -0.3V to 7V

BST# to LX# ..... -0.3V to 7V

AGND, DGND to GND ..... -0.3V to 0.3V

Storage temperature ..... -65°C to 150°C

Junction temperature ..... 150°C

Power dissipation ..... Internally Limited

Lead temperature (soldering, 10 seconds) ..... 260°C

CDM 700V

ESD rating (HBM – human body model) 2kV

Operating Conditions

V_{IN} ..... 4.5V to 14V

V_{CC} ..... 4.5V to 5.5V

LX# ..... -0.3V to 14V(1)

Junction temperature range (T_J) ..... -40°C to 125°C

XR77103 package power dissipation max at 25°C 3.4W

XR77103 thermal resistance θ_{JA} ..... 30°C/W

NOTE:

1. LX# pins' DC range is from -0.3V, transient -1V for less than 10ns.

Electrical Characteristics

T_A = 25°C, V_{IN} = 12V, EN = V_{CC}, f_{SW} = 1MHz, unless otherwise specified. Limits applying over the full operating temperature range are denoted by a •.

Symbol	Parameter	Conditions	•	Min	Typ	Max	Units
Power Supply Characteristics							
V_{IN}	Input voltage range		•	5.5		14	V
V_{IN}	Input voltage range	V_{CC} tied to V_{IN}	•	4.5		5.5	V
V_{UVLO}	UVLO threshold	V_{IN} rising/falling			4.22/4.1		V
$UVLO_{DEGLITCH}$	UVLO deglitch	Rising/falling			110		µs
I_{VIN}	V_{IN} supply current	EN = GND			250		µA
I_{VINQ}		EN = high, no load			2.6		mA
Internal Supply Voltage							
V_{CC}	Internal biasing supply	I_{LOAD} = 0mA	•	4.9	5	5.1	V
I_{VCC}	Internal biasing supply current	V_{IN} = 12V	•			10	mA
V_{UVLO}	UVLO threshold for V_{CC}	V_{CC} rising			3.8		V
		V_{CC} falling			3.6		V
$UVLO_{DEGLITCH}$	UVLO deglitch for V_{CC}	Falling edge			110		µs

Electrical Characteristics (Continued)

T_A = 25°C, V_{IN} = 12V, EN = V_{CC}, f_{SW} = 1MHz, unless otherwise specified. Limits applying over the full operating temperature range are denoted by a •.

Symbol	Parameter	Conditions	•	Min	Typ	Max	Units
Protections							
T_{SD}	Thermal shutdown temperature	Temperature rising, Non-latch off. T_{SD} release threshold, temperature = T_{SD}-HY_{TSD}			160		°C
HY_{TSD}	Thermal shutdown hysteresis				20		°C
$T_{SD_DEGLITCH}$	Thermal shutdown deglitch				110		µs
V_{OVBUCK}	Threshold voltage for buck overvoltage	Output rising (HS FET will be forced off)			109		%
		Output falling (HS FET will be allowed to switch)			107		%
Buck Converter							
f_{SW}	Switching frequency				1		MHz
t_{SS}	Soft-start period				3		ms
I_{LIMx}	Peak inductor current limit accuracy	Peak inductor current limit set at 4A		-30		+30	%
R_{ON_HSx}	HS switch on-resistance	V_{IN} = 12V			200		mΩ
R_{ON_LS1}	LS switch on-resistance of Buck1	V_{IN} = 12V			60		mΩ
$R_{ON_LS2/3}$	LS switch on-resistance of Buck2/3	V_{IN} = 12V			80		mΩ
I_{Ox}	Output current capability	Continuous loading(1)			2		A
D_{MAX}	Maximum duty cycle				95		%
$t_{ON\ MIN}$	Minimum on time				120		ns
	Line regulation ($\Delta V_{OX}/\Delta V_{INX}$)	V_{INX} = 5.5 to 14V, I_{OX} = 1A			0.5		$\%V_O$
	Load regulation ($\Delta V_{OX}/\Delta I_{OX}$)	I_O = 10 to 90%, I_O = MAX			0.5		$\%V_O/A$
	Output voltage accuracy	V_{IN} = 12V		-1	Normal	1	%
		5.5V ≤ V_{IN} ≤ 14V	•	-2	Normal	2	
$SYNC_{FREQ}$	Synchronization frequency			1.05			MHz
$SYNC_{D_MIN}$	Synchronization signal minimum duty cycle		•	40			%
$SYNC_{D_MAX}$	Synchronization signal maximum duty cycle		•			60	%

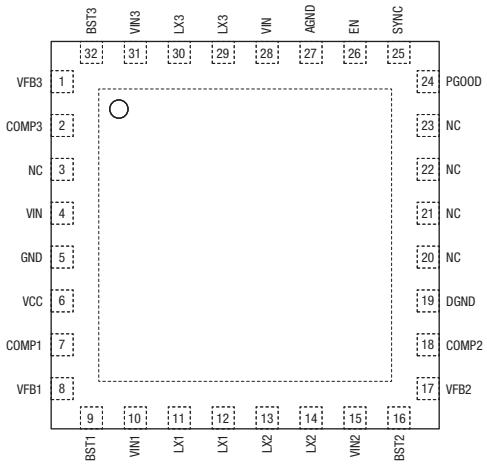
NOTE:
1. Subject to thermal derating. Design must not exceed the package thermal rating.

Electrical Characteristics (Continued)

T_A = 25°C, V_{IN} = 12V, EN = V_{CC}, f_{SW} = 1MHz, unless otherwise specified. Limits applying over the full operating temperature range are denoted by a •.

Symbol	Parameter	Conditions	•	Min	Typ	Max	Units
Power Good Reset Generator							
V_{UVBUCK}	Threshold voltage for buck under voltage	Output falling, (disabled after t_{ON_HICCUP})			85		%
		Output rising, (PG will be asserted)			90		
$t_{PG_DEGLITCH}$	Deglitch time	Rising and falling			11		ms
t_{ON_HICCUP}	Hiccup mode on time	$V_{UVBUCKX}$ asserted			12		ms
t_{OFF_HICCUP}	Hiccup mode off time	Once t_{OFF_HICCUP} elapses, all converters will start up again			15		ms
t_{RP}	Minimum reset period				1		s
	PGOOD output low	I_{SINK} = 1mA	•			0.4	V
Input Threshold (SYNC, EN)							
V_{IH}	Input threshold high	V_{INPUT} rising	•	2.53			V
V_{IL}	Input threshold low	V_{INPUT} falling	•			1.36	V

Pin Configuration



Pin Functions

Pin Number	Pin Name	Description
1	VFB3	Buck 3 feedback pin.
2	COMP3	Compensation pin for Buck 3. Connect a series RC circuit to this pin for compensation.
3	NC	No connect.
4	VIN	IC supply pin. Connect a capacitor as close as possible to this pin.
5	GND	Ground.
6	VCC	Internal supply. Connect a ceramic capacitor from this pin to ground.
7	COMP1	Compensation pin for Buck 1. Connect a series RC circuit to this pin for compensation.
8	VFB1	Buck 1 feedback pin.
9	BST1	Bootstrap capacitor for Buck 1. Connect a bootstrap capacitor from this pin to LX1.
10	VIN1	Input supply for Buck 1. Connect a capacitor as close as possible to this pin.
11	LX1	Switching node for Buck 1.
12	LX1	Switching node for Buck 1.
13	LX2	Switching node for Buck 2.
14	LX2	Switching node for Buck 2.
15	VIN2	Input supply for Buck 2. Connect a capacitor as close as possible to this pin.
16	BST2	Bootstrap capacitor for Buck 2. Connect a bootstrap capacitor from this pin to LX2.
17	VFB2	Buck 2 feedback pin.
18	COMP2	Compensation pin for Buck 2. Connect a series RC circuit to this pin for compensation.
19	DGND	Digital ground.
20	NC	No connect.

Pin Functions (Continued)

Pin Number	Pin Name	Description
21	NC	No connect.
22	NC	No connect.
23	NC	No connect.
24	PGOOD	Power good output. Open drain output asserted after all converters are sequenced and within regulation.
25	SYNC	External clock input pin. Connect to signal ground when unused.
26	EN	Enable control input. Set EN high to enable converters.
27	AGND	Analog ground.
28	VIN	IC supply pin. Connect a capacitor as close as possible to this pin.
29	LX3	Switching node for Buck 3.
30	LX3	Switching node for Buck 3.
31	VIN3	Input supply for Buck 3. Connect a capacitor as close as possible to this pin.
32	BST3	Bootstrap capacitor for Buck 3. Connect a bootstrap capacitor from this pin to LX3.
-	E-PAD	Connect to power ground.

Typical Performance Characteristics

All data taken at f_{SW} = 1MHz, T_A = 25°C, no airflow, unless otherwise specified.

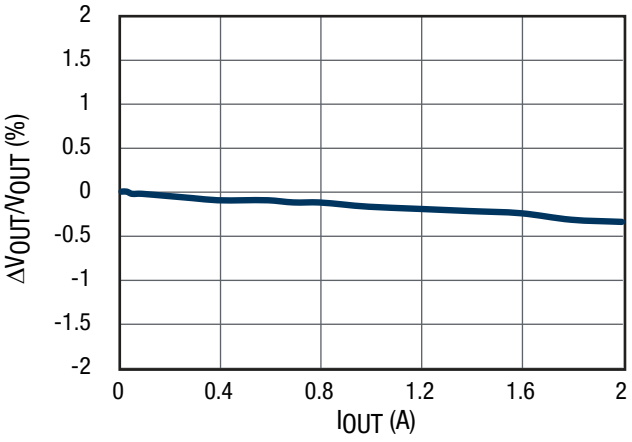


Figure 2. Load Regulation Channel 1, $12V_{IN}$, $3.3V_{OUT}$

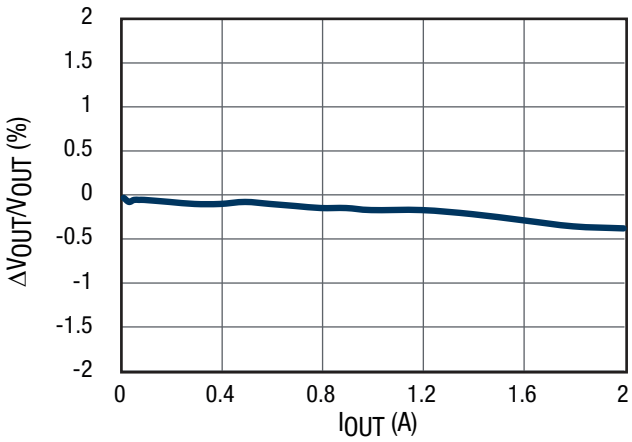


Figure 3. Load Regulation Channel 1, $5V_{IN}$, $3.3V_{OUT}$

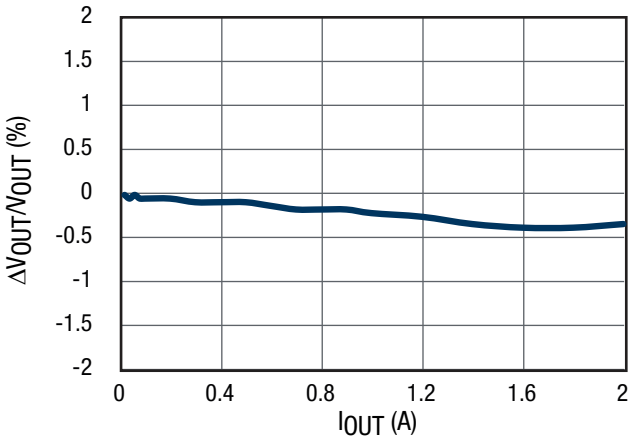


Figure 4. Load Regulation Channel 2, $12V_{IN}$, $1.8V_{OUT}$

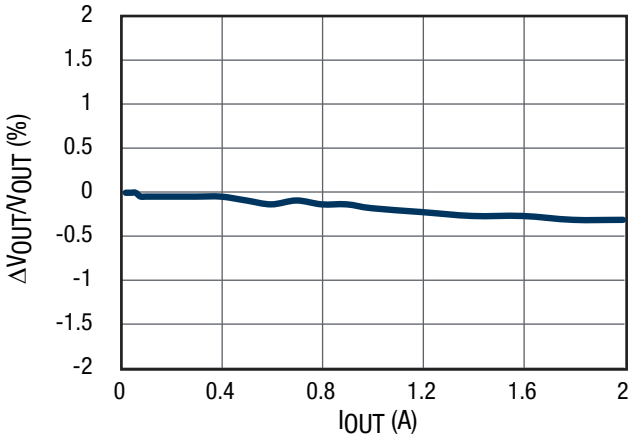


Figure 5. Load Regulation Channel 2, $5V_{IN}$, $1.8V_{OUT}$

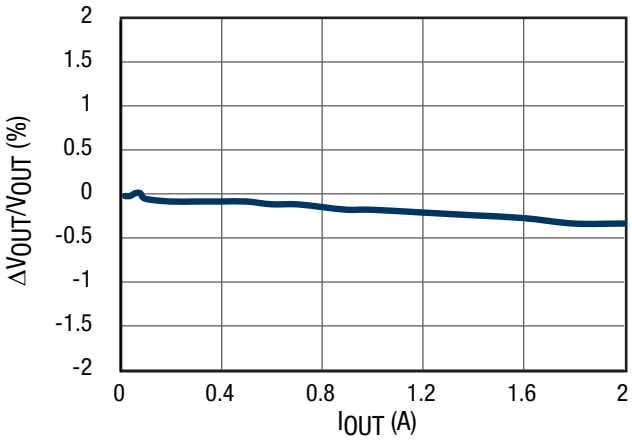


Figure 6. Load Regulation Channel 3, $12V_{IN}$, $2.5V_{OUT}$

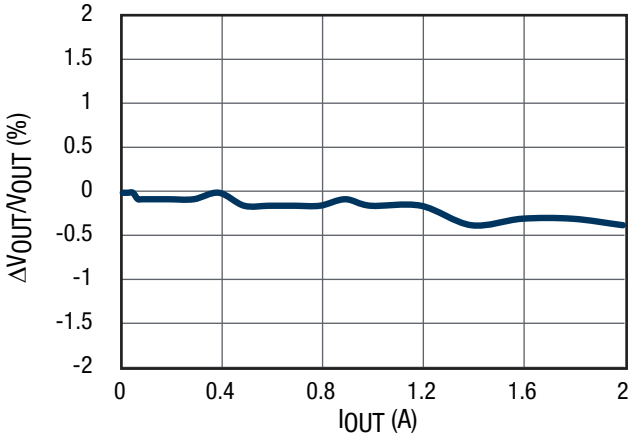


Figure 7. Load Regulation Channel 3, $5V_{IN}$, $1.2V_{OUT}$

Typical Performance Characteristics (Continued)

All data taken at f_{SW} = 1MHz, T_A = 25°C, no airflow, unless otherwise specified.

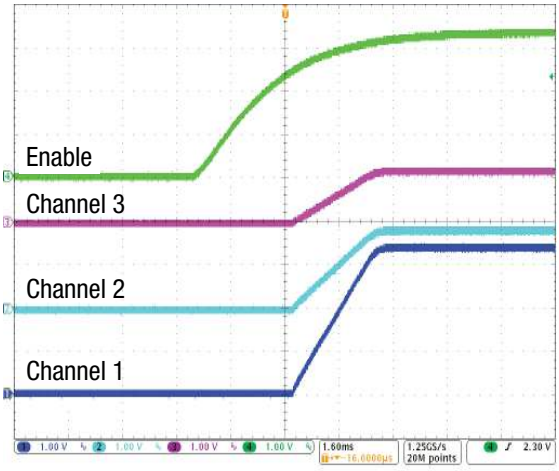


Figure 8. Power-up Sequence

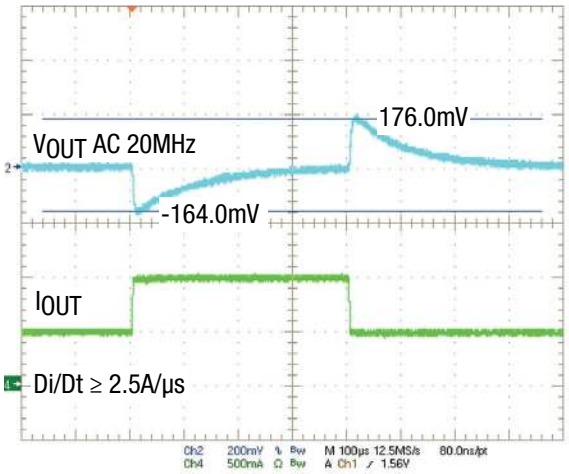


Figure 9. $12V_{IN}$, $5.0V_{OUT}$
Transient Response, 0.5A to 1.0A

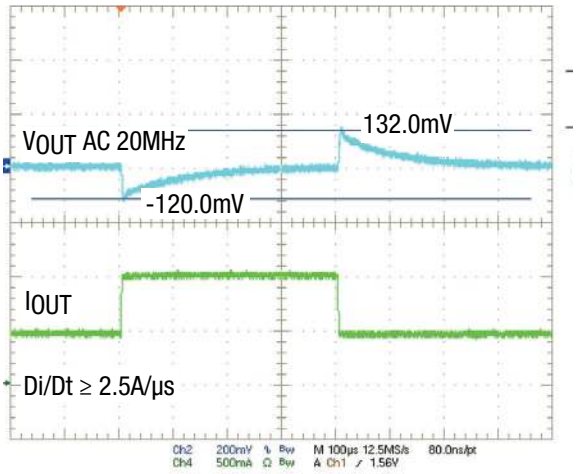


Figure 10. $12V_{IN}$, $3.3V_{OUT}$
Transient Response, 0.5A to 1.0A

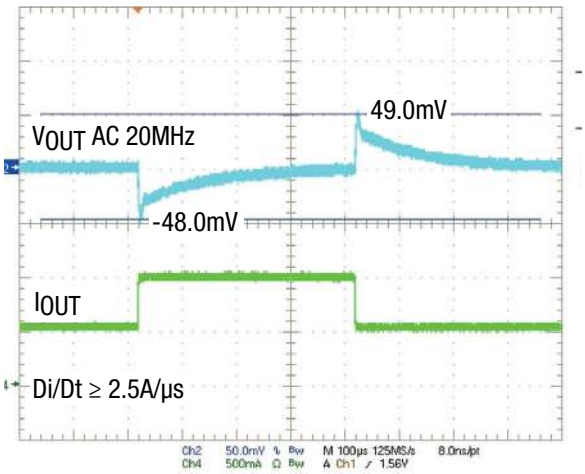


Figure 11. $12V_{IN}$, $1.8V_{OUT}$
Transient Response, 0.5A to 1.0A

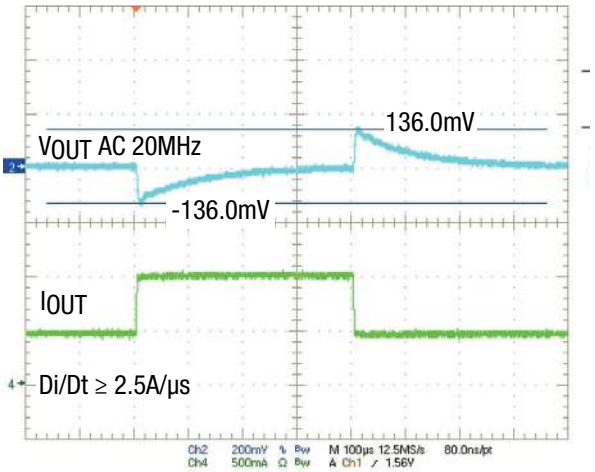


Figure 12. $5V_{IN}$, $3.3V_{OUT}$
Transient Response, 0.5A to 1.0A

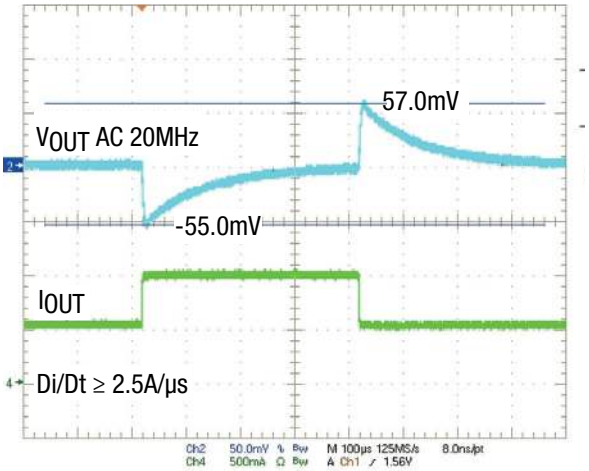


Figure 13. $5V_{IN}$, $1.8V_{OUT}$
Transient Response, 0.5A to 1.0A

Typical Performance Characteristics (Continued)

Efficiency

f_{SW} = 1MHz, T_A = 25°C, no airflow, only individual channel operating, inductor losses are included.

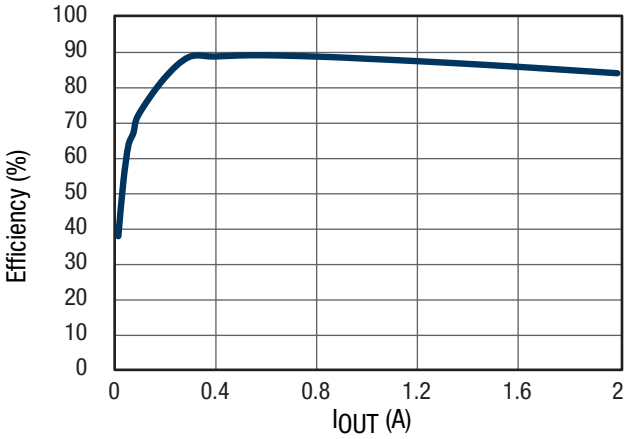


Figure 14. Efficiency Channel 1, $12V_{IN}$ $3.3V_{OUT}$

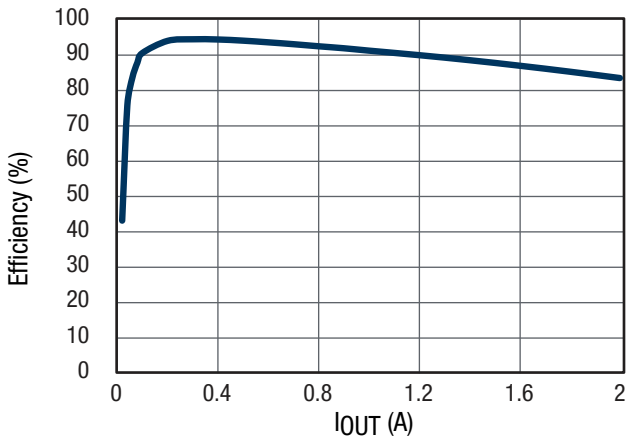


Figure 15. Efficiency Channel 1, $5V_{IN}$ $3.3V_{OUT}$

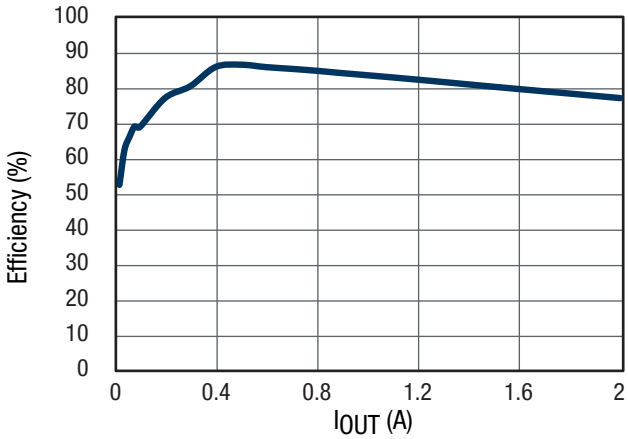


Figure 16. Efficiency Channel 2, $12V_{IN}$ $1.8V_{OUT}$

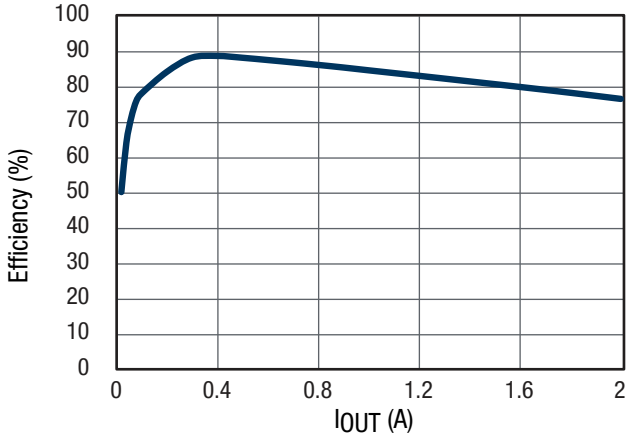


Figure 17. Efficiency Channel 2, $5V_{IN}$ $1.8V_{OUT}$

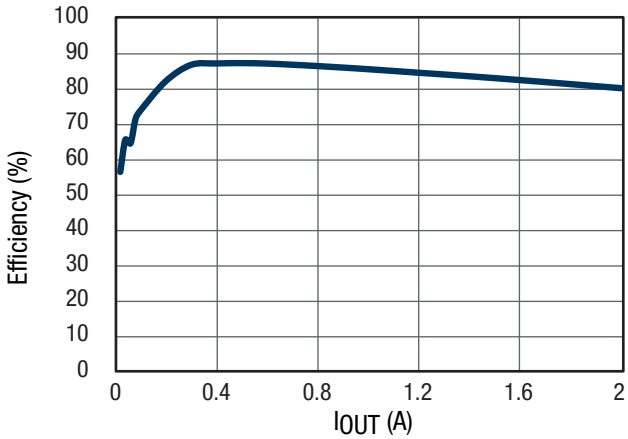


Figure 18. Efficiency Channel 3, $12V_{IN}$ $2.5V_{OUT}$

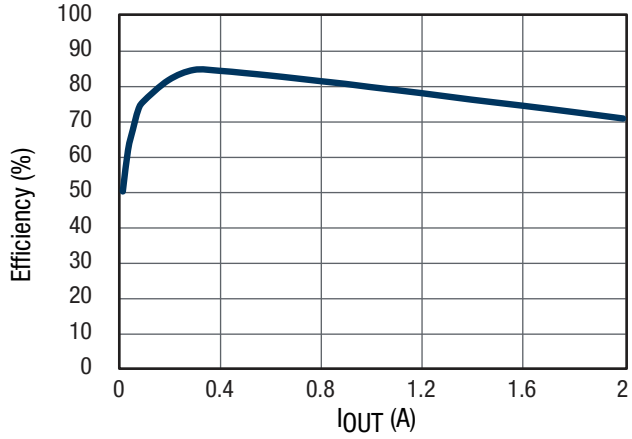


Figure 19. Efficiency Channel 3, $5V_{IN}$ $1.2V_{OUT}$

Typical Performance Characteristics (Continued)

Thermal Characteristics

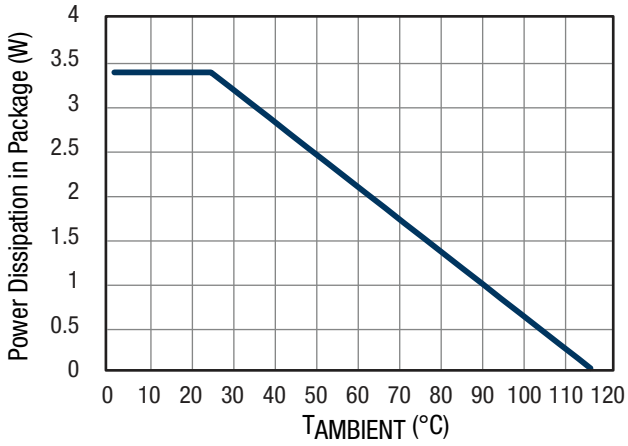


Figure 20. Package Thermal Derating

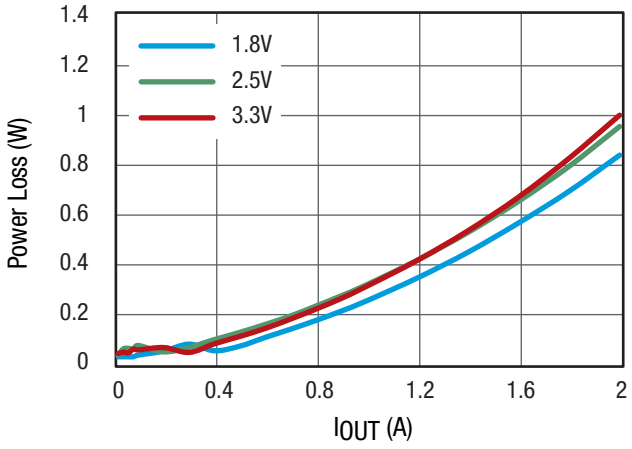


Figure 21. Channel 1 Power Loss at f_{SW} = 1MHz, V_{IN} = 12V, No Airflow

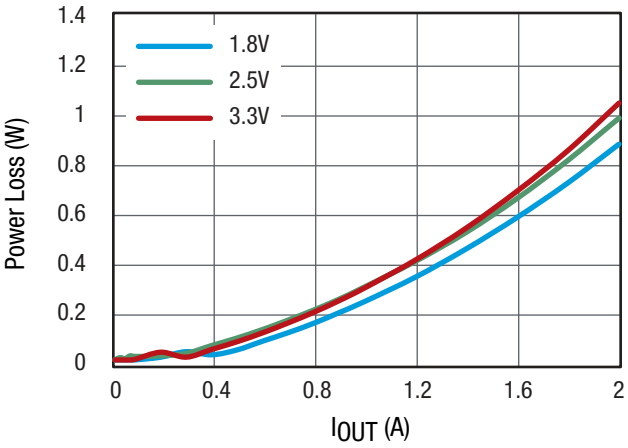


Figure 22. Channel 2 Power Loss at f_{SW} = 1MHz, V_{IN} = 12V, No Airflow

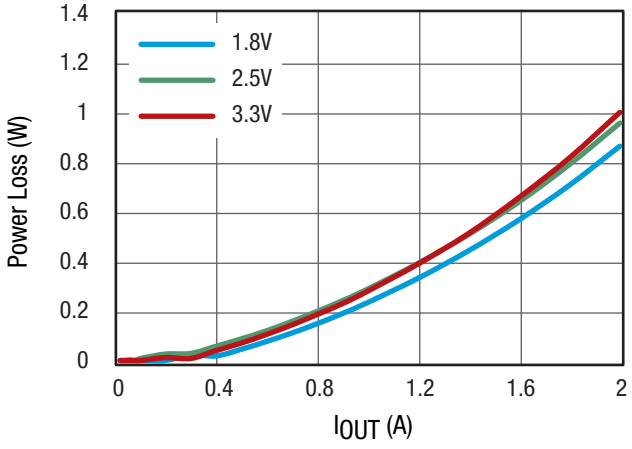


Figure 23. Channel 3 Power Loss at f_{SW} = 1MHz, V_{IN} = 12V, No Airflow

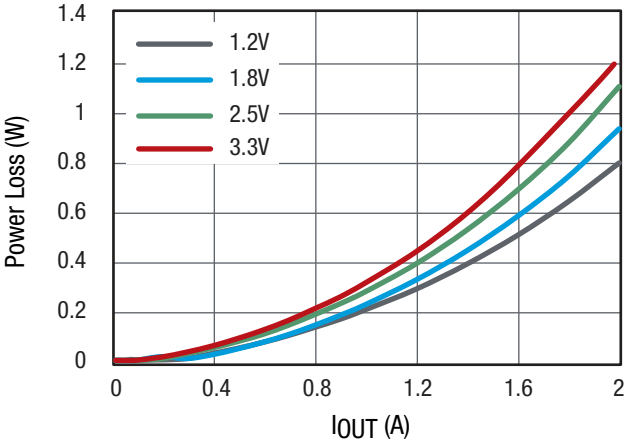


Figure 24. Channel 1 Power Loss at f_{SW} = 1MHz, V_{IN} = 5V, No Airflow

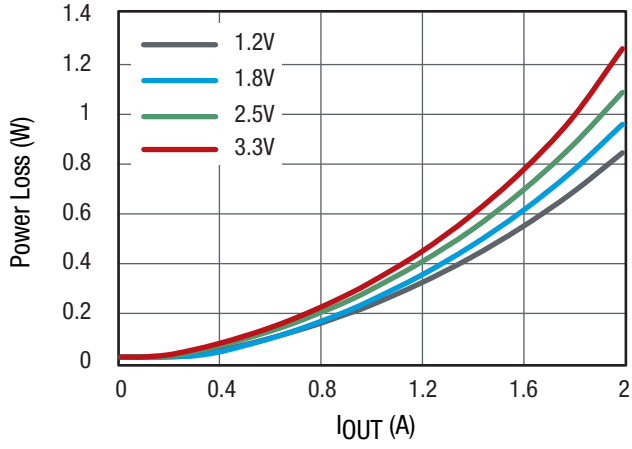


Figure 25. Channel 2 Power Loss at f_{SW} = 1MHz, V_{IN} = 5V, No Airflow

Typical Performance Characteristics (Continued)

Thermal Characteristics

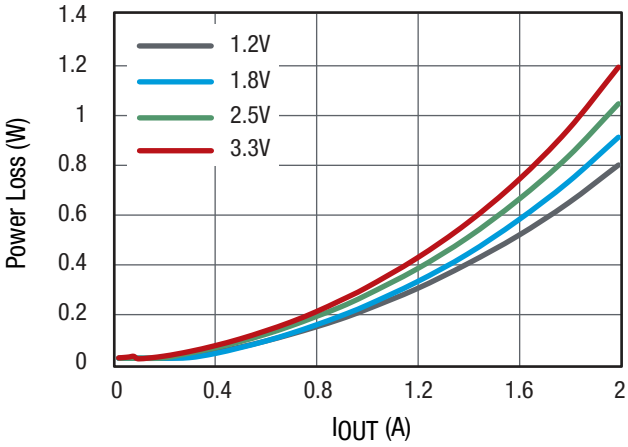


Figure 26. Channel 3 Power Loss at f_{SW} = 1MHz, V_{IN} = 5V, No Airflow

Functional Block Diagram

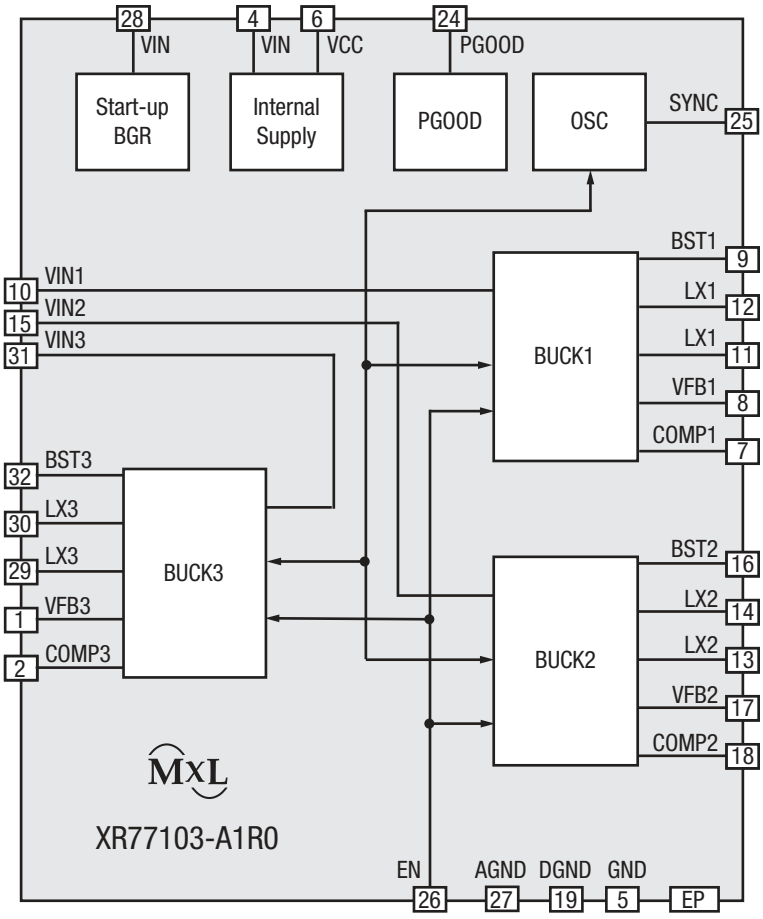


Figure 27. Functional Block Diagram

Applications Information

Operation

XR77103-A1R0 is a power management IC with three step-down buck converters. Both high-side and low-side MOSFETs are integrated to provide fully synchronous conversion with higher efficiency. XR77103-A1R0 can support 4.5V to 14V input supply, high load current, 1MHz clocking. The buck converters have a PSM mode which can improve power dissipation during light loads. As load is increased, the device transitions to its constant operating frequency of 1MHz. The SYNC pin also provides a means to synchronize the power converter to an external signal. Input ripple is reduced by 180 degree out-of-phase operation among converters. All three buck converters have peak current mode control which simplifies external frequency compensation. Each buck converter has peak inductor current limit of 4A. The device has a power good comparator monitoring the output voltage. Soft-start for each converter is 3ms. All outputs start up once EN pin is set high.

Minimum On-Time $t_{ON\ (min)}$ Considerations

The XR77103 can regulate with pulse widths as low as 95ns. However, to ensure sufficent control range, the design must use 120ns as the minimum on-time as stated in the electrical table. Failure to meet this condition can result in overcharging of the output and V_{OUT} not meeting specification.

Output Voltage Setting

Output voltage is set externally using an external resistor divider. Output voltage is determined by the following equation.

$$V_{OUTX} = 0.8V \times \left(1 + \frac{R1}{R2}\right)$$

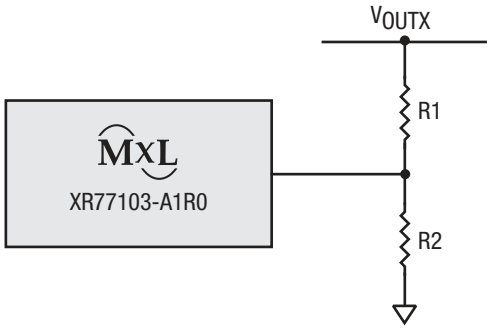


Figure 28. Output Voltage Setting

This can make the device applicable to AVS (automatic voltage scaling) system. Output voltage can be adjusted automatically by external DC voltage. Figure 29 shows application circuit of supply for AVS system.

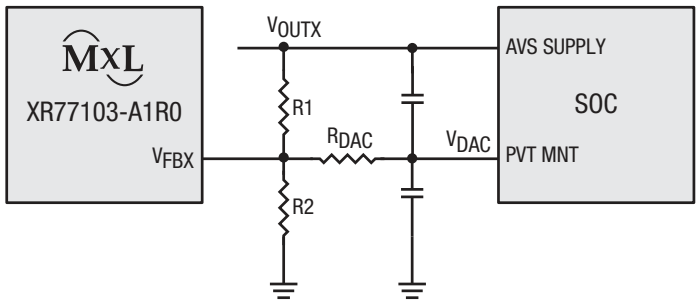


Figure 29. AVS Control

Frequency Compensation

In order to properly frequency compensate the device, the following component selection is recommended.

V_{IN} (V)	V_{OUT} (V)	L (µH)	C_{OUT} (µF)	R_{COMP} (kΩ)	C_{COMP} (nF)
5.0	1.0	1.5	22 x 3	20	2.2
5.0	1.2	1.5	22 x 3	20	2.2
5.0	1.5	1.5	22 x 2	20	4.7
12/5.0	1.8	1.5	22 x 2	20	4.7
12/5.0	2.5	3.3	22 x 1	20	4.7
12/5.0	3.3	3.3	22 x 1	20	4.7
12	5.0	3.3	22 x 1	20	4.7

Synchronization

The status of the SYNC pin will be ignored during start-up and the XR77103-A1R0's control will only synchronize to an external signal after the PGOOD signal is asserted. When synchronization is applied, the sync pulse frequency must be higher than the PWM oscillator frequency (1.05MHz) to allow the external signal trumping the oscillator pulse reliably. When synchronization is not applied, the SYNC pin should be connected to signal ground.

Although the device can lock to external clock running up to 2.31MHz, doing this will alter the timing characteristics and degrade thermal performance.

Applications Information (Continued)

Out-of-Phase Operation

Channels 1 and 2 operate in phase while channel 3 operates 180 degrees out-of-phase with the other two converters (see Figure 30). This enables the system, having less input ripple, to lower component cost, save board space and reduce EMI.

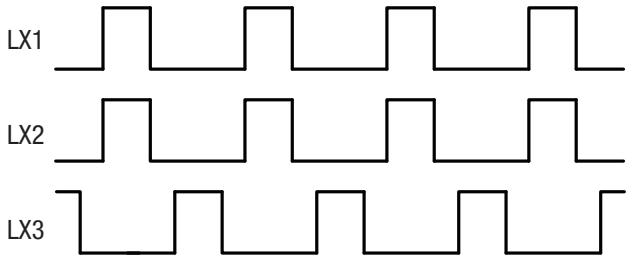


Figure 30. Out-of-Phase Operation

Two Buck Regulators in Parallel Operation (Current Sharing)

The XR77103-A1R0 can be used in parallel operation to increase output current capacity. To enable this, a user needs:

- To connect V_{OUT2} and V_{OUT3} together.
- To connect COMP2 and COMP3 together.
- Regulate the channels 2 and 3 to the same V_{OUT}.

Then, the channels 2 and 3 will run in parallel and load current is shared in average.

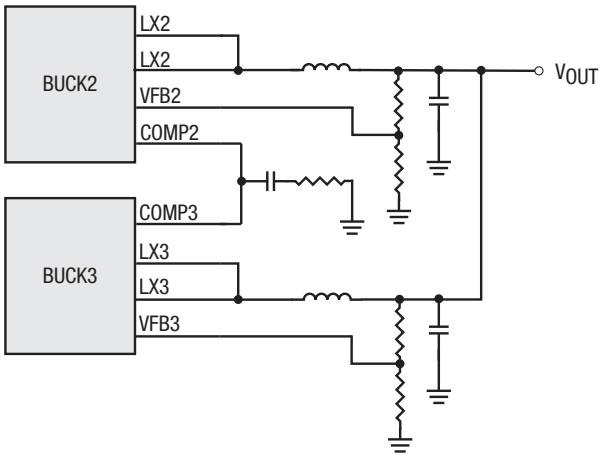


Figure 31. Parallel Operation

Power Good

The PGOOD pin is an open drain output. The PGOOD pin is pulled low when any buck converter is pulled below 85% of the nominal output voltage. The PGOOD is pulled up when all three buck converters' outputs are more than 90% of their nominal output voltage and the PGOOD reset timer expires. The polarity of the PGOOD is active high. The PGOOD reset time is 1s.

Thermal Design

Proper thermal design is critical in controlling device temperatures and in achieving robust designs. There are a number of factors that affect the thermal performance. One key factor is the temperature rise of the devices in the package, which is a function of the thermal resistances of the devices inside the package and the power being dissipated.

The thermal resistance of the XR77103-A1R0 (30°C/W) is specified in the Operating Conditions section of this datasheet. The θ_{JA} thermal resistance specification is based on the XR77103-A1R0 evaluation board operating without forced airflow. Since the actual board design in the final application will be different, the thermal resistances in the final design may be different from those specified.

The package thermal derating and power loss curves are shown in Figures 20 through 26. These correspond to input voltages of 12V and 5V.

Layout Guidelines

Proper PCB layout is crucial in order to obtain a good thermal and electrical performance.

For thermal considerations it is essential to use a number of thermal vias to connect the central thermal pad to the ground layer(s).

In order to achieve good electrical and noise performance following steps are recommended:

- Place the output inductor close to the LX pins and minimize the area of the connection. Doing this on the top layer is advisable.
- Central thermal pad shall be connected to the power ground connections to as many layers as possible.
- Output filtering capacitor shall share the same power ground connection as the input filtering capacitor. Connection to the signal ground plane shall be done with vias placed at the output filtering capacitors.
- AC current loops formed by input filtering capacitors, output filtering capacitors, output inductors, and the regulator pins shall be minimized.
- GND, AGND, DGND pins shall be connected to the signal ground plane.
- Compensation networks shall be placed close to the pins and referenced to the signal ground.
- V_{CC} bypass capacitor shall be placed close to the pin.

Applications Information (Continued)

Typical Applications

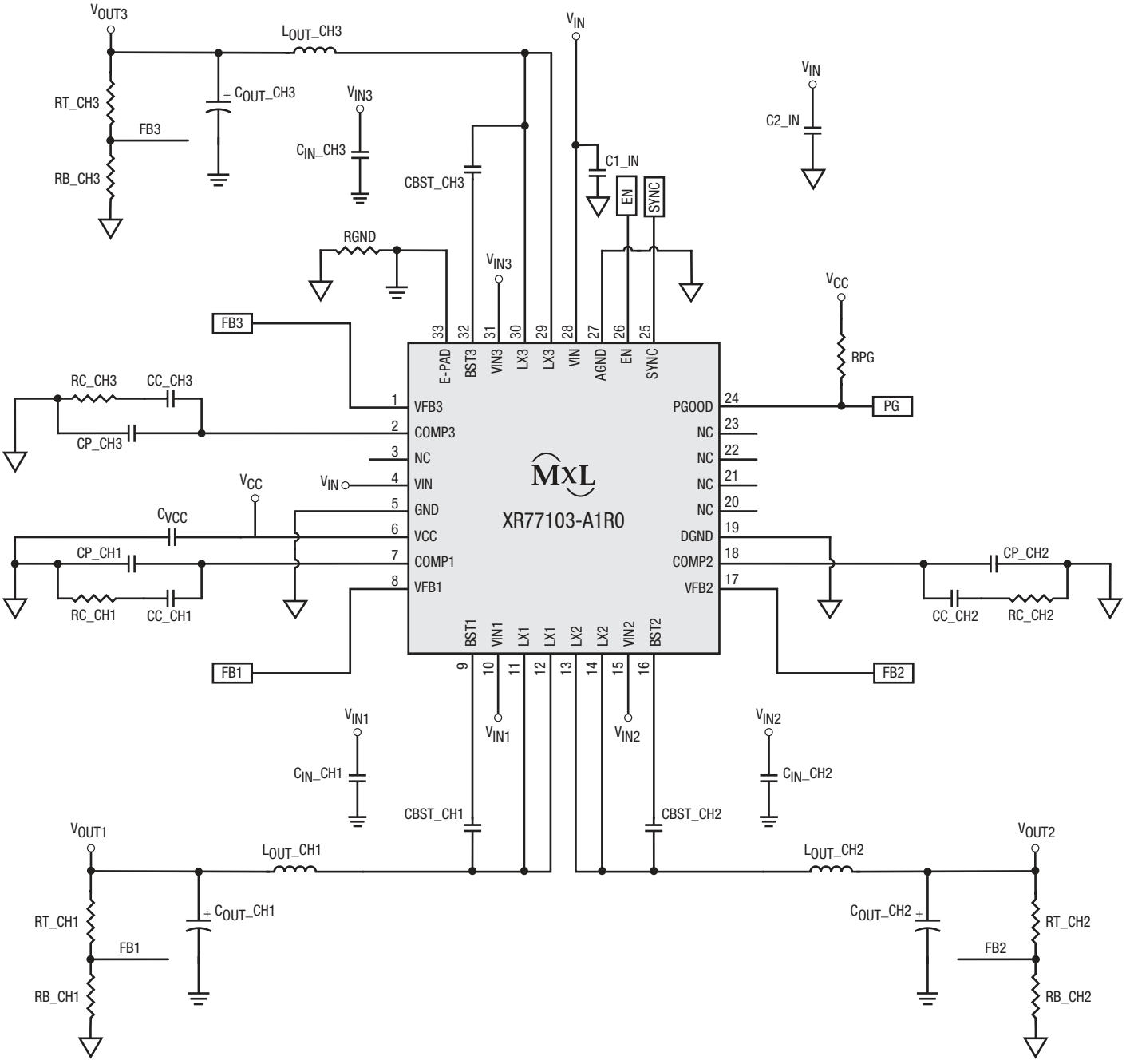
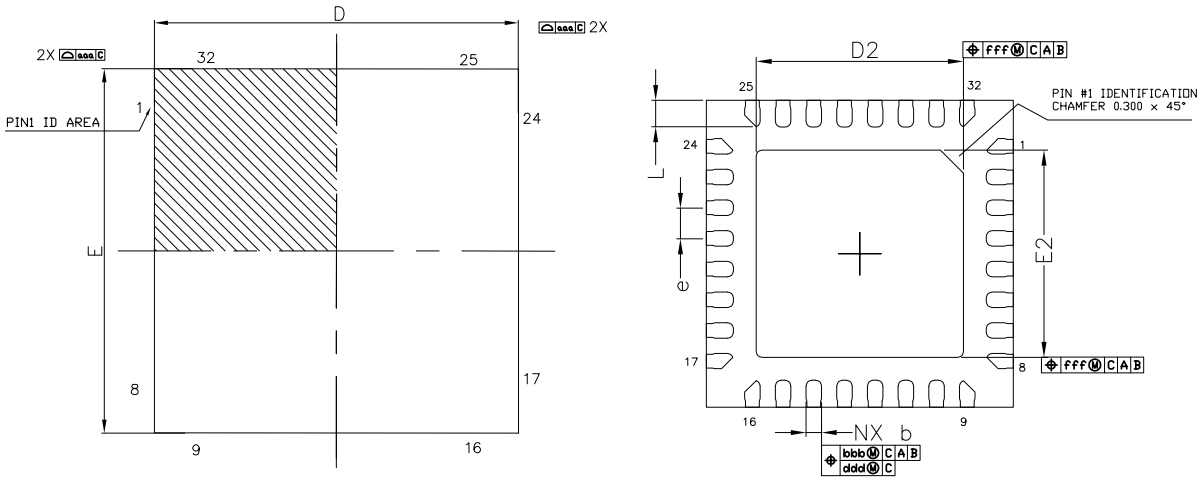


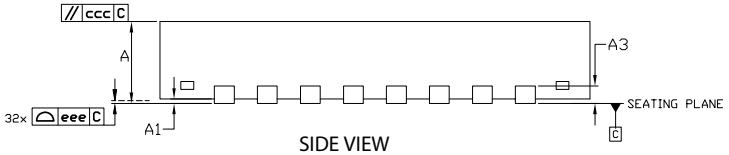
Figure 32. Typical Applications Schematic

Mechanical Dimensions



TOP VIEW

BOTTOM VIEW



SIDE VIEW

DIM / SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203Ref	
b	0.15	0.20	0.25
D		4.00 BSC	
E		4.00 BSC	
e		0.40 BSC	
D2	2.65	2.70	2.75
E2	2.65	2.70	2.75
L	0.30	0.35	0.40
K	0.20	–	–
aaa		0.10	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	
N		32	

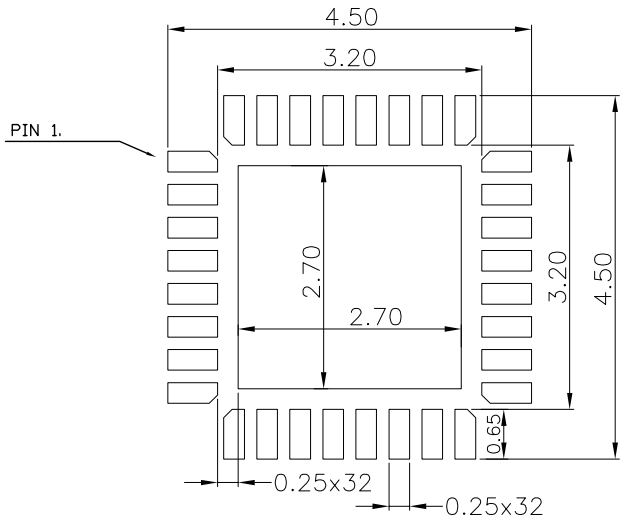
TERMINAL DETAILS

- ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES ARE IN DEGREES.
- DIMENSIONS AND TOLERANCE PER JEDEC MO-220.

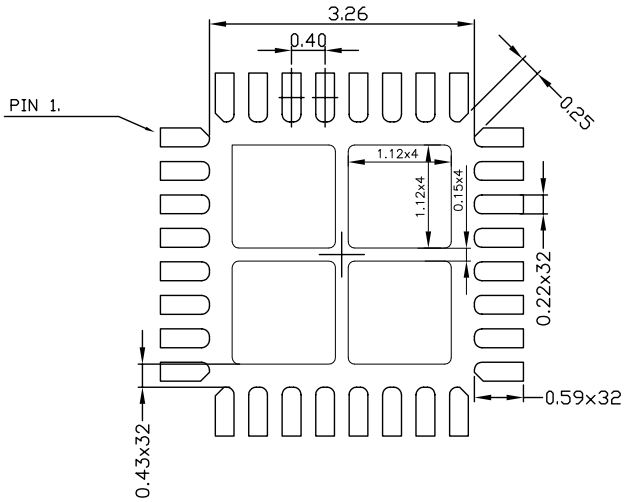
Drawing No.: POD-00000079

Revision: C

Recommended Land Pattern and Stencil



TYPICAL RECOMMENDED LAND PATTERN



TYPICAL RECOMMENDED STENCIL

Drawing No.: POD-00000079

Revision: C

Order Information[1]

Part Number	Operating Temperature Range	Lead-Free	Package	Packaging Quantity
XR77103ELBTR-A1R0	-40°C ≤ T_J ≤ 125°C	Yes[2]	32-pin, 4mm x 4mm TQFN package	Tape and Reel
XR77103EVB-A1R0	XR77103-A1R0 evaluation board			

NOTE:
1. Refer to www/maxlinear.com/XR77103-A1R0 for most up-to-date Ordering Information.
2. Visit www.maxlinear.com for additional information on Environmental Rating.

Revision History

Revision	Date	Description
1A	03/09/16	Initial Release
1B	11/21/17	Added MaxLinear logo. Updated format and ordering information format. Changed Packaging Description section name to Mechanical Dimensions and Recommended Land Pattern and Stencil. Corrected typo on Mechanical Dimensions, dimension A. Added revision history.
1C	1/17/19	Updated Frequency Compensation table. In Electrical Characteristics: updated Output voltage accuracy and changed power good pull-down on resistance row to PGOOD output low. Added Minimum On-Time section. Updated Applications Information Operation sentence. Updated input thresholds (SYNC, EN). Update Ordering Information.
1D	3/28/19	Change peak inductor current limit to accuracy. Increased peak inductor current limit to 4A.

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