SN74AHC1G09 Single 2–Input Positive-AND Gate With Open-Drain Output

1 Features

- Operating Range from 2 V to 5.5 V
- Maximum t_{pd} of 6 ns at 5 V
- ±8-mA Output Drive at 5 V
- Schmitt-Trigger Action at All Inputs Makes the Circuit Tolerant for Slower Input Rise and Fall Time
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22:
  - 2000-V Human-Body Model (A114-A)
  - 1000-V Charged-Device Model (C101)

2 Applications

- Barcode Scanners
- Cable Solutions
- E-Books
- Embedded PCs
- Field Transmitter: Temperature or Pressure Sensors
- Fingerprint Biometrics
- HVAC: Heating, Ventilating, and Air Conditioning
- Network-Attached Storage (NAS)
- Server Motherboard and PSU
- Software Defined Radios (SDR)
- TV: High Definition (HDTV), LCD, and Digital
- Video Communications Systems
- Wireless Data Access Cards, Headsets, Keyboards, Mice, and LAN Cards

3 Description

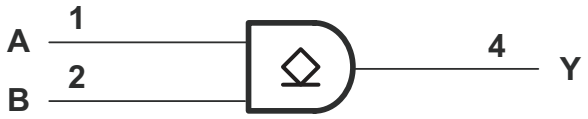
The SN74AHC1G09 is a single 2-input positive-AND gate with an open drain output configuration. The device performs the Boolean logic $Y = A \times B$ or $Y = \overline{\overline{A} + \overline{B}}$ in positive logic.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74AHC1G09DBVR	SOT-23 (5)	2.90 mm × 1.60 mm
SN74AHC1G09DCKR	SC70 (5)	2.00 mm × 1.25 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (January 2016) to Revision D — **Page**

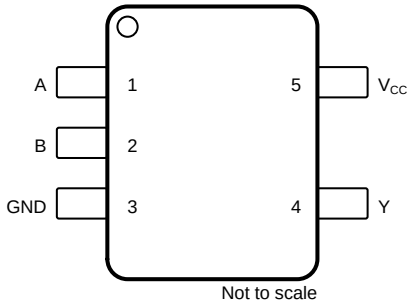
- Deleted 200-V Machine Model from *Features* ... 1
- Changed description for pin A from No connection to Input ... 3
- Added *Receiving Notification of Documentation Updates* section ... 10

Changes from Revision B (July 2011) to Revision C — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

5 Pin Configuration and Functions

DBV Package
5-Pin SOT-23
Top View



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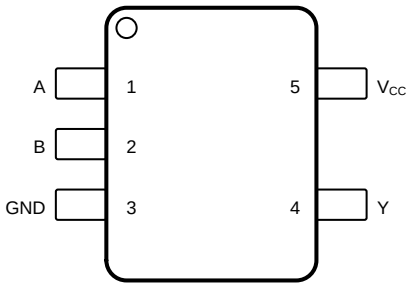
DCK Package
5-Pin SC70
Top View



Not to scale

Pin Functions(1)

PIN		I/O	DESCRIPTION
NAME	NO.		
A	1	I	Input
B	2	I	Input
GND	3	—	Ground
V_{CC}	5	—	Power pin
Y	4	O	Output

(1) See *Mechanical, Packaging, and Orderable Information* for dimensions.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	–0.5	7	V
V_I	Input voltage(2)	–0.5	7	V
V_O	Output voltage(2)	–0.5	V_{CC} + 0.7	V
I_{IK}	Input clamp current (V_I < 0)	–20		mA
I_{OK}	Output clamp current (V_O < 0 or V_O > V_{CC})	–20		mA
I_O	Continuous output current (V_O = 0 to V_{CC})	–25	+25	mA
	Continuous current through V_{CC} or GND	–50	+50	mA
T_J	Maximum junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 3 V	2.1		
		V_{CC} = 5.5 V	3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 3 V		0.9	
		V_{CC} = 5.5 V		1.65	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	5.5	V
I_{OL}	Low-level output current	V_{CC} = 2 V		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4	mA
		V_{CC} = 5 V ± 0.5 V		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20	
T_A	Operating free-air temperature		–55	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See *Implications of Slow or Floating CMOS Inputs*, SCBA004.

6.4 Thermal Information

THERMAL METRIC(1)		SN74AHC1G09		UNIT
		DBV (SOT-23)	DCK (SC70)	
		5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	206	252	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A	MIN	TYP	MAX	UNIT
V_{OL}	I_{OL} = 50 μA	2 V				0.1	V
		3 V				0.1	
		4.5 V				0.1	
	I_{OL} = 4 mA	3 V	T_A = 25°C			0.36	
			T_A = –40°C to +85°C			0.44	
			T_A = –55°C to +125°C			0.55	
	I_{OL} = 8 mA	4.5 V	T_A = 25°C			0.36	
			T_A = –40°C to +85°C			0.44	
			T_A = –55°C to +125°C			0.55	
I_I	V_I = 5.5 V or GND	0 V to 5.5 V	T_A = 25°C			±0.1	μA
			T_A = –40°C to +85°C			±1	
			T_A = –55°C to +125°C			±2	
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V	T_A = 25°C			1	μA
			T_A = –40°C to +85°C			10	
			T_A = –55°C to +125°C			20	
C_i	V_I = V_{CC} or GND	5 V	T_A = 25°C		4	10	pF
			T_A = –55°C to +125°C			10	

6.6 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	T_A	MIN	TYP	MAX	UNIT
t_{PD}	A or B	Y	C_L = 15 pF	T_A = 25°C		3.6	7	ns
				T_A = –40°C to +85°C	1		8	
				T_A = –55°C to +125°C	1		8.5	
	A or B	Y	C_L = 50 pF	T_A = 25°C		6.5	11	ns
				T_A = –40°C to +85°C	1.5		12	
				T_A = –55°C to +125°C	1.5		12.5	

6.7 Switching Characteristics, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range, V_{CC} = 5 V ±0.5 V (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	T_A	MIN	TYP	MAX	UNIT
t_{PD}	A or B	Y	C_L = 15 pF	T_A = 25°C		2.5	5	ns
				T_A = –40°C to +85°C	1		6	
				T_A = –55°C to +125°C	1		6.5	
	A or B	Y	C_L = 50 pF	T_A = 25°C		4.6	7.5	ns
				T_A = –40°C to +85°C	1.5		8	
				T_A = –55°C to +125°C	1.5		8.5	

6.8 Operating Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	5	pF

6.9 Typical Characteristics

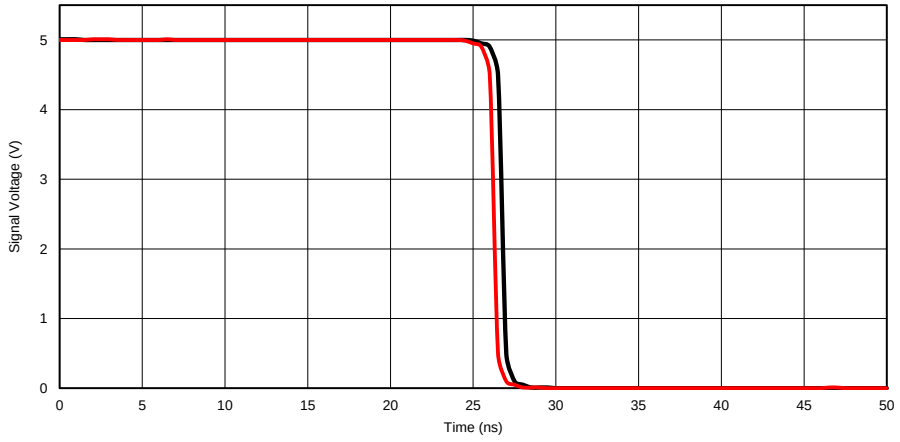
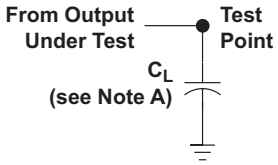
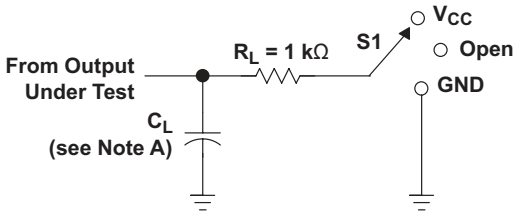


Figure 1. TPD Across V_{CC} at 25°C

7 Parameter Measurement Information

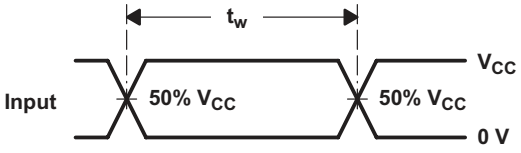


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

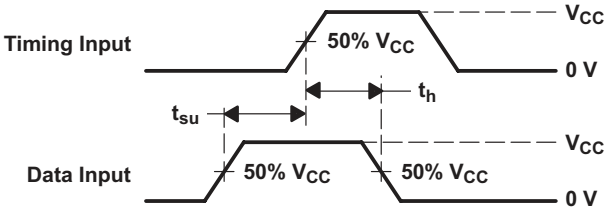


LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

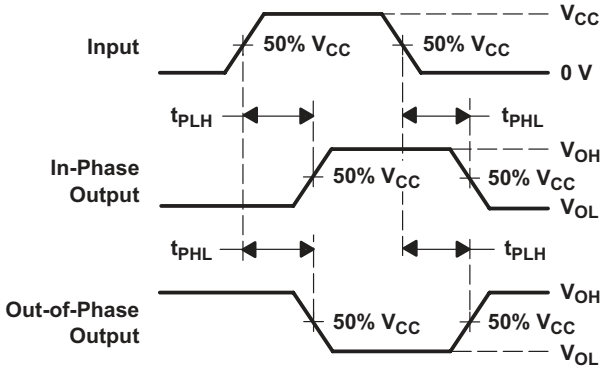
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}



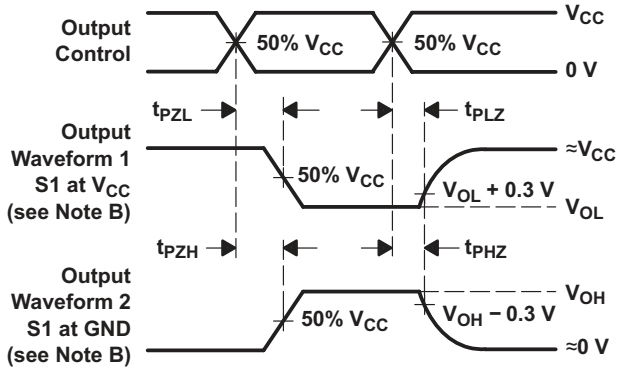
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.

D. The outputs are measured one at a time with one input transition per measurement.

E. All parameters and waveforms are not applicable to all devices.

F. Since this device has open-drain outputs, t_{PLZ} and t_{PZL} are the same as t_{PD}.

G. t_{PZL} is measured at $V_{CC}/2$.

H. t_{PLZ} is measured at V_{OL} + 0.3 V.

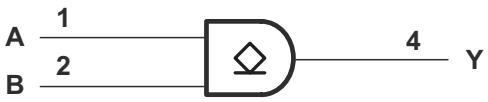
Figure 2. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74AHC1G09 device contains one open-drain positive-AND gate with a maximum sink current of 8 mA. A wide operating range of 2 V to 5.5 V enables this device to be used in many different systems, and a low t_{pd} qualifies this device to be used in high-speed applications.

8.2 Functional Block Diagram



8.3 Feature Description

The wide operating voltage range of 2 V to 5 V allows the SN74AHC1G09 to be used in systems with many different voltage rails. In addition, the voltage tolerance on the output allows the device to be used for inverting up-translation or down-translation. The device is also equipped with Schmitt-trigger inputs, which increase the ability of the device to reject noise.

8.4 Device Functional Modes

Table 1 lists the functional modes of the SN74AHC1G09.

Table 1. Function Table

INPUTS		OUTPUT
A	B	Y
H	H	H(Z)
L	X	L
X	L	L

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74AHC1G09 is used in the following example in a basic power sequencing configuration. Power sequencing is often used in applications that require a processor or other delicate device with specific voltage timing requirements in order to protect the device from malfunctioning.

9.2 Typical Application

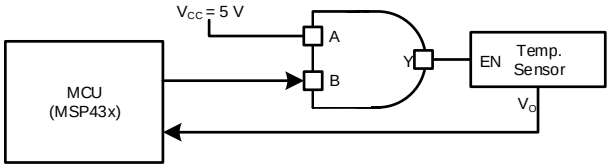


Figure 3. Typical Application Diagram

9.2.1 Design Requirements

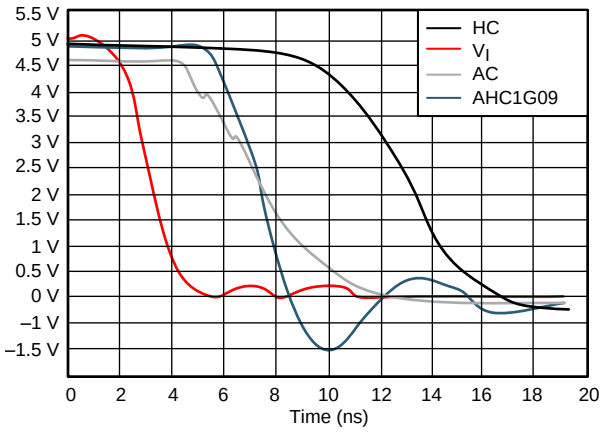
This device uses CMOS technology. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
   - Rise time and fall time specifications. See ($\Delta t/\Delta V$) in *Recommended Operating Conditions*.
   - Specified high and low levels. See (V_{IH} and V_{IL}) in *Recommended Operating Conditions*.
   - Inputs are overvoltage-tolerant, allowing them to go as high as (V_I maximum) in *Recommended Operating Conditions* at any valid V_{CC}.
2. Absolute Maximum Conditions:
   - Load currents should not exceed (I_O maximum) per output and should not exceed (Continuous current through V_{CC} or GND) total current for the part. These limits are located in *Absolute Maximum Ratings*.
   - Outputs should not be pulled above V_{CC}.

Typical Application (continued)

9.2.3 Application Curve



V_{CC} = 5 V, Load = 50 Ω / 50 pF

Figure 4. I_{CC} vs Input Voltage

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in *Recommended Operating Conditions*.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-μF capacitor is recommended; if there are multiple V_{CC} pins then a 0.01-μF or 0.022-μF capacitor is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. 0.1-μF and 1-μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices, inputs must not ever float. In many cases, functions or parts of functions of digital logic devices are unused (for example, when only two inputs of a triple-input AND gate are used, or only 3 of the 4 buffer gates are used). Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

The following are the rules that must be observed under all circumstances:

- All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating.
- The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever make more sense or is more convenient.

11.2 Layout Example

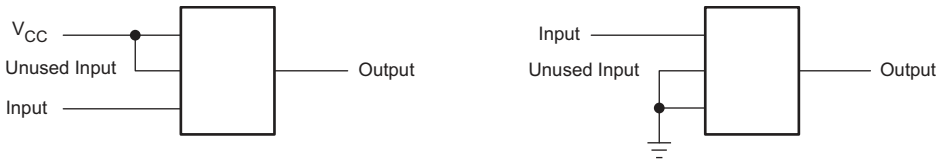


Figure 5. Layout Diagram

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- *Introduction to Logic*, SLVA700
- *Implications of Slow or Floating CMOS Inputs*, SCBA004

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AHC1G09DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 125	(A093, A09G, A09J)	Samples
SN74AHC1G09DCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 125	(AJ3, AJG, AJJ)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

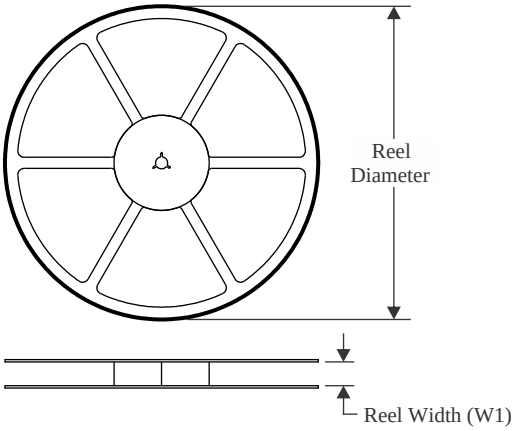
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

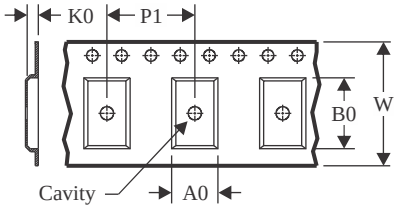
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

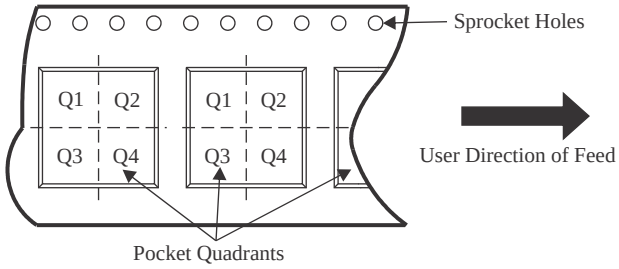


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

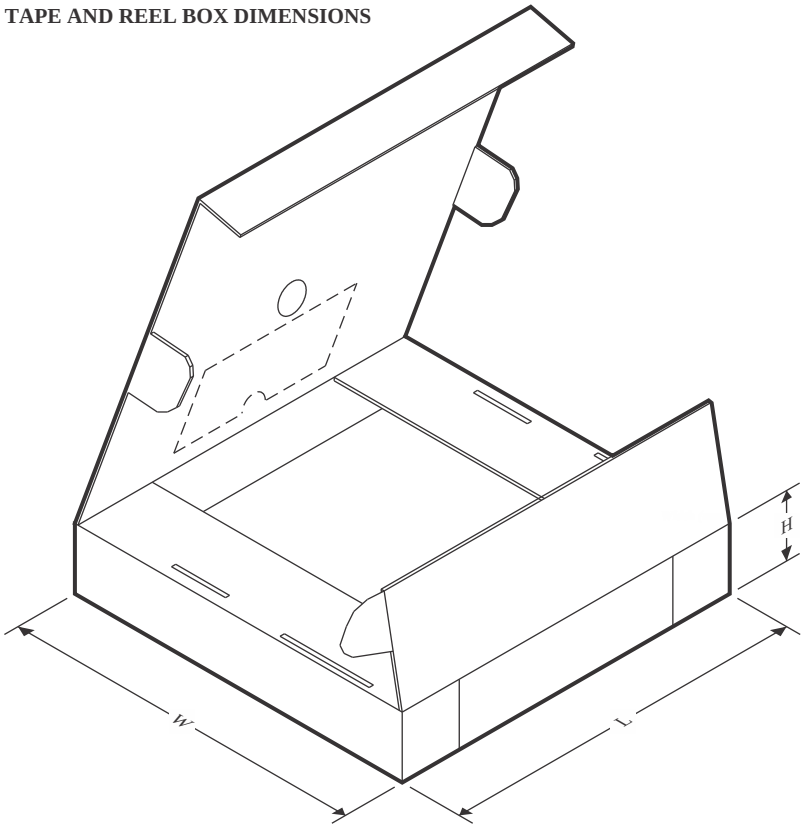
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC1G09DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
SN74AHC1G09DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74AHC1G09DCKR	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

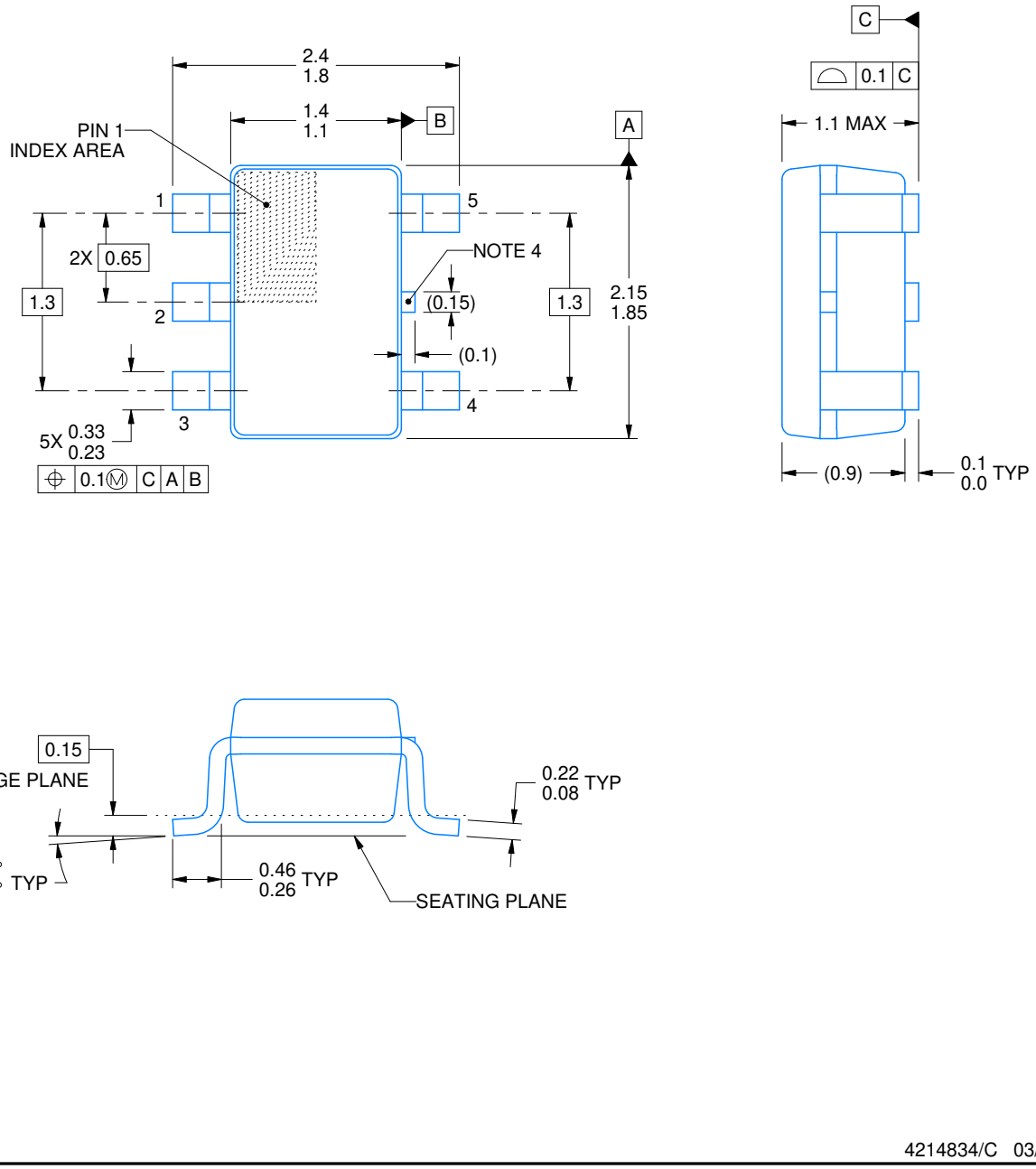
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC1G09DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74AHC1G09DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74AHC1G09DCKR	SC70	DCK	5	3000	180.0	180.0	18.0

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

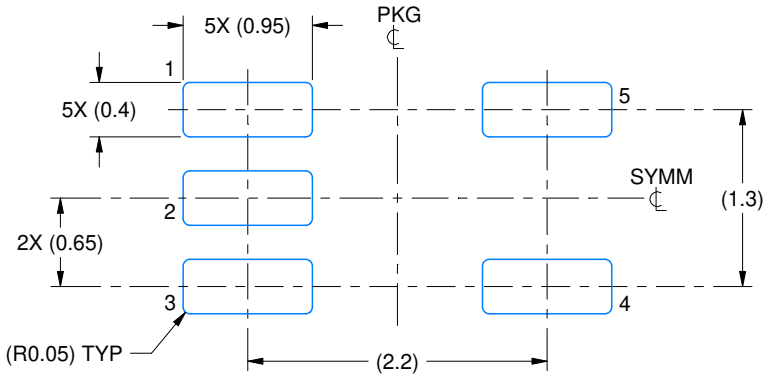
SMALL OUTLINE TRANSISTOR



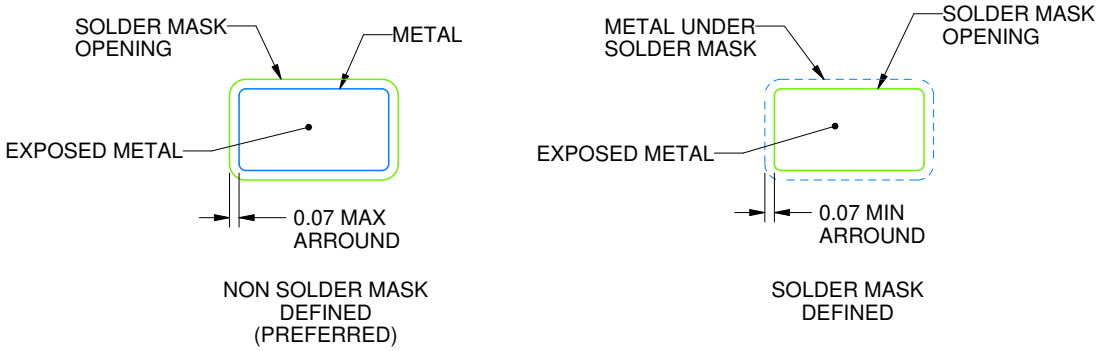
4214834/C 03/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

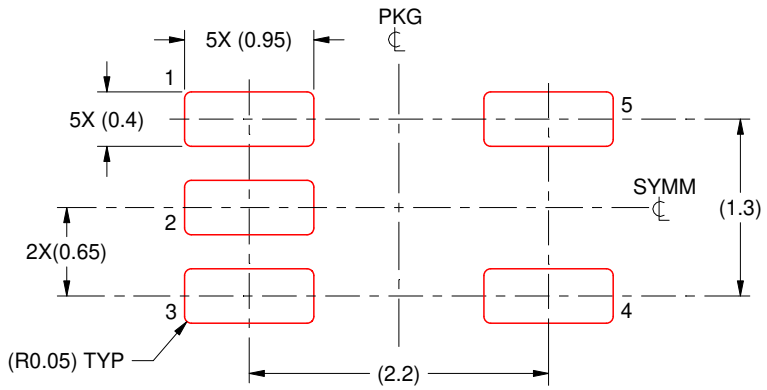


SOLDER MASK DETAILS

4214834/C 03/2023

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/C 03/2023

NOTES: (continued)

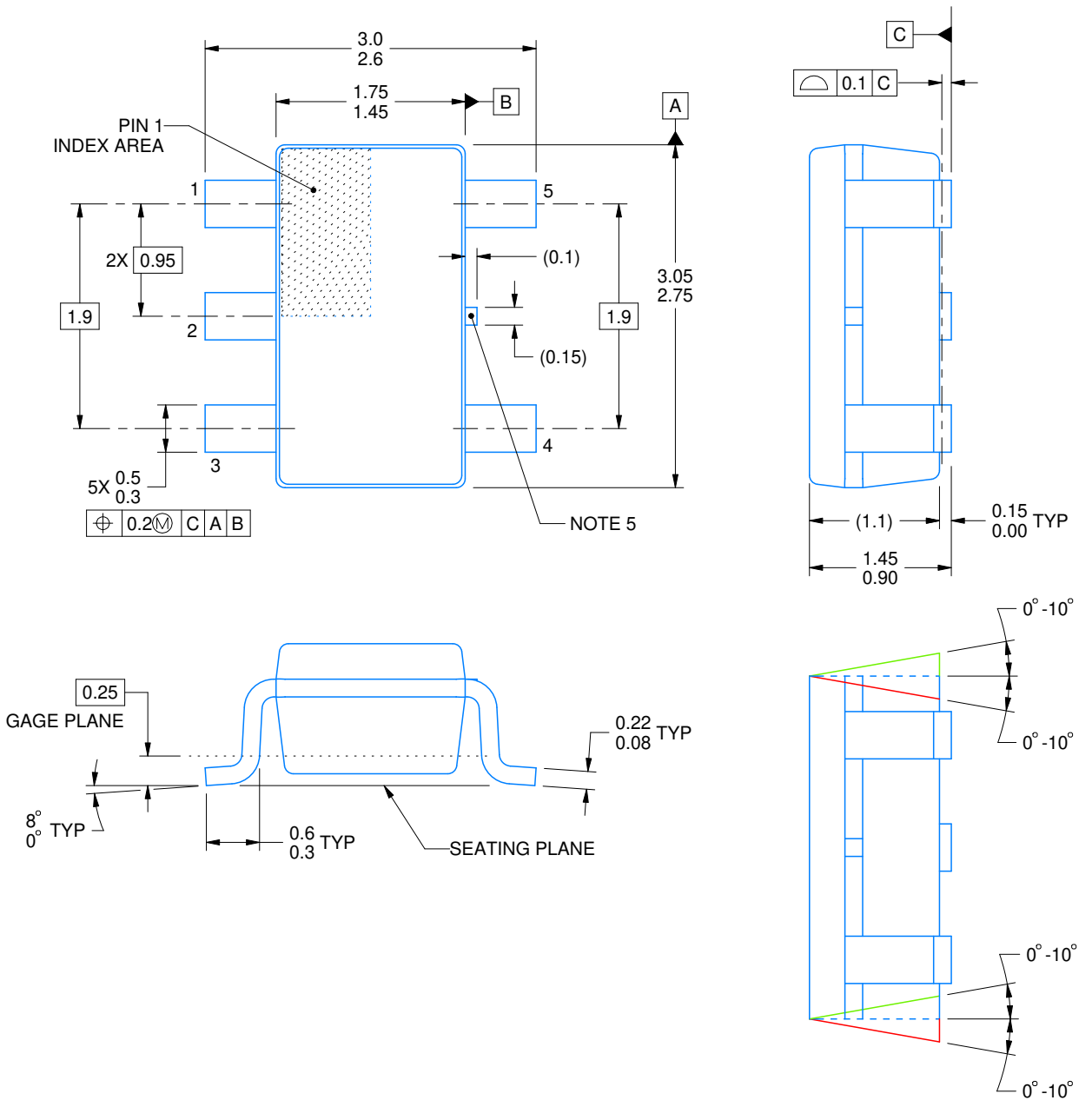
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

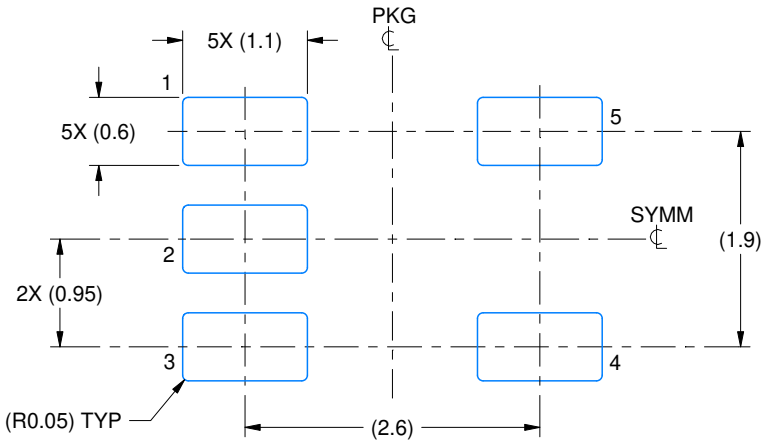


ALTERNATIVE PACKAGE SINGULATION VIEW

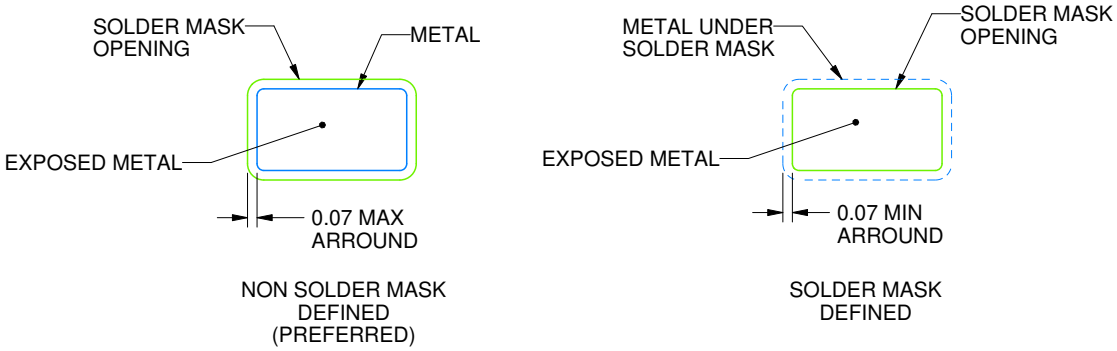
4214839/H 09/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

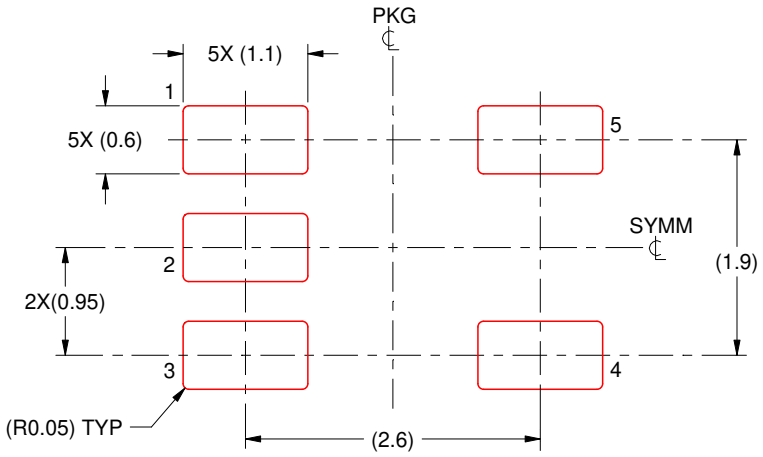


SOLDER MASK DETAILS

4214839/H 09/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/H 09/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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