

# FEATURES

Controlled Baseline

 One Assembly/Test Site, One Fabrication Site

- Extended Temperature Performance of -55°C to 125°C
- Enhanced Diminishing Manufacturing Sources (DMS) Support
- Enhanced Product-Change Notification
- Qualification Pedigree (1)
- Meets or Exceeds the Requirements of ANSI TIA/EIA-422-B, TIA/EIA-423-B, and ITU Recommendations V.10 and V.11
- ±7-V Common-Mode Range With ±200-mV Sensitivity
- Input Hysteresis . . . 50 mV Typ
- Operates From a Single 5-V Supply
- Low-Power Schottky Circuitry
- 3-State Outputs
- (1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

# **DESCRIPTION/ORDERING INFORMATION**

The AM26LS32A is a quadruple differential line receiver for balanced and unbalanced digital data transmission. The enable function is common to all four receivers and offers a choice of active-high or active-low input. The 3-state outputs permit connection directly to a bus-organized system. Fail-safe design ensures that, if the inputs are open, the outputs always are high.

The AM26LS32A incorporates an additional stage of amplification to improve sensitivity. The input impedance has been increased, resulting in less loading of the bus line. The additional stage has increased propagation delay, however, this does not affect interchangeability in most applications.

The AM26LS32AM is characterized for operation over the full military temperature range of -55°C to 125°C.

### **ORDERING INFORMATION**

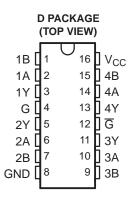
T <sub>A</sub>	PACKAG	GE <sup>(1)</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	SOIC – D	Tape and reel	AM26LS32AMDREP	26LS32EP

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

- Complementary Output-Enable Inputs
- Input Impedance . . . 12 k $\Omega$  Min
- Designed to Be Interchangeable With Advanced Micro Devices AM26LS32

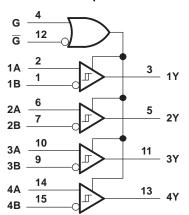


# AM26LS32AM-EP **QUADRUPLE DIFFERENTIAL LINE RECEIVER** SLLS730-OCTOBER 2006

### FUNCTION TABLE<sup>(1)</sup> (each receiver)

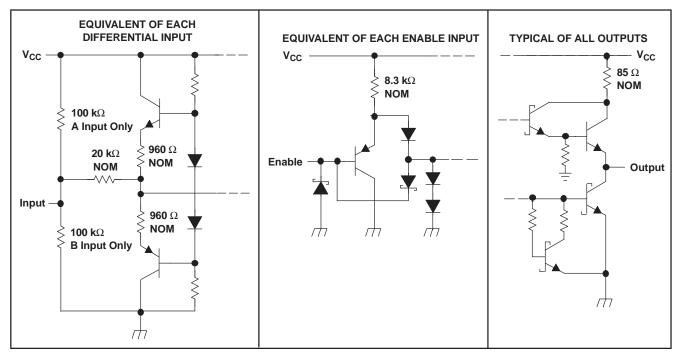
DIFFERENTIAL	ENA	BLES	OUTPUT
A – B	G	G	Y
N SN	Н	Х	Н
$V_{ID} \ge V_{IT+}$	Х	L	н
	Н	Х	?
$V_{IT-} \le V_{ID} \le V_{IT+}$	Х	L	?
	Н	Х	L
$V_{ID} \leq V_{IT-}$	Х	L	L
Х	L	Н	Z
Open	Н	Х	Н
Open	Х	L	н

(1) H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)



### LOGIC DIAGRAM (POSITIVE LOGIC)

### SCHEMATICS OF INPUTS AND OUTPUTS



# Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage <sup>(2)</sup>			7	V
V	lanut voltogo	Any differential input		±25	V
VI	Input voltage	Other inputs		7	
V <sub>ID</sub>	Differential input voltage <sup>(3)</sup>			±25	V
	Continuous total power dissipation		See Dissi	pation Ra	ating Table
$\theta_{JA}$	Package thermal impedance <sup>(4)</sup>	D package		111.6	°C/W
T <sub>stg</sub>	Storage temperature range <sup>(5)</sup>		-65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values, except differential voltages, are with respect to the network ground terminal.

(3) Differential voltage values are at the noninverting (A) input terminals with respect to the inverting (B) input terminals.

(4) The package thermal impedance is calculated in accordance with JESD 51-7.

(5) Long-term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See http://www.ti.com/ep\_quality for additional information on enhanced plastic packaging.

#### **DISSIPATION RATING TABLE**

PACKAGE	T <sub>A</sub> ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T <sub>A</sub> = 25°C	T <sub>A</sub> = 70°C POWER RATING	T <sub>A</sub> = 125°C POWER RATING
D	1075 mW	8.9 mW/°C	672 mW	179 mW

# AM26LS32AM-EP QUADRUPLE DIFFERENTIAL LINE RECEIVER



# **Recommended Operating Conditions**

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	4.5	5	5.5	V
$V_{\text{IH}}$	High-level input voltage	2			V
$V_{IL}$	Low-level input voltage			0.8	V
V <sub>IC</sub>	Common-mode input voltage			±7	V
I <sub>OH</sub>	High-level output current			-440	μΑ
I <sub>OL</sub>	Low-level output current			8	mA
T <sub>A</sub>	Operating free-air temperature	-55		125	°C

# **Electrical Characteristics**

over recommended ranges of  $V_{CC}$ ,  $V_{IC}$ , and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST	MIN	TYP <sup>(1)</sup>	MAX	UNIT		
V <sub>IT+</sub>	Positive-going input threshhold voltage	$V_{O} = V_{OH} \text{ min}, I_{OH} = -440 \text{ J}$			0.2	V		
V <sub>IT-</sub>	Negative-going input threshhold voltage	V <sub>O</sub> = 0.45 V, I <sub>OL</sub> = 8 mA	-0.2 <sup>(2)</sup>			V		
V <sub>hys</sub>	Hysteresis voltage (V <sub>IT+</sub> – V <sub>IT-</sub> )				50		mV	
V <sub>IK</sub>	Enable-input clamp voltage	$V_{CC} = MIN,$	I <sub>I</sub> = -18 mA			-1.5	V	
V <sub>OH</sub>	High-level output voltage	$V_{CC} = MIN, V_{ID} = 1 V, V_{I(G)}$	$V_{CC} = MIN, V_{ID} = 1 V, V_{I(G)} = 0.8 V, I_{OH} = -440 \mu A$				V	
V		$V_{CC} = MIN, V_{ID} = -1 V,$	$I_{OL} = 4 \text{ mA}$			0.4	.4 V	
V <sub>OL</sub>	Low-level output voltage	$V_{I(G)} = 0.8 V$	I <sub>OL</sub> = 8 mA			0.45		
_	Off-state		V <sub>O</sub> = 2.4 V			20		
I <sub>OZ</sub>	(high-impedance state) output current	V <sub>CC</sub> = MAX	V <sub>O</sub> = 0.4 V			–20 <sup>µ</sup>		
	Line input ourrept	V <sub>I</sub> = 15 V,	Other input at -10 V to 15 V			1.2	mA	
I <sub>I</sub>	Line input current	$V_{I} = -15 V,$	Other input at -15 V to 10 V			-1.7	ШA	
I <sub>I(EN)</sub>	Enable input current	V <sub>I</sub> = 5.5 V				100	μA	
IIH	High-level enable current	V <sub>I</sub> = 2.7 V				20	μA	
$I_{\rm IL}$	Low-level enable current	V <sub>I</sub> = 0.4 V				-0.36	mA	
r <sub>l</sub>	Input resistance	$V_{IC} = -15 \text{ V to } 15 \text{ V},$	One input to ac ground	12	15		kΩ	
I <sub>OS</sub>	Short-circuit output current <sup>(3)</sup>	$V_{CC} = MAX$		-15		-85	mA	
I <sub>CC</sub>	Supply current	V <sub>CC</sub> = MAX,	All outputs disabled		52	70	mA	

(1) All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ , and  $V_{IC} = 0$ . (2) The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold levels only.

(3) Not more than one output should be shorted to ground at a time, and duration of the short circuit should not exceed one second.

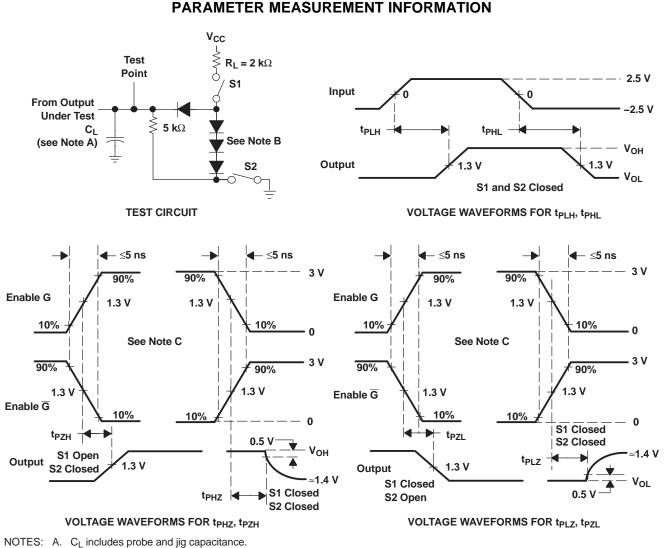
# **Switching Characteristics**

 $V_{CC} = 5 \text{ V}, \text{ T}_{A} = 25^{\circ}\text{C}$ 

	PARAMETER	TEST	TEST CONDITIONS			MAX	UNIT
t <sub>PLH</sub>	Propagation delay time, low-to-high-level output	0 15 55	See Figure 1		20	35	20
t <sub>PHL</sub>	Propagation delay time, high-to-low-level output	— C <sub>L</sub> = 15 pF,	See Figure 1		22	35	ns
t <sub>PZH</sub>	Output enable time to high level	0 15 55	See Figure 1		17	22	20
t <sub>PZL</sub>	Output enable time to low level	— C <sub>L</sub> = 15 pF,	See Figure 1		20	25	ns
t <sub>PHZ</sub>	Output disable time from high level		See Figure 1		21	30	20
t <sub>PLZ</sub>	Output disable time from low level	– C <sub>L</sub> = 5 pF,	See Figure 1		30	40	ns

# AM26LS32AM-EP QUADRUPLE DIFFERENTIAL LINE RECEIVER

SLLS730-OCTOBER 2006



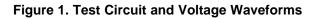
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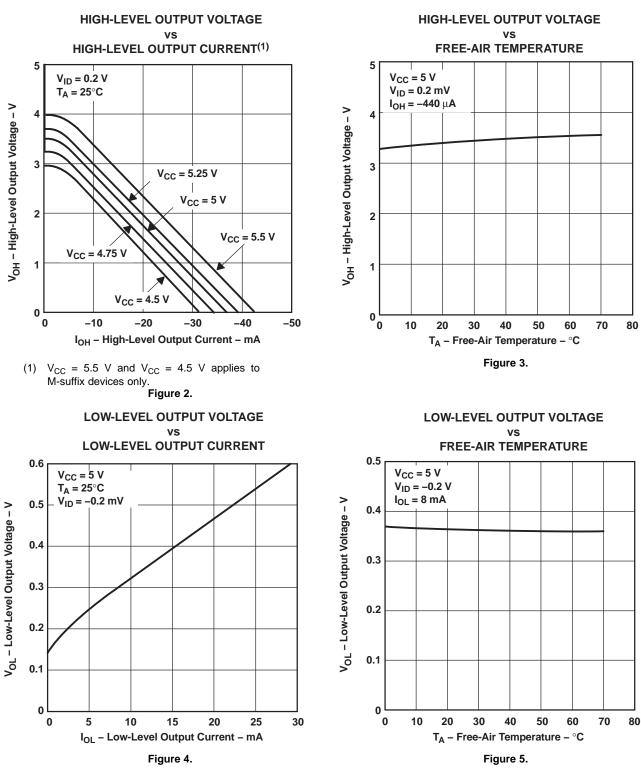
INSTRUMENTS www.ti.com

B. All diodes are 1N3064 or equivalent.

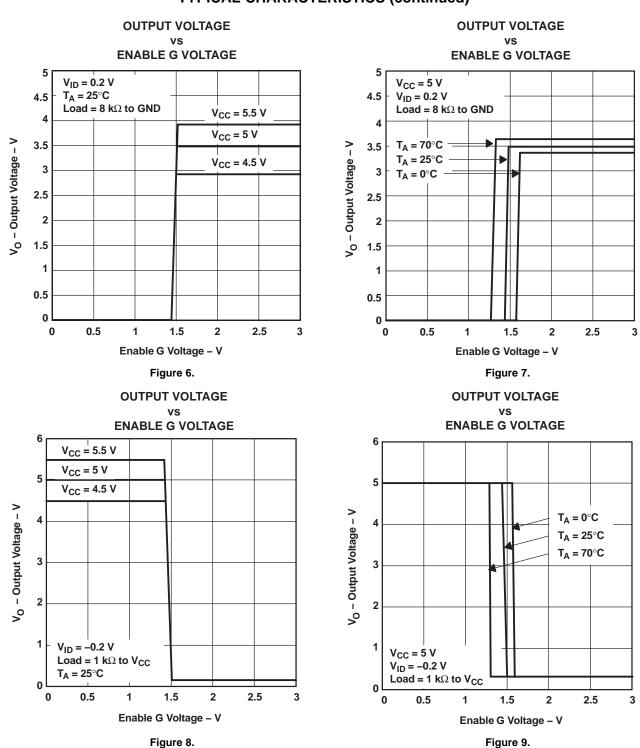
C. Enable G is tested with  $\overline{G}$  high;  $\overline{G}$  is tested with G low.



# **TYPICAL CHARACTERISTICS**

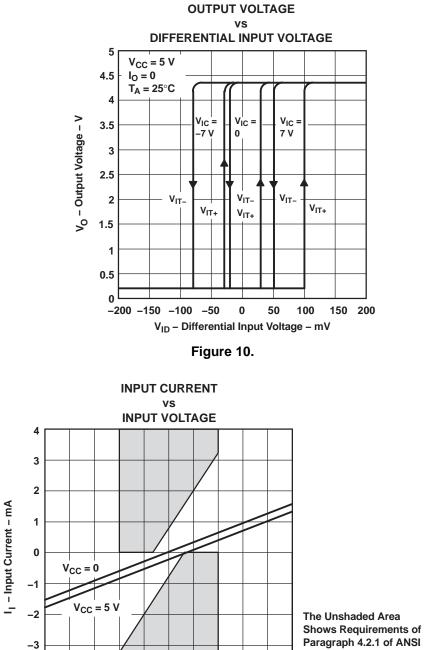






#### TYPICAL CHARACTERISTICS (continued)

# **TYPICAL CHARACTERISTICS (continued)**



Standards EIA/TIA-422-B and EIA/TIA-423-B.



20 25

-4 -25

-20 -15 -10

-5 0 5 10 15

V<sub>I</sub> – Input Voltage – V



29-May-2015

# **PACKAGING INFORMATION**

Orderable Device	Status	Package Type	Package	Pins	Package	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
AM26LS32AMDREP	LIFEBUY	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	26LS32EP	
V62/07603-01XE	LIFEBUY	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	26LS32EP	

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between

the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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# PACKAGE OPTION ADDENDUM

29-May-2015

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

#### OTHER QUALIFIED VERSIONS OF AM26LS32AM-EP :

Catalog: AM26LS32AM

NOTE: Qualified Version Definitions:

• Catalog - TI's standard catalog product

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



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