TOSHIBA Field-Effect Transistor Silicon P-Channel MOS Type (U-MOS V)

SSM6J409TU

- Power Management Switch Applications
- High-Speed Switching Applications

• 1.5V drive

Low ON-resistance: R_{on} = 72.3mΩ (max) (@V_{GS} = -1.5 V)

 $R_{on} = 46.2 m\Omega \text{ (max) } (@V_{GS} = -1.8 \text{ V})$

 $R_{on} = 30.2 \text{m}\Omega \text{ (max) (@V}_{GS} = -2.5 \text{ V)}$

 $R_{on} = 22.1 m\Omega \text{ (max) } (@V_{GS} = -4.5 \text{ V})$

Absolute Maximum Ratings (Ta = 25°C)

Characteristic		Symbol		Rating	Unit	
Drain-Source voltage		V_{DSS}		-20	(y)	
Gate-Source voltage		V _{GSS}		±8	$\langle \rangle$	
Drain current	DC	ID	(Note 1)	-9.5	A	
	Pulse	I _{DP}	(Note 1)	-19.0		
Drain power dissipation		P_{D}	(Note 2)	1	- W	
			t=10s	2		
Channel temperature			T _{ch}	150	°C	
Storage temperature range			T _{stg}	-55 to 150	⟨⟨c	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling

Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

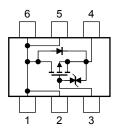
Note 1: The junction temperature should not exceed 150°C during use.

Note 2: Mounted on an FR4 board. (25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 645 mm²)

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Marking

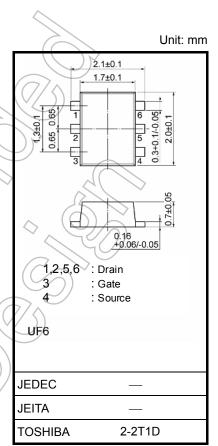
Equivalent Circuit (top view)



Handling Precaution

When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.

Start of commercial production 2009-06

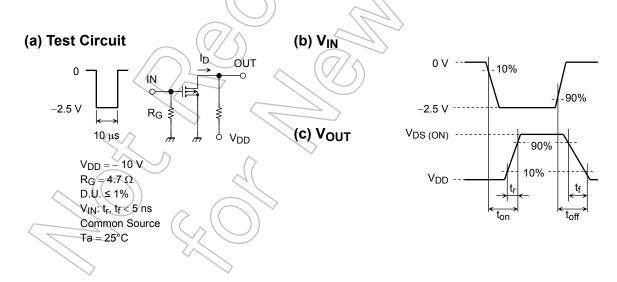


Electrical Characteristics (Ta = 25°C)

Chara	cteristic	Symbol	Test Conditions	Min	Тур.	Max	Unit		
Drain Course breekdown voltage	V (BR) DSS	$I_D = -1 \text{ mA}, V_{GS} = 0 \text{ V}$	-20	_	_	V			
Drain-Source breakdown voltage		V (BR) DSX	I _D = -1 mA, V _{GS} = +8 V	-12	_	_	v		
Drain cut-off curre	nt	I _{DSS}	V _{DS} = -20 V, V _{GS} = 0 V	$\overline{}$	_	-10	μΑ		
Gate leakage curre	ent	I_{GSS} $V_{GS} = \pm 8 \text{ V}, V_{DS} = 0 \text{ V}$			_	±1	μА		
Gate threshold vol	tage	V _{th}	$V_{DS} = -3 \text{ V}, I_D = -1 \text{ mA}$	-0.3	A.	-1.0	V		
Forward transfer a	dmittance	Y _{fs}	$V_{DS} = -3 \text{ V}, I_D = -3.0 \text{ A}$ (Note 3)	10	20	_	S		
Dania angga ON sasistana		R _{DS} (ON)	$I_D = -3.0 \text{ A}, V_{GS} = -4.5 \text{ V}$ (Note 3)	(/ / \)	17.8	22.1	- mΩ		
			$I_D = -2.0 \text{ A}, V_{GS} = -2.5 \text{ V}$ (Note 3)		23.5	30.2			
Drain-source ON-resistance	$I_D = -1.5 \text{ A}, V_{GS} = -1.8 \text{ V}$ (Note 3)		14	31.5	46.2				
			$I_D = -0.8 \text{ A}, V_{GS} = -1.5 \text{ V}$ (Note 3)	7_	40.0	72.3			
Input capacitance		C _{iss}		_	1100	1			
Output capacitance		Coss	$V_{DS} = -10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	_	240	//	pF		
Reverse transfer capacitance		C _{rss}	$(\langle // \rangle)$	<u>~</u> (180				
Total Gate Charge		Qg	V 10 V I - 0 F A	4	15.0)}	nC		
Gate-Source Charge		Q _{gs}	$V_{DD} = -10 \text{ V}, I_{D} = -9.5 \text{ A}$ $V_{GS} = -4.5 \text{ V}$	(7)	10.9	_			
Gate-Drain Charge		Q _{gd}	VGS4.5 V		4.1	_			
Switching time	Turn-on time	t _{on}	V _{DD} = -10 V, I _D = -2.0 A,	>	40	_	ns		
	Turn-off time	t _{off}	V_{GS} = 0 to -2.5 V, R_{G} = 4.7 Ω	$\supset +$	207	_			
Drain-Source forward voltage		V _{DSF}	$I_D = 9.5 \text{ A}, V_{GS} = 0 \text{ V}$ (Note 3)	_	0.83	1.2	V		

Note3: Pulse test

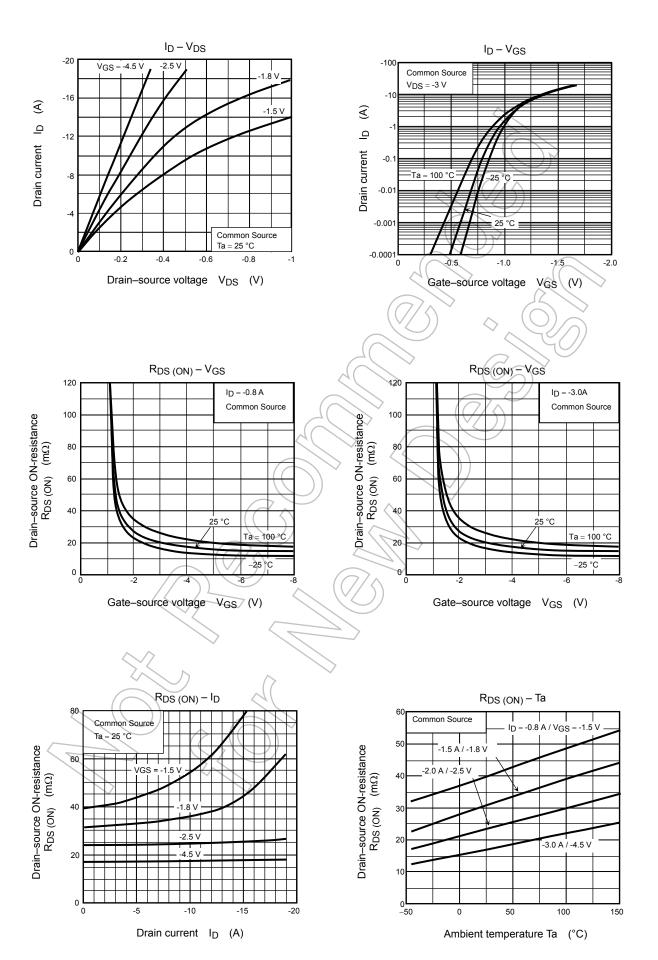
Switching Time Test Circuit



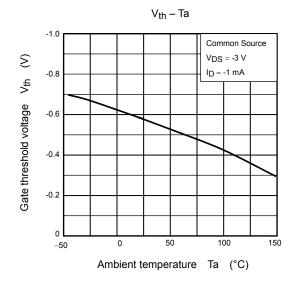
Notice on Usage

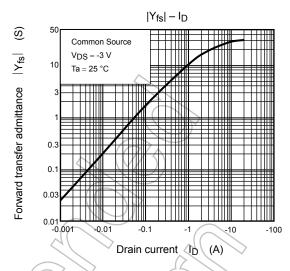
 V_{th} can be expressed as the voltage between gate and source when the low operating current value is I_D = -1 mA for this product. For normal switching operation, $V_{GS\ (on)}$ requires a higher voltage than V_{th} and $V_{GS\ (off)}$ requires a lower voltage than V_{th} . (The relationship can be established as follows: $V_{GS\ (off)} < V_{th} < V_{GS\ (on)}$.)

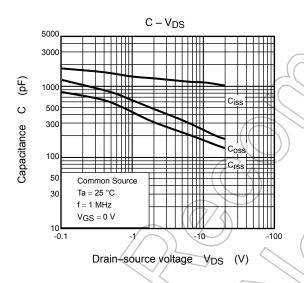
Take this into consideration when using the device.

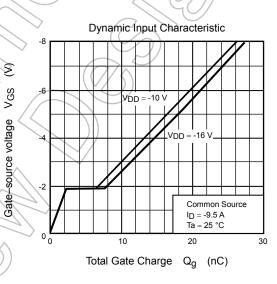


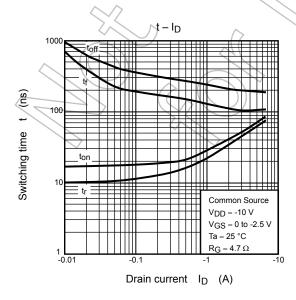
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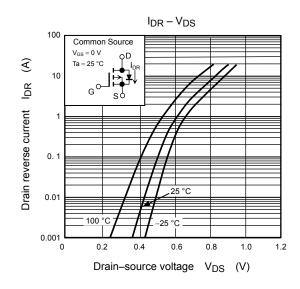


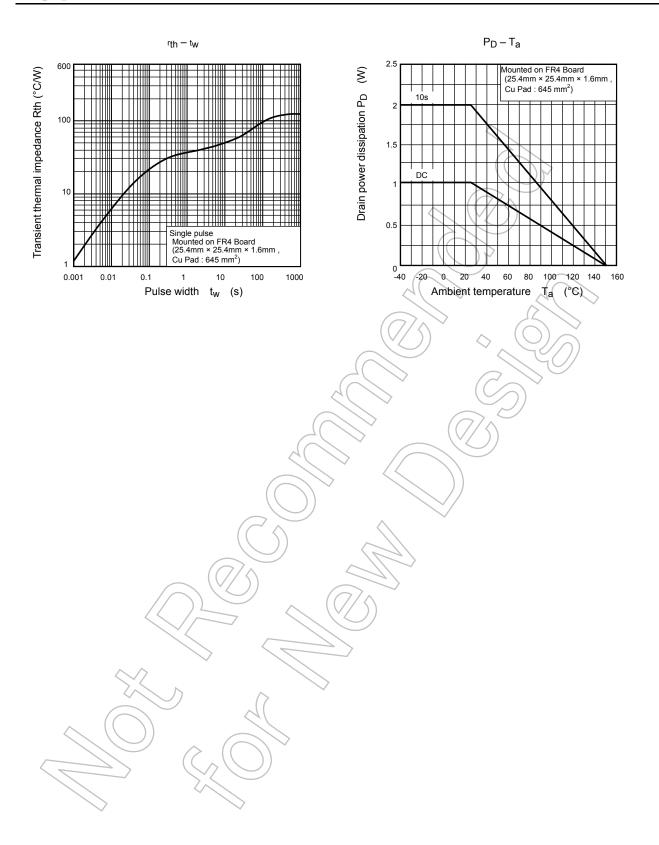












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