VL-1262
VL-12CT62

12-Bit Analog Output Card
for the STD Bus

Model VL-1262

12-Bit Analog Output Card for the STD Bus

REFERENCE MANUAL

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VL-12CT62 Rev. 2.00
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M1262

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Overview

This manual details the installation and operation of VersaLogic's VL-1262 analog output card. This card provides four independent channels of analog output each with 12-bit accuracy. Two of the channels may optionally be configured for 4-20 mA current loop operation.

Introduction

In its standard configuration the VL-1262 provides four single-ended analog output channels. It features 12-bit resolution, and an on-board DC to DC converter (requires +5 volt supply only). Each channel may be jumpered for 0 to 5, 0 to 10, -5 to +5, or -10 to +10 volt output at 5 mA. Optionally the board can be ordered with two of the channels equipped for 4-20 mA current loop output.

Output signals connect to the card through a single 26-pin header type connector. When operated in the voltage output mode, voltage sense lines are made available to compensate for voltage drops which can occur in cables and connectors.

The VL-1262 supports 8, 10, and 16-bit I/O addressing, and 16-bit memory addressing. Both the MEMEX and IOEXP STD Bus signals are supported. The board uses an 8-byte interface port and may be positioned on any 8- byte boundary.

The VL-1262 is plug-in compatible with the Analog Devices RTI-1262 card.

This card is available in standard (VL-1262) and extended temperature (VL-12CT62) versions. Throughout this manual "VL-1262" will be used to refer to both versions of these boards, unless specifically noted otherwise.

Features

- 12-bit (4096 count) output resolution
- 4 output channels with voltage sense
- 0-5, 0-10, ±5, or ±10 volt output ranges
- Two current loop outputs (optional)
- +5V single supply operation
- 16-bit memory or I/O addressed
- MEMEX and IOEXP supported
- Extended temperature version available
- Plug-in replacement for Analog Devices RTI-1262

Specifications

The specifications below are typical at 25°C with 5.0V supply unless otherwise noted.

Number of Channels: 4
Resolution: 12 bits (4096 counts)
Data Format: Straight binary or offset binary
Voltage Range: 0-5V, 0-10V, ±5V, ±10V @ 5 mA (max.)
Current Range: 4-20 mA (with current loop option)
Settling Time: 25 µs (to ±½ LSB)
Nonlinearity: ±½ LSB
Differential Nonlinearity: ±½ LSB
Temperature Coefficient:
Gain ±15 ppm/°C of FSR
Offset ±25 uV/°C
Addressing: Memory or I/O, 8-16 bits plus MEMEX or IOEXP
Mapping: 8-byte block on any 8-byte boundary
Size: Meets all STD Bus mechanical specifications
Storage Temperature: -40° to +85° C
Free Air Operating Temperature:

VL-1262	0° to +65° C
VL-12CT62	-25° to +85° C

Power Requirements:

VL-1262	5V ±5% @ 485 mA typ.
	15V to 30V @ 25 mA (with current loop option only)
VL-12CT62	5V ±5% @ 300 mA typ.
	15V to 30V @ 25 mA (with current loop option only)

Specifications subject to change without notice.

Configuration

Jumper Options

Various options available on the VL-1262 card are selected using removable jumper plugs (shorting plugs). Features are selected or deselected by installing or removing the jumper plugs as noted. The terms "In" or "Jumpered" are used to indicate an installed plug; "Out" or "Open" are used to indicate a removed plug.

Figure 2-1 shows the jumper block locations on the VL-1262 board. The figure indicates the position of the jumper plugs as shipped from the factory. The function of each jumper block is detailed in Figure 2-2.

VL-1262 Jumper Block Locations

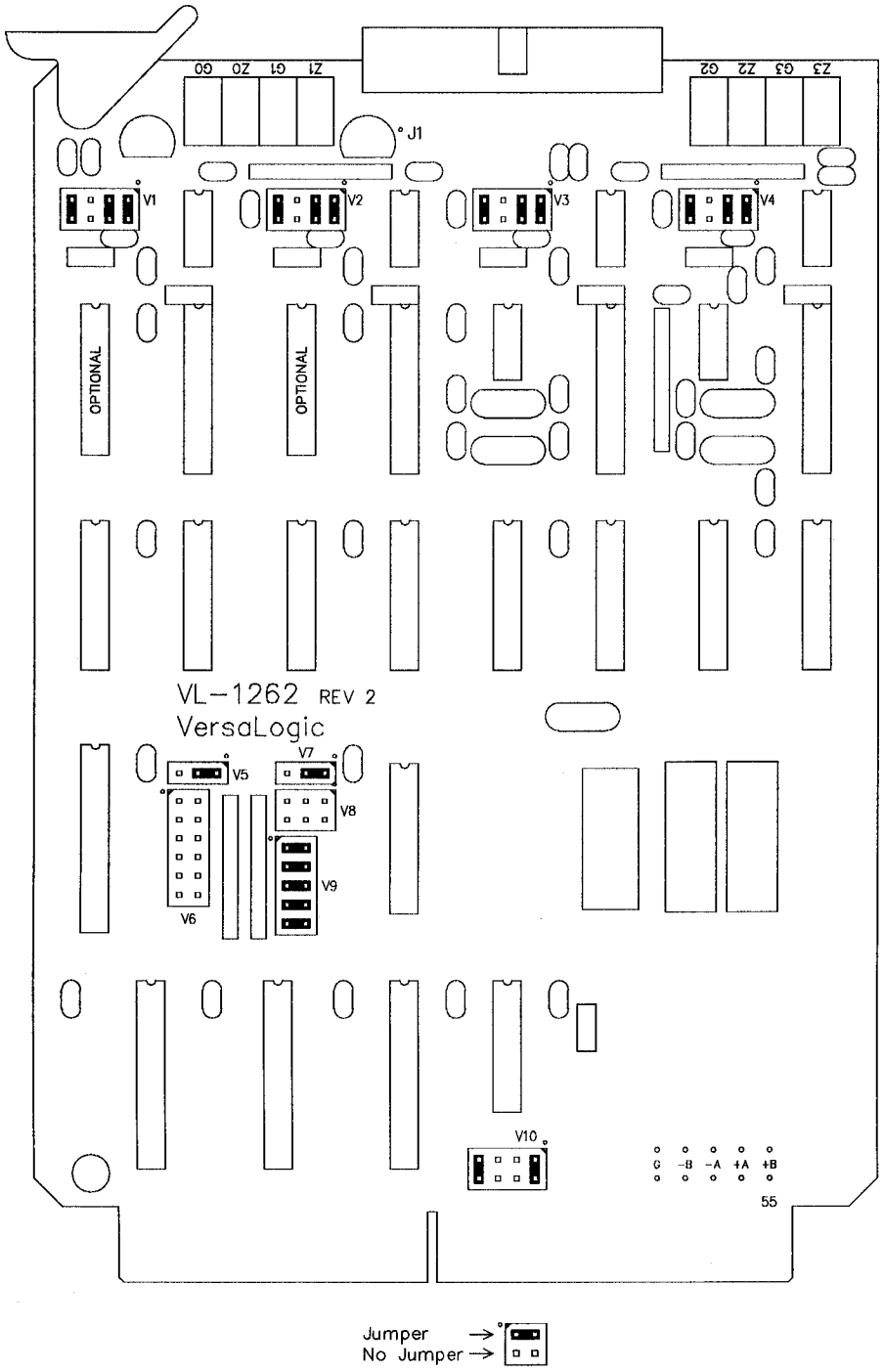


Figure 2-1. Jumper Block Locations for VL-1262

VL-1262 Jumper Options

Jumper Block	Description	As Shipped	Page
$V1_a$	Channel 0 Remote Sense In – Local Sense Out – Remote Sense	Local Sense	2-11
$V1_{b-d}$	Channel 0 Output Range c – 0 to +5V d – 0 to +10V b & c – ±5V b & d – ±10V	±10V	2-11
$V2_a$	Channel 1 Remote Sense In – Local Sense Out – Remote Sense	Local Sense	2-11
$V2_{b-d}$	Channel 1 Output Range c – 0 to +5V d – 0 to +10V b & c – ±5V b & d – ±10V	±10V	2-11
$V3_a$	Channel 2 Remote Sense In – Local Sense Out – Remote Sense	Local Sense	2-11
$V3_{b-d}$	Channel 2 Output Range c – 0 to +5V d – 0 to +10V b & c – ±5V b & d – ±10V	±10V	2-11
$V4_a$	Channel 3 Remote Sense In – Local Sense Out – Remote Sense	Local Sense	2-11
$V4_{b-d}$	Channel 3 Output Range c – 0 to +5V d – 0 to +10V b & c – ±5V b & d – ±10V	±10V	2-11
V5	MEMEX Select a – Board responds to MEMEX high and low (MEMEX ignored) b – Board responds to MEMEX low None – Board responds to MEMEX high	Ignored	2-10
V6	Board Address (A10 – A15) a – A15 b – A14 c – A13 d – A12 e – A11 f – A10	FF00H a Out b Out c Out d Out e Out f Out	2-4
V7	IOEXP Select a – Board responds to IOEXP high and low (IOEXP ignored) b – Board responds to IOEXP low None – Board responds to IOEXP high	Ignored	2-8
V8	Board Address (A8, A9) / 8-Bit mode selector a – A9 b – A8	FF00H a Out b Out	2-4
V9	Board Address (A3-A7) a – A7 b – A6 c – A5 d – A4 e – A3	FF00H a In b In c In d In e In	2-4
V10	Address Mode Select a & d – 16-bit memory addressing a & c – 8-bit I/O addressing b & d – 16-bit I/O addressing	16-Bit Mem.	2-4

Figure 2-2. VL-1262 Jumper Options

Board Addressing

The VL-1262 supports 8, 10, and 16-bit I/O addressing, and 16-bit memory addressing. 8-bit I/O addressing is used with most 8-bit processors (Z80, 8085, 6809, etc.) which provide 256 I/O addresses. 10 or 16-bit addressing can be used with 16-bit processors (i.e., 8088) to decode 1024 or 65536 I/O port addresses. 16-bit memory addressing can be used with most 8-bit processors (Z80, 8085, 6809, etc.) if desired.

I/O addressing can be extended (capacity doubled) using the IOEXP signal which is decoded by the VL-1262. Memory addressing can be extended (capacity doubled) using the MEMEX signal which is decoded by the VL- 1262.

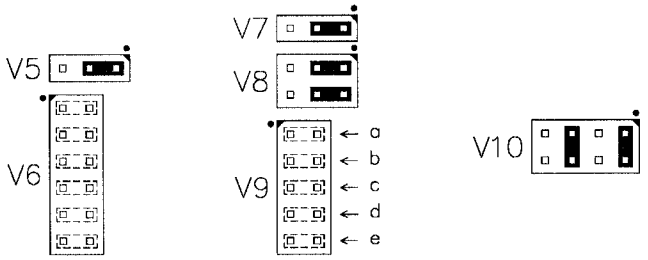
The VL-1262 occupies eight consecutive addresses in the map.

As shipped the board is configured for 16-bit memory addressing with a base address of hex FF00.

8-Bit I/O Addressing

To configure the board for an 8-bit I/O address refer to the figure below. Use the table to select the jumpering for the appropriate upper and lower halves of the desired address (i.e., "3" and "0" = hex address 30).

This jumper configuration ignores the state of the IOEXP signal in addressing the board. To use the IOEXP signal refer to the IOEXP section on page 2-8.



V9 a	V9 b	V9 c	V9 d	Upper Digit	V9 e	Lower Digit
X	X	X	X	0	X	0
X	X	X	–	1	–	8
X	X	–	X	2		
X	X	–	–	3		
X	–	X	X	4		
X	–	X	–	5		
X	–	–	X	6		
X	–	–	–	7		
–	X	X	X	8		
–	X	X	–	9		
–	X	–	X	A		
–	X	–	–	B		
–	–	X	X	C		
–	–	X	–	D		
–	–	–	X	E		
–	–	–	–	F		

X = Jumper installed
– = Jumper removed

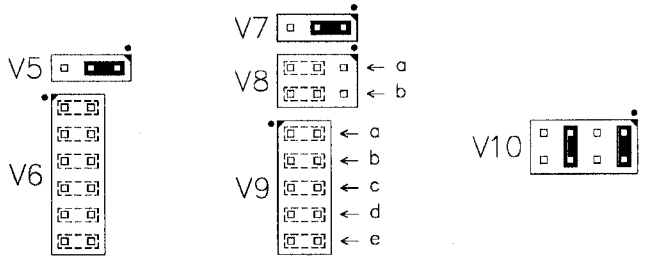
Jumper Block	Description	As Shipped
V9	Board Address (A3-A7)	FF00H
	a –A7	a In
	b –A6	b In
	c –A5	c In
	d –A4	d In
	e –A3	e In

Figure 2-3. 8-Bit I/O Address Jumpers

10-Bit I/O Addressing

To configure the board for a 10-bit I/O address refer to the figure below. Use the table to select the jumpering for the appropriate upper, middle, and lower hex digits of the desired address (i.e., "1" and "3" and "0" = hex address 130).

This jumper configuration ignores the state of the IOEXP signal in addressing the board. To use the IOEXP signal refer to the IOEXP Signal section on page 2-8.



—V8— a	b	Upper Digit	—— V9 —— a	b	c	d	Middle Digit	V9 e	Lower Digit
X	X	0	X	X	X	X	0	X	0
X	–	1	X	X	X	–	1	–	8
–	X	2	X	X	–	X	2		
–	–	3	X	X	–	–	3		
			X	–	X	X	4		
			X	–	X	–	5		
			X	–	–	X	6		
			X	–	–	–	7		
			–	X	X	X	8		
			–	X	X	–	9		
			–	X	–	X	A		
			–	X	–	–	B		
			–	–	X	X	C		
			–	–	X	–	D		
			–	–	–	X	E		
			–	–	–	–	F		

X = Jumper installed
– = Jumper removed

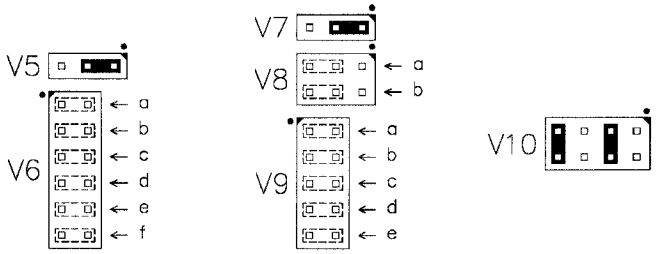
Jumper Block	Description	As Shipped
V8	Board Address (A8, A9) / 8-Bit mode selector	FF00H
	a – A9	a Out
	b – A8	b Out
V9	Board Address (A3-A7)	FF00H
	a – A7	a In
	b – A6	b In
	c – A5	c In
	d – A4	d In
	e – A3	e In

Figure 2-4. 10-Bit I/O Address Jumpers

16-Bit I/O Addressing

To configure the board for a 16-bit I/O address refer to the figure below. Use the table to select the jumpering for the appropriate four hex digits of the desired address (i.e., "6" and "1" and "3" and "0" = hex address 6130).

This jumper configuration ignores the state of the IOEXP signal in addressing the board. To use the IOEXP signal refer to the IOEXP Signal section page 2-8.



V6 a	V6 b	V6 c	V6 d	Top Digit	V6 e	V6 f	V8 a	V8 b	Second Digit	V9 a	V9 b	V9 c	V9 d	Third Digit	V9 e	Bottom Digit
X	X	X	X	0	X	X	X	X	0	X	X	X	X	0	X	0
X	X	X	–	1	X	X	X	–	1	X	X	X	–	1	–	8
X	X	–	X	2	X	X	–	X	2	X	X	–	X	2		
X	X	–	–	3	X	X	–	–	3	X	X	–	–	3		
X	–	X	X	4	X	–	X	X	4	X	–	X	X	4		
X	–	X	–	5	X	–	X	–	5	X	–	X	–	5		
X	–	–	X	6	X	–	–	X	6	X	–	–	X	6		
X	–	–	–	7	X	–	–	–	7	X	–	–	–	7		
–	X	X	X	8	–	X	X	X	8	–	X	X	X	8		
–	X	X	–	9	–	X	X	–	9	–	X	X	–	9		
–	X	–	X	A	–	X	–	X	A	–	X	–	X	A		
–	X	–	–	B	–	X	–	–	B	–	X	–	–	B		
–	–	X	X	C	–	–	X	X	C	–	–	X	X	C		
–	–	X	–	D	–	–	X	–	D	–	–	X	–	D		
–	–	–	X	E	–	–	–	X	E	–	–	–	X	E		
–	–	–	–	F	–	–	–	–	F	–	–	–	–	F		

X = Jumper installed
– = Jumper removed

Jumper Block	Description	As Shipped
V6	Board Address (A10 – A15)	FF00H
	a – A15	a Out
	b – A14	b Out
	c – A13	c Out
	d – A12	d Out
	e – A11	e Out
	f – A10	f Out
V8	Board Address (A8, A9) / 8-Bit mode selector	FF00H
	a – A9	a Out
	b – A8	b Out
V9	Board Address (A3-A7)	FF00H
	a – A7	a In
	b – A6	b In
	c – A5	c In
	d – A4	d In
	e – A3	e In

Figure 2-5. 16-Bit I/O Address Jumpers

IOEXP Signal

The IOEXP (I/O expansion) signal on the STD Bus is normally used to select between two different I/O banks or maps. It can also be used to double the number of available I/O addresses in the system (by selecting between two banks of I/O boards). The IOEXP signal is usually control led by (or jumpered to ground on) the system CPU card.

A low IOEXP signal usually selects the standard or normal I/O map. A high IOEXP signal usually selects the secondary or alternate I/O map. Boards that ignore (or do not decode) IOEXP will appear in both I/O maps.

As shipped the IOEXP jumper is configured to ignore the IOEXP signal. The board will be addressed whether the IOEXP signal is high or low. It can be jumpered for two other modes as shown below.

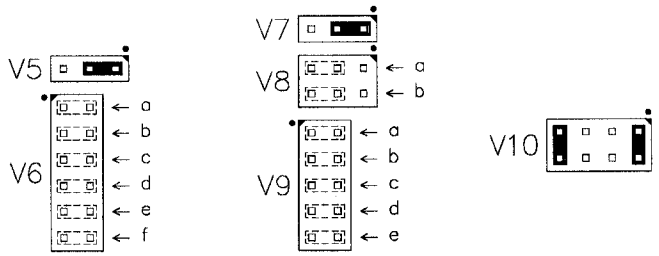
Jumper Block	Description	As Shipped
V7	IOEXP Select	Ignored
	a – Board responds to IOEXP high and low (IOEXP ignored)	
	b – Board responds to IOEXP low	
	None – Board responds to IOEXP high	

Figure 2-6. IOEXP Options

16-Bit Memory Addressing

To configure the board for a 16-bit memory address refer to the figure below. Use the table to select the jumpering for the appropriate four hex digits of the desired address (i.e., "6" and "1" and "3" and "0" = hex address 6130).

This jumper configuration ignores the state of the MEMEX signal in addressing the board. To use the MEMEX signal refer to the MEMEX Signal section on page 2-10.



V6 a	V6 b	V6 c	V6 d	Top Digit	V6 e	V6 f	V8 a	V8 b	Second Digit	V9 a	V9 b	V9 c	V9 d	Third Digit	V9 e	Bottom Digit
X	X	X	X	0	X	X	X	X	0	X	X	X	X	0	X	0
X	X	X	–	1	X	X	X	–	1	X	X	X	–	1	–	8
X	X	–	X	2	X	X	–	X	2	X	X	–	X	2		
X	X	–	–	3	X	X	–	–	3	X	X	–	–	3		
X	–	X	X	4	X	–	X	X	4	X	–	X	X	4		
X	–	X	–	5	X	–	X	–	5	X	–	X	–	5		
X	–	–	X	6	X	–	–	X	6	X	–	–	X	6		
X	–	–	–	7	X	–	–	–	7	X	–	–	–	7		
–	X	X	X	8	–	X	X	X	8	–	X	X	X	8		
–	X	X	–	9	–	X	X	–	9	–	X	X	–	9		
–	X	–	X	A	–	X	–	X	A	–	X	–	X	A		
–	X	–	–	B	–	X	–	–	B	–	X	–	–	B		
–	–	X	X	C	–	–	X	X	C	–	–	X	X	C		
–	–	X	–	D	–	–	X	–	D	–	–	X	–	D		
–	–	–	X	E	–	–	–	X	E	–	–	–	X	E		
–	–	–	–	F	–	–	–	–	F	–	–	–	–	F		

X = Jumper installed
– = Jumper removed

Jumper Block	Description	As Shipped
V6	Board Address (A10 – A15)	FF00H
	a – A15	a Out
	b – A14	b Out
	c – A13	c Out
	d – A12	d Out
	e – A11	e Out
	f – A10	f Out
V8	Board Address (A8, A9) / 8-Bit mode selector	FF00H
	a – A9	a Out
	b – A8	b Out
V9	Board Address (A3-A7)	FF00H
	a – A7	a In
	b – A6	b In
	c – A5	c In
	d – A4	d In
	e – A3	e In

Figure 2-7. 16-Bit Memory Address Jumpers

MEMEX Signal

The MEMEX (memory expansion) signal on the STD Bus is normally used to select between two different memory banks or maps. It can be used to double the number of available memory addresses in the system (by se lecting between the two memory banks). The MEMEX signal is usually controlled by (or jumpered to ground on) the system CPU card.

A low MEMEX signal usually selects the standard or normal memory map. A high MEMEX signal usually selects the secondary or alternate memory map. Boards that ignore (or do not decode) MEMEX will appear in both memory maps.

As shipped the MEMEX jumper is configured to ignore the MEMEX signal. The board will be addressed whether the MEMEX signal is high or low. It can be jumpered for two other modes as shown below.

Jumper Block	Description	As Shipped
V5	MEMEX Select	Ignored
	a – Board responds to MEMEX high and low (MEMEX ignored)	
	b – Board responds to MEMEX low	
	None – Board responds to MEMEX high	

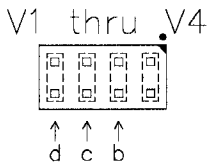
Figure 2-8. MEMEX Options

Analog Output Configuration

The VL-1262 has four output channels that can be independantly configured. The voltage range and voltage sense point are jumper selectable for each output channel. The output voltages are referenced to analog ground. Two channels can be converted to 4-20 mA operation with additional option kits.

Output Voltage Range

Each of the four output channels can be configured independently to produce an output voltage range of 0 to +5, 0 to +10, ±5, or ±10 volts as shown below.



Jumpers	Output Range
c	0 to +5V
d	0 to +10V
b&c	±5V
b&d	±10V

Jumper Block	Description	As Shipped
V1	Channel 0 output range	±10 volts
V2	Channel 1 output range	±10 volts
V3	Channel 2 output range	±10 volts
V4	Channel 3 output range	±10 volts

Figure 2-9. Output Range Options

Local/Remote Sense

When a load is driven over a long cable the resistance of the wire can cause a voltage drop to occur. This can result in erroneous signal levels at the remote end of the line. The VL-1262 board can compensate for this drop (up to 3 volts of loss) by measuring the voltage at the far end of the line thru a separate sense line.

Each channel can be jumpered for local sense (voltage measured at the card edge, no sense wire used), or remote sense (voltage measured at the destination, sense wire required). Typical local and remote sense connections are shown below.

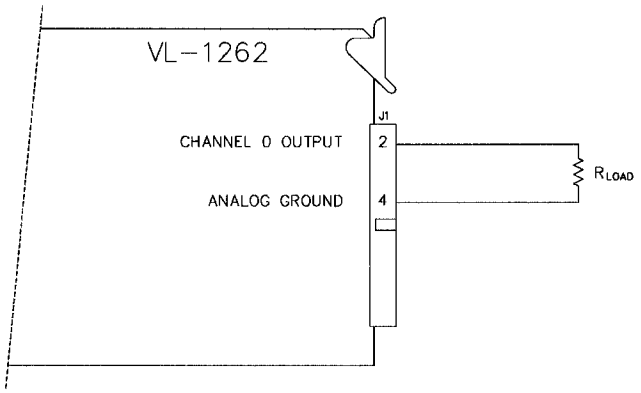


Figure 2-10. Standard (Local Sense) Output Connection

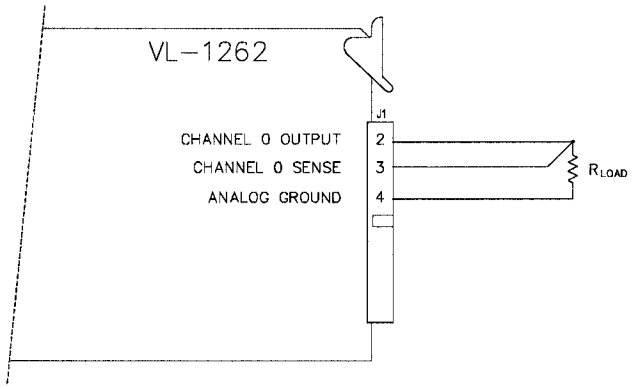
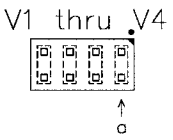


Figure 2-11. Remote Sense Connection



Channel	Jumper	Description	As Shipped
0	$V1_a$	IN – local sense, OUT – Remote sense	Local Sense
1	$V2_a$	IN – local sense, OUT – Remote sense	Local Sense
2	$V3_a$	IN – local sense, OUT – Remote sense	Local Sense
3	$V4_a$	IN – local sense, OUT – Remote sense	Local Sense

Figure 2-12. Remote Sense Jumpers

Current Loop Option

Channels 0 and 1 can optionally be configured to produce current loop output in the range of 4 to 20 mA. Normally this is a factory installed option. Contact VersaLogic for further information.

Note: When using the 4-20 mA option, the current loop channels must be configured for 0 to 10 volt output range.

An external loop power source between 15 and 30 volts must be provided to the Loop Power input on J1 as shown below for each channel that is configured for current loop operation. This power source must be capable of providing 25 mA of current.

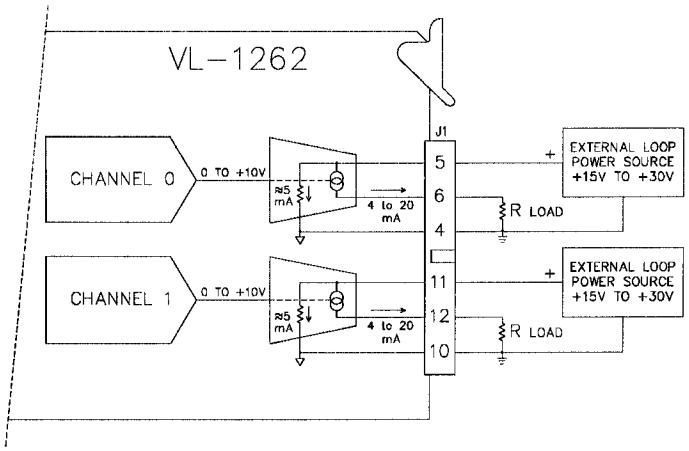


Figure 2-12. Current Loop Connection

Installation

Handling

** CAUTION ** The VL-1262 card uses chips which are sensitive to static electricity discharges. Normal precautions, such as discharging your self, work stations, and tools to ground before touching the board should be taken whenever the board is handled.

The board should also be protected during shipment or storage by placing it in a conductive bag (such as the one it was received in) or by wrapping it in metal foil.

Installation

The VL-1262 card can be installed in any slot of an STD Bus card cage, excluding Slot X in STD 32 cages, and should only be used with other standard (TTL level bus) STD Bus boards. When using CMOS STD Bus CPU boards use the VL-12CT62.

External Connections

J1 is an unlatched 26-pin dual-row (0.1" center) header type connector. External connections to the VL-1262 can be made with standard cable assemblies, or with the following mating connectors:

Mating Connectors

Connector	Mating Connector
J1	26-pin socket type connectors such as 3M #3399-6626

Figure 3-1. Mating Connectors

Physical Pin Locations

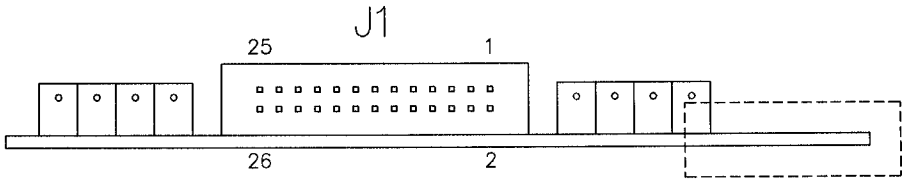
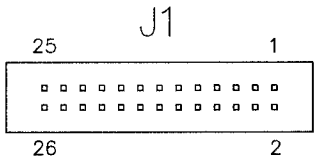


Figure 3-2. I/O Connector Physical Pin Locations

Connector Pinout



J1 Pin	Signal Name	J1 Pin	Signal Name
1	Analog Ground	14	Channel 2 Output
2	Channel 0 Output	15	Channel 2 Sense
3	Channel 0 Sense	16	Analog Ground
4	Analog Ground	17	N/C
5	Channel 0 Loop Power	18	N/C
6	Channel 0 Current Output	19	Analog Ground
7	Analog Ground	20	Channel 3 Output
8	Channel 1 Output	21	Channel 3 Sense
9	Channel 1 Sense	22	Analog Ground
10	Analog Ground	23	N/C
11	Channel 1 Loop Power	24	N/C
12	Channel 1 Current Output	25	Analog Ground
13	Analog Ground	26	Analog Ground

Figure 3-3. J1 Analog Output Connector Pinout

Channel 0–3 Output. These analog outputs are the voltage mode outputs from the A/D converters. Up to 5 mA can be drawn from each channel. The output range is set with jumpers V1 through V4.

Channel 0–3 Sense. These analog inputs are used to boost the Channel 0–3 outputs slightly to compensate for line loss over long cable runs. Their use is optional. See the Local/Remote Sense section on page 2-12 for further information.

Channel 0–1 Current Output. These analog outputs are the 4 to 20 mA current loop outputs from channels 0 and 1. For these outputs to work, the current loop option kit 9671 must be installed. Also, a loop power source must be provided for each channel.

Channel 0–1 Loop Power. These power supply inputs are used to power the current loop circuits for channels 0 and 1. An external power supply rated at 15 to 30 volts capable of supplying 25 mA must be connected to the Loop Power input of each channel configured for current loop operation. If desired, one power supply can be used for both channels, but it must be connected to both inputs. In this case, the supply would need to provide 50 mA.

Analog Ground. All voltage mode and current mode outputs are referenced to these pins. The use of multiple ground connections is recommended to maintain a high degree of signal integrity.

N/C — No Connection. These signals are not connected to on-board circuitry. They have no function.

Registers

This section includes information about registers, control and status bits, and data formats. It focuses primarily on the individual registers, the bits contained within them, and their functional descriptions.

Register Mapping

The VL-1262 occupies eight consecutive addresses in the I/O or memory map. The locations of the eight ports are determined by the board address, which is jumper selectable. For compatibility with Analog Devices RTI-1262 boards, VersaLogic ships the VL-1262 jumpered to memory address FF00H. However, most users configure the board using I/O mapping rather than memory mapping. For simplicity, this manual uses the as-shipped memory mapped addresses when referring to register locations. If you have reconfigured the card, you should substitute your own address for the FF0XH addresses indicated throughout this manual.

Output Port	Name	Port Address	As Shipped Address	Page
DAC3HI	Channel 3 D/A Data High Register	Board Address + 7	FF07H	4-3
DAC3LO	Channel 3 D/A Data Low Register	Board Address + 6	FF06H	4-2
DAC2HI	Channel 2 D/A Data High Register	Board Address + 5	FF05H	4-3
DAC2LO	Channel 2 D/A Data Low Register	Board Address + 4	FF04H	4-2
DAC1HI	Channel 1 D/A Data High Register	Board Address + 3	FF03H	4-3
DAC1LO	Channel 1 D/A Data Low Register	Board Address + 2	FF02H	4-2
DAC0HI	Channel 0 D/A Data High Register	Board Address + 1	FF01H	4-3
DAC0LO	Channel 0 D/A Data Low Register	Board Address + 0	FF00H	4-2

Figure 4-1. I/O Port Addresses

D/A Registers

D/A Data Low Register

Channel 0 (DAC0LO) — FF00H
Channel 1 (DAC1LO) — FF02H
Channel 2 (DAC2LO) — FF04H
Channel 3 (DAC3LO) — FF06H

7	6	5	4	3	2	1	0
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Figure 4-2. D/A Data Low Register

The DAC0LO and DAC1LO registers are write registers which receive the lower 8 bits of data used for D/A conversion. One register is assigned for each output channel. The registers are used in conjunction with the DAC0HI and DAC1HI registers to provide the complete 12-bit data word. These registers are set to zeros at power up or system reset.

The DACxLO register should be written to first, followed by the DACxHI register. A word-wide output instruction to the DACxLO register (out ax,dx) will write data to both registers in the proper sequence. This is true for both 8-bit and 16-bit modes as determined by jumper V9[1-2].

Data may be written to these registers as fast as desired, since the D/A conversion is virtually instantaneous.

D7-D0 — D/A Output Data (Least Significant Byte). The data written to these bits forms data bits D7 through D0 of the 12-bit digital value to be converted to an analog output voltage. See the D/A Data Representation section on page 4-4 for a discussion of data format.

D/A Data High Register

Channel 0 (DAC0HI) — FF01H
Channel 1 (DAC1HI) — FF03H
Channel 2 (DAC2HI) — FF05H
Chennel 3 (DAC3HI) — FF07H

7	6	5	4	3	2	1	0
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Figure 4-3. D/A Data High Register

The DAC0HI and DAC1HI registers are write registers which receive the upper 4 bits of data used for D/A conversion. One register is assigned for each output channel. The registers are used in conjunction with the DAC0LO and DAC1LO registers to provide the complete 12-bit data word. These registers are set to zeros at power up or system reset.

When writing data, the DACxLO register should be written to first, followed by the DACxHI register. The analog output value changes when DACxHI is updated. See the D/A Data Low Register section above for further information on register access.

D7-D4 — Not Used. These bits have no function on the VL-1262.

D3-D0 — D/A Output Data (Most Significant Nibble). The data written to these bits forms data bits D11 through D8 of the 12-bit digital value to be converted to an analog output voltage. See the D/A Data Representation section on page 4-4 for a discussion of data format.

Data Representation

The format of the data written to the Data Output registers depends on the output range and the output data format that is selected. Each of the data formats is discussed below.

Binary Format

Binary format is used only with the unipolar 0 to +5V or 0 to +10V output ranges. Binary format divides the full 5 or 10 Volt analog output range into 4096 steps. The code 000H produces an analog output of 0 Volts. The largest code (FFFH) produces a full scale analog output. All codes are considered positive.

The formulas for calculating analog or binary digital values are given by:

$$Digital = \left[\frac{Analog}{Step}\right] \qquad Analog = Step \times Digital$$

Where:

Analog = Output voltage

Digital = D/A Conversion Data

Step = 0.0024414 (0 to 10V Range)
0.0012207 (0 to 5V Range)

Output Range					
0–5V Output Voltage	**0–10V Output Voltage**	**4-20mA Output Current**	**Data (Hex)**	**Data (Dec)**	**Comment**
+4.9988	+9.9976	+19.9961	0FFF	4095	Maximum voltage
+2.5000	+5.0000	+12.0000	0800	2048	Half scale
+1.2500	+2.5000	+8.0000	0400	1024	Quarter scale
+0.00122	+0.00244	+4.00391	0001	1	1 LSB
0.0000	0.0000	+4.0000	0000	0	Zero

Figure 4-4. Binary Format

Offset Binary Format

Offset binary format is used with the bipolar ±5 or ±10V output ranges. It divides the full bipolar analog output range into 4096 steps. The code 000H produces a negative full scale output, and the largest code (FFFH) produces a positive full scale output.

The formulas for calculating analog or offset binary digital values are given by:

$$Digital = \left[\frac{Analog + Span}{Step} \right] \qquad Analog = Step \times (Digital - 1) - Span$$

Where:

Analog	=	Applied voltage	
Digital	=	D/A Conversion Data	
Span	=	9.9951172	(±10V Range)
		4.9975586	(±5V Range)
Step	=	0.0048828	(±10V Range)
		0.0024414	(±5V Range)

Sample values are shown in the table below:

Output Range				
±5V Output Voltage	±10V Output Voltage	Data (Hex)	Data (Dec)	Comment
+4.9976	+9.9951	0FFF	4095	Maximum positive voltage
+2.5000	+5.0000	0C00	3072	Positive half scale
+1.2500	+2.5000	0A00	2560	Positive quarter scale
+0.00244	+0.00488	0801	2049	Positive 1 LSB
0.0000	0.0000	0800	2048	Zero Volts
-0.00244	-0.00488	07FF	2047	Negative 1 LSB
-1.2500	-2.5000	0600	1536	Negative quarter scale
-2.5000	-5.0000	0400	1024	Negative half scale
-5.0000	-10.0000	0000	0	Maximum negative voltage

Figure 4-5. Offset Binary Format

Operation

This section includes general information about the use and operation of the VL-1262 card. Software examples written in 80x86 assembly language are included in the next section.

Analog Output

Changing one of the four analog outputs is simply done by writing 12-bits of data to the corresponding output ports. The order in which the two ports are written is important. First the DACxLO register is written to, then the DACxHI register is written to. If using 16-bit instructions in a high level language, make sure the DACxLO register is written to first.

Analog Output Steps

- Write LO data to DACxLO register.
- Write HI data to DACxHI register.

System Reset

When the STD Bus signal SYSRST* (active low) is applied to the card, the VL-1262 will clear all its buffer registers to zero. This will cause channels which are configured for 0–5V and 0–10V output to reset to zero volts. Channels which are configured for ±5V or ±10V will reset to -5V and -10V respectively. Those which are configured for current loop output will reset to 4 mA.

Software Example

This section shows a software example written in Intel assembly language, to assist you in constructing your own software routines.

Analog Output

The following example outputs 0 volts on channel 0. It is assumed that the board is addressed at I/O location 0050H.

```
                                                ;VL-1262 I/O PORT ADDRESSES
        = 0050   dac0lo  equ     0050h          ;Channel 0 Data Low Register
        = 0051   dac0hi  equ     0051h          ;Channel 0 Data High Register
        = 0052   dac1lo  equ     0052h          ;Channel 1 Data Low Register
        = 0053   dac1hi  equ     0053h          ;Channel 1 Data High Register
        = 0054   dac2lo  equ     0054h          ;Channel 2 Data Low Register
        = 0055   dac2hi  equ     0055h          ;Channel 2 Data High Register
        = 0056   dac3lo  equ     0056h          ;Channel 3 Data Low Register
        = 0057   dac3hi  equ     0057h          ;Channel 3 Data High Register

0000             write:                         ;OUTPUT ZERO VOLTS ON CHANNEL 0
0000  BA 0050            mov     dx,dac0lo      ;Select channel 0
0003  B8 0800            mov     ax,0800h       ;800h = Zero volts in offset binary
0006  EF                 out     dx,ax          ;Output data to D/A converter
                                                ;Data is written as follows:
                                                ;00h -> dac0lo
                                                ;08h -> dac0hi
```

Calibration

The VL-1262 is calibrated before shipment. However, it may be desirable to recalibrate the card after installation, and approximately once each year (depending on the accuracy requirements of the application).

The following equipment is required for calibration:

- A voltmeter with resolution and accuracy to ½ LSB of the output range being used (a milliammeter is required to calibrate channels which are configured for 4-20 mA operation).

The card should be calibrated as follows:

- Connect the voltmeter (or milliammeter) to the channel being calibrated.

  Note: If calibrating a channel which is configured for current loop operation, a 250 Ω, ¼ watt load resistor must be attached between the Current Output pin on J1 (of the channel being calibrated) and analog ground, in addition, a loop power source must be connected to the Loop Power input. Refer to the Current Loop Option section on page 2-13 for more information.

- Write the "zero" code to the channel being calibrated.
- Turn the zero adjustment pot (Z0-Channel 0, Z1-Channel 1, etc.) for a reading of 0.0000V (4.0000 mA) on the meter.
- Write the full scale code to the channel being calibrated.
- Turn the gain adjustment pot (G0-Channel 0, G1-Channel 1, etc.) until the meter shows the full scale value as shown in the table below (20.00 mA for current loop).

Output Range	"Zero" Data	"Full Scale" Data	Full Scale Reading
0 to 5V	0000	0FFF	4.9988V
0 to 10V	0000	0FFF	9.9976V
-5 to +5V	0800	0000	-5.0000V
-10 to +10V	0800	0000	-10.0000V
4 to 20 mA	0000	0FFF	19.9961 mA

Figure 7-1. Calibration Data

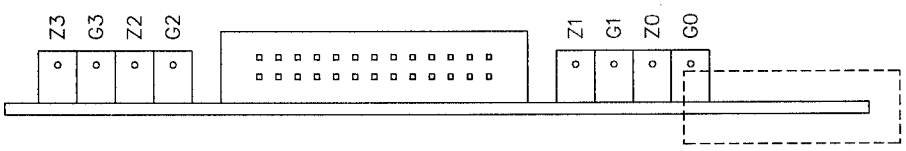


Figure 7-2. Calibration Pots

Reference

STD 80 Bus Pinout

COMPONENT SIDE				SOLDER SIDE			
Pin	**Signal**	**Flow**	**Description**	**Pin**	**Signal**	**Flow**	**Description**
P01	+5VDC	In	Logic Power	P02	+5VDC	In	Logic Power
P03	GND	In	Logic Ground	P04	GND	In	Logic Ground
P05	VBAT	—	Battery Power	P06	DCPDN*	—	DC Power Down
P07	A19/D3	I/O	Address/Data	P08	A23/D7	I/O	Address/Data
P09	A18/D2	I/O	Address/Data	P10	A22/D6	I/O	Address/Data
P11	A17/D1	I/O	Address/Data	P12	A21/D5	I/O	Address/Data
P13	A16/D0	I/O	Address/Data	P14	A20/D4	I/O	Address/Data
P15	A07	In	Address	P16	A15	In	Address
P17	A06	In	Address	P18	A14	In	Address
P19	A05	In	Address	P20	A13	In	Address
P21	A04	In	Address	P22	A12	In	Address
P23	A03	In	Address	P24	A11	In	Address
P25	A02	In	Address	P26	A10	In	Address
P27	A01	In	Address	P28	A09	In	Address
P29	A00	In	Address	P30	A08	In	Address
P31	WR*	In	Write Mem or I/O	P32	RD*	—	Read Mem or I/O
P33	IORQ*	In	I/O Address Select	P34	MEMRQ*	In	Memory Address Select
P35	IOEXP	In	I/O Expansion	P36	BHE* (MEMEX)	In	Byte High Enable (Mem Expansion)
P37	INTRQ1*	—	Interrupt Request 1	P38	ALE*	—	Address Latch Enable
P39	STATUS1*	—	CPU Status 1	P40	STATUS0*	—	CPU Status 0
P41	BUSAK*	—	Bus Acknowledge	P42	BUSRQ*	—	Bus Request
P43	INTAK*	—	Interrupt Acknowledge	P44	INTRQ*	—	Interrupt Request
P45	WAITRQ*	—	Wait Request	P46	NMIRQ*	—	Non-maskable Interrupt Request
P47	SYSRESET*	In	System Reset	P48	PBRESET*	—	Push-Button Reset
P49	CLOCK*	—	Clock	P50	CNTRL* (INTRQ2*)	—	Aux Timing
P51	PCO	Out	Priority Chain Out	P52	PCI	In	Priority Chain In
P53	AUX GND	In	AUX Ground	P54	AUX GND	In	AUX Ground
P55	AUX +V	In	AUX Positive (+12VDC)	P56	AUX -V	In	AUX Negative (-12VDC)

* Denotes an active low signal.
— Denotes signal not used on this board.

Figure 8-2. STD 80 Bus Pinout

VL-1262 Parts Placement

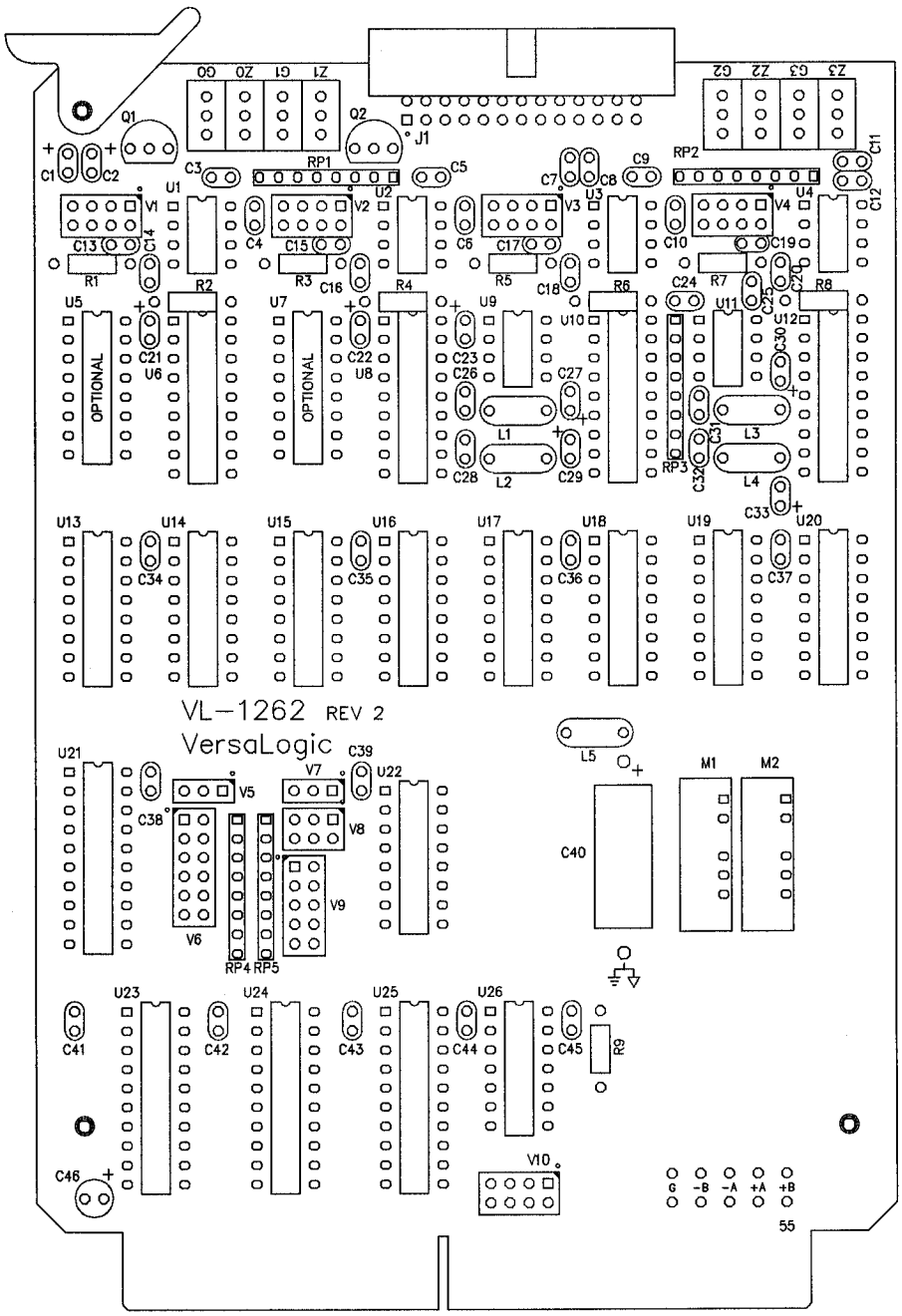
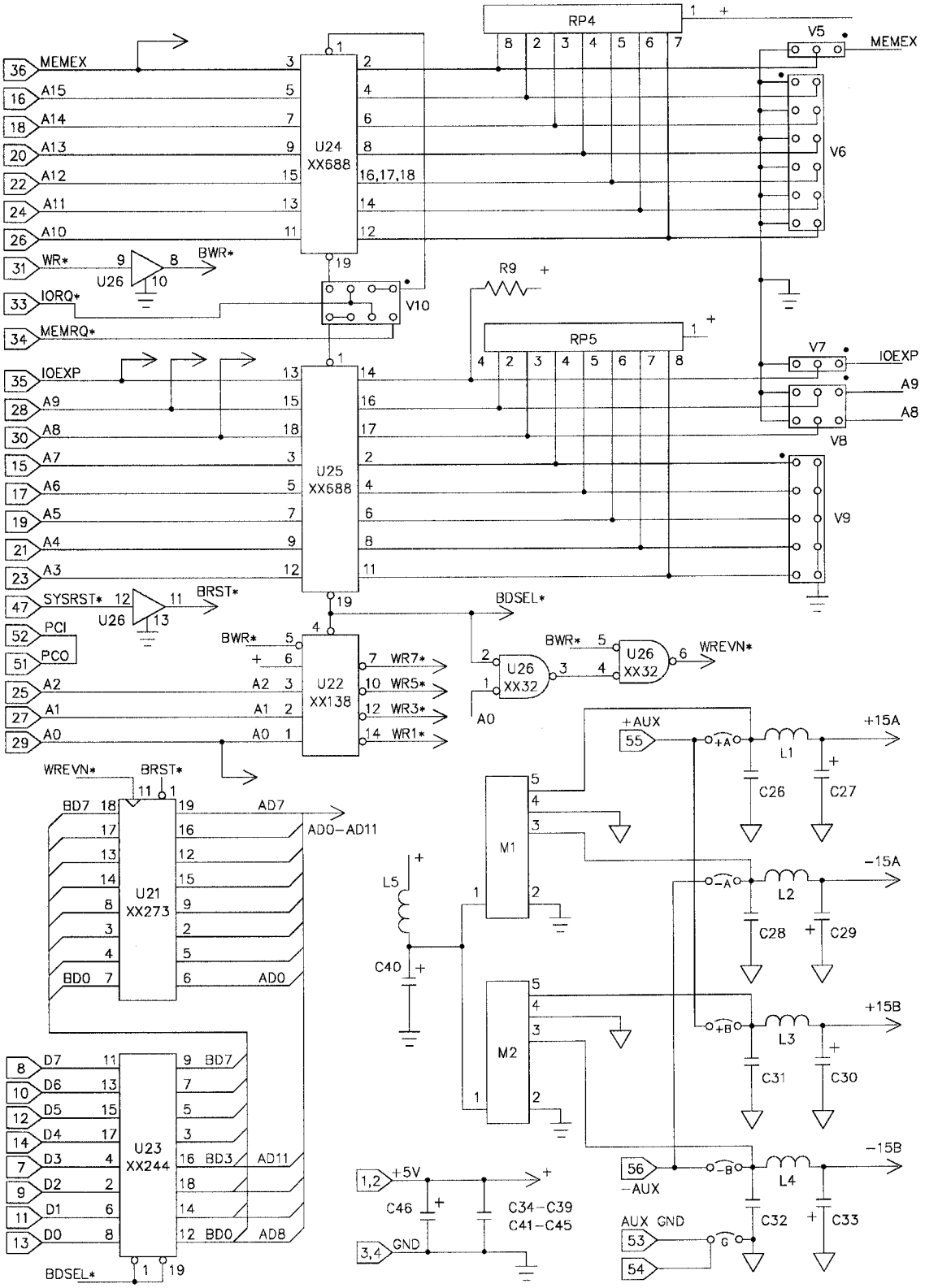


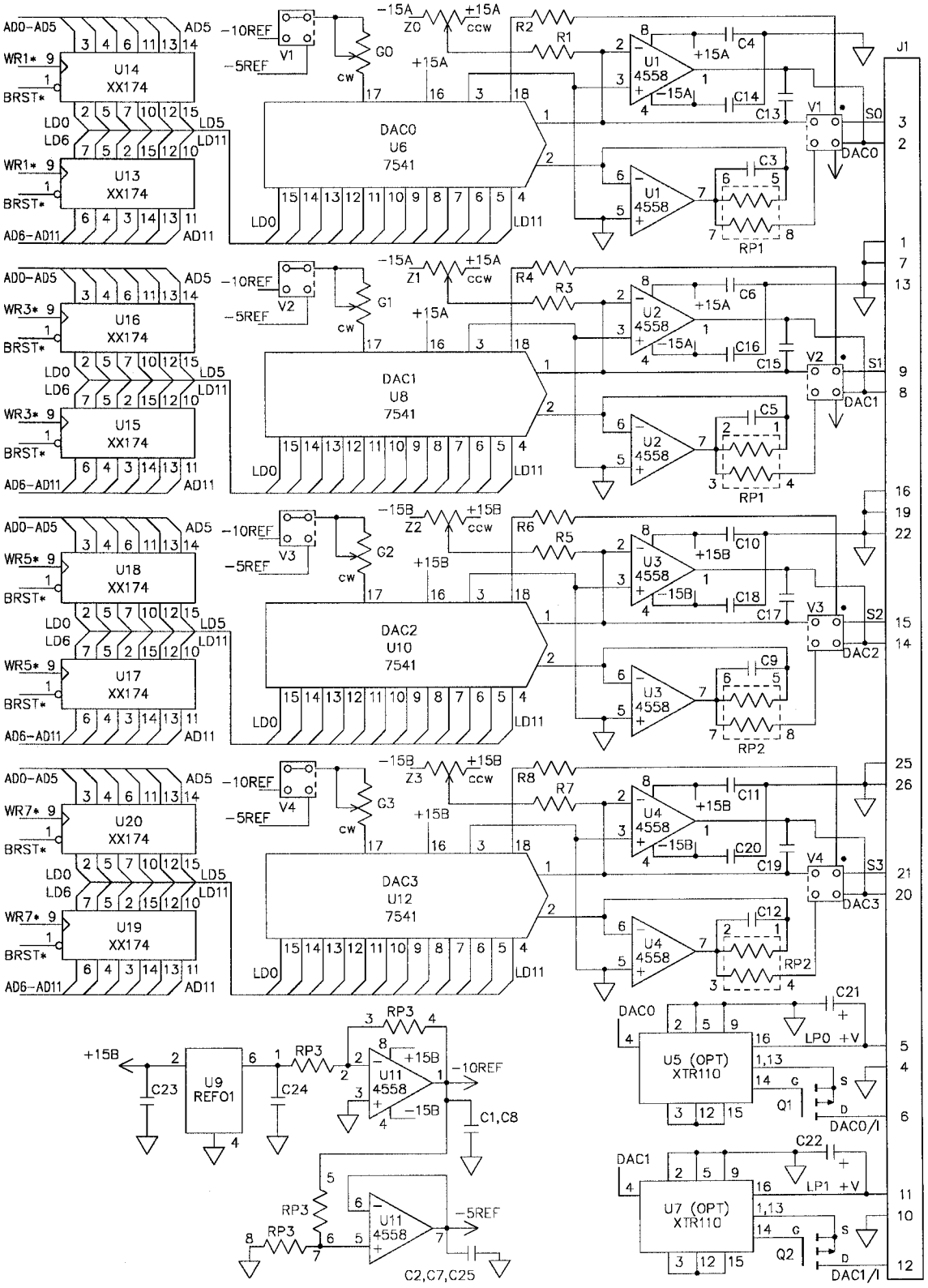
Figure 8-3. VL-1262 Parts Placement Diagram

VL-1262 Schematic



12/21/92 Rev2

VL-1262 Schematic



12/21/92 Rev2

VL-1262 Parts List

Rev. 2.00

Capacitors

C4, C6-C8, C10, C11, C14, C16, C18, C20 C23-C26, C28, C31, C32, C34-C39, C41-C45	.1 µf Z5U
C3, C5, C9, C12, C13, C15, C17, C19	39 pf, 10%, high Q
C21, C22	1 µf tantalum (optional)
C1, C2, C27, C29, C30, C33	1 µf tantalum
C40	220 µf 16V electrolytic
C46	22 µf 25V Elect. Cap. Radial

Inductors

L1-L5	10 µh, 250 ma Inductor

Integrated Circuits

M1, M2	HPR105
U1-U4, U11	4558
U5, U7	XTR110BG (optional)
U6, U8, U10, U12	7541A
U9	REF102AP
U13-U20	74LS174
U21	74LS273
U22	74LS138
U23	74LS244
U24, U25	74HCT688
U26	74LS32

Resistors

R1, R3, R5, R7	10M Ω, 1%, 1/4W
R2, R4, R6, R8	249 Ω, 1%, 1/4W
R9	4.7K Ω, 5%, 1/4W
G0-G3	500 Ω trim pot
Z0-Z3	100K Ω trim pot
RP1, RP2, RP3	10K Ω, 4 resistor SIP, 1%
RP4, RP5	10K Ω, 7 resistor SIP

Semiconductors

Q1, Q2	VP0300, FET (optional)

Miscellaneous

J1	26 pin R/A header

VL-12CT62 Parts List

Rev. 2.00

Capacitors

C4, C6-C8, C10, C11, C14, C16, C18, C20 C23-C26, C28, C31, C32, C34-C39, C41-C45	.1 µf Z5U
C3, C5, C9, C12, C13, C15, C17, C19	39 pf, 10%, high Q
C21, C22	1 µf tantalum (optional)
C1, C2, C27, C29, C30, C33	1 µf tantalum
C40	220 µf 16V electrolytic
C46	22 µf 25V electrolytic radial

Inductors

L1-L5	10 µh, 250 mA

Integrated Circuits

M1, M2	HPR105
U1-U4, U11	4558U/4558P
U5, U7	XTR110BG (optional)
U6, U8, U10, U12	DAC7541ABH
U9	REF102BP
U13-U20	74HC174
U21	74HCT273
U22	74HCT138
U23	74ACT244
U24, U25	74HCT688
U26	74HCT32

Resistors

R1, R3, R5, R7	10M Ω, 1%, 1/4W
R2, R4, R6, R8	249 Ω, 1%, 1/4W
R9	4.7K Ω, 5%, 1/4W
G0-G3	500 Ω trim pot
Z0-Z3	100K Ω trim pot
RP1,RP2,RP3	10K Ω, 4 resistor SIP, 1%
RP4,RP5	10K Ω, 7 resistor SIP

Semiconductors

Q1,Q2	VP0300, FET (optional)

Miscellaneous

J1	26 pin R/A header