# High-Speed CMOS Synchronous Presettable 4-Bit Binary Counters

**QS54/74FCT161T**
**QS54/74FCT163T**

**QS54/74FCT2161T**
**QS54/74FCT2163T**

## FEATURES/BENEFITS

- Pin and function compatible to the 74F161/3 74FCT 161/3 and 74FCT161T/3T
- CMOS power levels: <7.5 mW static
- Available in DIP, ZIP, SOIC, QSOP, LCC
- Undershoot clamp diodes on all inputs
- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883

**FCT-T 161T, 163T**

- JEDEC-FCT spec compatible
- Fastest CMOS logic family available
- Std through D speed grades with 5.0 ns tPD for D
- Iol = 48 mA Com., 32 mA Mil.

**FCT-T 2161T, 2163T**

- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- Std., A & C speed grades with 5.6 ns tPD for C
- Iol = 12mA Com.

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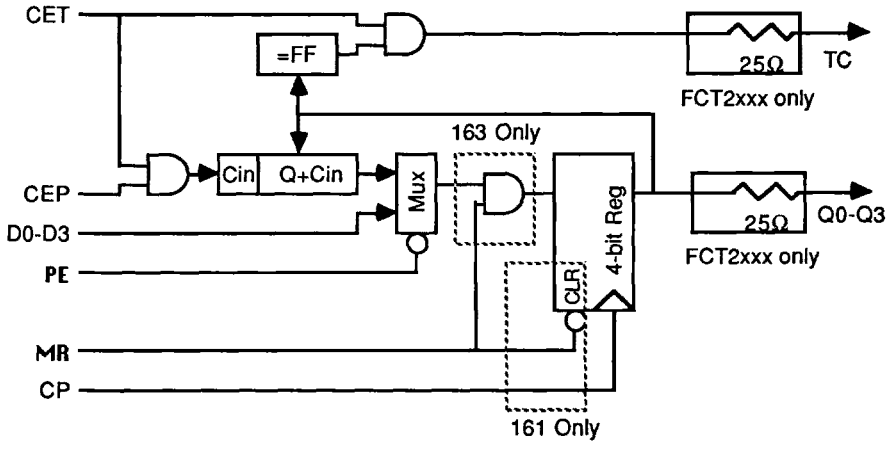
## DESCRIPTION

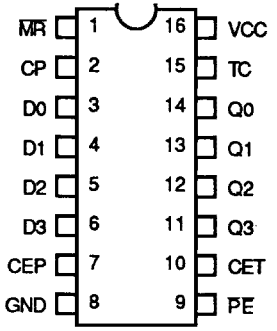
The QSFCT161T and QSFCT163T are high speed CMOS synchronous presettable 4-bit binary counters. The 161 has an asynchronous clear; the 163 has a clocked synchronous clear. The 2161 and 2163 are 25Ω resistor output versions of the 161 and 163, respectively, and are useful for driving transmission lines and reducing system noise. Data is preloaded or the counters count on the rising edge of the clock. Count enable inputs and terminal count outputs allow these counters to be cascaded without loss of speed. Preset inputs override count inputs, and clear inputs override both preset and count inputs. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001).

## FUNCTIONAL BLOCK DIAGRAM

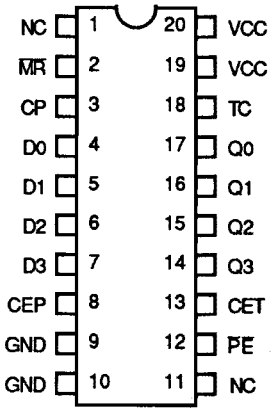


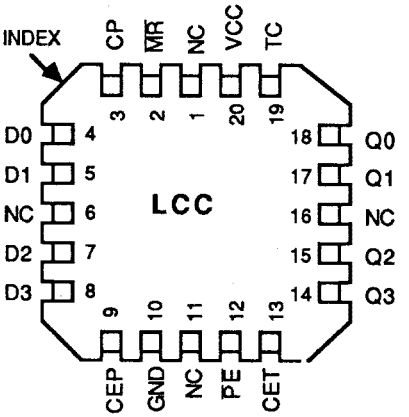
## PIN CONFIGURATIONS

### PDIP, SOIC, QSOP

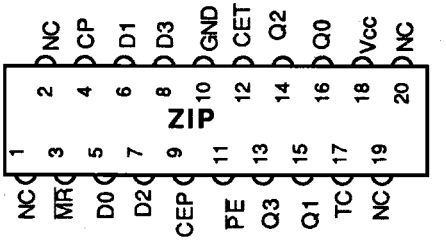



### HQSOP




### ALL PINS TOP




Note: Available in both 150 mil wide SOIC (package code S1) and 300 mil SOIC (package code SO).

## PIN DESCRIPTION

| Name | I/O | Description |
|---|---|---|
| D0-3 | I | Data Inputs |
| Q0-3 | O | Data Outputs |
| CP | I | Clock |
| $\overline{MR}$ | I | Master Reset |

| Name | I/O | Description |
|---|---|---|
| CEP | I | Count Enable |
| CET | I | Count and TC Enable |
| TC | O | Terminal Count |
| $\overline{PE}$ | I | Parallel Load Enable |

## FUNCTION TABLE

| Inputs | | | | | | Outputs | | | Function |
|---|---|---|---|---|---|---|---|---|---|
| $\overline{MR}$ | $\overline{PE}$ | CP | CEP | CET | Di | Q0-3 | | TC | |
| | | | | | | 161 | 163 | | |
| L | X | X | X | X | X | L | - | L | Clear 161 |
| L | X | ↑ | X | X | X | - | L | L | Clear 163 |
| H | L | ↑ | X | X | D0-3 | D0-3 | D0-3 | X | Load Data |
| H | H | ↑ | H | H | X | Q+1 | Q+1 | X | Count |
| H | H | ↑ | L | X | X | Q | Q | X | Count Inhibit P |
| H | H | ↑ | X | L | X | Q | Q | X | Count Inhibit T |
| H | H | X | X | H | X | F | F | H | Count = 1111 |
| H | H | X | X | H | X | 0-E | 0-E | L | Count ≠ 1111 |
| H | H | X | X | L | X | X | X | L | TC Inhibit |

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## ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground..... -0.5V to +7.0V
DC Output Voltage $V_O$ ..... -0.5V to 7.0V
DC Input Voltage $V_I$ ..... -0.5V to 7.0V
AC Input Voltage (for a pulse width ≤20 ns)..... -3.0V
DC Input Diode Current with $V_I$<0..... -20 mA
DC Output Diode Current with $V_O$ <0..... -50 mA
DC Output Current Max. sink current/pin..... 120 mA
Maximum Power Dissipation..... 0.5 watts
$T_{STG}$ Storage Temperature..... -65° to +165°C

## CAPACITANCE

TA = 25 °C, f = 1 MHz, Vin = 0V, Vout = 0 V

| Pins | SOIC | QSOP | PDIP,LCC | ZIP | Unit |
|---|---|---|---|---|---|
| 1-7,9,10 | 4 | 4 | 5 | 7 | pF |
| 11-15 | 6 | 6 | 7 | 9 | pF |
| ——— | 8 | 8 | 9 | 10 | pF |

Note: Capacitance is characterized but not tested

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial $T_A$=0°C to 70°C, $V_{CC}$=5.0V±5% Military $T_A$=-55°C to 125°C, $V_{CC}$=5.0V±10%

| Symbol | Parameter | Test Conditions | | Min | Typ (1) | Max | Unit |
|---|---|---|---|---|---|---|---|
| Vih | Input High Voltage | Logic HIGH for All Inputs | | 2.0 | - | - | Volts |
| Vil | Input LOW Voltage | Logic LOW for All Inputs | | - | - | 0.8 | |
| ΔVt | Input Hysterisis | Vth - Vthl for All Inputs | | - | 0.2 | - | |
| \| Iih \| \| Iil \| | Input Current Input HIGH or LOW | Vcc = MAX | 0 ≤ Vin < Vcc | - | - | 5 | µA |
| \| Ioz \| | Off State Output Current (Hi-Z) | Vcc = MAX, 0 ≤ Vin ≤ Vcc | | - | - | 5 | |
| Ios | Short Circuit Current FCTXXX | Vcc = MAX, Vo = GND (2,3) | | -60 | - | -225 | mA |
| Ior | Current Drive FCT2XXX | Vcc = Min, Vo =2.0V (3) | | 50 | - | - | mA |
| Vic | Input Clamp Voltage | Vcc = MIN, Iin = 18 mA (3) | | - | -0.7 | -1.2 | Volts |
| Voh | Output HIGH Voltage FCTXXX & FCT2XXX | Vcc = MIN | Ioh = 12 mA (MIL) | 2.4 | - | - | Volts |
| | | | Ioh = 15 mA (COM) | 2.4 | - | - | |
| Vol | Output LOW Voltage FCTXXX | Vcc = MIN | Iol = 32 mA (MIL) | - | - | 0.50 | |
| | | | Iol = 48 mA (COM) | - | - | 0.50 | |
| | Output LOW Voltage FCT2XXX (25Ω) | Vcc = MIN | Iol = 12 mA (MIL) | - | - | 0.50 | |
| | | | Iol = 12 mA (COM) | - | - | 0.50 | |
| Rout | Output Resistance FCT2XXX (25Ω) | Vcc = MIN | Iol = 12 mA (MIL) | - | 25 | - | Ω |
| | | | Iol = 12 mA (COM) | 20 | 28 | 40 | |

**Notes:**
1. Typical values indicate $V_{CC}$=5.0V and $T_A$=25°C.
2. Not more than one output should be shorted and the duration is ≤1 second.
3. These parameters are guaranteed by design but not tested.

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## POWER SUPPLY CHARACTERISTICS

| Symbol | Parameter | Test Conditions (1) | Min | Max | Unit |
|---|---|---|---|---|---|
| Icc | Quiescent Power Supply Current | Vcc = MAX, freq = 0<br>0V≤Vin≤0.2V or Vcc-0.2V≤Vin≤Vcc | - | 1.5 | mA |
| ΔIcc | Supply Current per Input @ TTL HIGH | Vcc = MAX, Vin =3.4 V, freq = 0 (2) | - | 2.0 | |
| Qccd | Supply Current per input per mHz | Vcc = MAX, Outputs open and enabled<br>One bit toggling @ 50% duty cycle<br>Other inputs at GND or Vcc (3,4) | - | 0.25 | mA/ MHz |

1. For conditions shown as MIN or MAX use the appropriate values specified under DC specifications.
2. Per TTL driven input (Vi=3.4V)
3. For flipflops Qccd is measured by switching one of the data in pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. Ic can be computed using the above parameters as explained in the Technical Overview section.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0° C to 70°C, Vcc = 5.0V±5%  Military TA = -55°C to 125° C, Vcc = 5.0V±10%
Cload = 50 pF, Rload = 500Ω unless otherwise noted

| Symbol | Description | | Notes (1) | 161 163 2161 2163 | | 161A 163A 2161A 2163A | | 161C 163C 2161C 2163C | | 161D 163D | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| t CPQ | Propagation Delay CP to Qi, 161/3 | COM | | 2 | 9.5 | 2 | 6.2 | 2 | 5.6 | 1.5 | 5.0 | ns |
| | | MIL | | 2 | 10 | 2 | 6.5 | 2 | 6.1 | | | |
| | Propagation Delay CP to Qi, 2161/3 | COM | | 2 | 9.5 | 2 | 6.2 | 2 | 5.6 | | | |
| | | MIL | | 2 | 10 | 2 | 6.5 | 2 | 6.1 | | | |
| t MRQ | Propagation Delay $\overline{MR}$ to Qi, 161 | COM | | 2 | 13 | 2 | 8.5 | 2 | 7.8 | 1.5 | 6.5 | |
| | | MIL | | 2 | 14 | 2 | 9.1 | 2 | 8.3 | | | |
| | Propagation Delay $\overline{MR}$ to Qi, 2161 | COM | | 2 | 14 | 2 | 9.1 | 2 | 7.8 | | | |
| | | MIL | | 2 | 13 | 2 | 8.5 | 2 | 8.3 | | | |
| t CPTC | Propagation Delay CP to TC | COM | | 2 | 15 | 2 | 9.8 | 2 | 8.8 | 1.5 | 7.5 | |
| | | MIL | | 2 | 16.5 | 2 | 10.8 | 2 | 9.8 | | | |
| t CETC | Propagation Delay CET to TC | COM | | 1.5 | 8.5 | 1.5 | 5.5 | 1.5 | 5.0 | 1.5 | 4.2 | |
| | | MIL | | 1.5 | 9 | 1.5 | 5.9 | 1.5 | 5.4 | | | |
| t MRTC | Propagation Delay MR to TC | COM | | 1.5 | 11.5 | 1.5 | 7.5 | 1.5 | 6.8 | 1.5 | 6.2 | |
| | | MIL | | 1.5 | 12.5 | 1.5 | 8.2 | 1.5 | 7.4 | | | |

Notes:
1) Minimums guaranteed but not tested.
2) This parameter is guaranteed by design but not tested.
3) See Test Circuit and Waveforms.

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Commercial TA = 0° C to 70°C, Vcc = 5.0V±5%  Military TA = -55°C to 125° C, Vcc = 5.0V±10%
Cload = 50 pF, Rload = 500Ω unless otherwise noted

| Symbol | Description | | Notes | 161 163 2161 2163 | | 161A 163A 2161A 2163A | | 161C 163C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | Min | Max | |
| t DS | Data Setup Time Di to CP | COM | | 5 | | 4 | | 3.5 | | ns |
| | | MIL | | 5.5 | | 4.5 | | 4.0 | | |
| t DH | Data Hold Time Di to CP | COM | | 1.5 | | 1.5 | | 1.5 | | |
| | | MIL | | 2 | | 2 | | 2 | | |
| t CS | Count Enab. Setup Time CEP, CET to CP | COM | | 11.5 | | 9.5 | | 8.5 | | |
| | | MIL | | 13 | | 11 | | 10 | | |
| t CH | Count Enable Hold Time CEP, CET to CP | COM | | 0 | | 0 | | 0 | | |
| | | MIL | | 0 | | 0 | | 0 | | |
| t MRS t PES | Control Setup Time $\overline{MR}$, $\overline{PE}$ to CP | COM | | 11.5 | | 9.5 | | 8.5 | | |
| | | MIL | | 13.5 | | 11.5 | | 10.5 | | |
| t MRH t PEH | Control Hold Time $\overline{MR}$, $\overline{PE}$ to CP | COM | | 1.5 | | 1.5 | | 1.5 | | |
| | | MIL | | 1.5 | | 1.5 | | 1.5 | | |
| t CPW | Clock Pulse Width HIGH or LOW | COM | 2 | 5 | | 4 | | 3 | | |
| | | MIL | 2 | 5 | | 4 | | 3 | | |
| t MRW | $\overline{MR}$ Reset Pulse Width 161, 2161 | COM | 2 | 5 | | 4 | | 3 | | |
| | | MIL | 2 | 5 | | 4 | | 3 | | |
| t MRW | Reset Recovery Time $\overline{MR}$ to CP, 161, 2161 | COM | 2 | 6 | | 5 | | 4 | | |
| | | MIL | 2 | 6 | | 5 | | 4 | | |

Notes:
1) Minimums guaranteed but not tested.
2) This parameter is guaranteed by design but not tested.
3) See Test Circuit and Waveforms.