



# High-Speed, Current Feedback Operational Amplifier

## OP-160

### FEATURES

- Easy To Use – Drives Large Capacitive Loads
- Very High Slew Rate ( $A_V = +1$ ) ..... 1300 V/ $\mu$ s Typ
- Bandwidth ( $A_V = +1$ ) ..... 90MHz Typ
- Low Supply Current ..... 6.5mA Typ
- Bandwidth Independent of Gain
- Unity-Gain Stable
- Power Shutdown Pin

### APPLICATIONS

- High-Speed Data Acquisition
- Communication Systems/RF Amplifiers
- Video Gain Block
- High-Speed Integrators
- Driving High-Speed ADCs

### ORDERING INFORMATION

$T_A = +25^\circ\text{C}$ $V_{OS}$ MAX (mV)	PACKAGE			OPERATING TEMPERATURE RANGE
	CERDIP 8-PIN	PLASTIC 8-PIN	LCC 20-CONTACT	
5.0	OP160AZ*	—	OP160ARC/883	MIL
5.0	OP160FZ	OP160GP	—	XIND
5.0	—	OP160GS <sup>††</sup>	—	XIND

\* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

<sup>†</sup> Burn-in is available on extended industrial temperature range parts in CerDIP and plastic packages.

<sup>††</sup> For availability and burn-in information on SO package, contact your local sales office.

### GENERAL DESCRIPTION

The OP-160 is an easy-to-use high-speed, current feedback op amp. Designed to handle large capacitive loads, the OP-160 resists unstable operation. The OP-160 combines PMI's high-speed complementary bipolar process with a current feedback

topology for very high slew rate and wide bandwidth performance.

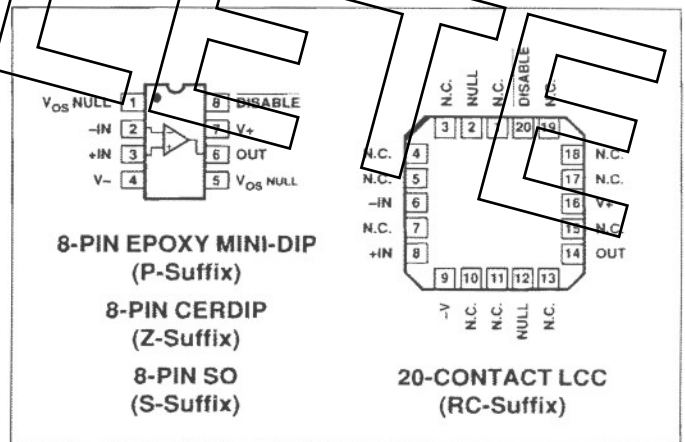
Slew rate of the OP-160 is typically 1300V/ $\mu$ s and is guaranteed to exceed 1000V/ $\mu$ s. In addition, the OP-160's current feedback design has the added advantage of nearly constant bandwidth versus gain. In a gain of +1 the -3dB bandwidth is 90MHz! The OP-160 also requires only 6.5mA of supply current, a considerable power savings over other high-speed amplifiers.

Applications using the OP-160 can be implemented with the same circuit assumptions utilized for conventional voltage feedback op amps. With its high speed and bandwidth, the OP-160 is ideal for a variety of applications including video amplifiers, RF amplifiers, and high-speed data acquisition systems.

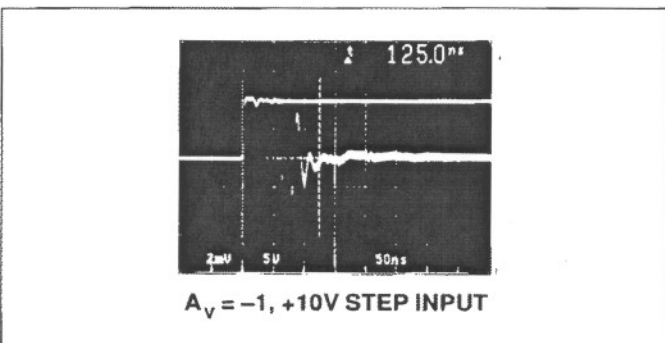
The OP-160 is an easy-to-use alternative to the AD844, AD846, EL2020 and EL2030.

For applications requiring a high-speed, wide bandwidth dual amplifier, see the OP-260.

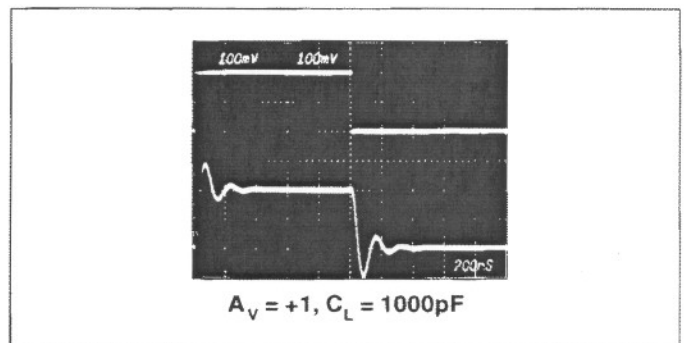
### PIN CONNECTIONS



### FAST SETTLING (0.01%)



### DRIVES CAPACITIVE LOADS



# OP-160

## ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage .....	±18V
Input Voltage .....	Supply Voltage
Differential Input Voltage .....	±1V
Inverting Input Current .....	±7mA Continuous
.....	±20mA Peak
Output Short-Circuit Duration .....	10 sec
Operating Temperature Range	
OP-160A (Z, RC) .....	-55°C to +125°C
OP-160A,F (Z) .....	-40°C to +85°C
OP-160G (P,S) .....	-40°C to +85°C
Storage Temperature (Z, RC) .....	-65°C to +175°C
(P, S) .....	-65°C to +150°C
Junction Temperature (Z, RC) .....	-65°C to +175°C
(P, S) .....	-65°C to +150°C
Lead Temperature (Soldering, 10 sec) .....	+300°C

PACKAGE TYPE	$\theta_{JA}$ (Note 2)	$\theta_{JC}$	UNITS
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
20-Contact LCC (RC)	98	38	°C/W
8-Pin SO (S)	158	43	°C/W

### NOTES:

1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2.  $\theta_{JA}$  is specified for worst case mounting conditions, i.e.,  $\theta_{JA}$  is specified for device in socket for CerDIP, P-DIP, and LCC packages;  $\theta_{JA}$  is specified for device soldered to printed circuit board for SO package.

## ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$ , $V_{CM} = 0V$ , $R_F = 820\Omega$ , $T_A = +25^\circ C$ , unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-160A/F			OP-160G			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX		
Input Offset Voltage	$V_{IOS}$		-	2	5	-	2	5	mV	
Input Bias Current	$I_{B+}$	Noninverting Input	-	0.2	1	-	0.4	1.5	$\mu A$	
	$I_{B-}$	Inverting Input	-	6	20	-	10	30		
Input Bias Current Common-Mode Rejection Ratio	$CMRR _{B+}$	$V_{CM} = \pm 11V$ Noninverting Input	-	40	75	-	50	125	nA/V	
	$CMRR _{B-}$	Inverting Input	-	30	75	-	40	125		
Input Bias Current Power Supply Rejection Ratio	$PSRR _{B+}$	$V_S = \pm 9V$ to $\pm 18V$ Noninverting Input	-	1	5	-	1.5	10	nA/V	
	$PSRR _{B-}$	Inverting Input	-	20	50	-	25	75		
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	60	65	-	60	65	-	dB	
Power Supply Rejection	PSR	$V_S = \pm 9V$ to $\pm 18V$	74	80	-	74	80	-	dB	
Open-Loop Transimpedance	$R_T$	$R_L = 500\Omega$ $V_O = \pm 10V$	3	4	-	3	4	-	$M\Omega$	
Input Voltage Range	IVR	(Note 1)	±11	-	-	±11	-	-	V	
Output Voltage Swing	$V_O$	$R_L = 500\Omega$	±11	-	-	±11	-	-	V	
Output Current	$I_O$	$V_O = \pm 10V$	±35	+60/-45	-	±35	+60/-45	-	mA	
Supply Current	$I_{SV}$	No Load	-	6.5	8	-	6.5	8	mA	
Slew Rate	SR	$A_V = +1$ , $V_O = \pm 10V$ , $R_L = 500\Omega$ , Test at $V_O = \pm 5V$	All Grades	-	1300	-	-	1300	-	V/ $\mu s$
		$A_V = +2$ , $V_O = \pm 10V$ , $R_L = 500\Omega$ , Test at $V_O = \pm 5V$	OP-160A	1000	1300	-	-	-	-	
		OP-160F	800	1300	-	-	-	-		
			OP-160G	-	-	-	800	1300	-	

**OP-160**

**ELECTRICAL CHARACTERISTICS** at  $V_S = \pm 15V$ ,  $V_{CM} = 0V$ ,  $R_F = 820\Omega$ ,  $T_A = +25^\circ C$ , unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	OP-160A/F			OP-160G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Rise Time	$t_R$	$A_V = +1$ $A_V = -1$ $V_O = \pm 100mV$	-	4 6.4	-	-	4 6.4	-	ns
-3dB Bandwidth	BW	-3dB Point $R_L = 500\Omega$ $A_V = -1$ $A_V = +1$ $A_V = +2$	-	55 90 65	-	-	55 90 65	-	MHz
Settling Time	$t_s$	$A_V = -1$ , 10V Step 0.01% 0.1%	-	125 75	-	-	125 75	-	ns
Input Capacitance	$C_{IN}$	Noninverting Input	-	4	-	-	4	-	pF
Input Resistance	$R_{IN}$	Noninverting Input Inverting Input	-	17 60	-	-	10 60	-	M $\Omega$ $\Omega$
Voltage Noise Density	$e_n$	$f = 1kHz$	-	5.5	-	-	5.5	-	nV/ $\sqrt{Hz}$
Current Noise Density	$i_n$	$f = 1kHz$ Noninverting Input Inverting Input	-	5 20	-	-	5 20	-	pA/ $\sqrt{Hz}$
Total Harmonic Distortion	THD	$f = 1kHz$ , $A_V = +1$ $V_O = 2V_{RMS}$ , $R_L = 500\Omega$	-	0.004	-	-	0.004	-	%
Differential Gain		$f = 3.58MHz$ $A_V = +1$ , $R_L = 500\Omega$	-	0.04	-	-	0.04	-	%
Differential Phase		$f = 3.58MHz$ $A_V = +1$ , $R_L = 500\Omega$	-	0.04	-	-	0.04	-	degrees
Disable Supply Current	$I_{SV DIS}$	DISABLE = 0V No Load	-	2.3	-	-	2.3	-	nA

**NOTE:**

1. Guaranteed by CMR test.

# OP-160

**ELECTRICAL CHARACTERISTICS** at  $V_S = \pm 15V$ ,  $V_{CM} = 0V$ ,  $R_F = 820\Omega$ ,  $-55^\circ C \leq T_A \leq +125^\circ C$ , for the OP-160A, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-160A			UNITS
			MIN	TYP	MAX	
Input Offset Voltage	$V_{IOS}$		-	3	8	mV
Average Input Offset Voltage Drift	$TC_{VOS}$		-	10	-	$\mu V/^\circ C$
Input Bias Current	$I_{B+}$	Noninverting Input	-	0.35	2	$\mu A$
	$I_{B-}$	Inverting Input	-	12	30	
Input Bias Current Common-Mode Rejection	$CMRRI_{B+}$	$V_{CM} = \pm 10V$ Noninverting Input	-	55	150	nA/V
	$CMRRI_{B-}$	Inverting Input	-	45	150	
Input Bias Current Power Supply Rejection Ratio	$PSRRI_{B+}$	$V_S = \pm 9V$ to $\pm 18V$ Noninverting Input	-	2	10	nA/V
	$PSRRI_{B-}$	Inverting Input	-	40	100	
Common Mode Rejection	CMR	$V_{CM} = \pm 10V$	56	60	-	dB
Power Supply Rejection	PSR	$V_S = \pm 9V$ to $\pm 18V$	70	76	-	dB
Open Loop Transimpedance	$R_T$	$R_F = 500\Omega$ $V_O = \pm 10V$	1.75	3	-	$M\Omega$
Input Voltage Range	I <sub>VR</sub>	(Note 1)	$\pm 10$	-	-	V
Output Voltage Swing	$V_O$	$R_L = 500\Omega$	$\pm 10$	-	-	V
Supply Current	$I_{SY}$	No Load	-	6.75	9	mA

**NOTE:**

1. Guaranteed by CMR test.

**OP-160**

**ELECTRICAL CHARACTERISTICS** at  $V_S = \pm 15V$ ,  $V_{CM} = 0V$ ,  $R_F = 820\Omega$ ,  $-40^\circ C \leq T_A \leq +85^\circ C$ , for the OP-160F/G, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-160F			OP-160G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$V_{IOS}$		-	2.75	8	-	2.75	8	mV
Average Input Offset Voltage	$TCV_{OS}$		-	10	-	-	10	-	$\mu V/^\circ C$
Input Bias Current	$I_{B+}$	Noninverting Input	-	0.3	2	-	0.5	3	$\mu A$
	$I_{B-}$	Inverting Input	-	10	30	-	15	40	
Input Bias Current Common-Mode Rejection Ratio	$CMRR I_{B+}$	$V_{CM} = \pm 10V$ Noninverting Input	-	45	150	-	55	250	nA/V
	$CMRR I_{B-}$	Inverting Input	-	35	150	-	45	250	
Input Bias Current Power Supply Rejection Ratio	$PSRR I_{B+}$	$V_S = \pm 9V$ to $\pm 18V$ Noninverting Input	-	1.5	10	-	2.5	20	nA/V
	$PSRR I_{B-}$	Inverting Input	-	30	100	-	3.5	150	
Common-Mode Rejection	CMR	$V_{CM} = \pm 10V$	56	62	-	56	62	-	dB
Power Supply Rejection	PSR	$V_S = \pm 9V$ to $\pm 18V$	70	80	-	70	80	-	dB
Open-Loop Transimpedance	$Z_T$	$R_L = 300\Omega$ $V_O = \pm 10V$	1.75	3	-	1.75	3	-	$M\Omega$
Input Voltage Range	IVR	(Note 1)	$\pm 10$	-	-	$\pm 10$	-	-	V
Output Voltage Swing	$V_O$	$R_L = 500\Omega$	$\pm 10$	-	-	$\pm 10$	-	-	V
Supply Current	$I_{SY}$	No Load, Both Amplifiers	-	6.75	9	-	6.75	9	mA

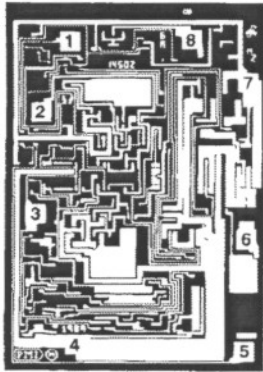
**NOTE:**

1. Guaranteed by CMR test.

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# OP-160

## DICE CHARACTERISTICS



- 1.  $V_{OS}$  NULL
- 2. -IN
- 3. +IN
- 4.  $V_-$
- 5.  $V_{OS}$  NULL
- 6. OUT
- 7.  $V_+$
- 8. DISABLE

DIE SIZE 0.071 x 0.099 inch, 7,029 sq. mils  
(1.80 x 2.52 mm, 4.54 sq. mm)

WAFER TEST LIMITS at  $V_S = \pm 15V$ ,  $V_{CM} = 0V$ ,  $R_C = 820\Omega$ ,  $T_A = +25^\circ C$ , unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-160GBC LIMITS	UNITS
Input Offset Voltage	$V_{IOS}$		5	mV MAX
Input Bias Current	$I_{B+}$	Noninverting Input	15	$\mu A$ MAX
	$I_{B-}$	Inverting Input	30	
Input Bias Current Common-Mode Rejection Ratio	$CMRRI_{B+}$	$V_{CM} = \pm 11V$ Noninverting Input	125	nA/V MAX
	$CMRRI_{B-}$	Inverting Input	125	
Input Bias Current Power Supply Rejection Ratio	$PSRRI_{B+}$	$V_S = \pm 9V$ to $\pm 18V$ Noninverting Input	10	nA/V MAX
	$PSRRI_{B-}$	Inverting Input	75	
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	60	dB MIN
Power Supply Rejection	PSR	$V_S = \pm 9V$ to $\pm 18V$	74	dB MIN
Open-Loop Transimpedance	$R_T$	$R_L = 500\Omega$ $V_O = \pm 10V$	3	$M\Omega$ MIN
Input Voltage Range	IVR		$\pm 11$	V MIN
Output Voltage Swing	$V_O$	$R_L = 500\Omega$	$\pm 11$	V MIN
Supply Current	$I_{SY}$	No Load	8	mA MAX

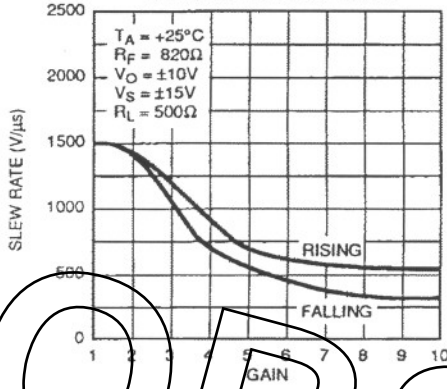
**NOTES:**

1. Guaranteed by CMR test.

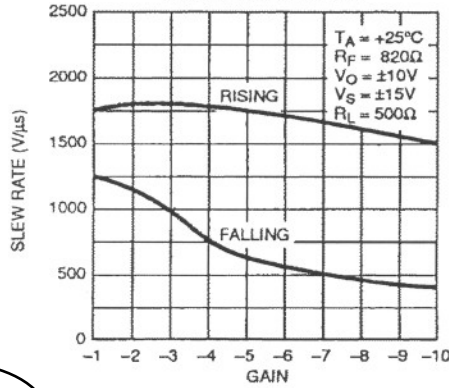
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

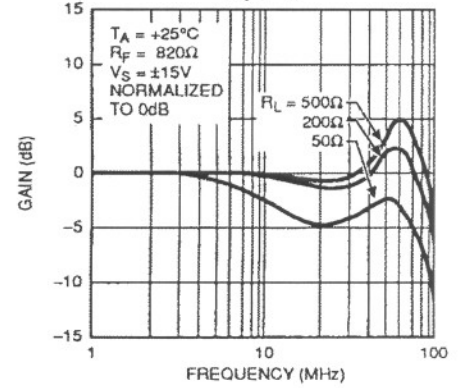
SLEW RATE vs NONINVERTING GAIN



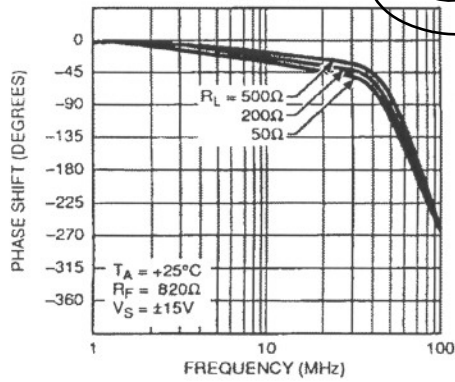
SLEW RATE vs INVERTING GAIN



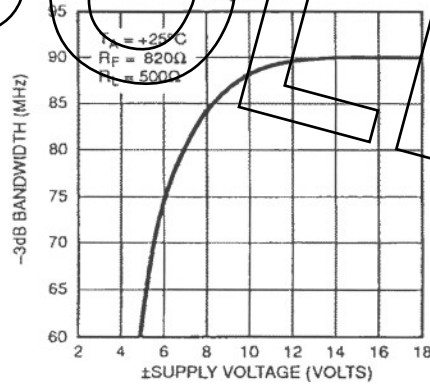
GAIN vs FREQUENCY AV = +1



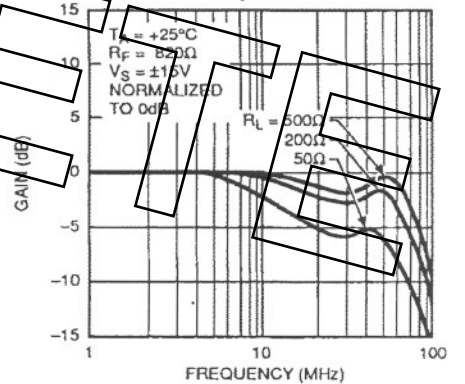
PHASE SHIFT vs FREQUENCY AV = +1



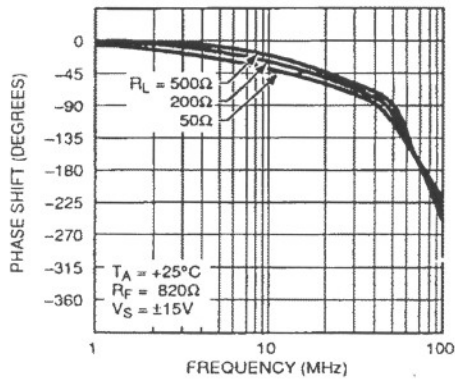
-3dB BANDWIDTH vs SUPPLY VOLTAGE AV = +1



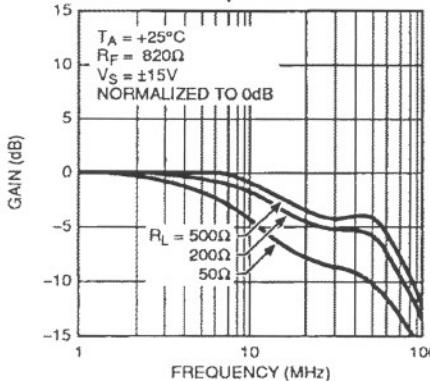
GAIN vs FREQUENCY AV = +2



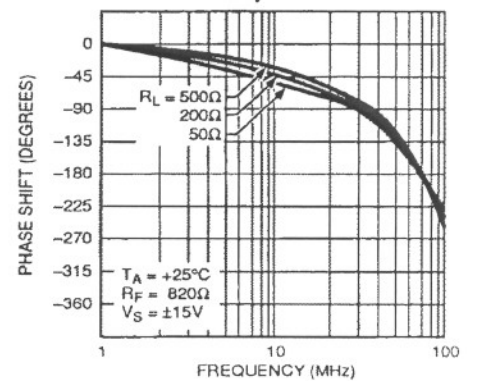
PHASE SHIFT vs FREQUENCY AV = +2



GAIN vs FREQUENCY AV = +5



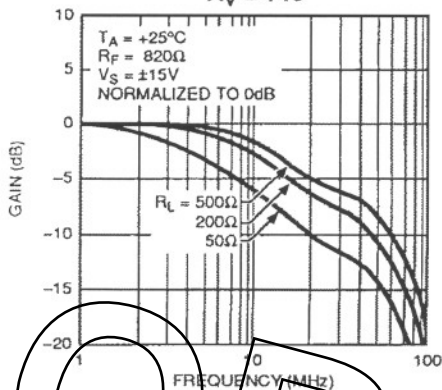
PHASE SHIFT vs FREQUENCY AV = +5



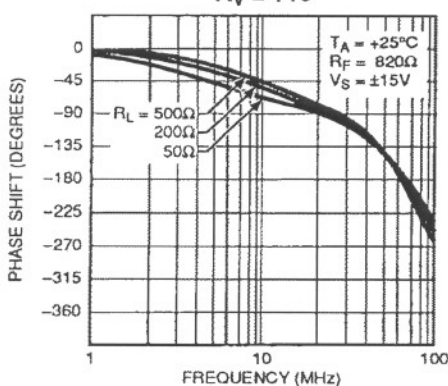
# OP-160

## TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

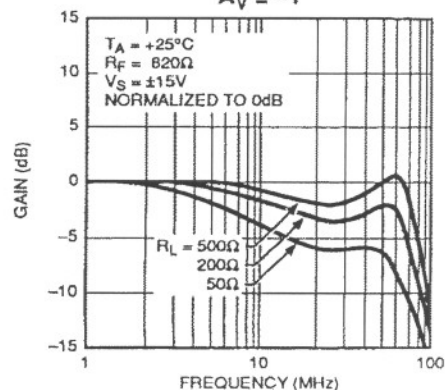
**GAIN vs FREQUENCY**  
 $A_V = +10$



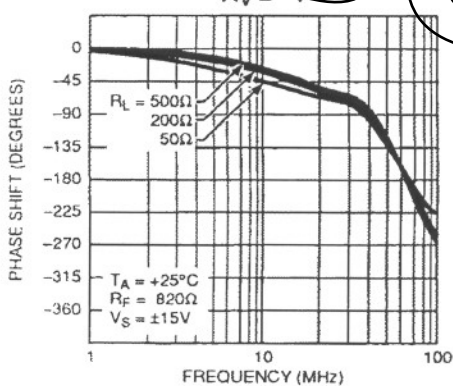
**PHASE SHIFT vs FREQUENCY**  
 $A_V = +10$



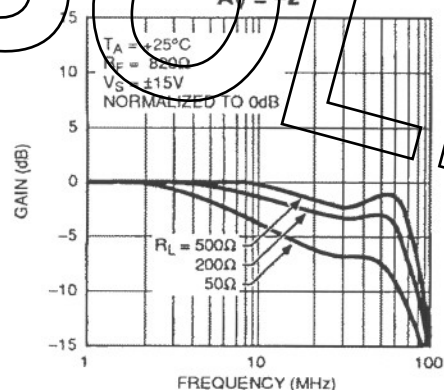
**GAIN vs FREQUENCY**  
 $A_V = -1$



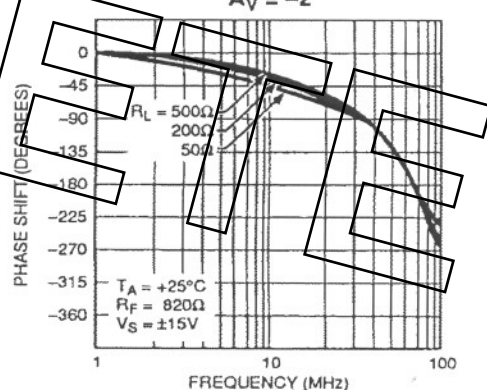
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 $A_V = -1$



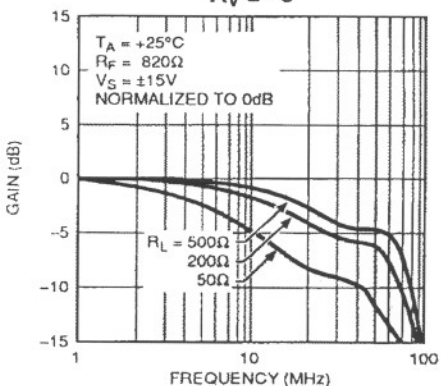
**GAIN vs FREQUENCY**  
 $A_V = -2$



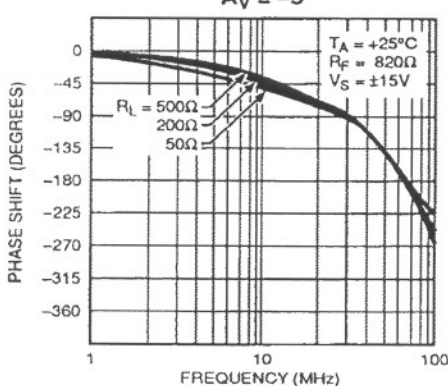
**PHASE SHIFT vs FREQUENCY**  
 $A_V = -2$



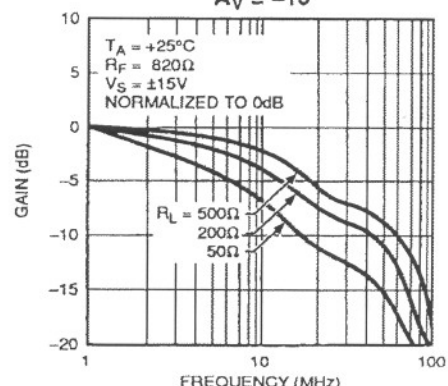
**GAIN vs FREQUENCY**  
 $A_V = -5$



**PHASE SHIFT vs FREQUENCY**  
 $A_V = -5$



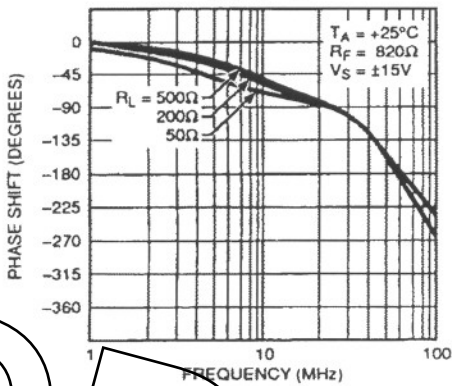
**GAIN vs FREQUENCY**  
 $A_V = -10$



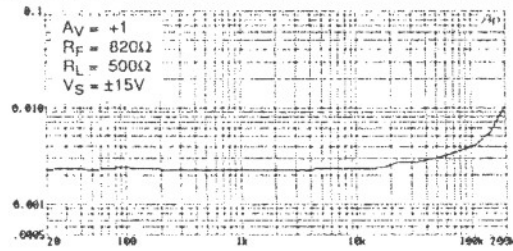


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

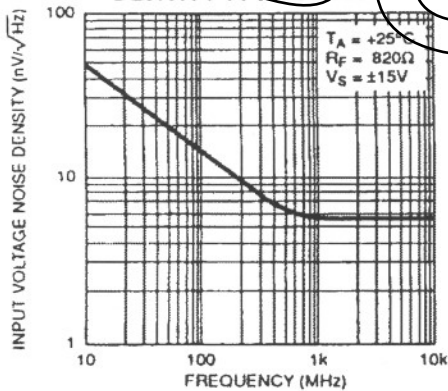
**PHASE SHIFT vs FREQUENCY**  
 $A_V = -10$



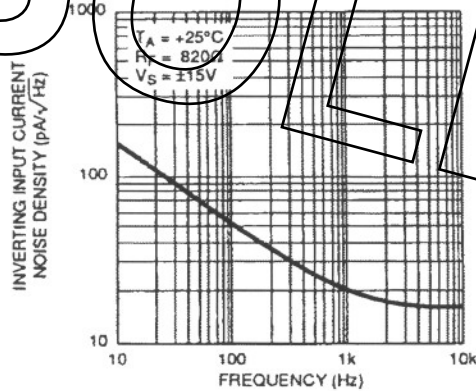
**TOTAL HARMONIC DISTORTION vs FREQUENCY**



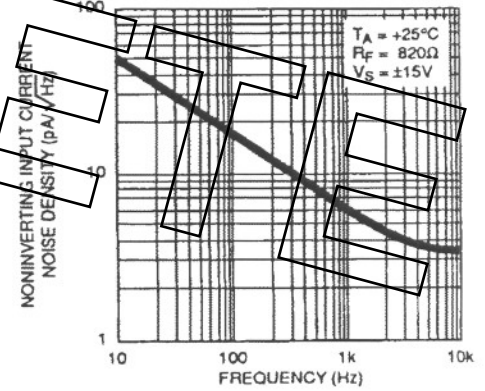
**INPUT VOLTAGE NOISE DENSITY vs FREQUENCY**



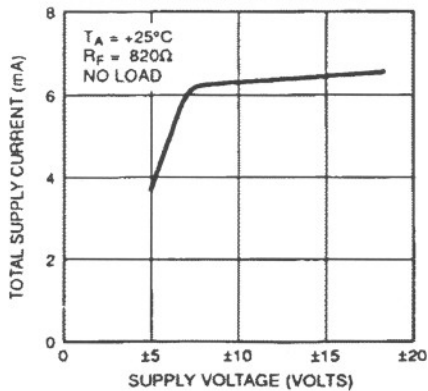
**INVERTING INPUT CURRENT NOISE DENSITY vs FREQUENCY**



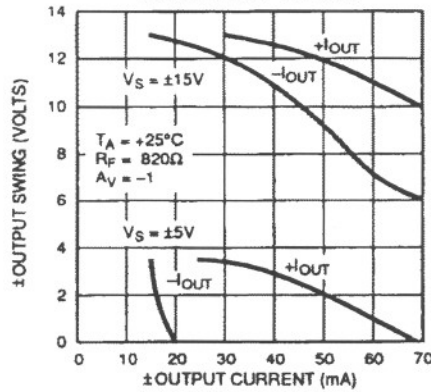
**NONINVERTING INPUT CURRENT NOISE DENSITY vs FREQUENCY**



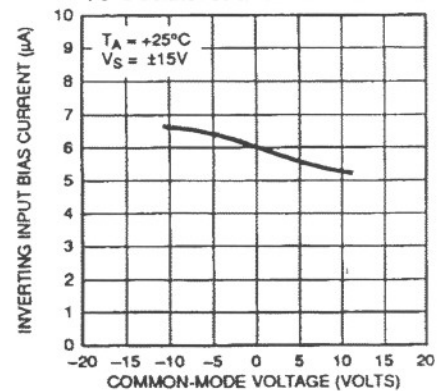
**TOTAL SUPPLY CURRENT vs SUPPLY VOLTAGE**



**OUTPUT CURRENT vs OUTPUT SWING**

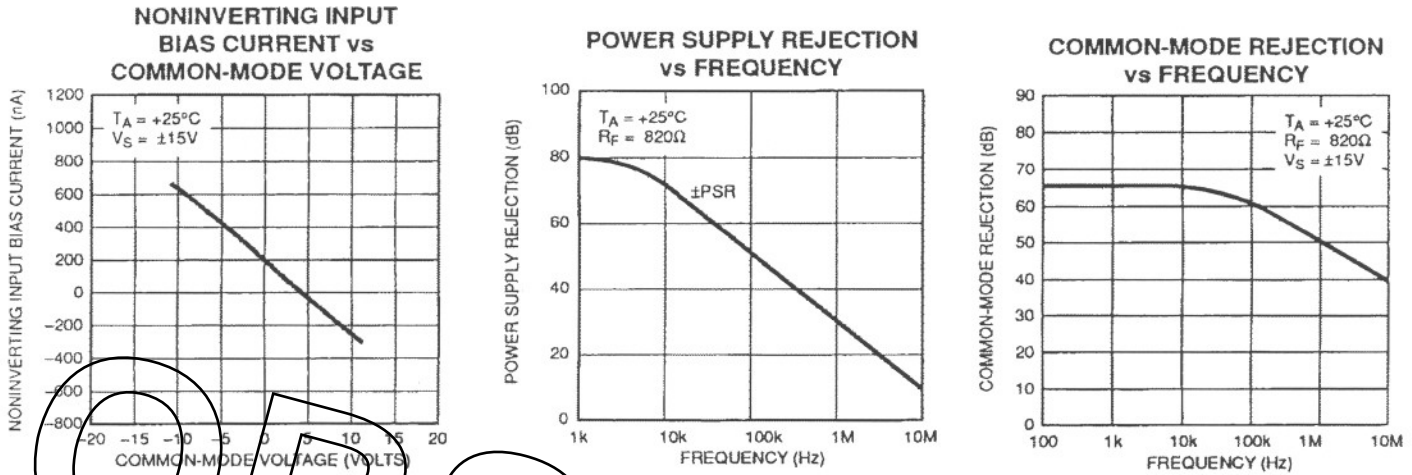


**INVERTING INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE**



# OP-160

## TYPICAL PERFORMANCE CHARACTERISTICS *Continued*



### APPLICATIONS INFORMATION

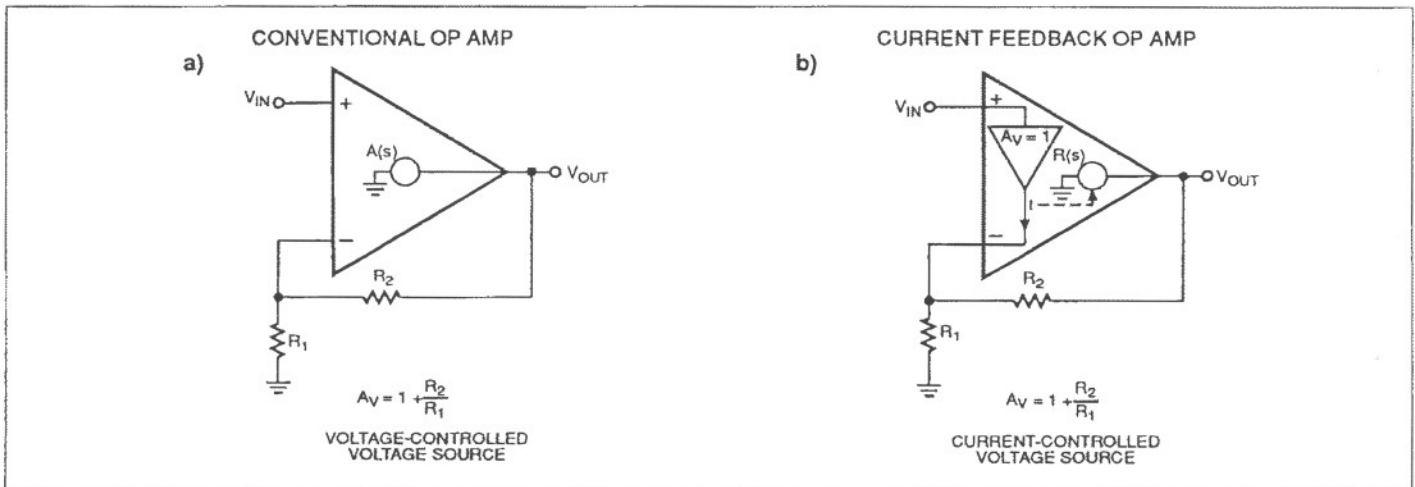
#### CURRENT VERSUS VOLTAGE FEEDBACK AMPLIFIERS

The OP-160 employs a unique circuit topology that sets it apart from conventional op amps. By using a transimpedance amplifier configuration, the OP-160 provides substantial improvements in bandwidth and slew rate over voltage feedback op amps. Figure 1 compares models of these two different amplifier configurations.

A voltage feedback op amp multiplies the differential voltage at its inputs by its open-loop gain. The feedback loop forces the output to a voltage that, when divided by  $R_1$  and  $R_2$ , equalizes the input voltages. Unlike a voltage feedback op amp, which has

high impedance inputs, the current feedback amplifier has a high and a low impedance input. The current feedback amplifier's input stage consists of a unity-gain voltage buffer between the noninverting and inverting inputs. The inverting "input" is in reality a low impedance output. Current can flow into or out of the inverting input. A transimpedance stage follows the input buffer that converts the buffer output current into a linearly proportional amplifier output voltage.

The current feedback amplifier loop works in the following fashion (Figure 1b). As the noninverting input voltage rises, the inverting input follows and the buffer sources current through  $R_1$



**FIGURE 1:** The conventional op amp (a) can be modelled as a voltage-controlled voltage source. In contrast, the current feedback op amp (b), resembles a current-controlled voltage source.

This current, multiplied by the transimpedance stage, causes the amplifier's output voltage to rise until the current flowing into  $R_2$  from the amplifier's output equalizes the current through  $R_1$ , replacing the buffer's output current. At steady state, only a very small buffer output current must flow to sustain the proper output voltage. The ratio  $(1 + R_2/R_1)$  determines the closed-loop gain of the circuit. The result is that when designing with current feedback amplifiers the familiar op amp assumptions can still be used for circuit analysis:

1. The voltage across the inputs equals zero.
2. The current into the inputs equals zero.

**BANDWIDTH VERSUS GAIN**

A unique feature of the current feedback amplifier design is that the closed-loop bandwidth remains relatively constant as a function of closed-loop gain. Voltage feedback op amps suffer from a bandwidth reduction as closed-loop gain increases, as quantified by the gain-bandwidth product (GBWP). This is illustrated in Figure 2 which shows the frequency response of the OP-160 for various closed-loop gains and the frequency response of a voltage feedback op amp with a gain-bandwidth product of 30MHz. The bandwidth of the OP-160 is much less dependent upon closed-loop gain than the voltage feedback op amp.

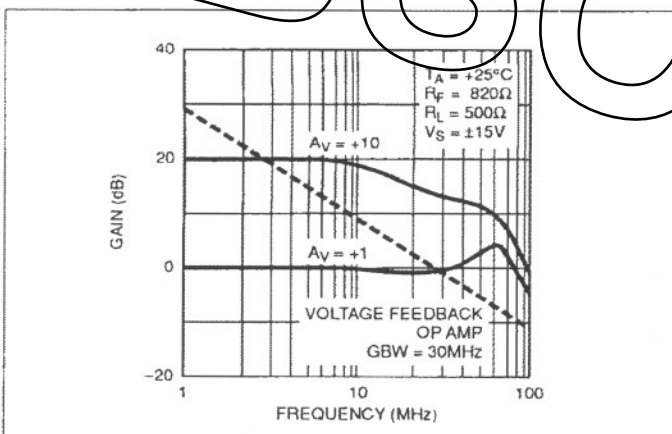


FIGURE 2: Frequency response of the OP-160 when connected in various closed-loop gains with  $R_F = 820\Omega$  and  $R_L = 100\Omega$ . Note that the frequency response of the OP-160 does not follow the asymptotic roll-off characteristic of a voltage feedback op amp.

**FEEDBACK RESISTANCE AND BANDWIDTH**

The closed-loop frequency response of the OP-160 shown in Figure 2 applies for a fixed feedback resistor of  $820\Omega$ . The frequency response of a current feedback amplifier is primarily dependent on the value of the feedback resistor value. The design of the OP-160 has been optimized for a feedback resistance of  $820\Omega$ . By holding the feedback resistor value constant, the  $-3\text{dB}$  frequency point will also remain constant within a moderate range of closed-loop gain.

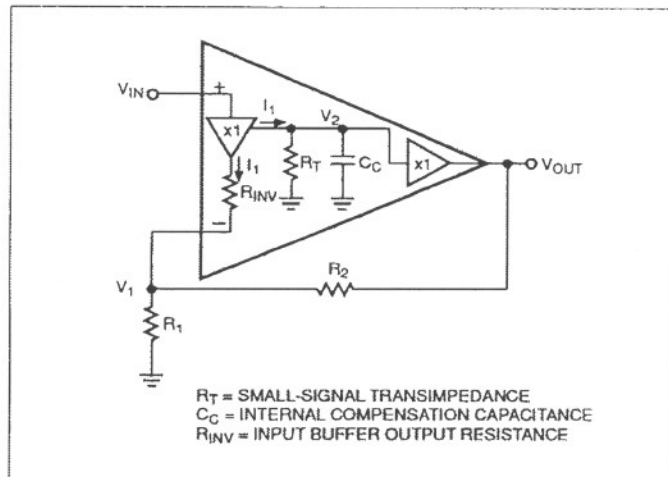


FIGURE 3: Simple frequency response model of the current feedback amplifier.

The model shown in Figure 3 can be used to determine the frequency response of a current feedback amplifier. With this model, the frequency response dependency on the value of the feedback resistance is easily seen.

From the model of Figure 3, nodal equations may be written for  $V_1$  and  $V_2$ .

$$V_1 = \frac{V_{IN} \left( \frac{R_2}{R_{INV}} \right) + V_{OUT}}{1 + \frac{R_2}{R_1} + \frac{R_2}{R_{INV}}}$$

$$V_2 = \frac{R_T}{1 + sR_T C_C} I_1$$

where  $I_1 = \frac{V_{IN} - V_1}{R_{INV}} = V_1 \left( \frac{1}{R_1} + \frac{1}{R_2} \right) - \frac{V_{OUT}}{R_2}$ , and  $V_{OUT} = V_2$

Combining these equations yields:

$$V_{OUT} = \left[ \frac{\left( V_{IN} \left( \frac{R_2}{R_{INV}} \right) + V_{OUT} \right)}{1 + \frac{R_2}{R_1} + \frac{R_2}{R_{INV}}} \right] \left[ \left( \frac{1}{R_1} + \frac{1}{R_2} \right) - \frac{V_{OUT}}{R_2} \right] \frac{R_T}{1 + sR_T C_C}$$

If the transimpedance of the amplifier,  $R_T$ , is  $\gg R_2$  and  $R_{INV}$ , then the transfer function may be simplified to:

$$\frac{V_{OUT}}{V_{IN}} \approx \frac{1 + \frac{R_2}{R_1}}{1 + s \left[ R_2 + \left( 1 + \frac{R_2}{R_1} \right) R_{INV} \right] C_C}$$

# OP-160

The transfer function shows that the dominant closed-loop pole is mainly dependent on the value of the feedback resistance,  $R_2$ , and the internal compensation capacitor,  $C_C$ . For example, at unity gain, where  $R_1$  is infinite,  $R_2$  determines the  $-3\text{dB}$  frequency.

$$\frac{V_{OUT}}{V_{IN}} \approx \frac{1}{1 + sR_2 C_C}$$

$$f_{-3\text{dB}} = \frac{1}{2\pi R_2 C_C}$$

where  $R_2 \gg R_{INV}$

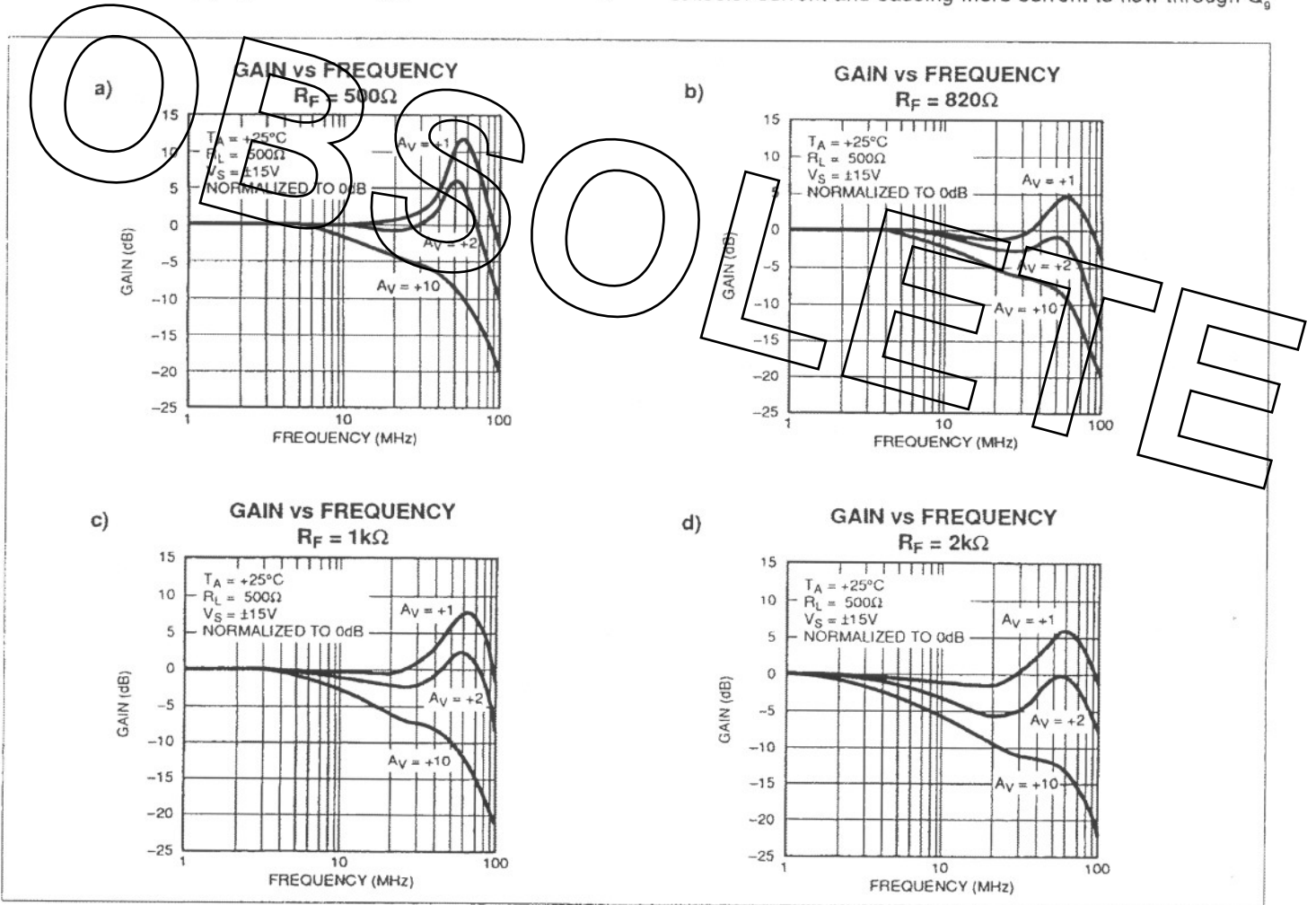
For higher gains, the  $-3\text{dB}$  frequency is determined by  $R_2$  plus the output resistance of the buffer,  $R_{INV}$  (typically  $60\Omega$ ), which is multiplied by the closed-loop gain. As the closed-loop gain increases, the multiplying effect on  $R_{INV}$  becomes dominant,

causing the bandwidth to decrease. However, the closed-loop bandwidth of a current feedback amplifier still far exceeds that of a voltage feedback op amp for moderate values of gain.

Figure 4 shows the effect of the feedback resistance on the bandwidth of the OP-160 for various closed-loop gains.

### SLEW RATE AND GAIN

The simplified schematic in Figure 5 shows the three stages of the OP-160. The input stage consists of a unity-gain emitter-follower amplifier.  $Q_5$  and  $Q_6$  form a class AB output stage at the inverting input which can source or sink current. The current flowing through the inverting input is sensed by the top current mirror, formed by  $Q_7$ ,  $Q_9$ , and  $Q_{10}$ , or the bottom current mirror, formed by  $Q_8$ ,  $Q_{11}$ , and  $Q_{12}$ . When the buffer sources current to a load, current flows out of the inverting input, increasing  $Q_5$ 's collector current and causing more current to flow through  $Q_6$



**FIGURE 4:** Bandwidth will vary with feedback resistance. Peaking increases as the feedback resistance is decreased.  $R_F = 820\Omega$  is the recommended value. All graphs are normalized to  $0\text{dB}$ .

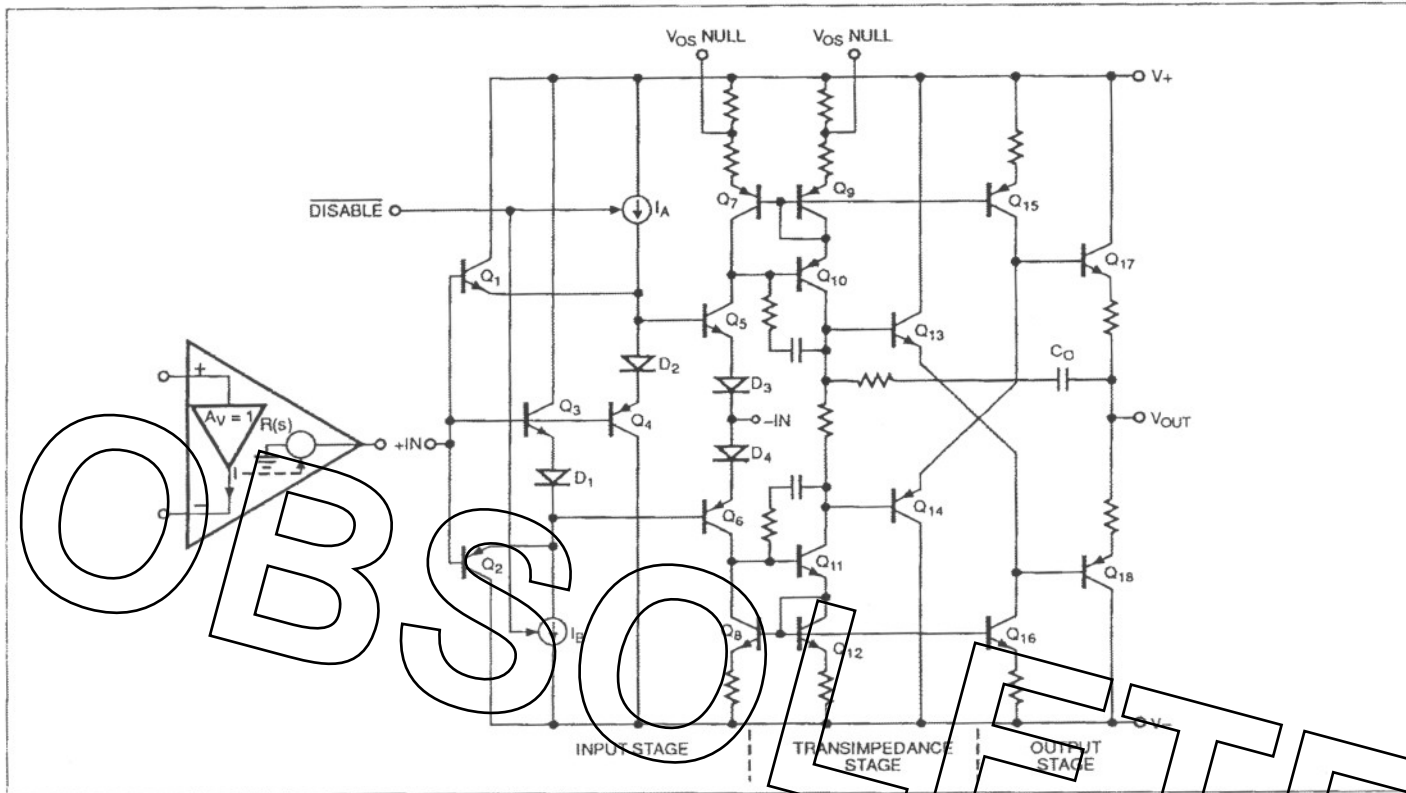


FIGURE 5: Simplified schematic of the OP-160 showing the three stages of the amplifier.

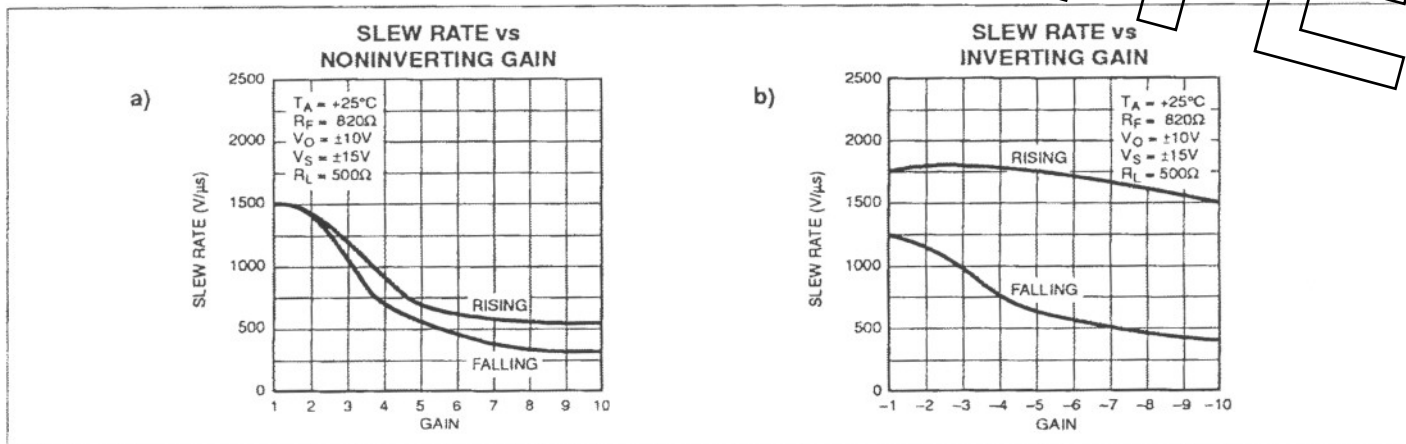


FIGURE 6: Slew rate of the OP-160 in noninverting (a) and inverting (b) configurations.

and  $Q_{15}$ . This increases the base drive to the output transistor  $Q_{17}$ . Simultaneously, the increased current in  $Q_9$  drives  $Q_{13}$  which reduces base drive to the complementary output transistor  $Q_{18}$ . This push-pull action produces a very fast output slew rate. For a small voltage step, the OP-160's slew rate is dependent on the available current from the two current sources ( $I_A$  and  $I_B$ ) that drive  $Q_5$  and  $Q_6$ .

To increase the slew rate, transistors  $Q_1$  and  $Q_2$  have been added to boost the base drive to  $Q_5$  and  $Q_6$ . In low gains, a large input step will turn on  $Q_1$  or  $Q_2$  increasing the slew rate dramatically as illustrated in Figure 6.

# OP-160

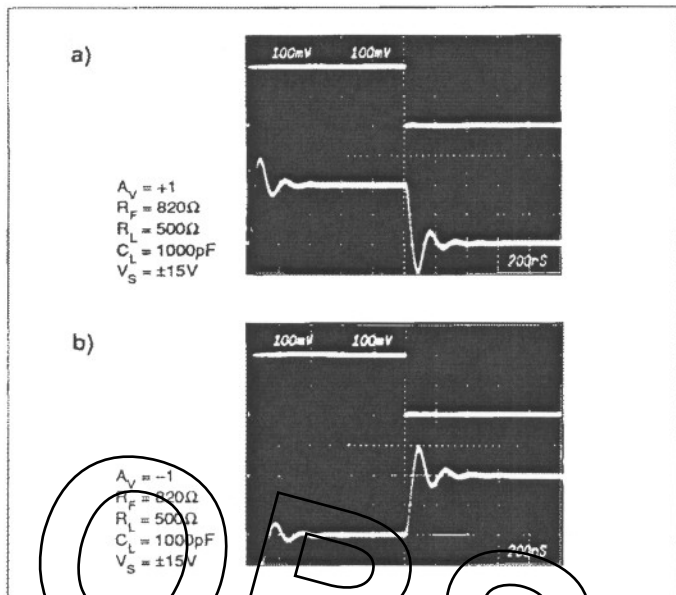


FIGURE 7: The OP-160 remains stable when driving large capacitive loads.

## DRIVING CAPACITIVE LOADS

The OP-160 is capable of driving capacitive loads at high speed. Output stage compensation is used to reduce the effects of capacitive loading. With low capacitive loads, the gain from the compensation node to the output is unity and  $C_o$  does not contribute to the overall compensation. As the load capacitance is increased, a pole is formed with the output resistance of the amplifier. The gain is reduced and  $C_o$  begins to contribute to the overall compensation capacitance leading to a reduction in bandwidth. As the load capacitance is increased, the bandwidth

is further reduced and the amplifier remains stable. Figure 7 shows the OP-160 in a gain of +1 and -1 driving a 1000pF load without any sign of oscillation. Table 1 shows the effects of capacitive load on the -3dB bandwidth for  $A_v = -1$ .

TABLE 1: -3dB Bandwidth vs. Capacitive Load;  $A_v = -1$ ,  $R_f = 820\Omega$ ,  $R_L = 500\Omega$ ,  $V_S = \pm 15V$ .

CAPACITANCE (pF)	-3dB BANDWIDTH (MHz)
0	55
20	55
50	50
75	48
100	40
200	24
500	13
1000	9

## AMPLIFIER NOISE PERFORMANCE

Simplified noise models of the OP-160 in the noninverting and inverting amplifier configurations are shown in Figure 8. All resistors are assumed to be noiseless.

For the noninverting amplifier, the equivalent input voltage noise, referred to the input, is:

$$E_N = \sqrt{(R_S i_{nn})^2 + e_n^2 + (R_2 i_{ni})^2 / A_{VCL}}$$

where:

- $E_N$  = total input referred noise
- $e_n$  = amplifier voltage noise
- $i_{nn}$  = noninverting input current noise
- $i_{ni}$  = inverting input current noise
- $R_S$  = source resistance
- $A_{VCL}$  = closed loop gain =  $1 + R_2/R_1$

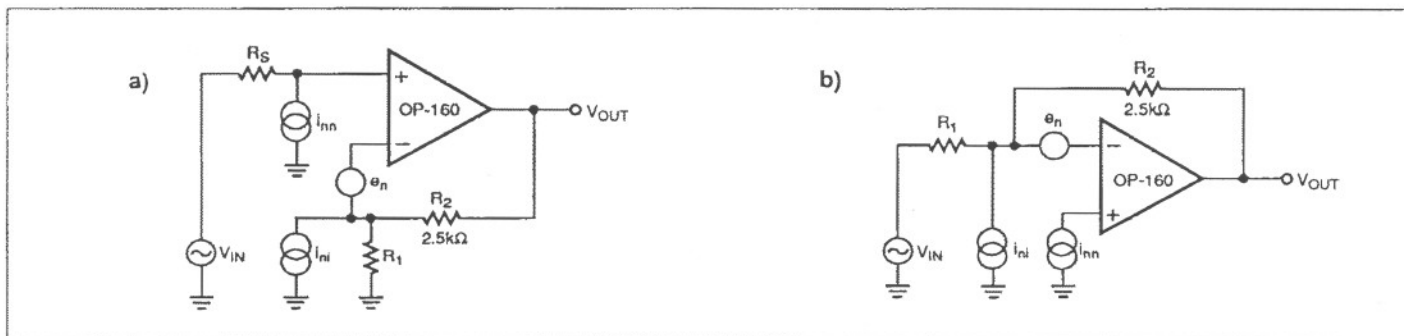


FIGURE 8: Simplified noise models for the OP-160 in noninverting (a) and inverting (b) gain.

OP-160

For the inverting amplifier, the equivalent input voltage noise, referred to the input, is:

$$E_N = \sqrt{e_n^2 \left( \frac{1 + |A_{VCL}|}{|A_{VCL}|} \right) + \frac{(R_2 i_{ni})^2}{|A_{VCL}|}}$$

assuming  $R_S \ll R_1$ ,  $A_{VCL}$  = closed-loop gain =  $-R_2/R_1$ .

Typical values @ 1kHz for the noise parameters of the OP-160 are:

- $e_n = 5.5nV/\sqrt{Hz}$
- $i_{nn} = 5pA/\sqrt{Hz}$
- $i_{ni} = 20pA/\sqrt{Hz}$

**SHORT-CIRCUIT PERFORMANCE**

To avoid sacrificing bandwidth and slew rate performance the OP-160's output is **not** short-circuit protected. Do not short the amplifier's output to ground or to the supplies. Also, the buffer output current should not exceed a value of  $\pm 20mA$  peak or  $\pm 7mA$  continuous.

**POWER SUPPLY BYPASSING AND LAYOUT CONSIDERATIONS**

Proper power supply bypassing is critical in all high-frequency circuit applications. For stable operation of the OP-160, the power supplies must maintain a low impedance-to-ground over an extremely wide bandwidth. This is most critical when driving a low resistance or large capacitance, since the current required to drive the load comes from the power supplies. A  $10\mu F$  and

$0.1\mu F$  bypass capacitor are recommended for each supply, as shown in Figure 9, and will provide adequate high-frequency bypassing in most applications. The bypass capacitors should be placed at the supply pins of the OP-160. As with all high frequency amplifiers, circuit layout is a critical factor in obtaining optimum performance from the OP-160. Proper high-frequency layout reduces unwanted signal coupling in the circuit. When breadboarding a high-frequency circuit, use direct point-to-point wiring, keeping all lead lengths as short as possible. Do not use wire-wrap boards or "plug-in" prototyping boards.

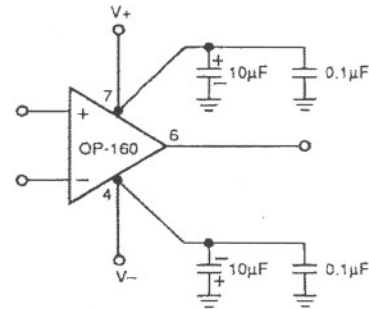


FIGURE 9: Proper power supplying bypassing is required to obtain optimum performance with the OP-160.

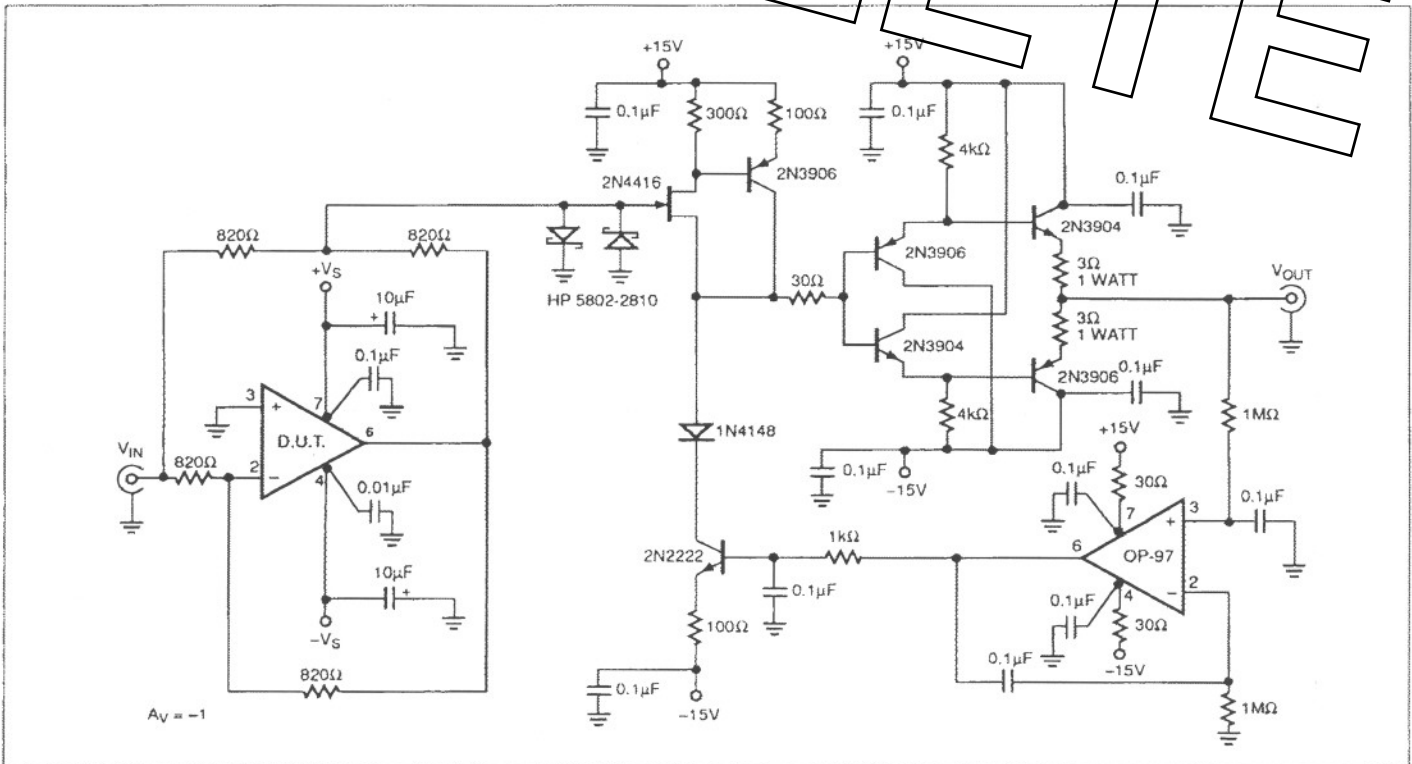


FIGURE 10: High-Speed Settling Time Fixture (for 0.1 and 0.01%)

# OP-160

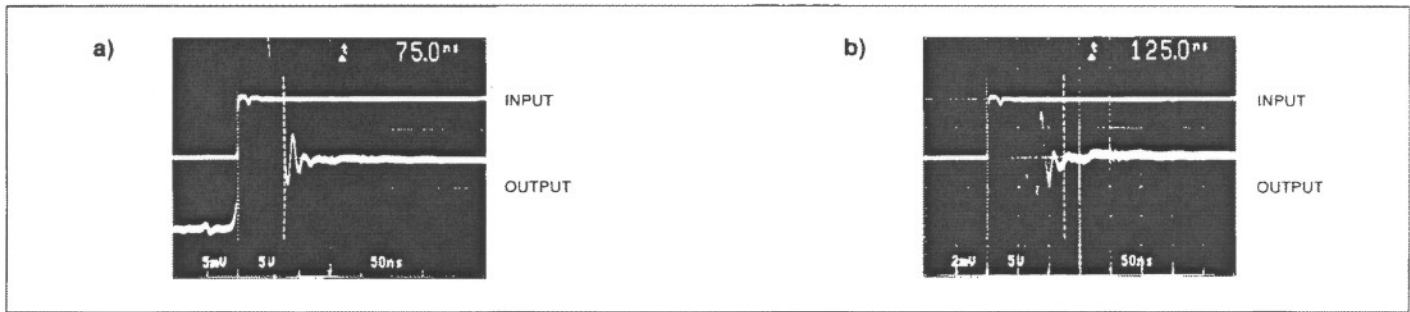


FIGURE 11: Settling Time Performance of the OP-160 to 0.1% (a) and 0.01% (b)  $A_V = -1$

## SETTLING TIME

Settling time is the time between when the input signal begins to change and when the output permanently enters a prescribed error band. Figure 10 illustrates the artificial summing node test configuration, used to characterize the OP-160 settling time. The OP-160 is set in a gain of -1 with a 10V step input. The error bands on the output are 5mV and 0.5mV, respectively, for 0.1% and 0.01% accuracy.

The test circuit, built on a copper clad circuit board, has a FET input stage which maintains extremely low loading capacitance at the artificial sum node. Preceding stages are complementary emitter follower stages, providing adequate drive current for a 50Ω oscilloscope input. The OP-97 establishes biasing for the input stage, and eliminates excessive offset voltage errors.

## TRANSIENT OUTPUT IMPEDANCE

Settling characteristics of operational amplifiers also includes an amplifier's ability to recover, i.e., settle, from a transient current output load condition. An example of this includes an op amp driving the input from a SAR type A/D converter. Although the comparison point of the converter is usually diode clamped, the input swing of plus-and-minus a diode drop still gives rise to a significant modulation of input current. If the closed-loop output impedance is low enough and bandwidth of the amplifier is sufficiently large, the output will settle before the converter makes a comparison decision which will prevent linearity errors or missing codes.

Figure 12 shows a settling measurement circuit for evaluating recovery from an output current transient. An output disturbing current generator provides the transient change in output load current of 1mA. As seen in Figure 13, the OP-160 has extremely fast recovery of 80ns, (to 0.01%), for a 1mA load transient. The performance makes it an ideal amplifier for data acquisition systems.

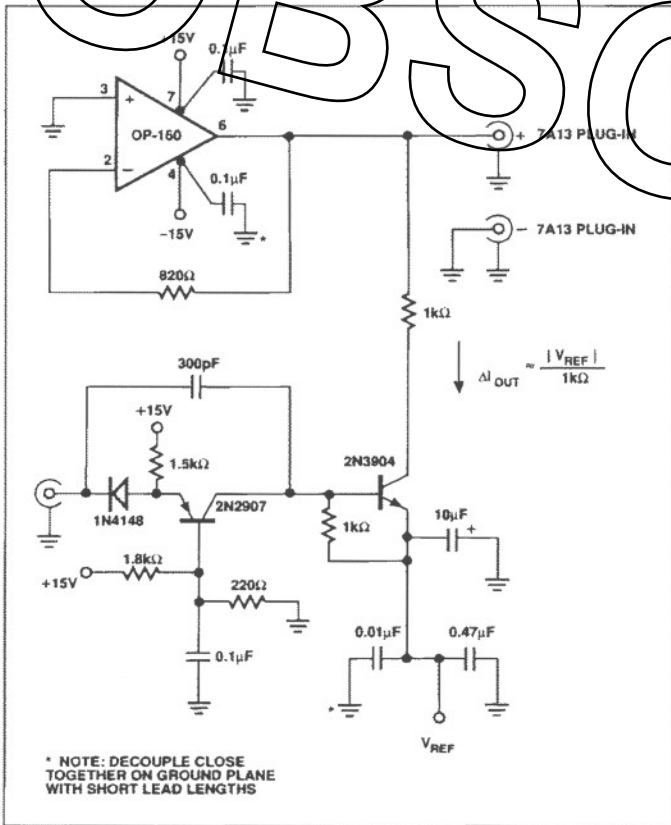


FIGURE 12: Transient Output Impedance Test Fixture

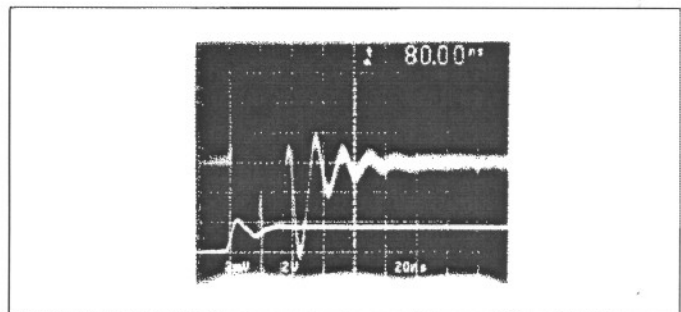


FIGURE 13: OP-160's Extremely Fast Recovery Time from a 1mA Load Transient to 1mV (0.01%)



OP-160

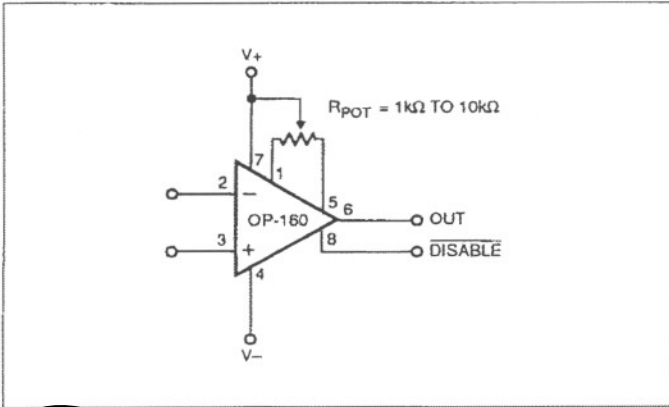


FIGURE 14: Input Offset Voltage Nulling

**OFFSET VOLTAGE ADJUSTMENT**

Offset voltage is adjusted with a 20kΩ potentiometer as shown in Figure 14. The potentiometer should be connected between pins 1 and 5 with its wiper connected to the V+ supply. The typical trim range is ±40mV.

**DISABLE AMPLIFIER SHUTDOWN**

Pin 8 of the OP-160,  $\overline{\text{DISABLE}}$ , is an amplifier shutdown control input. The OP-160 operates normally when Pin 8 is left floating. When greater than 1000μA is drawn from the  $\overline{\text{DISABLE}}$  pin, the OP-160 is disabled. To draw current from the  $\overline{\text{DISABLE}}$  pin, an open collector output logic gate or a discrete NPN transistor can be used as shown in Figure 15. An internal resistor limits the  $\overline{\text{DISABLE}}$  current to around 500μA if the  $\overline{\text{DISABLE}}$  pin is grounded with the OP-160 powered by ±15V supplies. These logic interface methods have the added advantage of level

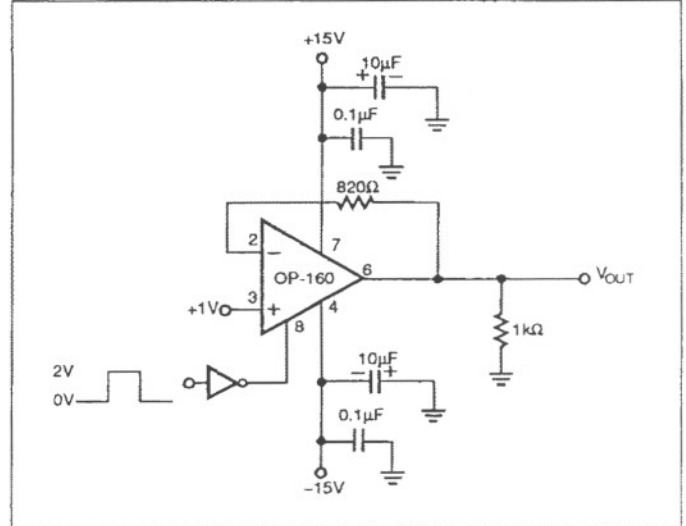


FIGURE 16:  $\overline{\text{DISABLE}}$  Turn-On/Turn-Off Test Circuit

shifting the TTL signal to whatever supply voltage is used to power the OP-160.

In the  $\overline{\text{DISABLE}}$  mode, the OP-160 maintains 40dB of input-to-output isolation if the input signal remains below ±1.5V. Output resistance is very high, over 100kΩ, if the output is driven by signals of less than ±1.5V. Higher signals will be distorted.

Figure 16 shows a test circuit for measuring the turn-on and turn-off times for the OP-160. The OP-160 is in a gain of +1 with a +1V DC input. As the input pulse to the inverter rises its output falls, drawing current from the  $\overline{\text{DISABLE}}$  pin and disabling the

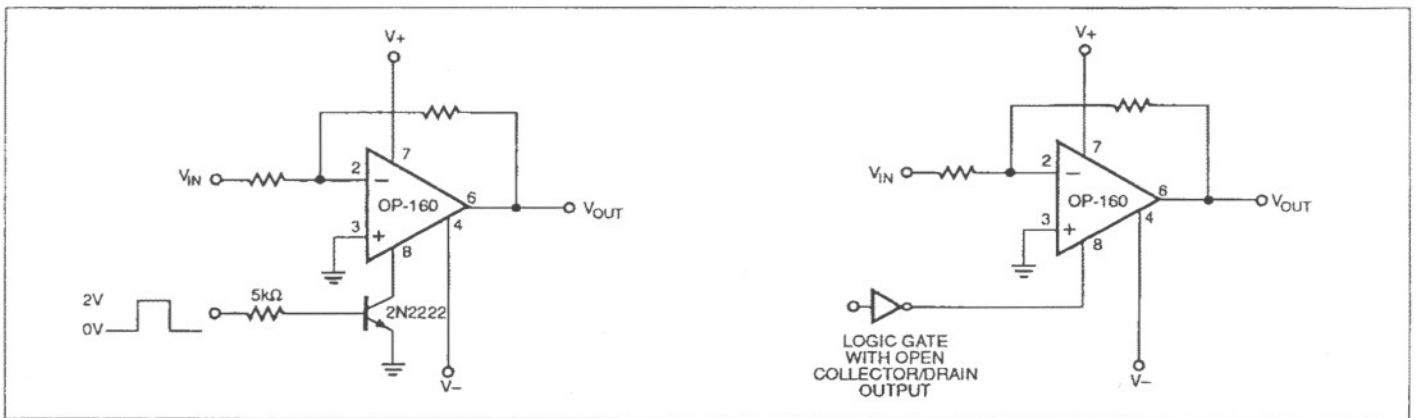


FIGURE 15: Simple circuits allow the OP-160 to be shut down.

# OP-160

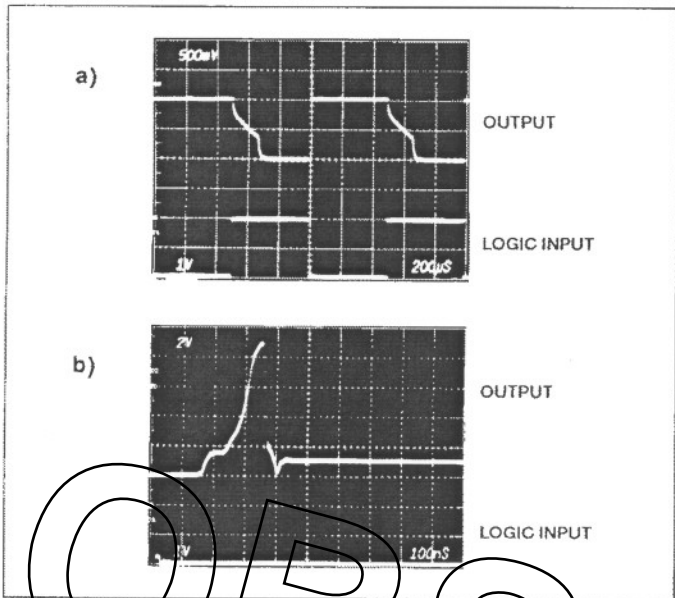


FIGURE 17: (a) OP-160 turn-on and turn-off performance. (b) Expanded scale showing turn-on performance of the OP-160. Be aware of the high-frequency spike during turn-on.

amplifier. The output voltage delay is shown in Figure 17 and takes 200µs to reach ground. The turn-on time is much quicker than the turn-off time. In this situation as the input to the inverter falls its output rises, returning the OP-160 to normal operation. The amplifier's output reaches its proper output voltage in 450ns.

### OVERDRIVE RECOVERY

Figure 19 shows the overdrive recovery performance of the OP-160. Typical recovery time is 120ns from positive and negative overdrive.

### APPLICATIONS

#### NONINVERTING AMPLIFIER

The OP-160 can be used as a voltage-follower or noninverting amplifier as shown in Figure 20. A current feedback amplifier in this configuration yields the same transfer function as a voltage feedback op amp:

$$\frac{V_{OUT}}{V_{IN}} = 1 + \frac{R_2}{R_1}$$

Remember to use a 820Ω feedback resistor in voltage-follower applications.

In noninverting applications, stray capacitance at the inverting input of a current feedback amplifier will cause peaking which will increase as the closed-loop gain decreases. The gain setting resistor, R<sub>1</sub>, is in parallel with this stray capacitance creating a zero in the

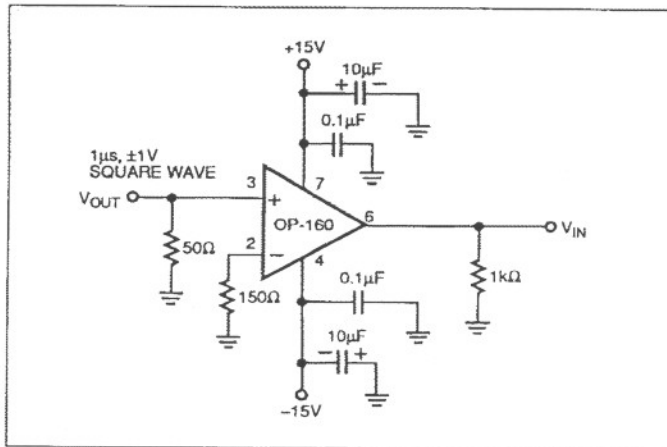


FIGURE 18: Overdrive Recovery Test Circuit

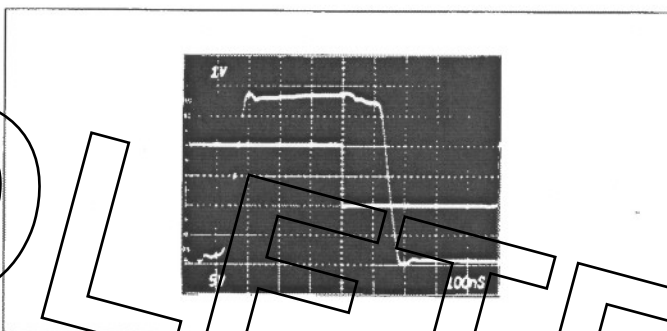


FIGURE 19: The OP-160 recovers from both positive and negative overdrive in 120ns.

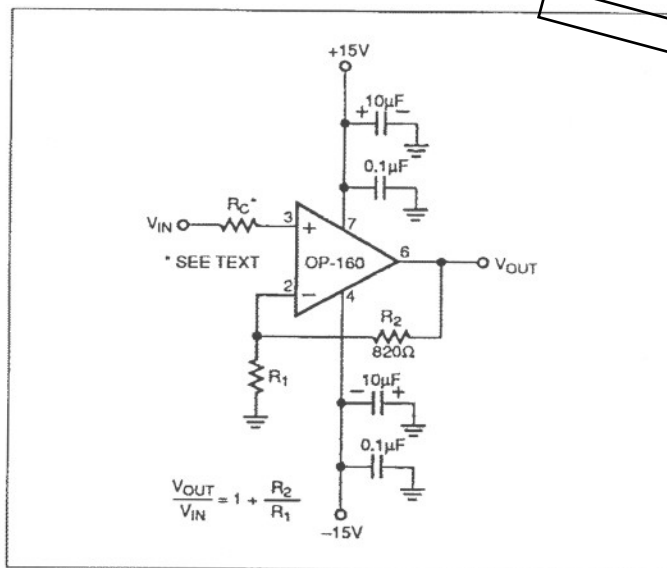


FIGURE 20: The OP-160 as a voltage follower or noninverting amplifier.

closed-loop response. For large noninverting gains,  $R_1$  is small, creating a very high-frequency open-loop pole which has limited effect on the closed-loop response. As the noninverting gain is decreased,  $R_1$  becomes larger and the stray zero becomes lower in frequency, having a much greater effect on the closed-loop response. To reduce peaking at low noninverting gains, place a series resistor,  $R_C$ , in series with the noninverting input as shown in Figure 20. This resistor combines with the stray capacitance at the noninverting input to form a low-pass filter that will reduce the peaking. The value of  $R_C$  should be determined experimentally in the actual PCB layout. Less peaking will occur in inverting gain configurations since the inverting input is a virtual ground which forces a constant voltage across the stray capacitance.

A common practice to stabilize voltage feedback op amps is to use a capacitor across the feedback resistance. This creates a zero in the voltage feedback amplifier response to offset the loss of phase margin due to a parasitic pole. In current feedback amplifiers, this technique will cause the amplifier to become unstable because the closed-loop bandwidth will increase beyond the stable operating frequency.

**INVERTING AMPLIFIER**

The OP-160 is also capable of operation as an inverting amplifier (see Figure 21). The transfer function of this circuit is identical to that using a voltage feedback op amp:

$$\frac{V_{OUT}}{V_{IN}} = -\frac{R_2}{R_1}$$

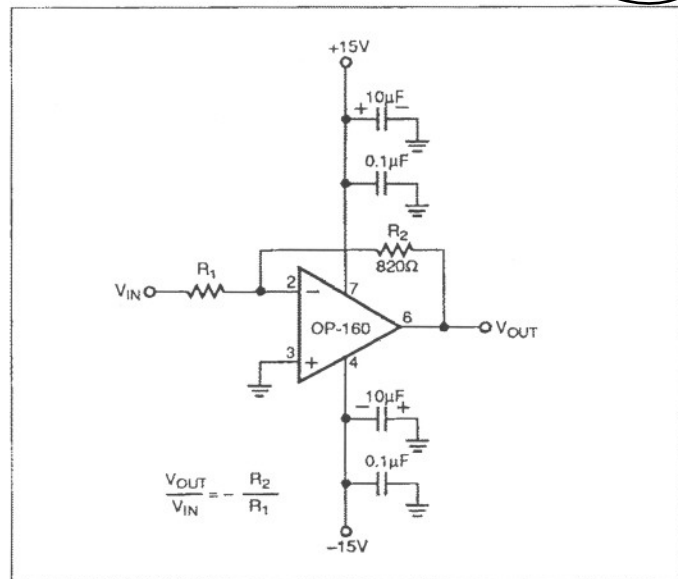


FIGURE 21: The OP-160 as an inverting amplifier.

**USING CURRENT FEEDBACK OP AMPS IN INTEGRATOR APPLICATIONS**

The small-signal model of a current feedback op amp shown earlier in Figure 3 assumes a non-varying value of feedback impedance. A non-varying feedback impedance ensures that the bandwidth of the amplifier does not extend beyond its 180° phase shift point and create unwanted oscillations. In integrator circuits, the feedback element is a capacitor whose impedance does vary with frequency. By definition then, integrator applications using current feedback amplifiers should be unstable. However, a simple trick, shown in Figure 22, enables high-speed, wide bandwidth current feedback op amps to be used in integrator applications.

Resistor  $R_F$  is placed between an artificial sum node and the inverting input of the amplifier. This resistor maintains a minimum value of feedback impedance over all frequencies. At high signal frequencies, the integrator capacitor,  $C_1$ , is a short circuit; the feedback impedance is equal to  $R_F$  only and the amplifier has maximum bandwidth. At low frequencies,  $C_1$  adds to the overall feedback impedance. This lowers the amplifier's bandwidth but not enough to affect the integrator's performance.

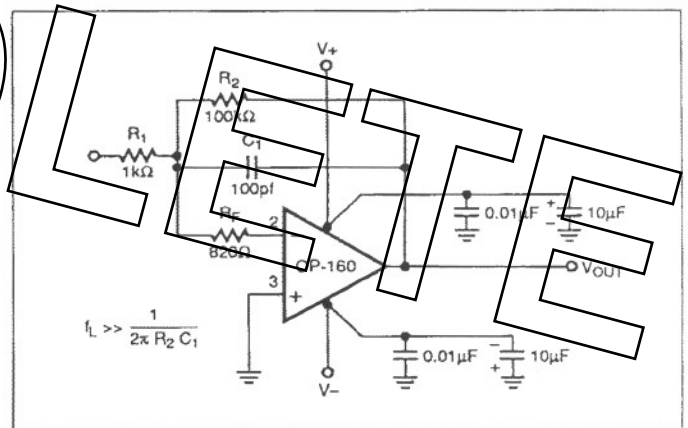


FIGURE 22: An Integrator Using a Current Feedback Op Amp

# OP-160

Figure 23 shows the gain and phase performance of the integrator. The integrator has the desired one-pole response for signal frequencies

$$f_c \gg 1/(2\pi R_2 C_1) \approx 16\text{kHz.}$$

A more strenuous test of integrator performance is the pulse response. Ideally, this should be a linear ramp. The current feedback integrator's pulse response is exhibited in Figure 24. The response closely approximates the ideal linear ramp.

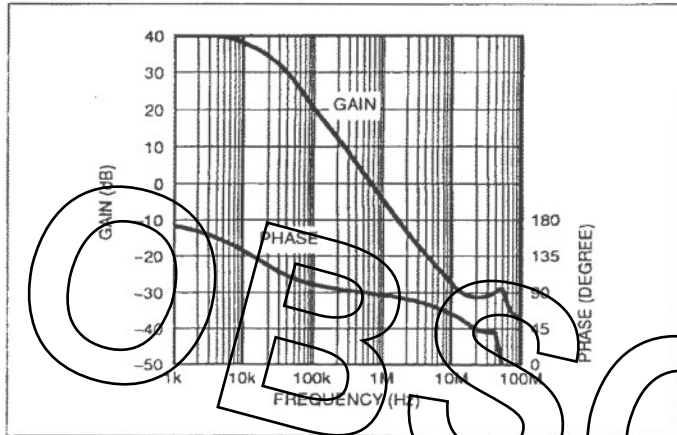


FIGURE 23: Gain and phase response of the integrator shows a one-pole response.

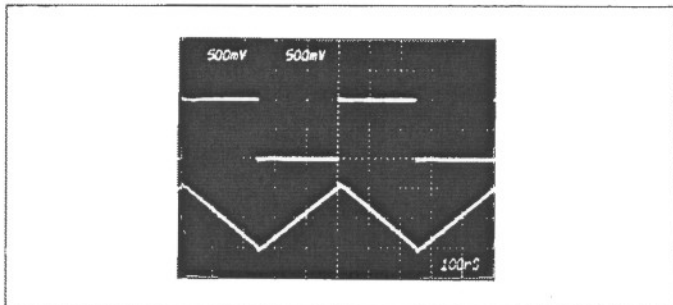


FIGURE 24: Pulse response of the current feedback integrator.  $f = 2\text{MHz.}$

## ACHIEVING FLAT GAIN RESPONSE WITH CURRENT FEEDBACK OP AMPS

In high-performance systems, flat gain response is often required. Current feedback op amps provide wide bandwidth performance but even these may not fulfill the gain flatness requirements of some systems.

Current feedback op amps exhibit both gain roll-off and peaking as shown in Figure 25. Peaking is primarily due to parasitic

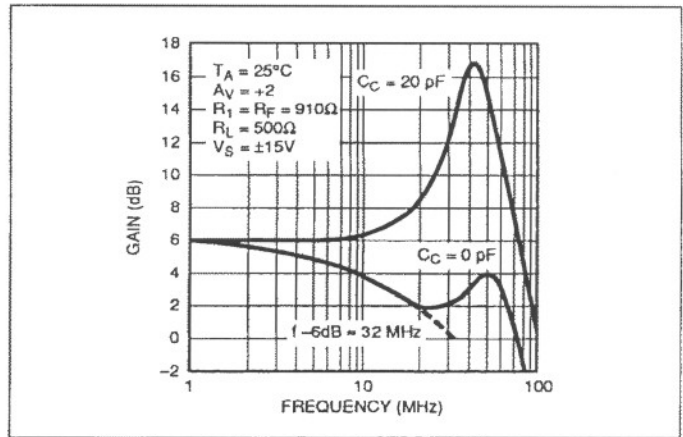


FIGURE 25: Gain roll-off and peaking of current feedback amplifiers is dependent upon a number of factors including loading and parasitic capacitance.

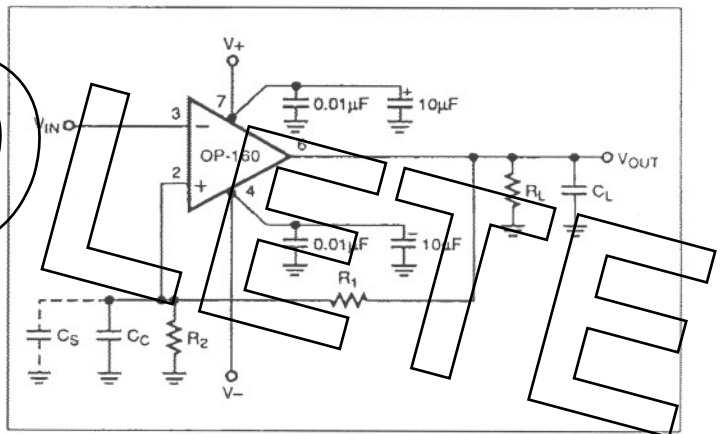


FIGURE 26: A current feedback op amp configured for non-inverting gain. Parasitic capacitances affecting gain are also shown.

capacitance; gain roll-off is determined by the amount and type of load on the amplifier. Peaking is controlled by careful layout and circuit design; however, its cause can provide a method of improving gain flatness over a desired frequency range.

Consider the noninverting amplifier of Figure 26. The gain equals:

$$1 + \frac{R_2}{R_1 // Z_{(C_C // C_S)}}$$

and at low frequencies

$$A_V = 1 + \frac{R_2}{R_1} = 1 + \frac{910\Omega}{910\Omega} = 2$$

**OP-160**

At higher frequencies the gain increases or peaks due to the effect of the parasitic capacitance,  $C_S$ , on the gain equation. Any capacitance at the inverting input will create a zero in the amplifier's response. This fact can be used to compensate for gain roll-off due to loading on the amplifier.

Begin by measuring or estimating the amplifier's -6dB point (this is the frequency at which the output signal is half its original amplitude). This can be easily determined from a network analyzer plot of the amplifier's frequency performance. From this the amount of capacitance,  $C_C$ , which will double the gain at the -6dB frequency and restore the original gain, can be determined.

From the -6dB frequency,  $C_C$  can be calculated:

$$C_C = C_S + \frac{1}{2\pi R_1 f_{-6dB}} + \frac{1}{2\pi R_2 f_{-6dB}}$$

for noninverting configuration, where  $C_S$  is the combination of the amplifier's input capacitance and the stray capacitance at the input.

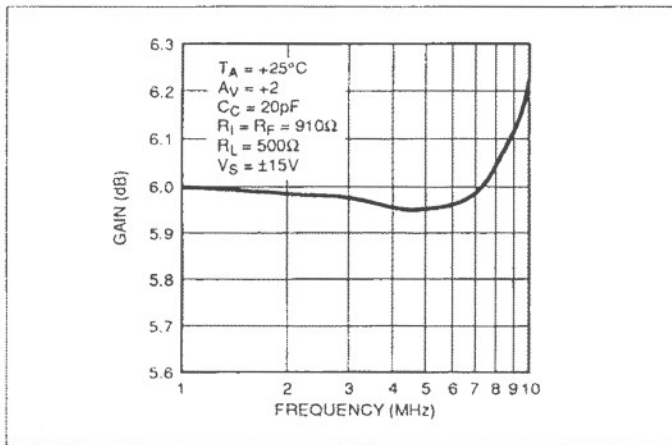
In the example shown,

$C_S = 9\text{pF} = \text{OP-160 input capacitance (4pF)} + \text{stray capacitance (5pF)}$

$$C_C = 9\text{pF} + \frac{1}{2\pi(910\Omega)32\text{MHz}} + \frac{1}{2\pi(910\Omega)32\text{MHz}}$$

$\approx 20\text{pF}$

Figure 27 is an expanded scale plot of the gain performance of the compensated amplifier at  $A_V = +2$ . Gain performance is flat to  $\pm 0.1\text{dB}$  out to beyond 9MHz. For low gains ( $A_V \leq 5$ ) peaking



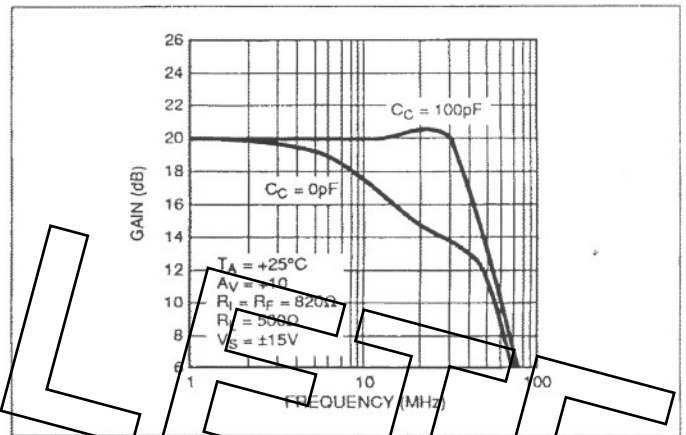
**FIGURE 27:** Expanded Gain/Frequency Graph of the Compensated Amplifier,  $A_V = +2$

will be increased. At higher gains, gain flatness can be significantly improved without gain peaking. Figure 28 depicts the OP-160 with  $A_V = +10$ . In this example  $f_{-6dB} \approx 22\text{MHz}$  so,

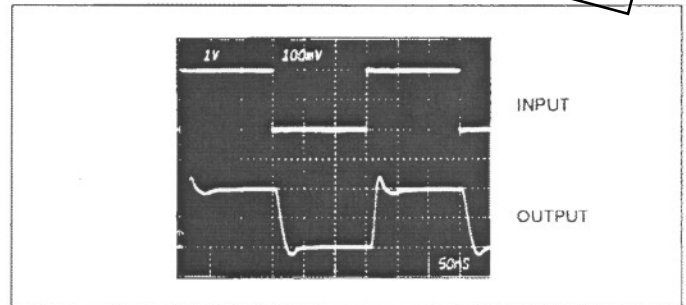
$$C_C = 9\text{pF} + \frac{1}{2\pi(91\Omega)22\text{MHz}} + \frac{1}{2\pi(820\Omega)22\text{MHz}} = 97\text{pF}$$

The nearest standard capacitor value is 100pF.

Gain performance is flat to 0.5dB to 30MHz and the amplifier's -3dB point is 38MHz. This gives the amplifier an effective gain-bandwidth of 380MHz! Compensating the OP-160 does not effect the pulse response as shown in Figure 29.



**FIGURE 28:** Gain/frequency graph for the compensated amplifier,  $A_V = +10$ , showing the effect of the compensation capacitance,  $C_C$ , on gain flatness.



**FIGURE 29:** Pulse Response of the OP-160 in a Gain of +10 Compensated for Gain Flatness

## OP-160

### OP-160 SPICE MACRO-MODEL

Figures 30 and 31 show the SPICE macro-model for the OP-160 high-speed, current feedback operational amplifier. This model was tested with, and is compatible with PSpice\* and HSpice\*\*. The schematic and net-list are included here so that the model can easily be used. This model uses a unique current feedback topology to accurately model both the AC and DC characteristics of the OP-160. In addition, this model can accommodate any number of poles and zeros to further shape the AC response.

The OP-160 SPICE macro-model uses four BJT transistors to create the input buffer as in the actual device. However, the rest of the model contains only ideal linear elements and ideal diodes to model the OP-160's behavior. Using only four transistors reduces simulation time and simplifies model development. It simulates important DC parameters such as  $V_{OS}$ ,  $I_B$ , CMR,  $V_O$  and  $I_{SY}$ . AC parameters such as slew rate, open-loop transimpedance and phase response and CMR changes with frequency are also simulated by the model. In addition, the model includes the change in input bias current with varying common-mode and power supply voltages. Both output swing and supply current are accurately modelled.

One aspect of the OP-160's behavior is that slew rate varies with closed-loop gain. Slew rate of the basic model is set to the typical values for the OP-160 in a gain of +1. For other gains, the

rising and falling slew rates can be adjusted by varying the values of  $V_1$  and  $V_2$  in the model. Slew rates for various gains can be determined from Figures 6a and 6b.

$$\text{Rising Slew Rate} = \frac{V_1 + 0.6V}{(1k\Omega)(5pF)}$$

$$\text{Falling Slew Rate} = \frac{V_2 + 0.6V}{(1k\Omega)(5pF)}$$

To keep the OP-160 model as simple as possible and thus save computer and development time, not all features of the op amp were modelled as listed below:

- PSR
- Crosstalk
- No limits on power supply voltages
- Maximum input voltage range
- Temperature effects (i.e., model parameters are assumed at 25°C)
- Input noise voltage and current sources
- Parameter variations for Monte Carlo analysis (i.e., all parameters are typical only)

These parameters are considered second-order effects and are not considered necessary for circuit simulation under normal operating conditions. However, users can easily add these functions as needed.

\* PSpice is a registered trademark of MicroSim Corporation.

\*\* HSPICE is a tradename of Meta-Software, Inc.

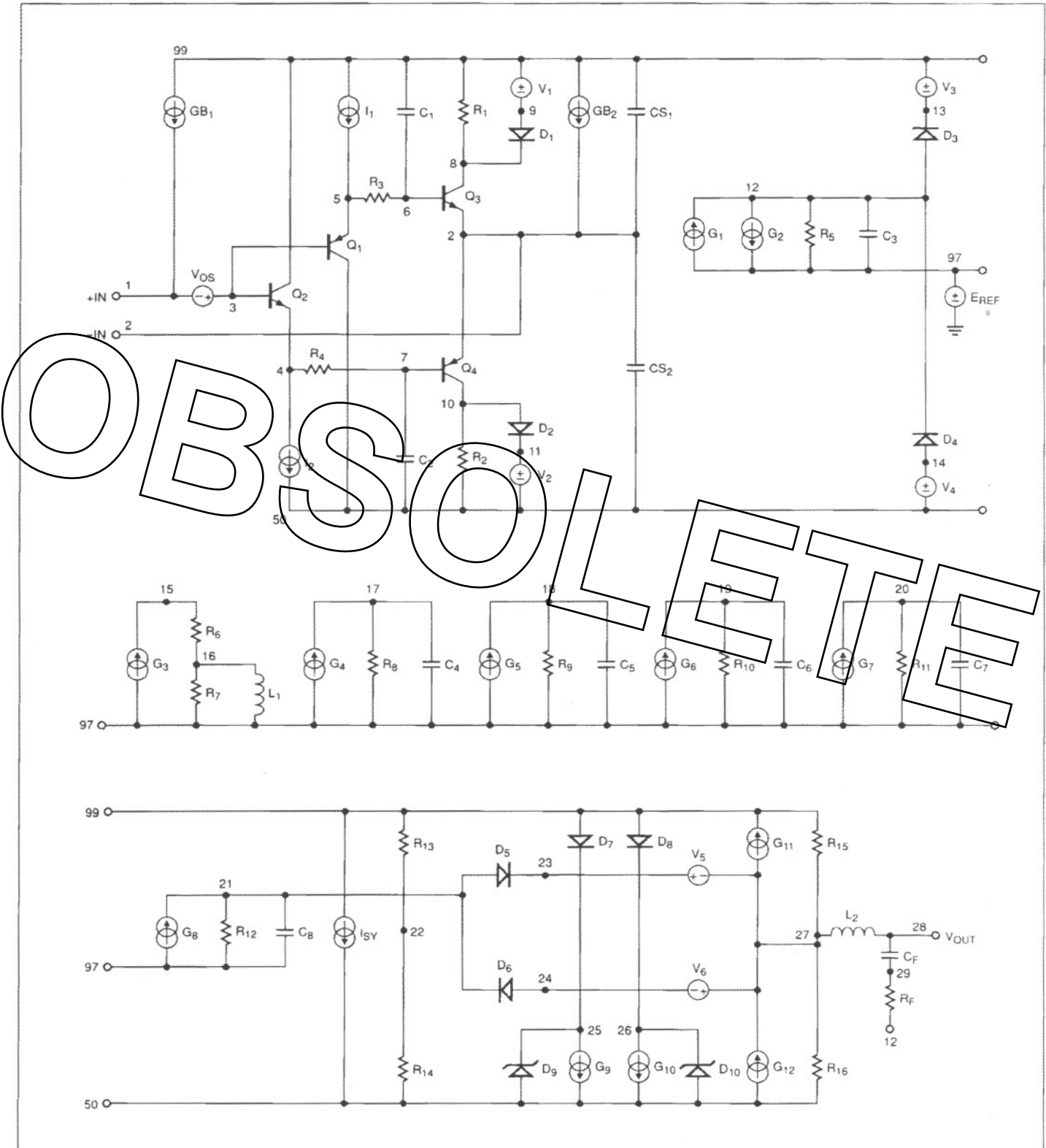


FIGURE 30: OP-160 SPICE Model

OP-160

```

* OP-160 MACRO-MODEL © PMI 1990
*
* NODE ASSIGNMENTS
NONINVERTING INPUT
INVERTING INPUT
OUTPUT
POSITIVE SUPPLY
NEGATIVE SUPPLY
SUBCKT OP-160 1 2 24 99 50
* INPUT STAGE
R1 99 8 1K
R2 10 50 1K
V1 99 9 9.4
D1 9 8 DX
V2 11 50 4.4
D2 10 11 DX
I1 99 5 125U
I2 4 50 125U
Q1 50 3 5 QP
Q2 99 3 4 QN
Q3 8 6 2 QN
Q4 10 7 2 QP
R3 5 6 143K
R4 4 7 143K
C1 99 6 0.0159P
C2 50 7 0.0133P
* INPUT ERROR SOURCES
GB1 99 1 POLY(1) 1 22 2E-7 4E-8
GB2 99 2 POLY(1) 1 22 5E-6 4E-8
VOS 3 1 1E-3
CS1 99 2 2.5E-12
CS2 50 2 2.5E-12
*
EREF 97 0 22 0 1
* GAIN STAGE & DOMINANT POLE
R5 12 97 5E6
C3 12 97 5P
G1 97 12 99 8 1E-3
G2 12 97 10 50 1E-3
V3 99 13 2.2
V4 14 50 2.2
D3 12 13 DX
D4 14 12 DX
CF 29 28 30P
RF 12 29 300
* ZERO/POLE PAIR AT 50MHZ/300MHZ
R6 15 16 1E6
L1 16 97 2.65E-3
R7 16 97 5E6
G3 97 15 12 22 1E-6
* POLE AT 300MHZ
R8 17 97 1E6
C4 17 97 0.531E-15
G4 97 17 15 22 1E-6
* POLE AT 300MHZ
R9 18 97 1E6
C5 18 97 0.531E-15
G5 97 18 17 22 1E-6
* POLE AT 500MHZ
R10 19 97 1E6
C6 19 97 0.318E-15
G6 97 19 18 22 1E-6
* POLE AT 500MHZ
R11 20 97 1E6
C7 20 97 0.318E-15
G7 97 20 19 22 1E-6
* POLE AT 500MHZ
R12 21 97 1E6
C8 21 97 0.318E-15
G8 97 21 20 22 1E-6
* OUTPUT STAGE
SY 99 50 1.75E-3
R13 22 99 3.333E3
R14 22 50 3.333E3
R15 27 99 40
R16 27 50 40
L2 27 28 4E-8
G9 25 50 21 27 25E-3
G10 26 50 27 21 25E-3
G11 27 99 99 21 25E-3
G12 50 27 21 50 25E-3
V5 23 27 1.55
V6 27 24 1.55
D5 21 23 DX
D6 24 21 DX
D7 99 25 DX
D8 99 26 DX
D9 50 25 DY
D10 50 26 DY
* MODELS USED
* MODEL QN NPN (BF=1E9 IS=1E-15 VAF=92)
* MODEL QP PNP (BF=1E9 IS=1E-15 VAF=92)
* MODEL DX D(IS=1E-15)
* MODEL DY D(IS=1E-15 BV=50)
* ENDS OP-160
    
```

FIGURE 31: OP-160 SPICE Net-List