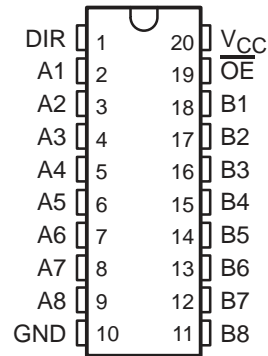


# SN74ALS638A, SN74ALS639A, SN74AS638A, SN74AS639 OCTAL BUS TRANSCEIVERS

SDAS123A – DECEMBER 1983 – REVISED JANUARY 1995

- Bidirectional Bus Transceivers in High-Density 20-Pin Packages
- Choice of True or Inverting Logic
- A-Bus Outputs Are Open Collector; B-Bus Outputs Are 3 State
- Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic (N) 300-mil DIPs

DW OR N PACKAGE  
(TOP VIEW)



DEVICE	A OUTPUT	B OUTPUT	LOGIC
SN74ALS638A, SN74AS638A	Open collector	3 state	Inverting
SN74ALS639A, SN74AS639	Open collector	3 state	True

## description

These octal bus transceivers are designed for asynchronous two-way communication between open-collector and 3-state buses. The devices transmit data from the A bus (open-collector) to the B bus (3 state) or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so the buses are isolated.

The -1 version of SN74ALS638A is identical to the standard version, except that the recommended maximum  $I_{OL}$  is increased to 48 mA.

The SN74ALS638A, SN74ALS639A, SN74AS638A, and SN74AS639 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

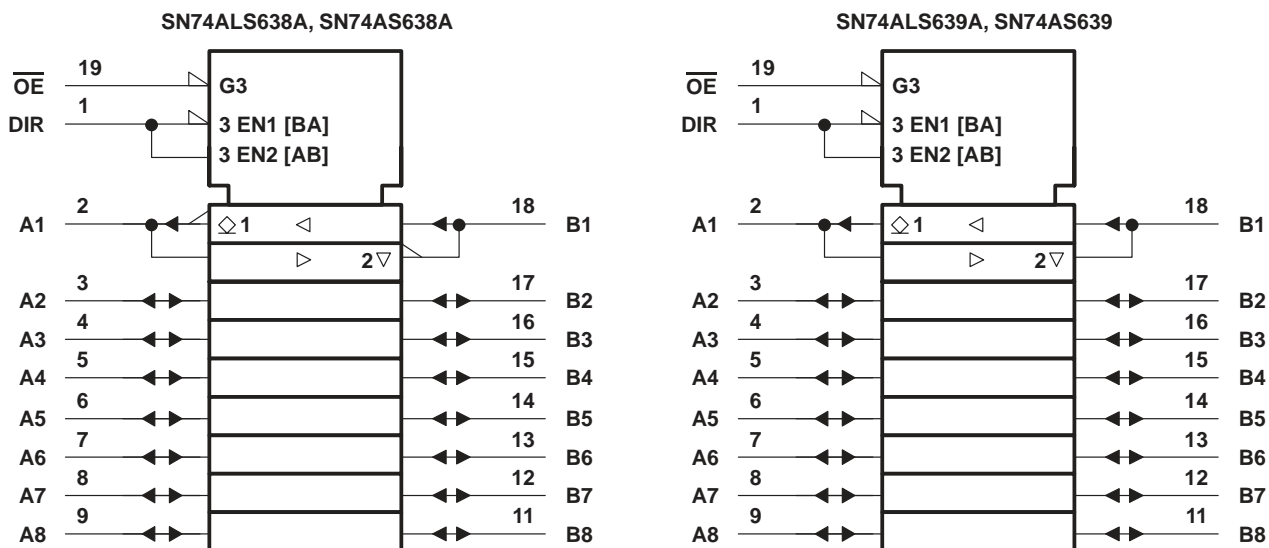
INPUTS		OPERATION	
$\overline{OE}$	DIR	SN74ALS638A SN74AS638A	SN74ALS639A SN74AS639
L	L	$\overline{B}$ data to A bus	B data to A bus
L	H	$\overline{A}$ data to B bus	A data to B bus
H	X	Isolation	Isolation

# SN74ALS638A, SN74ALS639A, SN74AS638A, SN74AS639

## OCTAL BUS TRANSCEIVERS

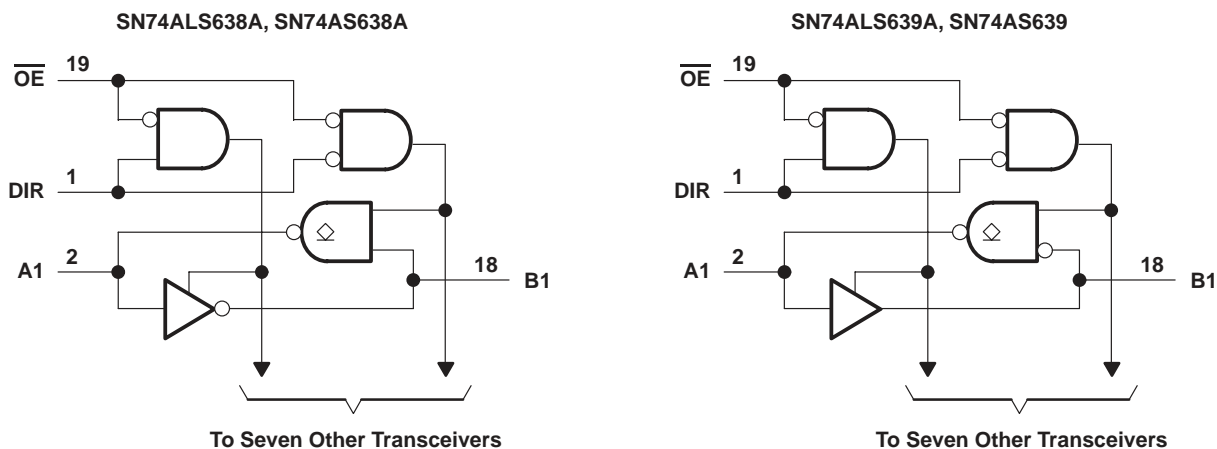
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### logic symbols†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

### logic diagrams (positive logic)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, $V_{CC}$ .....	7 V
Input voltage, $V_I$ : All inputs .....	7 V
A-bus I/O ports .....	7 V
B-bus I/O ports .....	5.5 V
Operating free-air temperature range, $T_A$ : SN74ALS638A, SN74ALS639A .....	0°C to 70°C
Storage temperature range .....	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

# SN74ALS638A, SN74ALS639A, SN74AS638A, SN74AS639A OCTAL BUS TRANSCEIVERS

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## recommended operating conditions

			SN74ALS638A SN74ALS639A			UNIT
			MIN	NOM	MAX	
$V_{CC}$	Supply voltage		4.5	5	5.5	V
$V_{IH}$	High-level input voltage		2			V
$V_{IL}$	Low-level input voltage		0.8			V
$V_{OH}$	High-level output voltage	A ports	5.5			V
$I_{OH}$	High-level output current	B ports	-15			mA
$I_{OL}$	Low-level output current	A or B ports	24			mA
			48†			
$T_A$	Operating free-air temperature		0	70		°C

† Applies only to the SN74ALS638A-1 version and only if  $V_{CC}$  is between 4.75 V and 5.25 V

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN74ALS638A SN74ALS639A		UNIT	
			MIN	TYP‡		MAX
$V_{IK}$		$V_{CC} = 4.5\text{ V}$ , $I_I = -18\text{ mA}$	-1.5		V	
$I_{OH}$	A ports	$V_{CC} = 4.5\text{ V}$ , $V_{OH} = 5.5\text{ V}$	0.1		mA	
$V_{OH}$	B ports	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ , $I_{OH} = -0.4\text{ mA}$	$V_{CC} - 2$		V	
		$V_{CC} = 4.5\text{ V}$ , $I_{OH} = -3\text{ mA}$	2.4	3.2		
		$V_{CC} = 4.5\text{ V}$ , $I_{OH} = -15\text{ mA}$	2			
$V_{OL}$	A or B ports	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 12\text{ mA}$	0.25	0.4	V
			$I_{OL} = 24\text{ mA}$	0.35		
			$I_{OL} = 48\text{ mA}^\dagger$	0.35		
$I_I$	Control inputs	$V_{CC} = 5.5\text{ V}$	$V_I = 7\text{ V}$	0.1		mA
	A or B ports		$V_I = 5.5\text{ V}$	0.1		
$I_{IH}$	Control inputs	$V_{CC} = 5.5\text{ V}$ , $V_I = 2.7\text{ V}$	20		$\mu\text{A}$	
	A or B ports§		20			
$I_{IL}$	Control inputs	$V_{CC} = 5.5\text{ V}$ , $V_I = 0.4\text{ V}$	-0.1		mA	
	A or B ports§		-0.1			
$I_{O}^\parallel$	B ports	$V_{CC} = 5.5\text{ V}$ , $V_O = 2.25\text{ V}$	-30	-112		mA
$I_{CC}$	SN74ALS638A	$V_{CC} = 5.5\text{ V}$	Outputs high	18	30	mA
			Outputs low	26	41	
			Outputs disabled	16	30	
	SN74ALS639A		Outputs high	25	40	
			Outputs low	30	50	
			Outputs disabled	33	54	

† Applies only to the SN74ALS638A-1 version and only if  $V_{CC}$  is between 4.75 V and 5.25 V

‡ All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

§ For I/O ports, the parameters  $I_{IH}$  and  $I_{IL}$  include the off-state output current.

¶ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .



# SN74ALS638A, SN74ALS639A, SN74AS638A, SN74AS639

## OCTAL BUS TRANSCEIVERS

SDAS123A – DECEMBER 1983 – REVISED JANUARY 1995

### switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 680 Ω (A outputs), R <sub>1</sub> = R <sub>2</sub> = 500 Ω (B outputs), T <sub>A</sub> = MIN to MAX†				UNIT
			SN74ALS638A		SN74ALS639A		
			MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A	B	2	12	2	12	ns
t <sub>PHL</sub>			2	12	2	12	
t <sub>PLH</sub>	B	A	8	25	10	30	ns
t <sub>PHL</sub>			8	30	5	22	
t <sub>PLH</sub>	$\overline{OE}$	A	5	25	10	30	ns
t <sub>PHL</sub>			10	45	10	35	
t <sub>PZH</sub>	$\overline{OE}$	B	5	20	6	21	ns
t <sub>PZL</sub>			5	22	8	25	
t <sub>PHZ</sub>	$\overline{OE}$	B	2	10	2	10	ns
t <sub>PLZ</sub>			3	15	3	16	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V <sub>CC</sub>	7 V
Input voltage, V <sub>I</sub> : All inputs	7 V
A-bus I/O ports	7 V
B-bus I/O ports	5.5 V
Operating free-air temperature range, T <sub>A</sub> : SN74AS638A, SN74AS639	0°C to 70°C
Storage temperature range	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### recommended operating conditions

		SN74AS638A SN74AS639			UNIT
		MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage	2			V
V <sub>IL</sub>	Low-level input voltage			0.8	V
V <sub>OH</sub>	High-level output voltage			5.5	V
I <sub>OH</sub>	High-level output current			–15	mA
I <sub>OL</sub>	Low-level output current			64	mA
T <sub>A</sub>	Operating free-air temperature	0		70	°C



# SN74ALS638A, SN74ALS639A, SN74AS638A, SN74AS639A OCTAL BUS TRANSCEIVERS

SDAS123A – DECEMBER 1983 – REVISED JANUARY 1995

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		SN74AS638A SN74AS639			UNIT	
				MIN	TYP†	MAX		
V <sub>IK</sub>		V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA		-1.2			V	
I <sub>OH</sub>	A ports	V <sub>CC</sub> = 4.5 V, V <sub>OH</sub> = 5.5 V		0.1			mA	
V <sub>OH</sub>	B ports	V <sub>CC</sub> = 4.5 V to 5.5 V, I <sub>OH</sub> = -2 mA		V <sub>CC</sub> - 2			V	
		V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3 mA		2.4	3.2			
		V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -15 mA		2.4				
V <sub>OL</sub>	A or B ports	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 64 mA		0.35	0.55		V	
I <sub>I</sub>	Control inputs	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 7 V		0.1			mA	
	A or B ports	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 5.5 V		0.1				
I <sub>IH</sub>	Control inputs	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 2.7 V		20			μA	
	A or B ports‡			70				
I <sub>IL</sub>	Control inputs	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 0.4 V		-0.5			mA	
	A or B ports‡			-0.75				
I <sub>OS</sub> §		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.25 V		-50	-150		mA	
I <sub>CC</sub>	SN74AS638A	V <sub>CC</sub> = 5.5 V		Outputs high		24	54	mA
				Outputs low		75	122	
				Outputs disabled		37	61	
	SN74AS639	V <sub>CC</sub> = 5.5 V		Outputs high		56	92	
				Outputs low		95	154	
				Outputs disabled		62	100	

† All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

‡ For I/O ports, the parameters I<sub>IH</sub> and I<sub>IL</sub> include the off-state output current.

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I<sub>OS</sub>.

## switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω (A outputs), R <sub>1</sub> = R <sub>2</sub> = 500 Ω (B outputs), T <sub>A</sub> = MIN to MAX¶				UNIT
			SN74AS638A		SN74AS639		
			MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A	B	2	7	2	9.5	ns
t <sub>PHL</sub>			2	6.5	2	9	
t <sub>PLH</sub>	B	A	5	20	5	22	ns
t <sub>PHL</sub>			2	7	2	9	
t <sub>PLH</sub>	OE	A	5	19	5	21.5	ns
t <sub>PHL</sub>			2	9	2	11.5	
t <sub>PZH</sub>	OE	B	2	8	2	10.5	ns
t <sub>PZL</sub>			2	10	2	10.5	
t <sub>PHZ</sub>	OE	B	2	7	2	7	ns
t <sub>PLZ</sub>			2	10	2	10.5	

¶ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

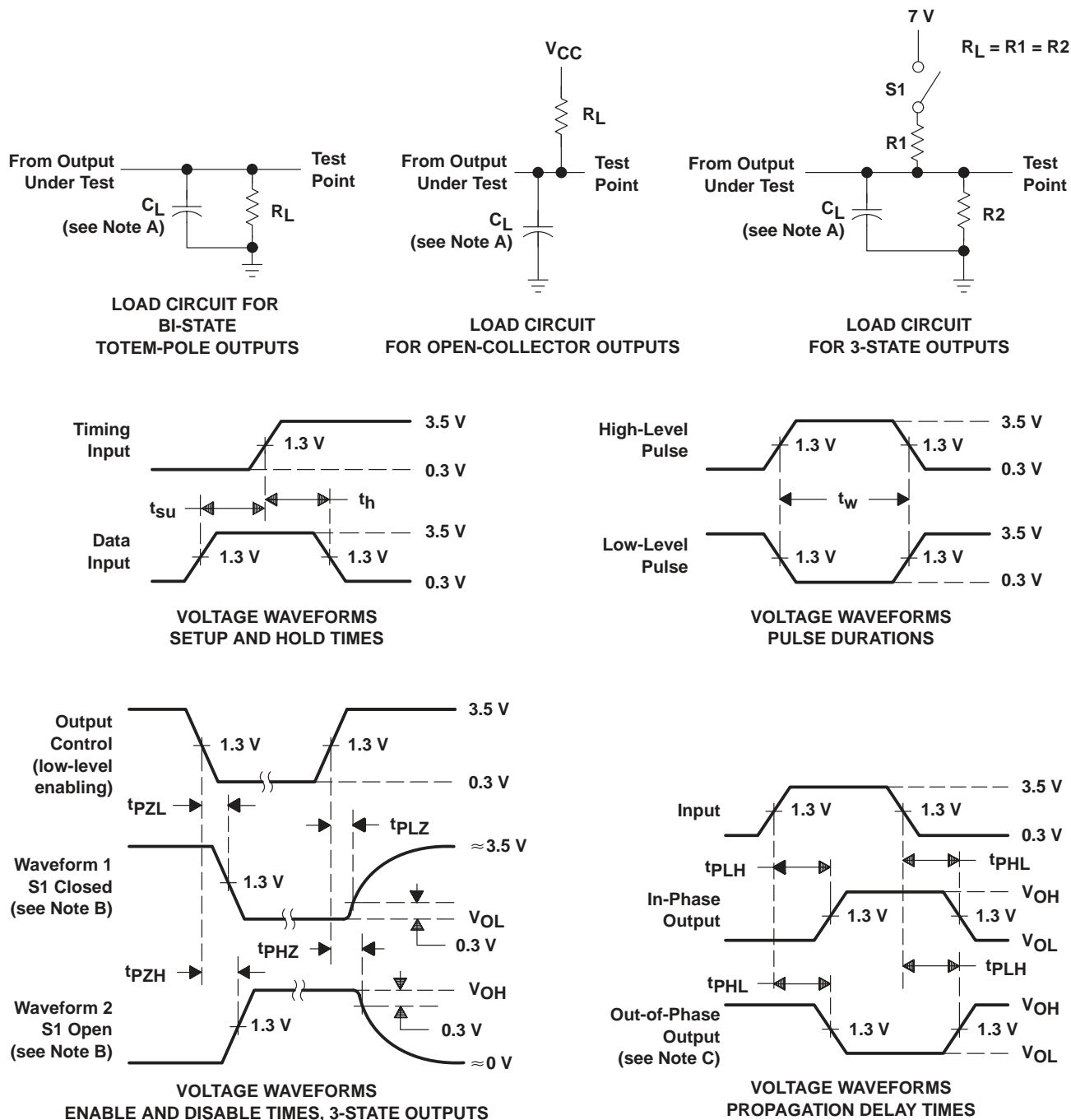


# SN74ALS638A, SN74ALS639A, SN74AS638A, SN74AS639

## OCTAL BUS TRANSCEIVERS

SDAS123A – DECEMBER 1983 – REVISED JANUARY 1995

### PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.  
 D. All input pulses have the following characteristics:  $PRR \leq 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.  
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ALS638AN	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS638AN	<a href="#">Samples</a>
SN74ALS639ADW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS639A	<a href="#">Samples</a>
SN74ALS639AN	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS639AN	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74ALS638AN	N	PDIP	20	20	506	13.97	11230	4.32
SN74ALS639ADW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74ALS639AN	N	PDIP	20	20	506	13.97	11230	4.32

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

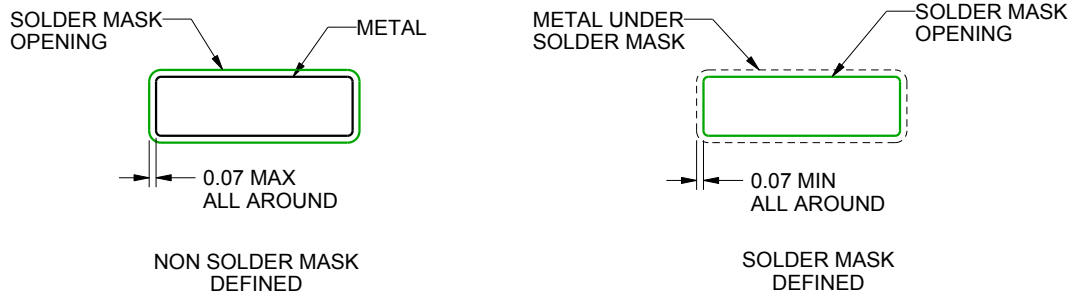
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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